Report on IEEE-ISSCC 2018 micro-nano-pico : we must go on

Erik H.M. HEIJNE

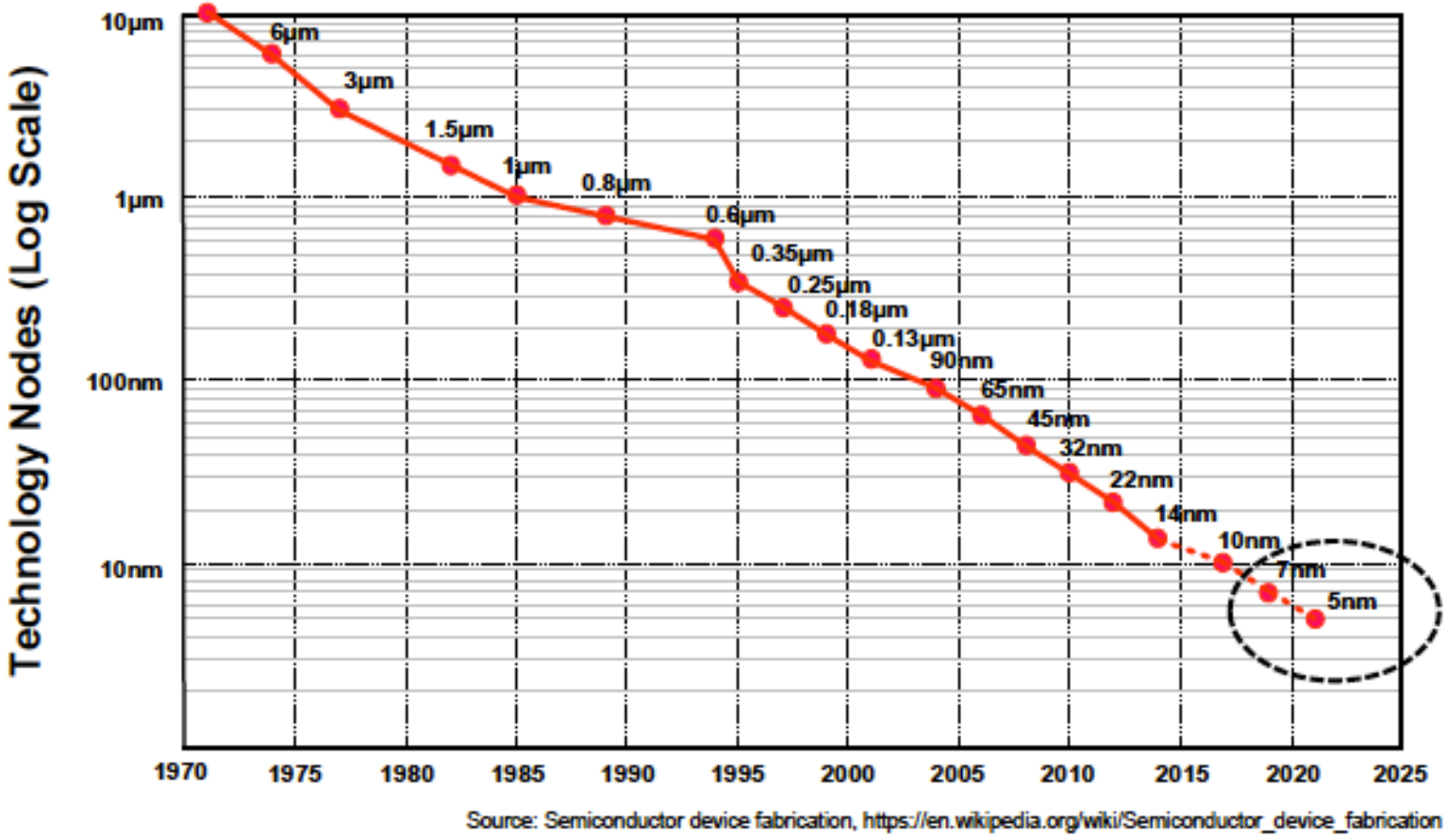
IEAP/CTU Prague & CERN CH1211 Geneva 23

CERN ESE Seminar, 13 March 2018

"Moore's law" technology shrinkage finished?

Transistor Scaling

Technology has scaled transistor in the past and should do in the future



Source: Semiconductor device fabrication, https://en.wikipedia.org/wiki/Semiconductor_device_fabrication

IEEE-ISSC Taejoong Song et al. Samsung; paper 11.2

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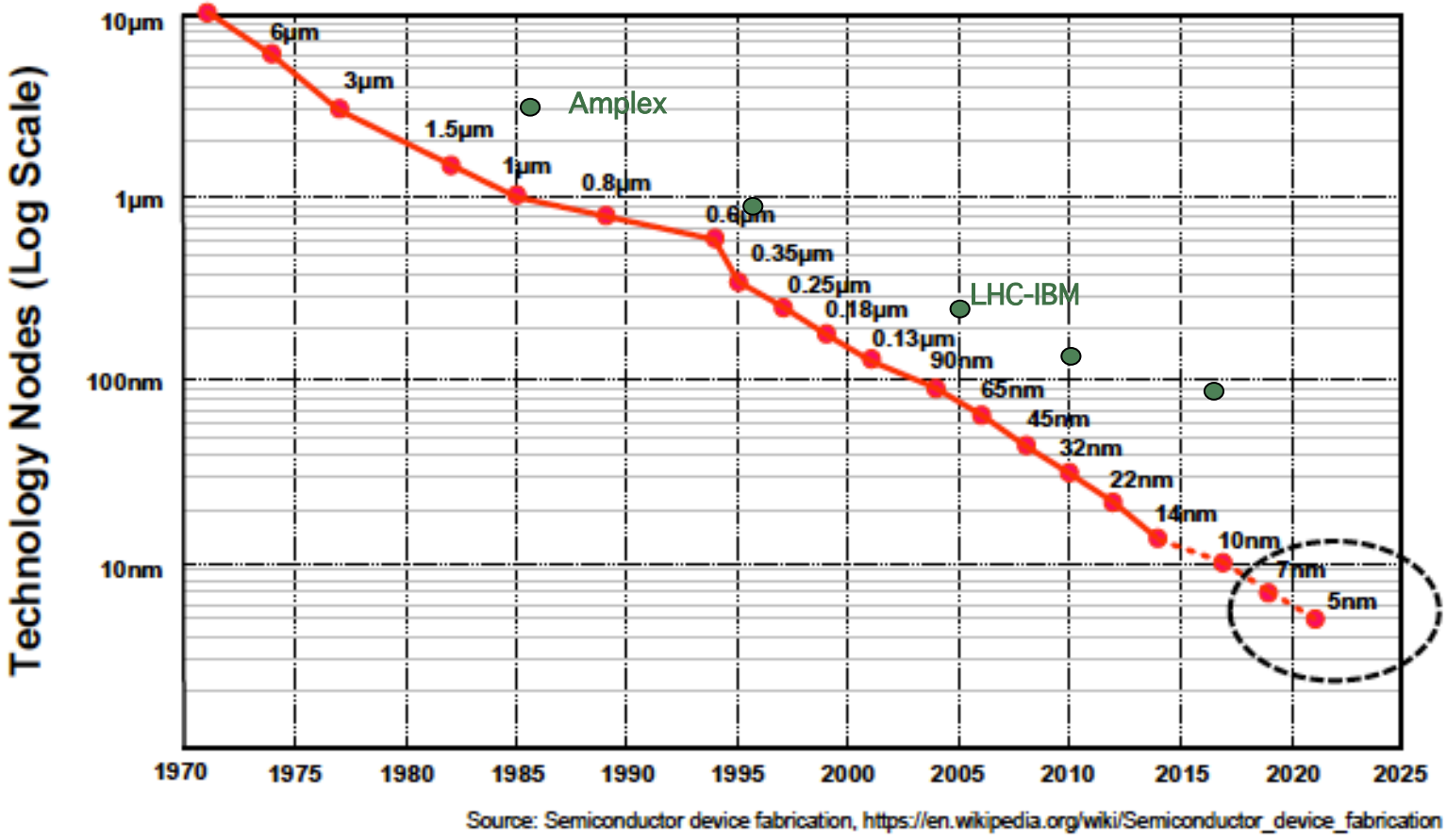

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IEEE-ISSC Taejoong Song et al. Samsung; paper 11.2

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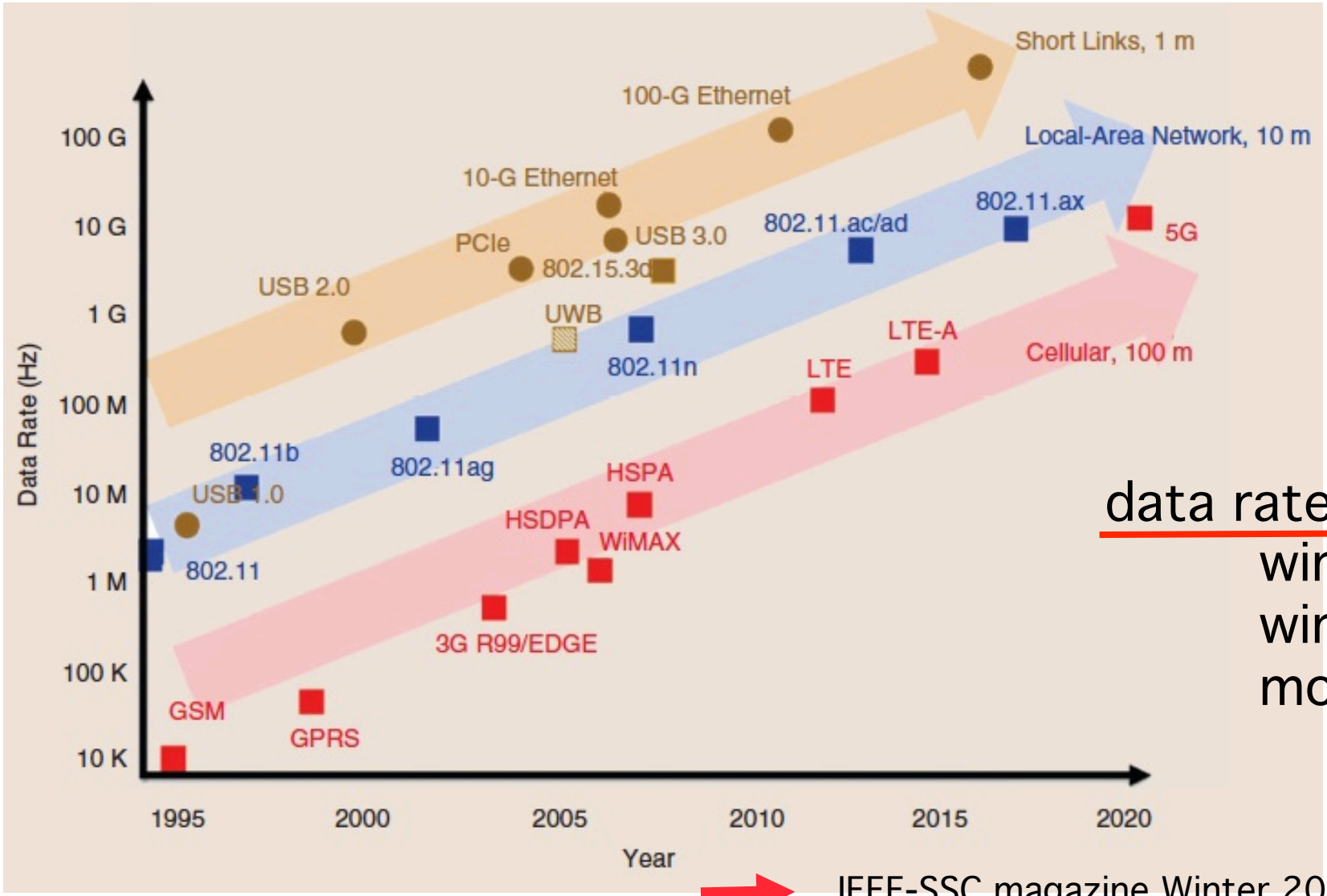
13 March 2018

most amazing:
continued exponential trends, up+downward



data rates vs time

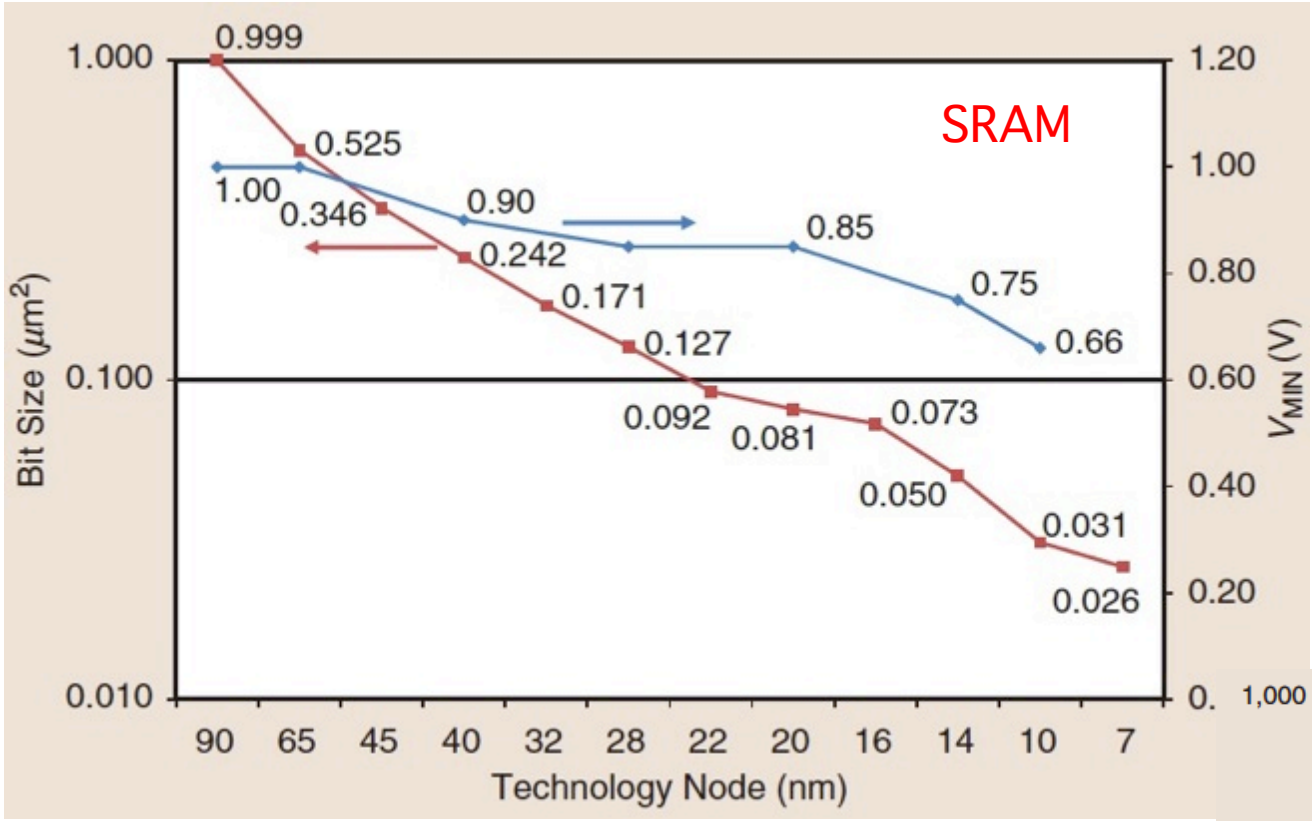
wires

wireless LAN

mobile

IEEE-SSC magazine Winter 2018 p.40

SRAM : driver towards smaller technology

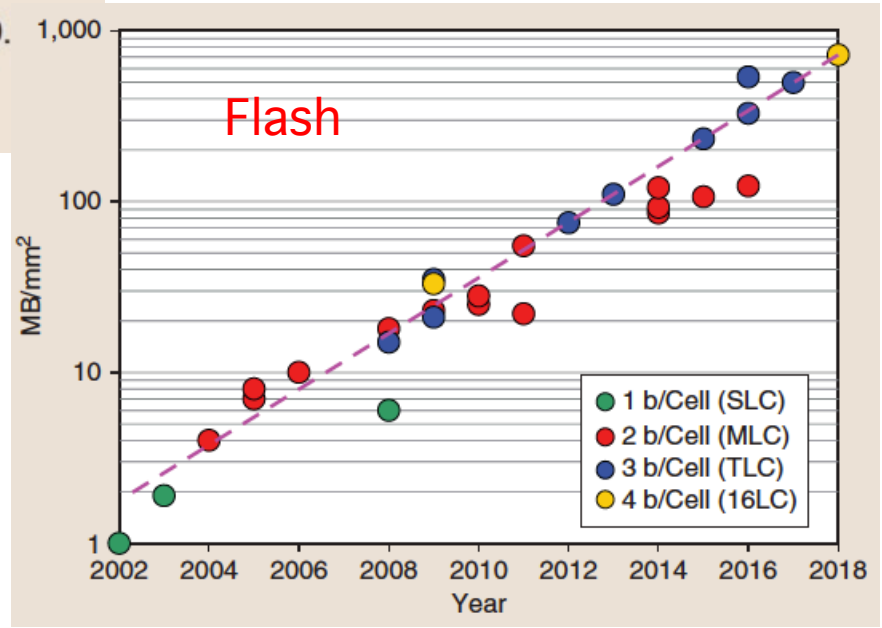


in 7nm EUV 0.026 μm^2/bit

38.5Mb per mm^2

more details later

in NAND Flash:
~180Mb per mm^2 4b/cell



IEEE-SSC magazine Winter 2018 p.43-45

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even towards **femto and atto ?**

particle physics in some way
explores atto- and zepto-meter domain

Higgs boson with mean lifetime of 10^{-22}s
decays in ~ 30 femtometer (~diameter of nucleus)

how can nanoelectronics be exploited
to improve particle physics experiments?

There's plenty of room at the bottom

Richard P. Feynman 1959, APS at Caltech

Overview

this introduction -->

the conference

processors

memory : SRAM, Flash, (DRAM, others,.)

new lithography: EUV

the semiconductor industry

data transmission

electrical power handling

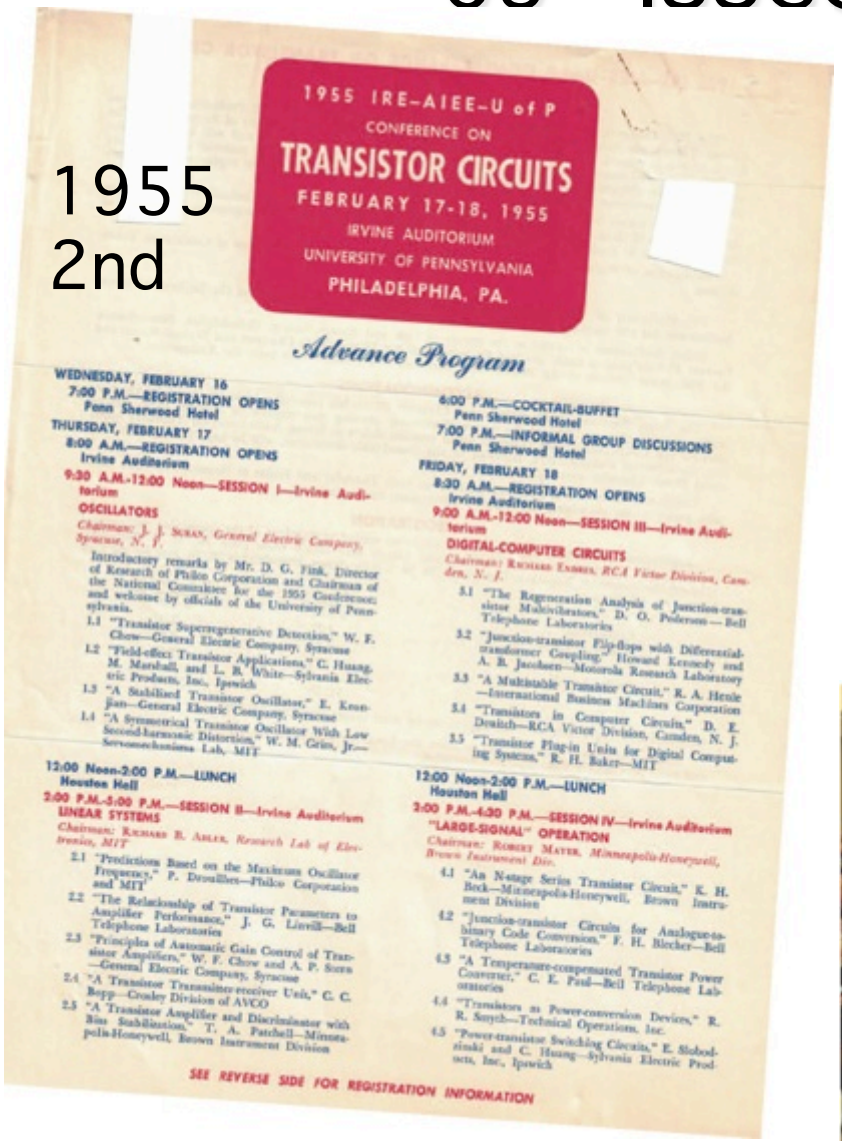
imagers

our future..?

do we really know what we will need in 2030?

65th ISSCC in San Francisco

1955
2nd



1955 IRE-AIEE-U of P
CONFERENCE ON
TRANSISTOR CIRCUITS
FEBRUARY 17-18, 1955
IRVINE AUDITORIUM
UNIVERSITY OF PENNSYLVANIA
PHILADELPHIA, PA.

Advance Program

WEDNESDAY, FEBRUARY 16
7:00 P.M.—REGISTRATION OPENS
Penn Sherwood Hotel

THURSDAY, FEBRUARY 17
8:00 A.M.—REGISTRATION OPENS
Irvine Auditorium

9:30 A.M.-12:00 Noon—SESSION I—Irvine Auditorium

OSCILLATORS

Chairman: J. J. Suran, General Electric Company, Syracuse, N. Y.

Introductory remarks by Mr. D. G. Fink, Director of Research of Philco Corporation and Chairman of the National Committee for the 1955 Conference; and welcome by officials of the University of Pennsylvania.

1.1 "Transistor Superregenerative Detection," W. F. Chow—General Electric Company, Syracuse

1.2 "Field-effect Transistor Applications," C. Huang, M. Marshall, and L. R. White—Sylvania Electric Products, Inc., Ipswich

1.3 "A Stabilized Transistor Oscillator," E. Keonjian—General Electric Company, Syracuse

1.4 "A Symmetrical Transistor Oscillator With Low Second-harmonic Distortion," W. M. Gries, Jr.—Servomechanisms Lab, MIT

12:00 Noon-2:00 P.M.—LUNCH
Houston Hall

2:00 P.M.-5:00 P.M.—SESSION II—Irvine Auditorium

LINEAR SYSTEMS

Chairman: Richard B. Adler, Research Lab of Electronics, MIT

2.1 "Predictions Based on the Maximum Oscillator Frequency," P. Drouilhet—Philco Corporation and MIT

2.2 "The Relationship of Transistor Parameters to Amplifier Performance," J. G. Linvill—Bell Telephone Laboratories

2.3 "Principles of Automatic Gain Control of Transistor Amplifiers," W. F. Chow and A. P. Stern—General Electric Company, Syracuse

2.4 "A Transistor Transmitter-receiver Unit," C. C. Bopp—Crosley Division of AVCO

2.5 "A Transistor Amplifier and Discriminator with Bias Stabilization," T. A. Patchell—Minneapolis-Honeywell, Brown Instrument Division

6:00 P.M.—COCKTAIL-BUFFET
Penn Sherwood Hotel

7:00 P.M.—INFORMAL GROUP DISCUSSIONS
Penn Sherwood Hotel

FRIDAY, FEBRUARY 18
8:30 A.M.—REGISTRATION OPENS
Irvine Auditorium

9:00 A.M.-12:00 Noon—SESSION III—Irvine Auditorium

DIGITAL-COMPUTER CIRCUITS

Chairman: Richard Tanner, RCA Victor Division, Camden, N. J.

3.1 "The Regeneration Analysis of Junction-transistor Multivibrators," D. O. Pederson—Bell Telephone Laboratories

3.2 "Junction-transistor Flip-flops with Differential-transformer Coupling," Howard Kennedy and A. B. Jacobsen—Motorola Research Laboratory

3.3 "A Multistable Transistor Circuit," R. A. Henle—International Business Machines Corporation

3.4 "Transistors in Computer Circuits," D. E. Deutsch—RCA Victor Division, Camden, N. J.

3.5 "Transistor Flip-in Units for Digital Computing Systems," R. H. Baker—MIT

12:00 Noon-2:00 P.M.—LUNCH
Houston Hall

2:00 P.M.-4:30 P.M.—SESSION IV—Irvine Auditorium

"LARGE-SIGNAL" OPERATION

Chairman: Robert Mayer, Minneapolis-Honeywell, Brown Instrument Div.

4.1 "An N-stage Series Transistor Circuit," K. H. Beck—Minneapolis-Honeywell, Brown Instrument Division

4.2 "Junction-transistor Circuits for Analogue-to-binary Code Conversion," F. H. Blecher—Bell Telephone Laboratories

4.3 "A Temperature-compensated Transistor Power Converter," C. E. Paul—Bell Telephone Laboratories

4.4 "Transistors as Power-conversion Devices," R. R. Smyth—Technical Operations, Inc.

4.5 "Power-transistor Switching Circuits," E. Slobodzinski and C. Huang—Sylvania Electric Products, Inc., Ipswich

SEE REVERSE SIDE FOR REGISTRATION INFORMATION

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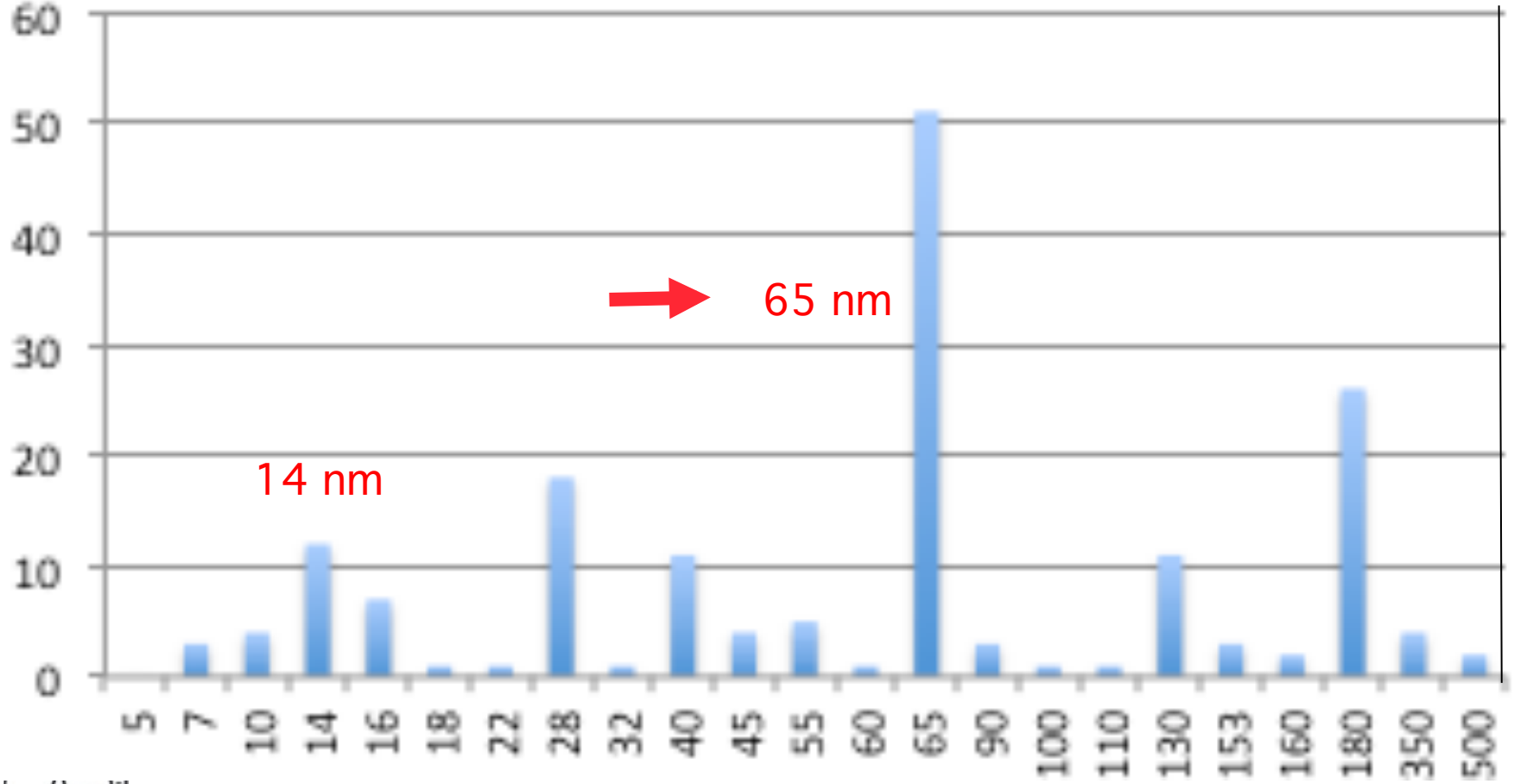
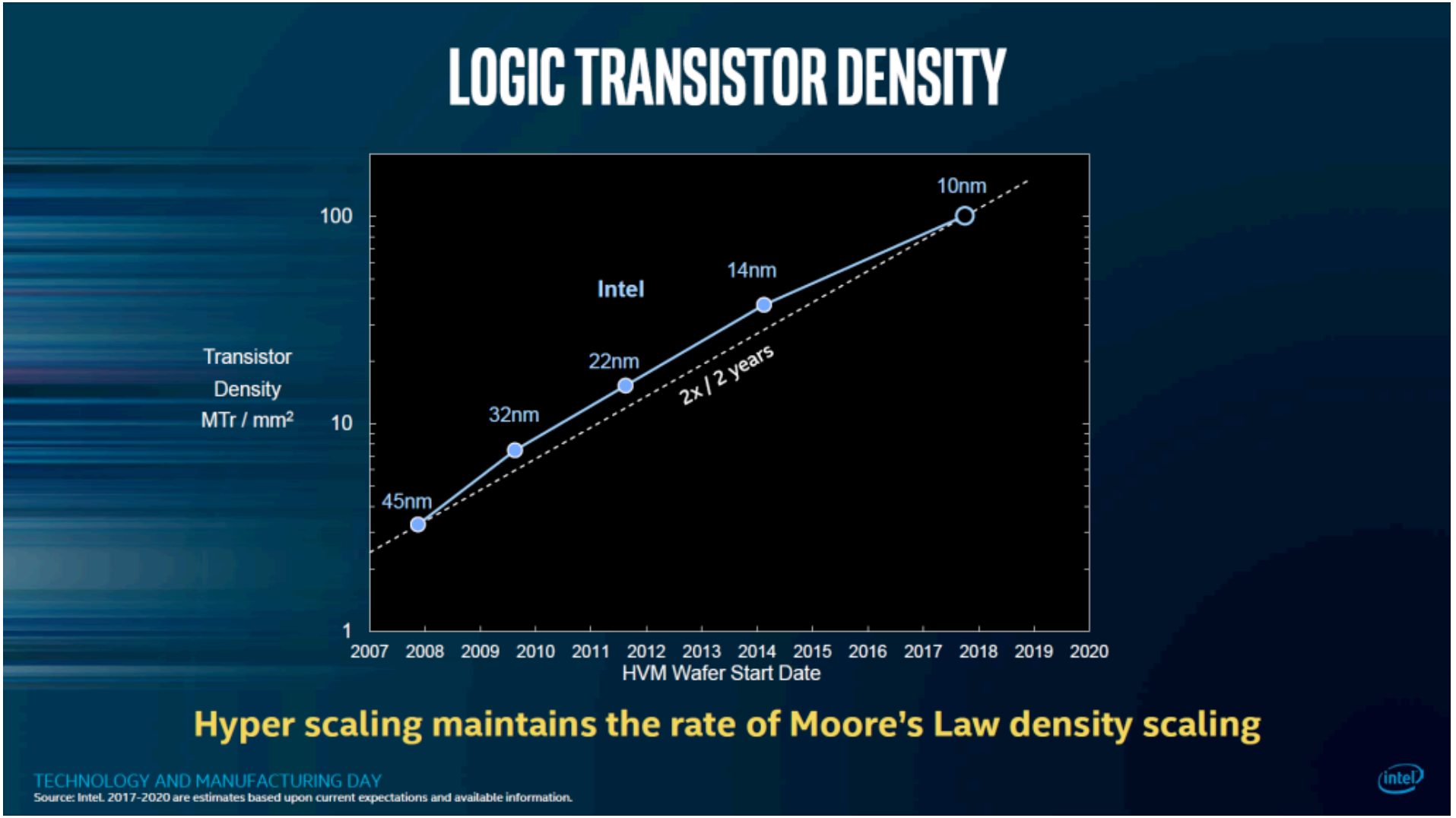
Si CMOS technology nodes in papers ISSCC 2018

~300 papers acceptance <40%



'Hyperscaling' at Intel



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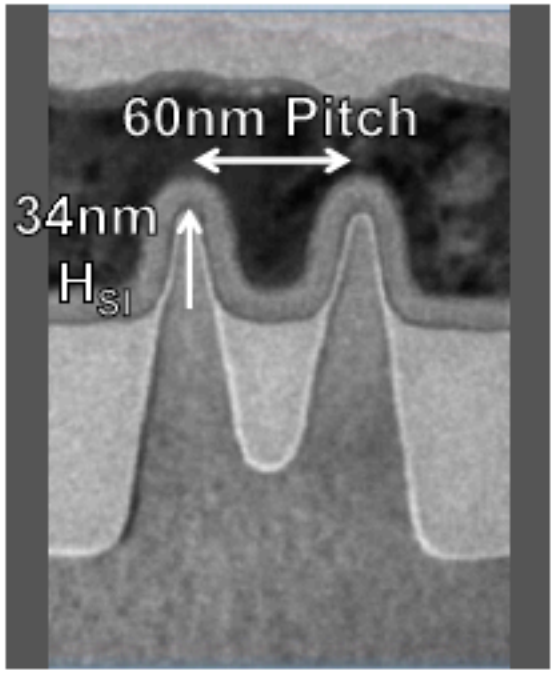
reach 100 Mtrans/mm²

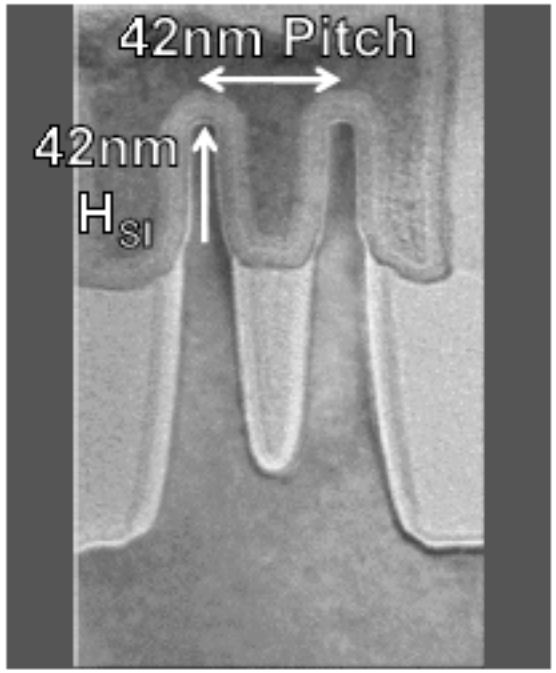
13 March 2018

FinFET evolution at Intel



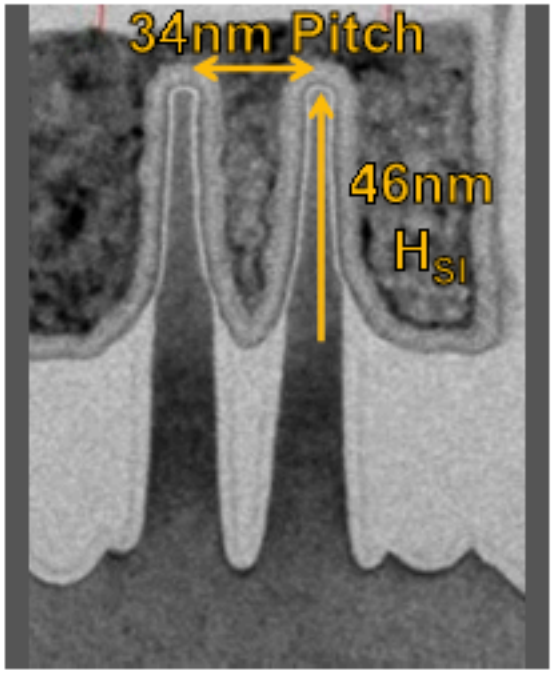
22nm Process

1st Generation FinFET



14nm Process

2nd Generation FinFET



10nm Process

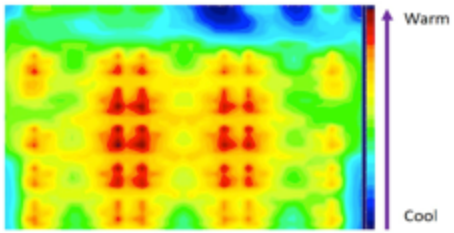
3rd Generation FinFET

Intel 10nm technology: 54nm contacted poly pitch, 34nm fin pitch and 46nm fin height
Fins are tighter, straighter and taller for better SCE, Id and matching

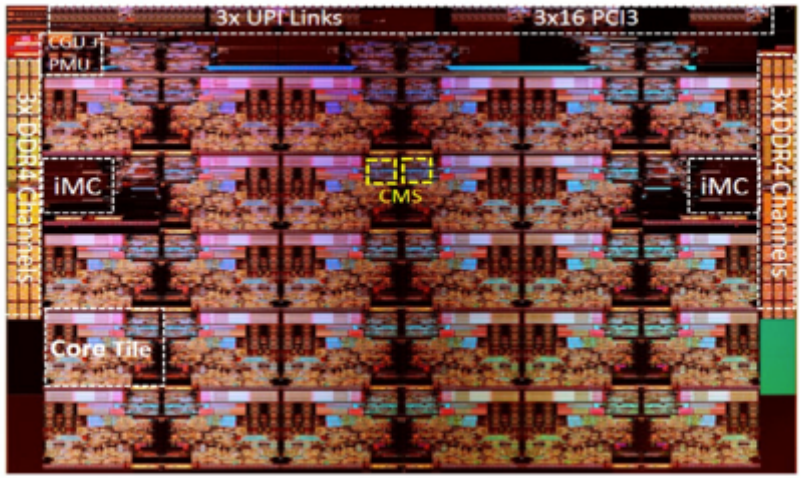
Zheng Guo et al. Intel. paper 11.1

Processors

- Intel SkyLake Xeon processors 14nm, 28 cores
  S.M. Tam et al. paper 2.1



Skylake-SP Processor Blocks

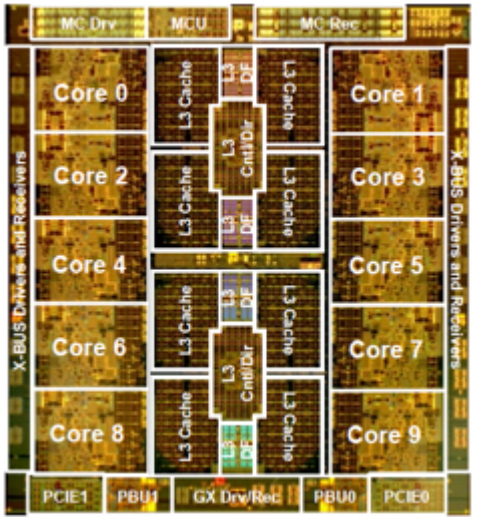


Converged Mesh Stop (CMS) interfaces to Mesh

power (heating) and soft error rate
are major issues

- IBM z14 processor 14nm
  C. Berry et al. paper 2.2

server system has large number of chips
14nm FinFET in SOI
17 metals (see next slide)
GlobalFoundries



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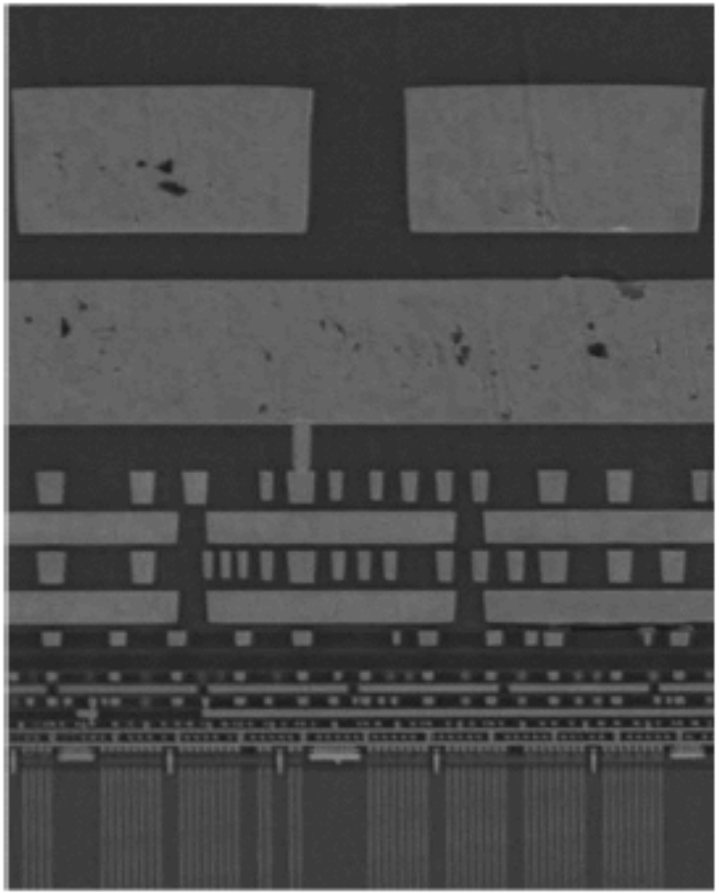
Technology Overview

- GlobalFoundries 14nm High-Perf (HP) FinFET SOI technology w/embedded DRAM

Technology Overview	
Ultra-thick wires	2400nm - 2 levels
5.6X pitch wiring	360nm - 4 levels
4X pitch wiring	256nm - 2 levels
2X pitch wiring	128nm - 4 levels
1.3X pitch wiring	80nm - 2 levels
1X pitch, fine wiring (LELE)	64nm - 3 levels
Logic Device VT pairs	L, R, H
SRAM Cell Sizes	0.102µm² (HP & LL), 0.143µm²
eDRAM Cell Size	0.0174µm²



GlobalFoundries 14nm SOI C.Berry et al. paper 2.2

memory as the technology driver

new lithography now needed: Extended Ultra Violet EUV

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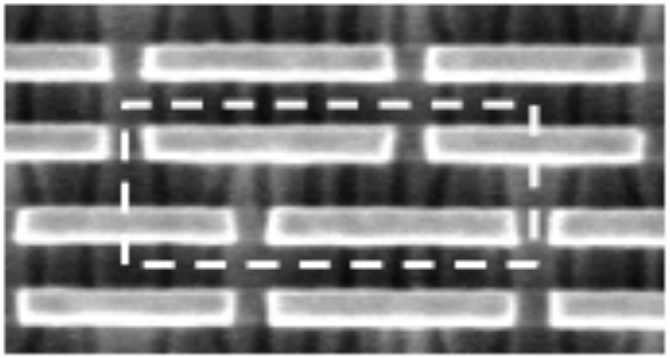
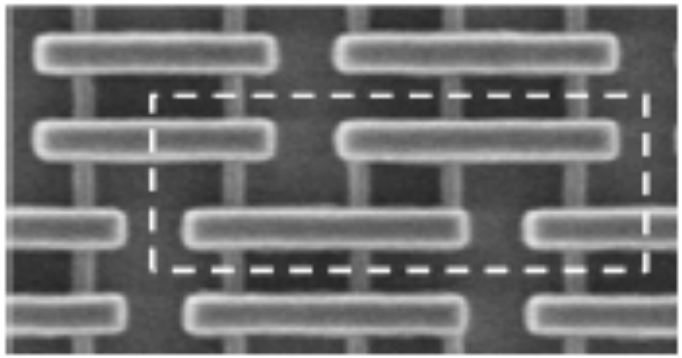
13 March 2018

SRAM cell Intel

10 nm FinFET Intel 23.6 Mb/mm2 paper 11.1



32nm Planar
Continuous Sizing
$W_{PU} < W_{PG} < W_{PD}$

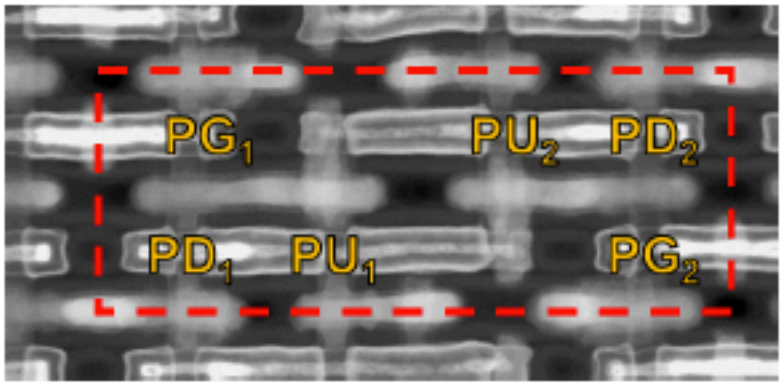


22/14/10nm FinFET
Quantized Sizing
$W_{PU} = W_{PG} = W_{PD}$

→ more typica photo on next slide

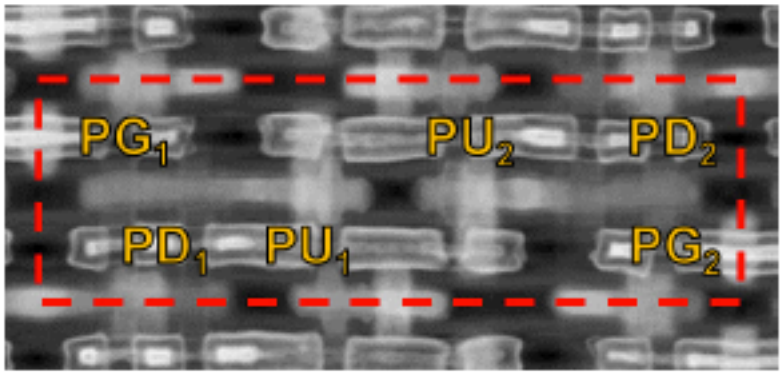
10nm Trigate/FinFET SRAM Bitcells

HDC
0.0312 µm²



Optimized for Highest Bit Density

LVC
0.0367 µm²



Optimized for Low Voltage and Higher Performance

HDC SRAM Bitcell: 1:1:1 PU:PG:PD fin ratio

LVC SRAM Bitcell: 1:1:2 PU:PG:PD fin ratio

→ Zheng Guo et al. Intel. paper 11.1

NEW APPLICATIONS NEED MORE ADVANCED nm CMOS

INTEL : IMPROVED LITHOGRAPHY in 45 nm

my seminar in 2009

MINIMAL SRAM CELL

ALSO, SEVERAL CHARACTERISTICS IMPROVED BEYOND EXPECTATIONS

NOT TO SCALE

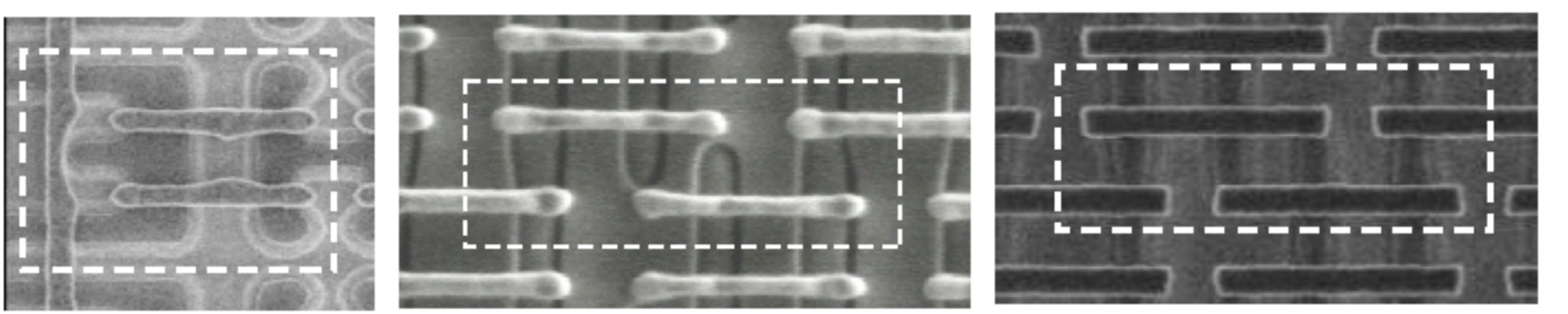


Fig.7 Cell topology enhancements for mismatch improvement

NOT TO SCALE

Mrs Kelin KUHN, IEEE IEDM 2007

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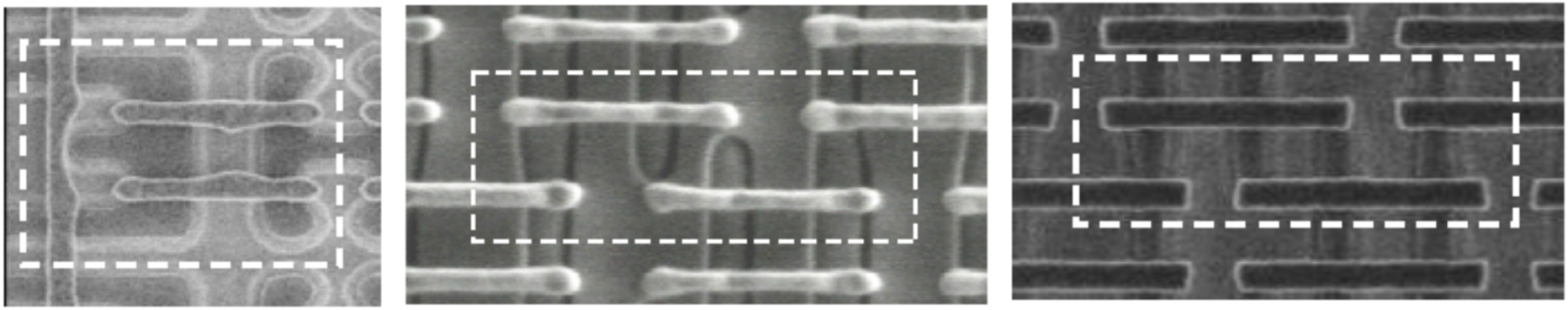
90 nm **65 nm** **NOT TO SCALE** **45 nm**



90nm – tall
1.0 μm^2

65nm – wide
0.57 μm^2

45nm – wide
w/ patterning enhancement 0.346 μm^2

Fig.7 Cell topology enhancements for mismatch improvement

NOT TO SCALE

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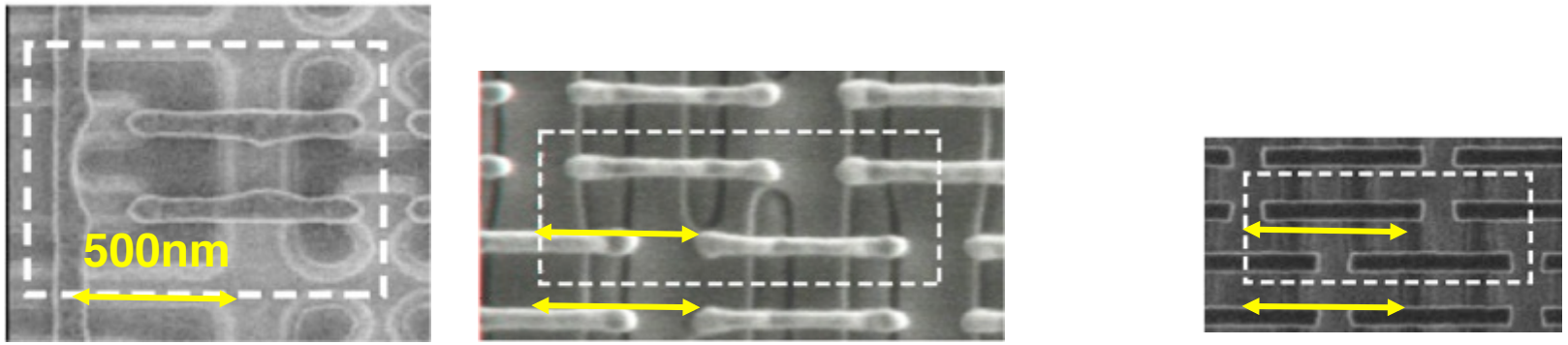

~ TO SCALE

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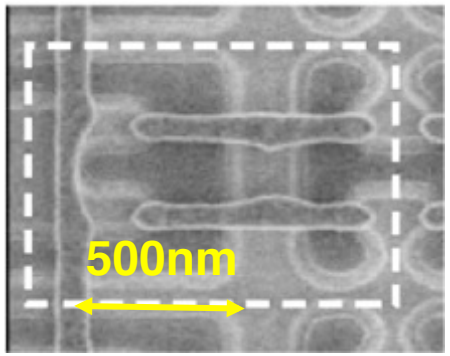
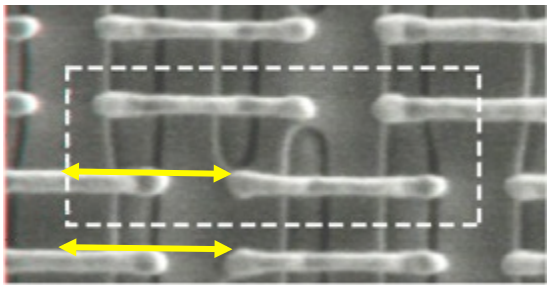
MINIMAL SRAM CELL

ALSO, SEVERAL CHARACTERISTICS IMPROVED BEYOND EXPECTATIONS

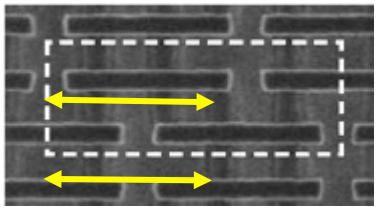
90 nm



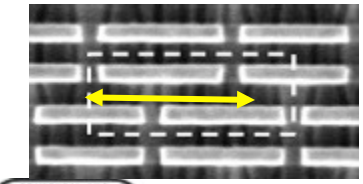
65 nm



45 nm



32 nm



est. 640 x270 nm

ISSCC in 2018

'10 nm'

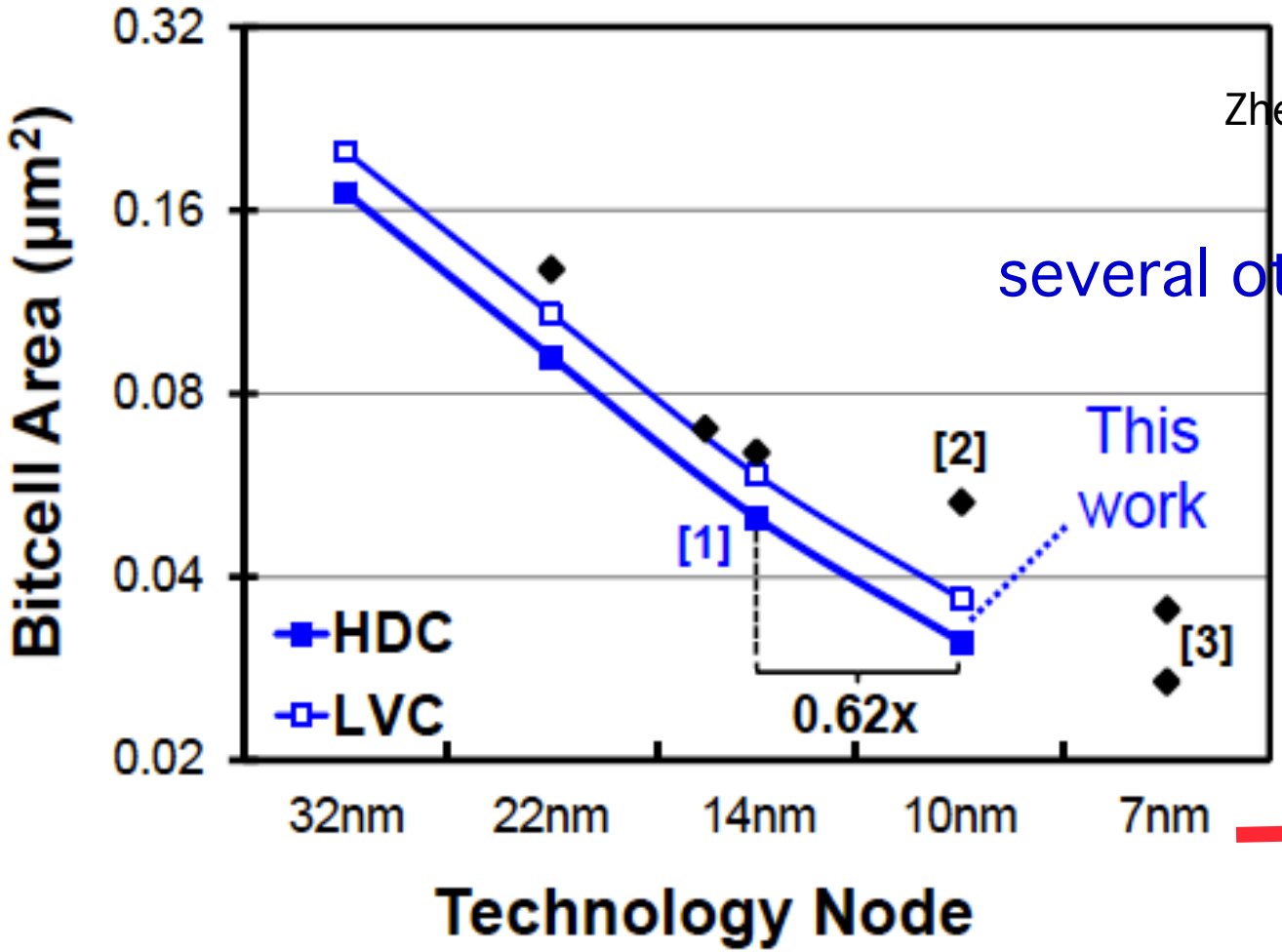
est. 280 x112 nm

~ TO SCALE

500nm Zheng Guo et al. Intel. paper 11.1 ISSCC 2018

Mrs Kelin KUHN, IEEE IEDM 2007

SRAM Technology Scaling



Zheng Guo et al. Intel. paper 11.1

several other improvements increase density & speed

[1] Karl, ISSCC 2015
[2] Seo, VLSI-T 2014
[3] Narasimha, IEDM 2017

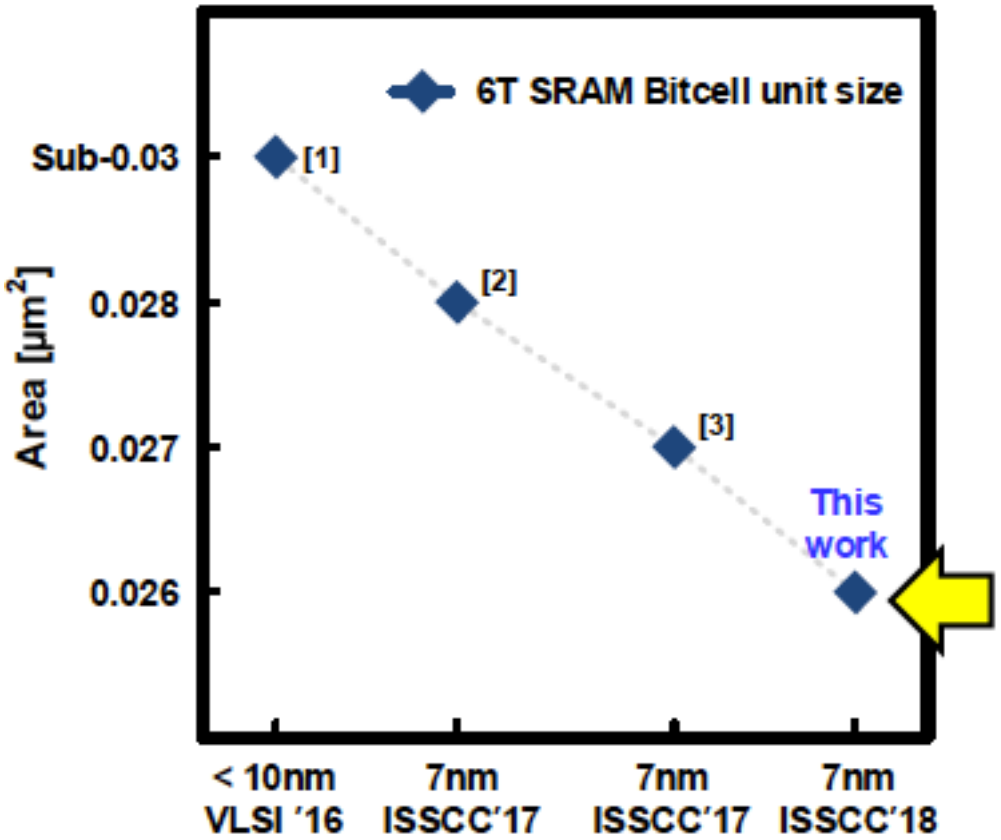
32 Mb/mm²
next paper
38 Mb/mm²

10nm SRAM bitcell area scales by 0.62x from 14nm node

HDC: smallest reported bitcell in 10nm technology (0.0312μm²)

SRAM scaling at Samsung : 7nm using EUV

Taejoong Song et al.Samsung. paper 11.2



EUV single-patterning

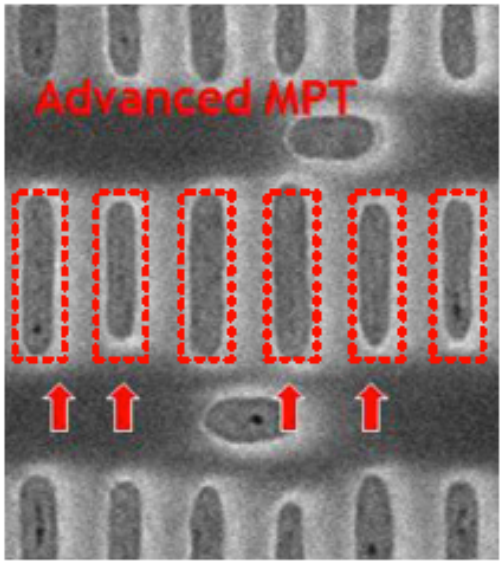
0.026 μm^2
38 Mb/mm^2

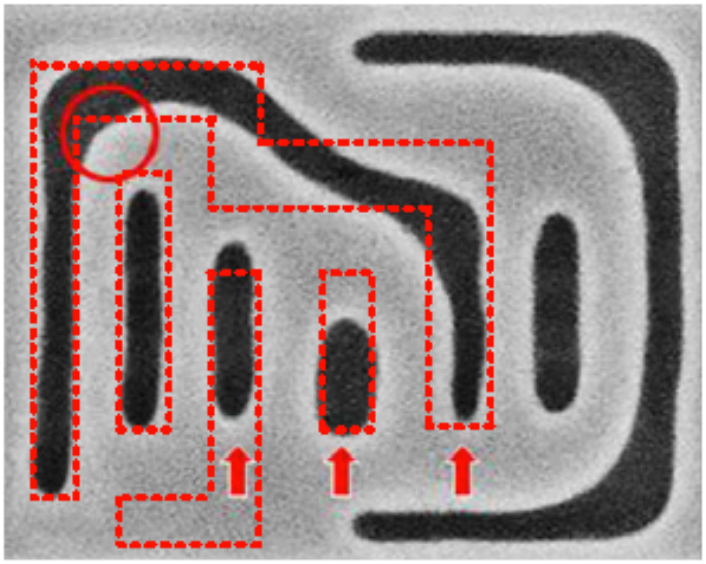
this test SRAM 256 Mb

Samsung SRAM

Patterning Limitation in Advanced Technology

Advanced technology faces challenge to make smaller pattern
Conventional multi-patterning has limitation to apply in an advanced technology

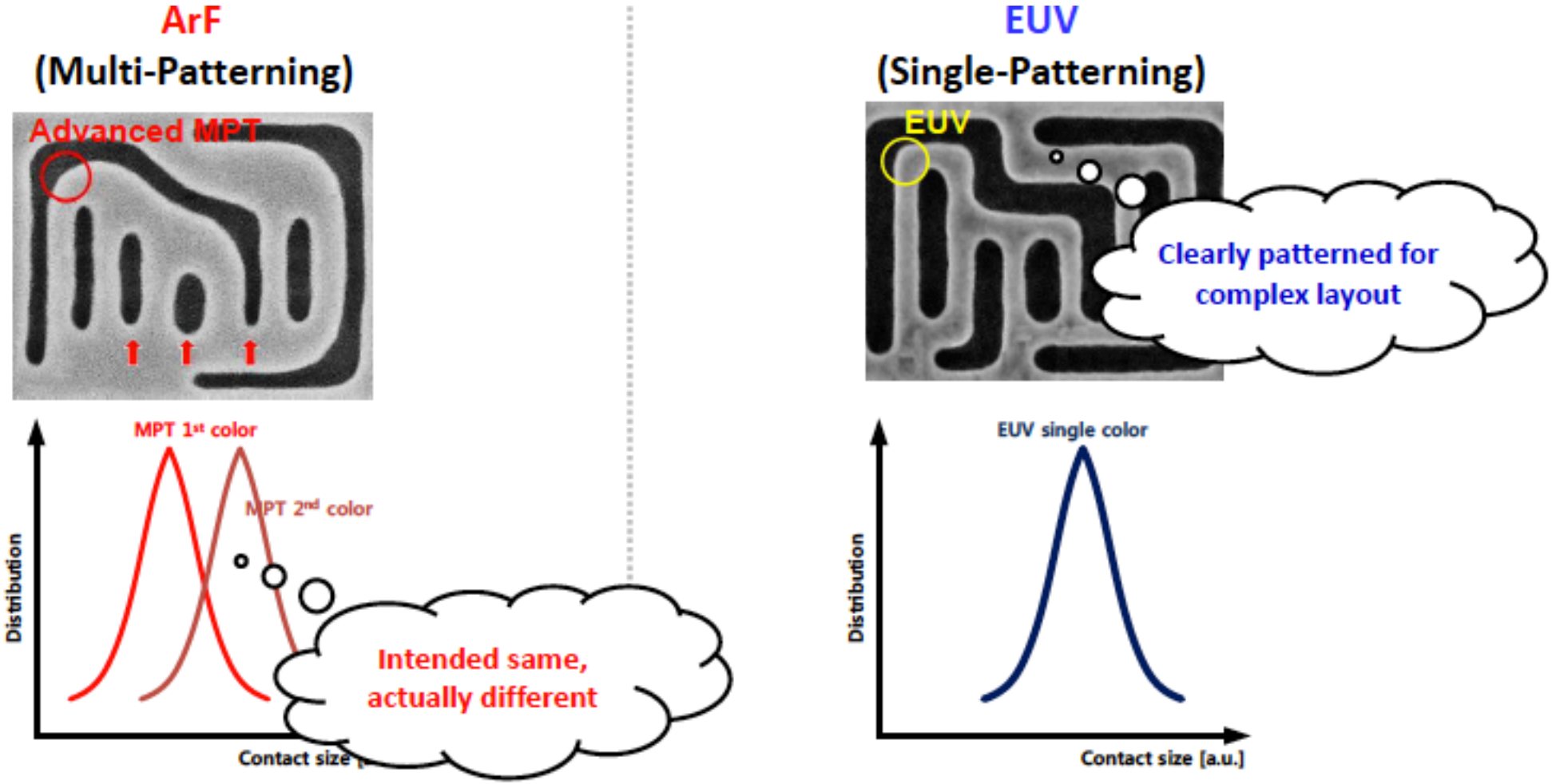




Taejoong Song et al.Samsung. paper 11.2

Source : *Daewon Ha*, "Highly Manufacturable 7nm FinFET Technology featuring EUV lithography for Low Power and High Performance Applications," *VLSI Tech. 2017*, pp.T68-T69

193nm light vs Extreme UV lithography



Taejoong Song et al.Samsung. paper 11.2

→ first reported EUV SRAM chip

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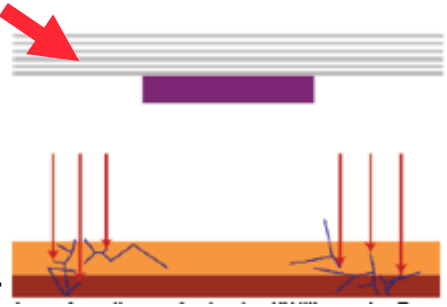
13 March 2018

Extreme UV lithography at Samsung

Hwaseong
new fab at ~6 B$
steppers ~0.2B$/unit
6-10B$ yearly turnover ??

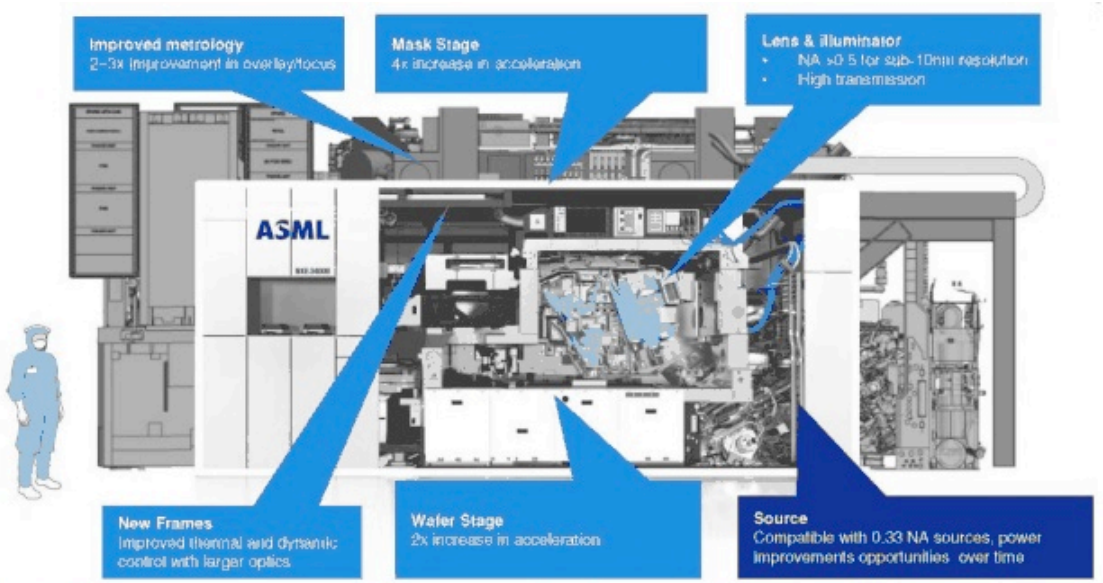
reflected light on photoresist:
mask



PR
wafer

13.5nm source: laser on tin droplets in vacuum ~1ps at 50kHz
tin deposit on concentrator mirror, hydrogen/vacuum ambient for cleaning
all reflective mirror optics, no lenses ; 30-60% loss per reflection: total 96%
for 240 (>500?)W power on wafer, need to start with >6-15 kW light
--> 140 wafers/hour EUV stepper uses several MW

Foundry equipment gets similar to particle physics experiment



In de high-NA-scanner moet de waferstage twee keer sneller kunnen versnellen dan de huidige euv-systemen. Bron: ASML, SPIE-presentatie 2017

EUVL manufactured by ASML in NL

estimated cost ~200M$ per stepper

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Basics of microelectronics industry: low-cost mass production

NXP assembly lines
Guandong

they only use own equipment
if > 5-10 x10^9 pieces/year

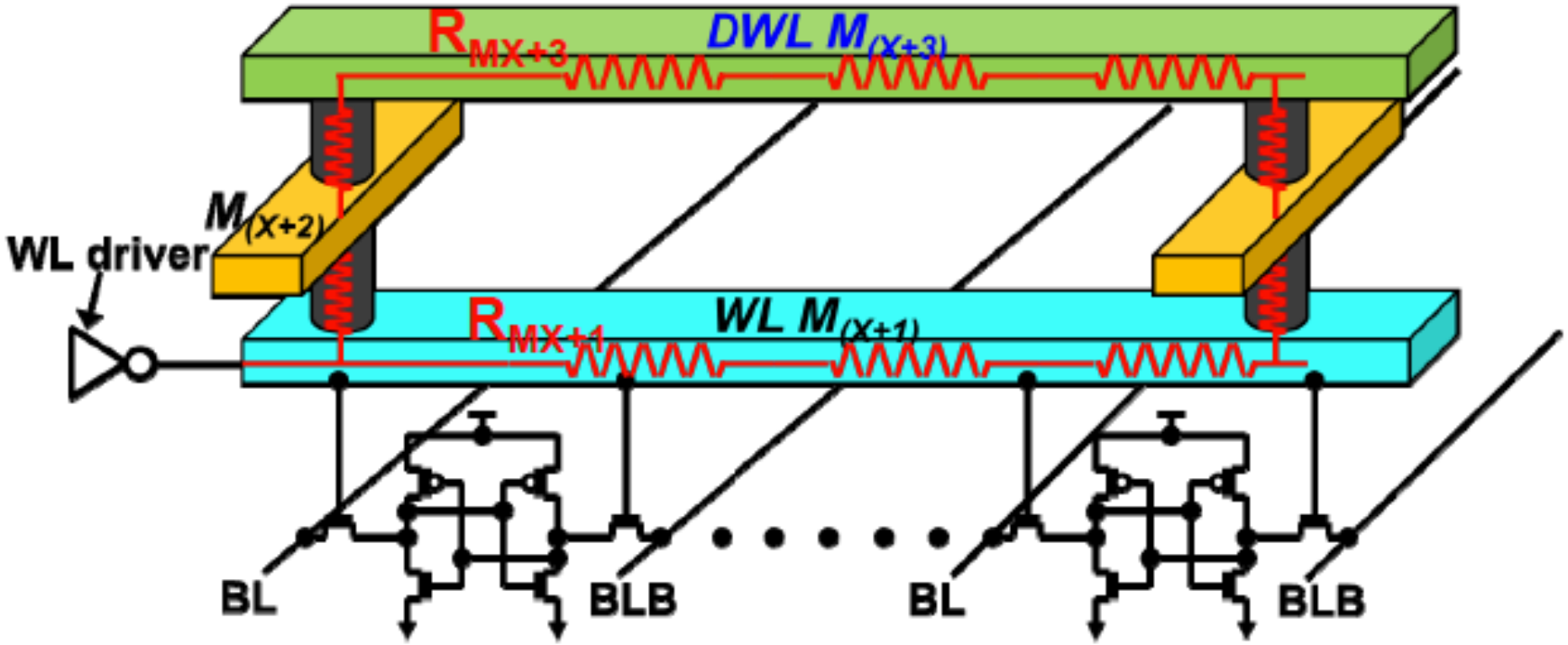
cost reduction e.g.
by flip-chip bonding

→ operators??

Double WL Scheme

Using upper metal as "Double WL" for WL resistance reduction without area overhead

$$Effective\ WL\ Resistance = R_{MX+1} \parallel R_{MX+3}$$



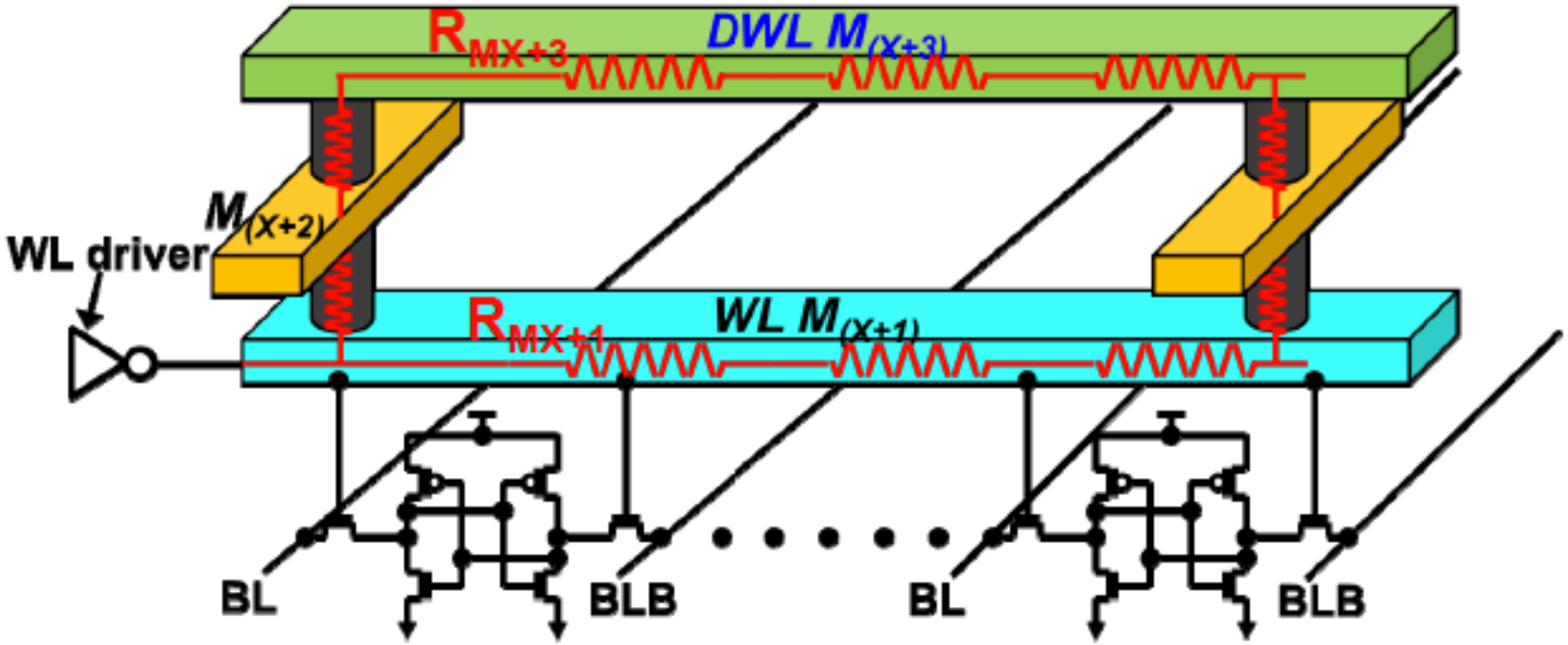
Michael Clinton et al.TSMC. paper 11.3

Double WL Scheme

another improvement to increase speed

resistance reduction without area overhead

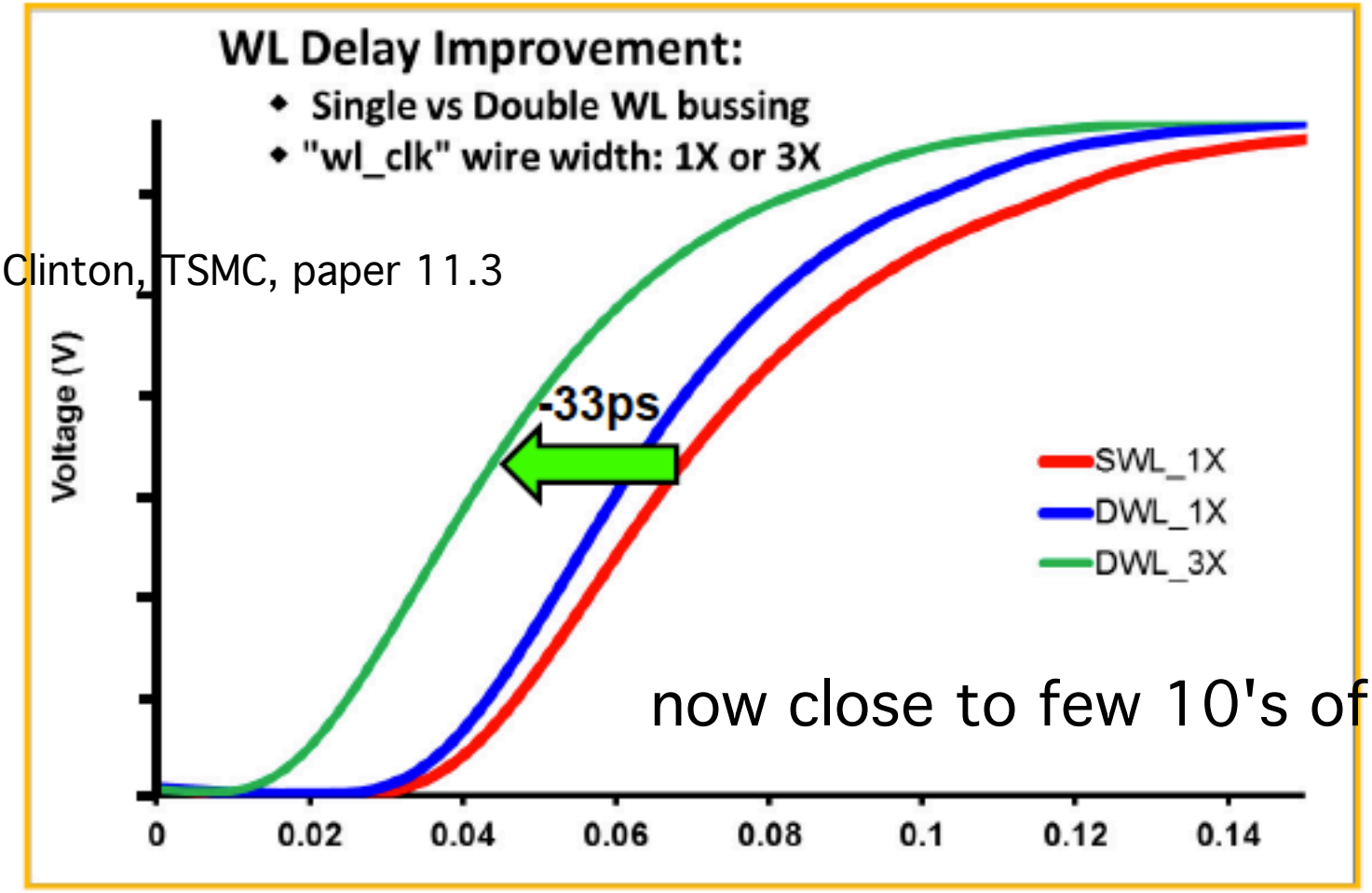
$$Effective\ WL\ Resistance = R_{MX+1} \parallel R_{MX+3}$$



Michael Clinton et al.TSMC. paper 11.3

WL Activation Improvement

WL activation improvement from "Double WL" and "wl_clk" timing improvement due to 3X wider wires



Michael Clinton, TSMC, paper 11.3

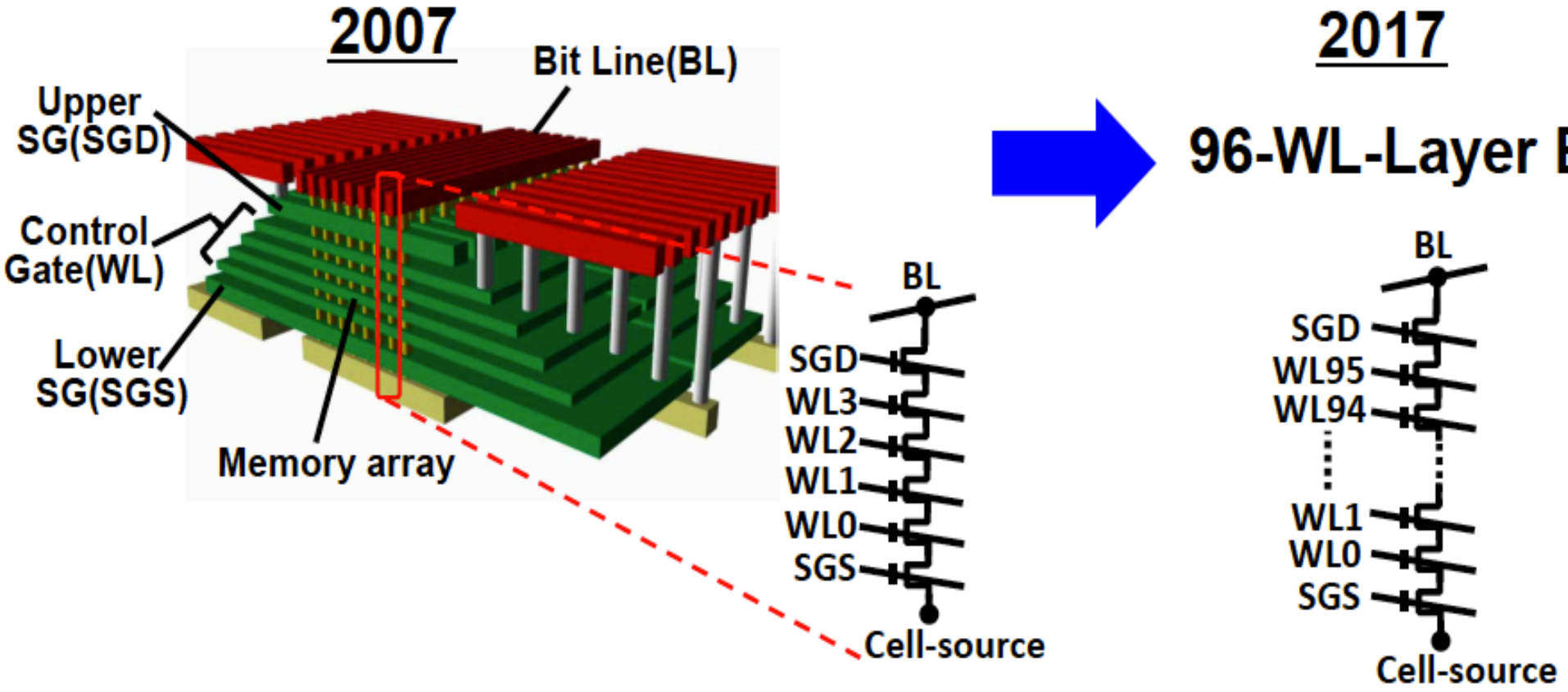
7nm

now close to few 10's of picosec

flash memory drives 3D stacking

Toshiba announced at this conference: 96 layers

10 years from 1st proposed BiCS technology



■ **Multi-layered 3D-flash was reported as BiCS FLASH technology in 2007.**

- [1] H. Tanaka, et al., IEEE Symp. VLSI Technology, pp.14-15, Jun. 2007.

Hiroshi Maejima et al.Toshiba. paper 20.1 512 Gb 3b/cell

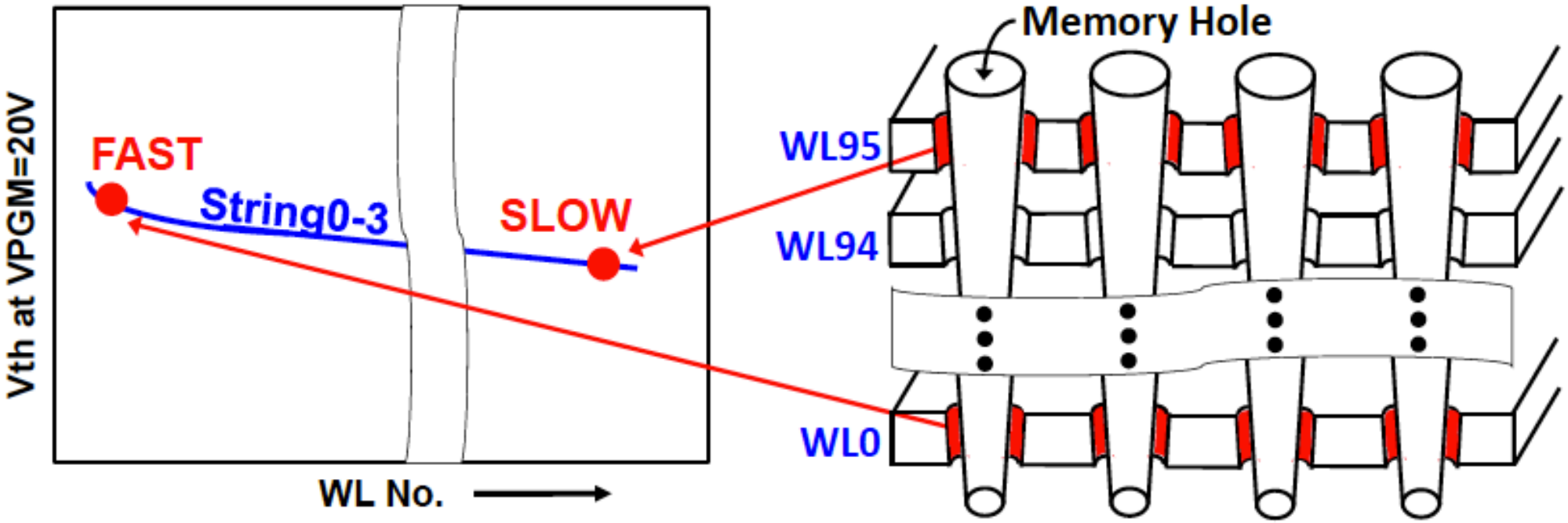
3b/Cell 3D Flash Memory Comparison

ISSCC	[2] J.W.Im, et al., 2015	[3] D.Kang, et al., 2016	[7] T. Tanaka, et al., 2016	[4] R.Yamashita, et al., 2017	[5] C.Kim, et al., 2017	Our work 2018
Technology	32-WL-layer, VNAND	48-WL-layer, VNAND	Floating Gate, CMOS under array	64-WL-layer, BiCS	64-WL-layer, VNAND	96-WL-layer, BiCS
Capacity	128Gb	256Gb	768Gb	512Gb	512Gb	512Gb
# of plane	2	2	4	2	2	2
Die size [mm^2]	68.9	97.6	179.2	132	128.5	86.1
Bit density [Gb/mm^2]	1.86	2.62	4.29	3.88	3.98	5.95

53% up

Hiroshi Maejima et al.Toshiba. paper 20.1

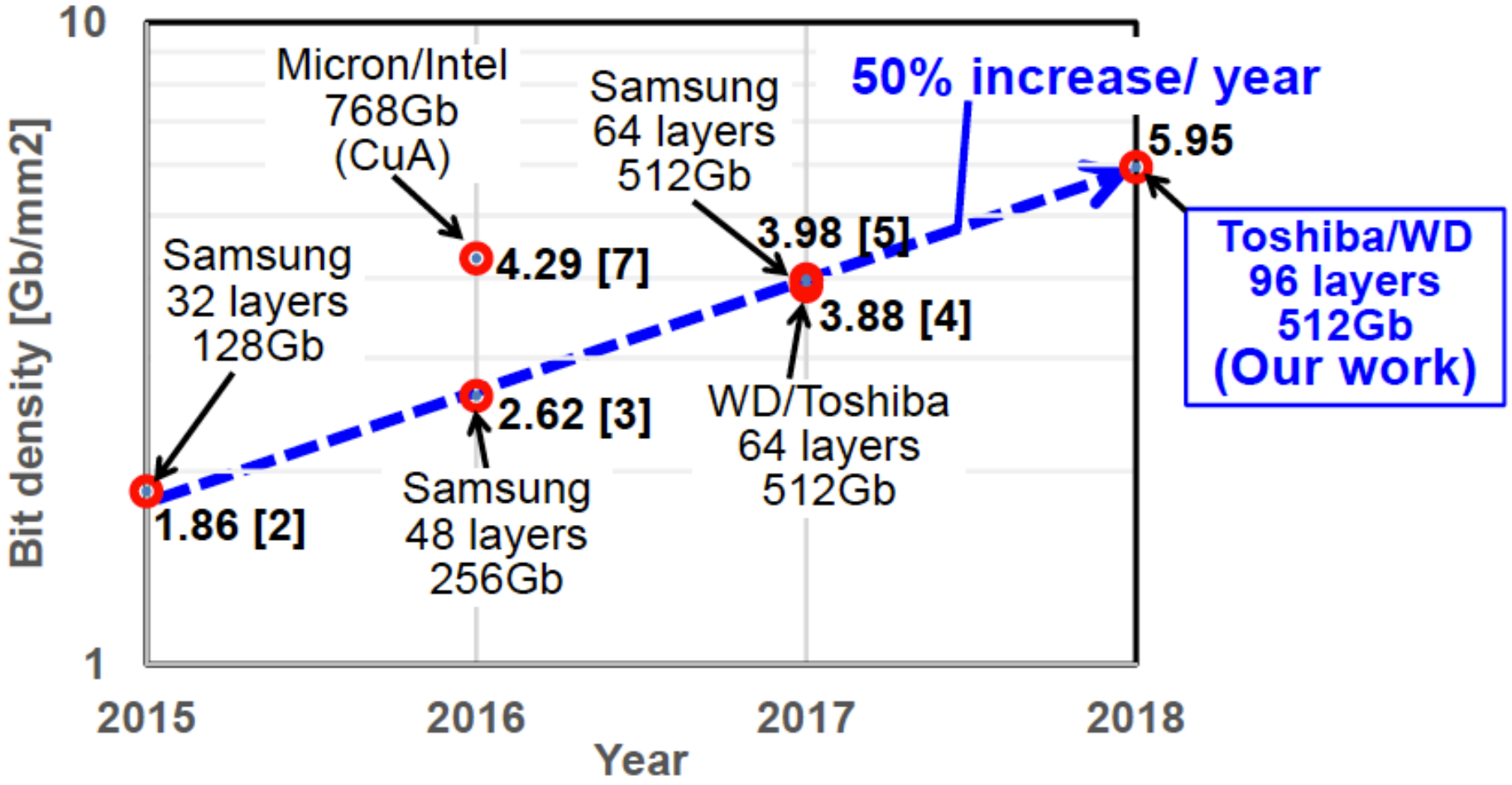
3D FLASH Program speed feature



- 3D Flash memory, program speed characteristic
  - ➔ Strong dependency on WL layers because the memory-hole size gradually varies from layer to layer.
  - ➔ Program speed of cells on common WL layers is almost the same.

Hiroshi Maejima et al.Toshiba. paper 20.1

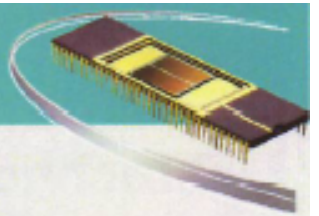
Bit Density Trend(3b/cell 3D Flash Memory)



Hiroshi Maejima et al.Toshiba. paper 20.1

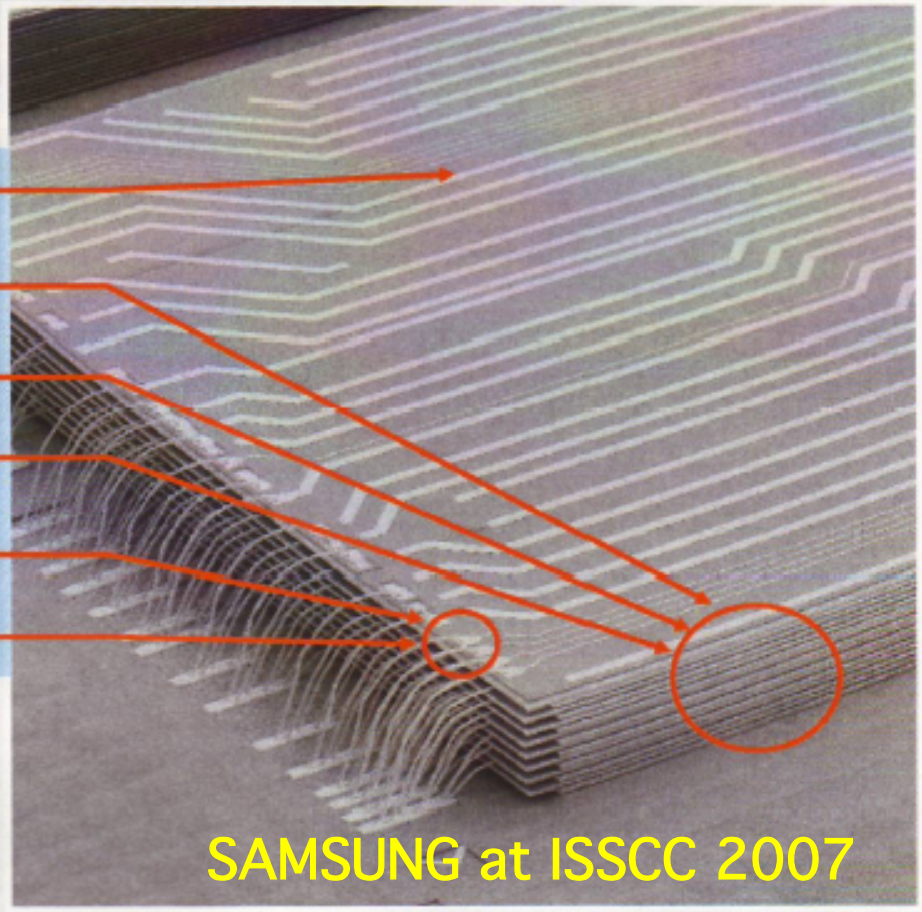
3D STACKING TECHNOLOGY

16 Chip Stacking Technology



❑ 16 Same Die Stack Package Development

- Pad Relocation using WLI
- 30 um Wafer Thinning
- Laser Sawing
- Damage-less Die Pick-up
- 250um Overhang
- 50um Loop Height



SAMSUNG at ISSCC 2007

my seminar in 2009

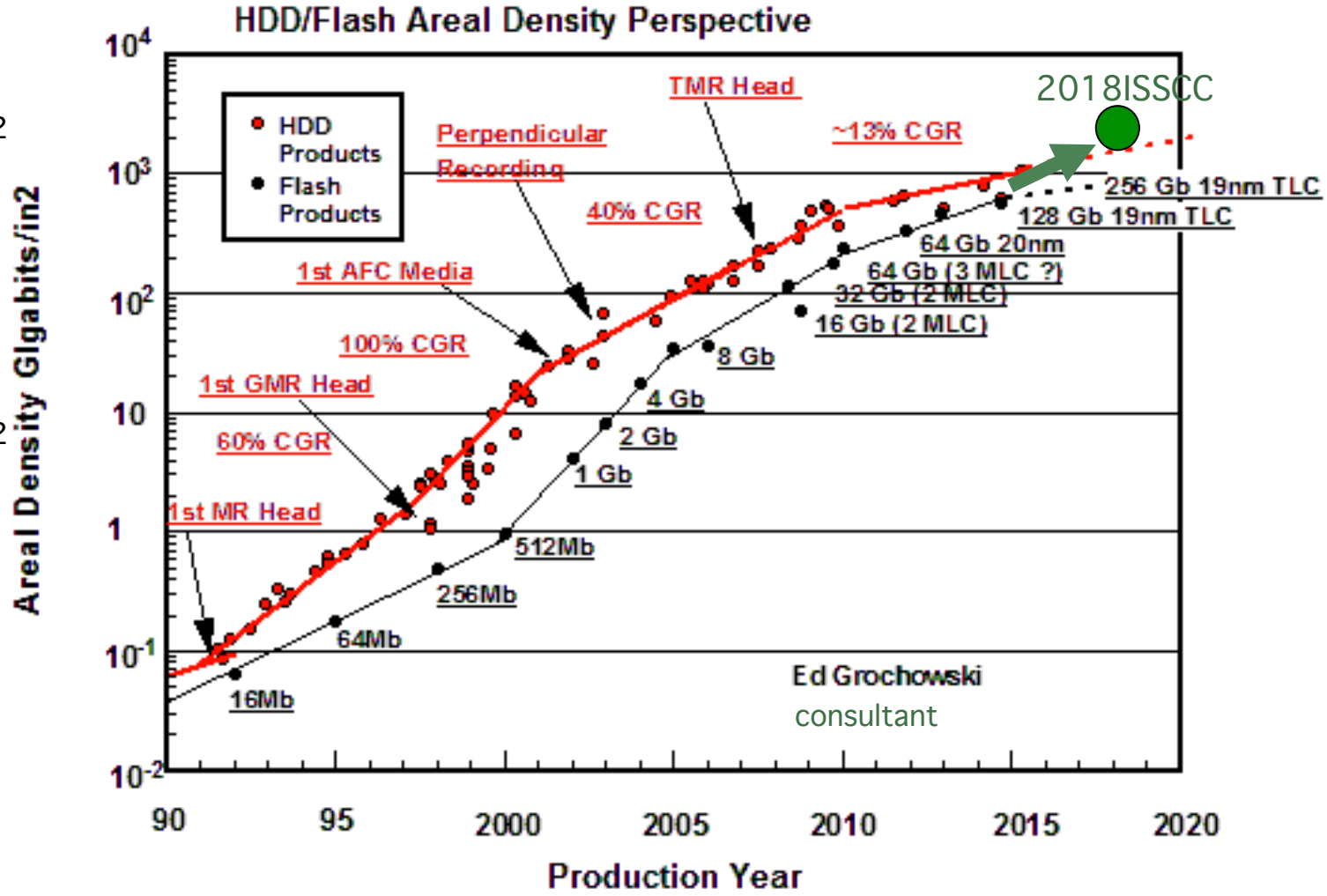
data density in NAND-Flash and magnetic HDD

1 in^2 = 655.4mm^2

2018 ISSCC

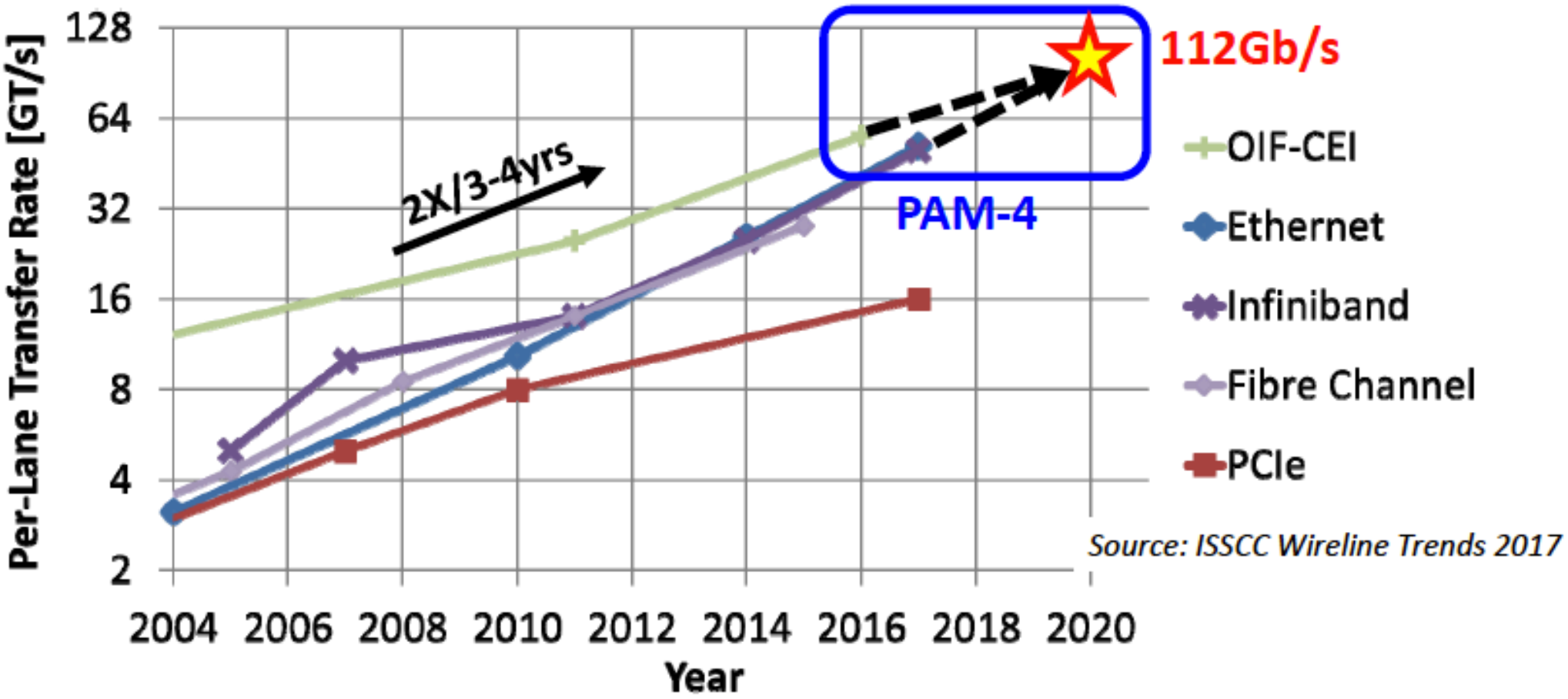
Toshiba chip 512 Gb
5.95 Gb/mm^2
= 3.9Tb / in^2
paper 20.1

Samsung chip 1Tb
5.63 Gb/mm^2
= 3.7Tb / in^2
paper 20.3



data transmission

Data Rate Scaling for Datacenter



- Per-lane data rate has doubled every 3-4 years
- PAM-4 has been adopted for long-reach wireline starting at 56Gb/s

Jihwan Kim et al. Intel; paper 6.1 2.07 pJ/bit

data transmission

Jihwan Kim et al. Intel; paper 6.1

Performance Comparison

	Steffan ISSCC '17	Dickson ISSCC '17	Bassi ISSCC '16	Frans ISSCC '16	This Work		
Technology	28nm FDSOI	14nm FinFET	28nm FDSOI	16nm FinFET	10nm FinFET		
Architecture	Quarter-rate	Half-rate	Half-rate	Quarter-rate	Quarter-rate		
Modulation	PAM-4	PAM-4	PAM-4	NRZ	NRZ	PAM-4	PAM-4
Data Rate	64Gb/s	56Gb/s	45Gb/s	64Gb/s	56Gb/s	56Gb/s	112Gb/s
Clock Source	On-chip PLL	External	External	On-chip PLL	On-chip PLL		
FFE	4-tap	3-tap	4-tap	3-tap	3-tap		
Driver Type	CML	SST	SST-hybrid	CML	CML		
Output Network	Double T-coil	None	T-coil	T-coil	π-coil		
Output Swing w/o FFE	$1.2V_{ppd}$	$0.9V_{ppd}$	$1.3V_{ppd}$	$0.8V_{ppd}$	$0.75V_{ppd}$		
RJ - Clock Pattern	$290fs_{rms}$	$318fs_{rms}$	NA	$150fs_{rms}$	$154fs_{rms}$		
RLM	94%	NA	94%	NA	NA	99.3%	98.5%
SNR	NA	NA	NA	NA	NA	>31dB	31dB
Energy/bit (TX+Clock Distribution)	2.26pJ/bit** (w/o PLL)	1.8pJ/bit (w/o PLL)	NA	5.31pJ/bit	4.14pJ/bit	1.9pJ/bit	2.07pJ/bit
Energy/bit (TX FE only)	NA	NA	2.66pJ/bit	3.51pJ/bit	3.44pJ/bit	1.7pJ/bit	1.72pJ/bit
TX Area (w/o PLL)	NA	$0.035mm^2$	$0.28mm^2$	$0.32mm^2$	$0.0302mm^2$		

data transmission

Christian Menolfi et al. IBM+ETHZ+EPFL; paper 6.2

including Thomas Toifl

Summary / Conclusion

2.55 pJ/bit

DAC based CMOS Transmitters at Fs > 50GS/s				
	[2] Greshishchev ISSCC 2011	[3] Cao ISSCC 2017	Huang RFIC 2014	This work
Technology	65 nm	20 nm	28 nm	14 nm
Sampling Rate	56GS/s	64GS/s	100GS/s	56GS/s
Data Rate	56Gb/s NRZ	64Gb/s NRZ		112Gb/s PAM4
Resolution	6b	8b	8b	8b
SFDR < 10GHz	38dBc	~47dBc	~36dBc @80GS/s	42dBc
Full Scale Output	600 mVppd	700 mVppd	~879 mVppd	920 mVppd
Driver	CML	CML	CML (distributed)	SST
Supply	1.1V + 2.5V	1V + 1.8V	1.1V + 1.5V + 2V	0.95V
Power	750mW (PLL incl)	620 mW	2.5W	286 mW (FFE incl)

power conversion

GaN or SiC have larger bandgaps

allows higher voltages, larger steps and lower leakage

D. Risbud/ Dialog Semiconductor Santa Clara
mentioned GaN DC-DC 100V --> 1V also in magn field??

Si CMOS imagers

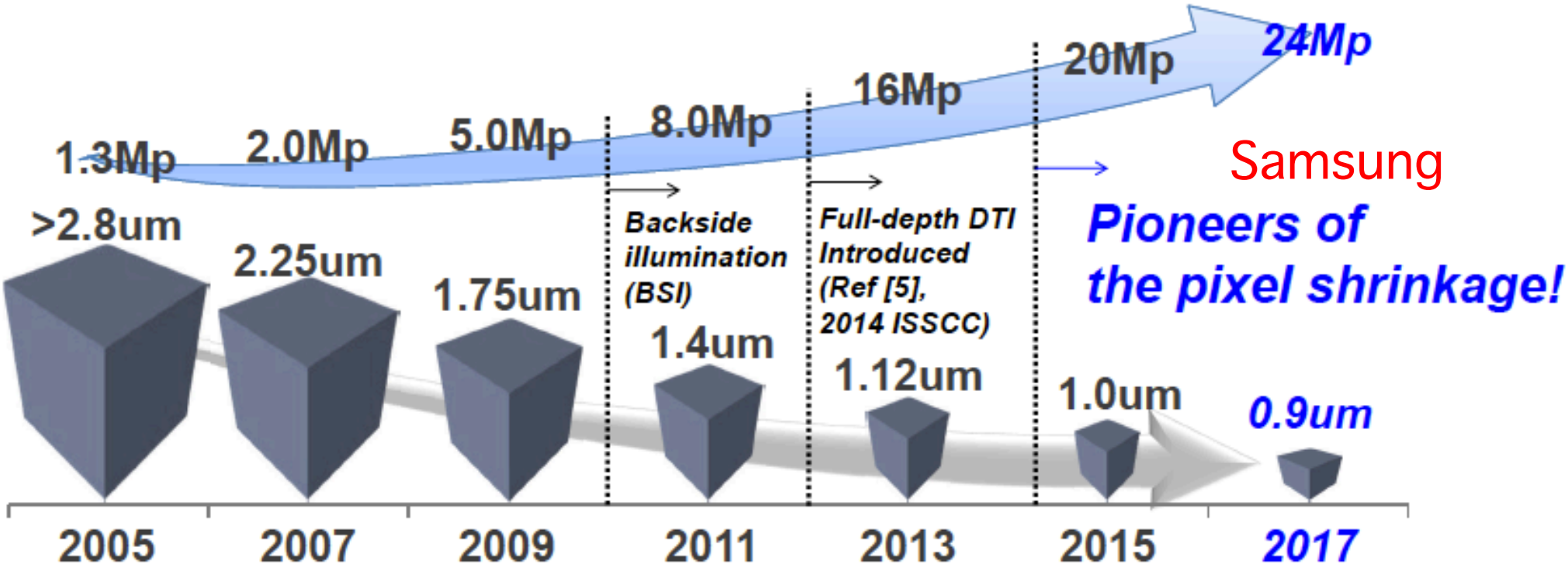
Si CMOS imagers

- turnover growing >10% per year since ~2005
- more than 4×10^9 sold in 2015

Pixel shrinkage and resolution trend

Recent mobile market trend

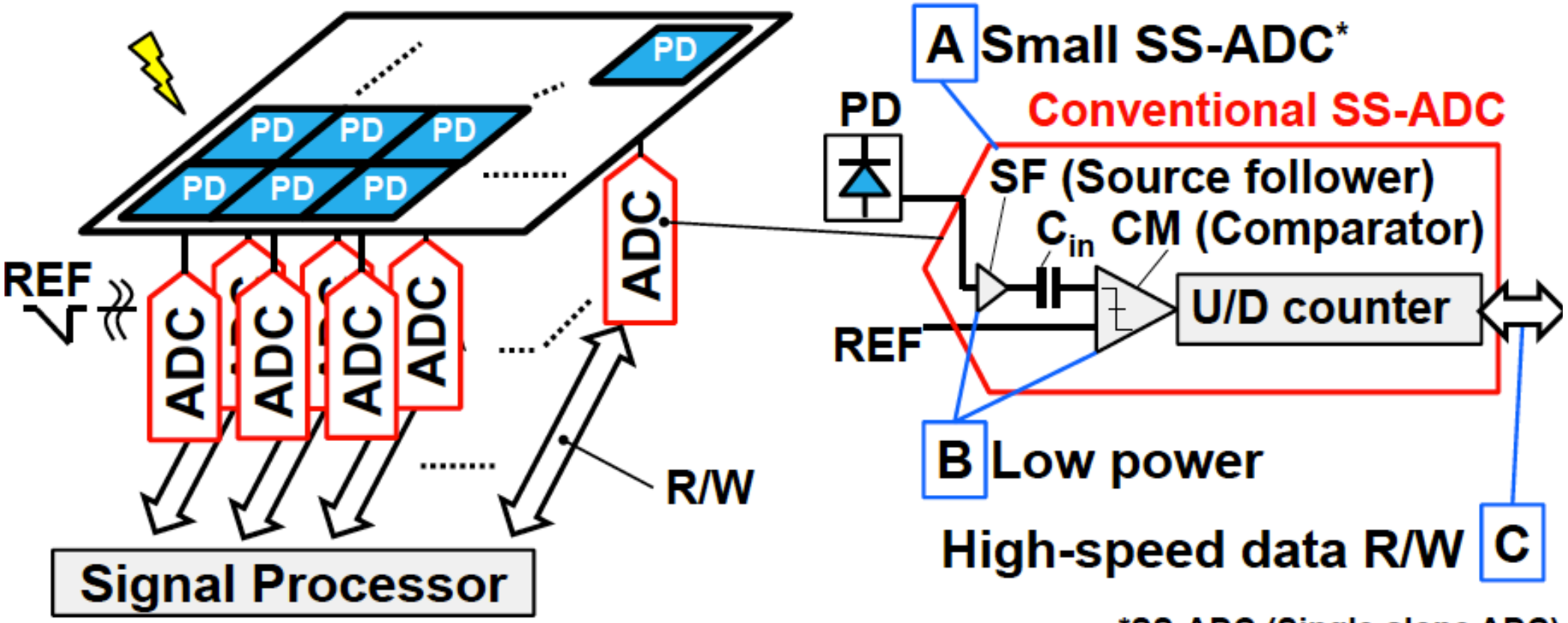
➔ ***Higher-resolution images*** and ***smaller module size***



Wonchul Choi et al.Samsung; paper 5.3

visible imaging with ADC on each pixel

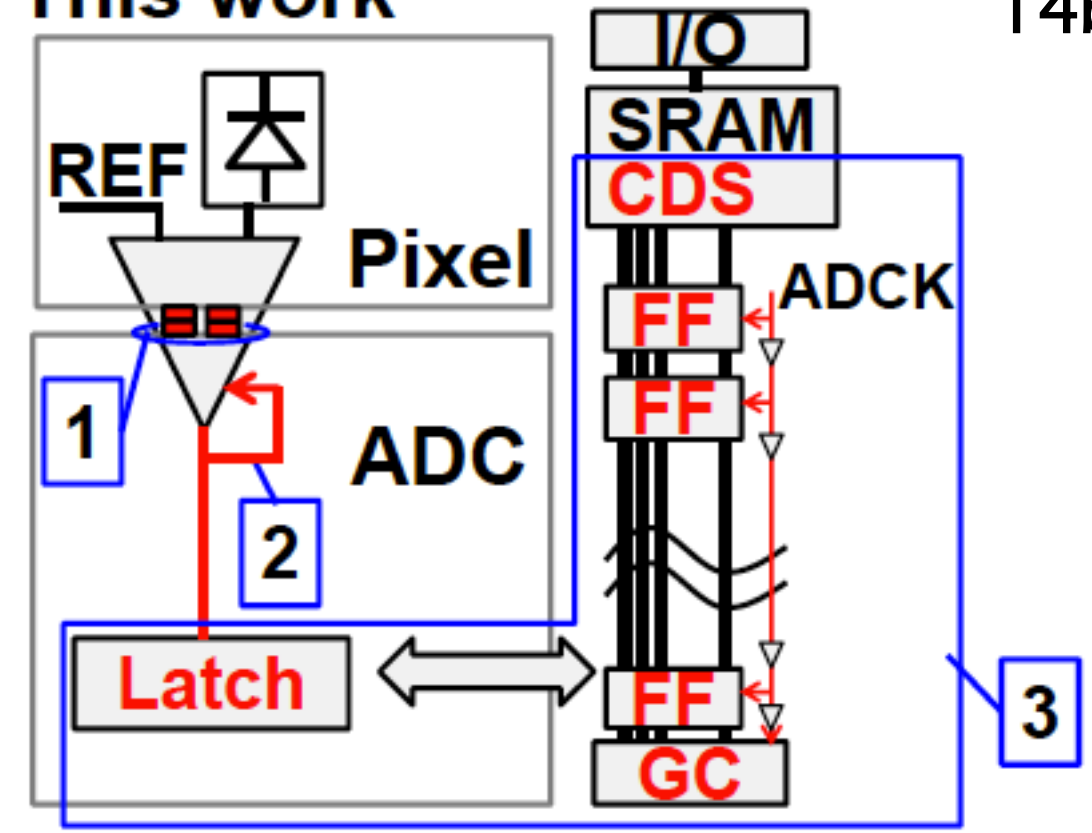
Three main issues in implementing SS-ADC* per pixel



M. Sakakibara et al.Sony; paper 5.1

This work

14b ADC per pixel in 6.9μm^2

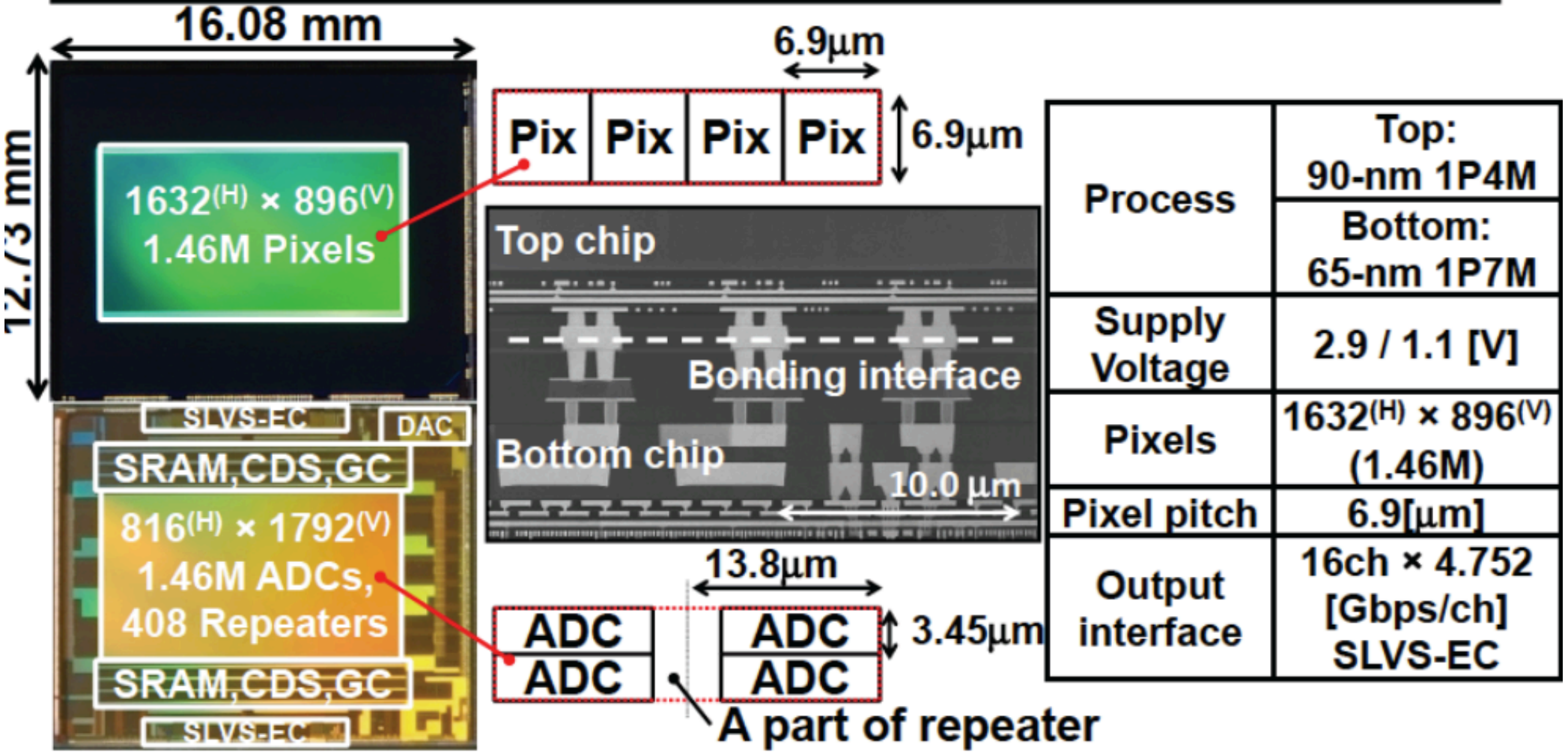


1 Pixel-level Cu-Cu connection
2 Subthreshold + standby control
3 Data transmission architecture

M. Sakakibara et al.Sony; paper 5.1

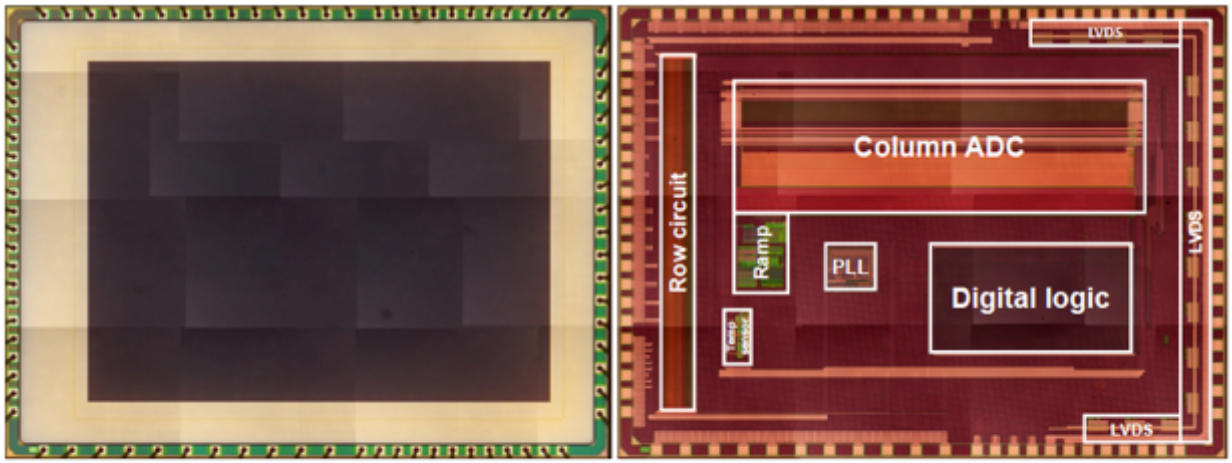
Stacked imager

Implementation result



Process	Top: 90-nm 1P4M Bottom: 65-nm 1P7M
Supply Voltage	2.9 / 1.1 [V]
Pixels	1632(H) × 896(V) (1.46M)
Pixel pitch	6.9[µm]
Output interface	16ch × 4.752 [Gbps/ch] SLVS-EC

Stacked imagers now commonplace (5 in10 papers)



Top Chip
Pixel array

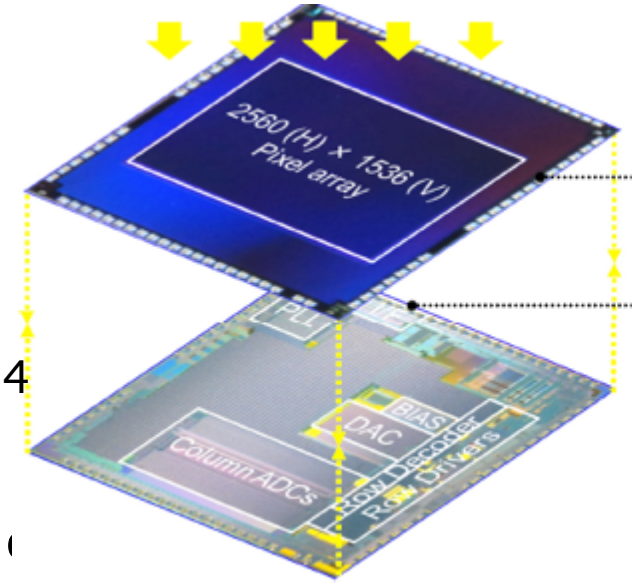
Bottom Chip
Peripheral circuit

1.1 μm pixels
motion detection

Po-Sheng Chou et al.TSMC; paper 5.5

1.5 μm pixels
event driven
10b ADC

Oichi Kumagai et Sony; paper 5.4



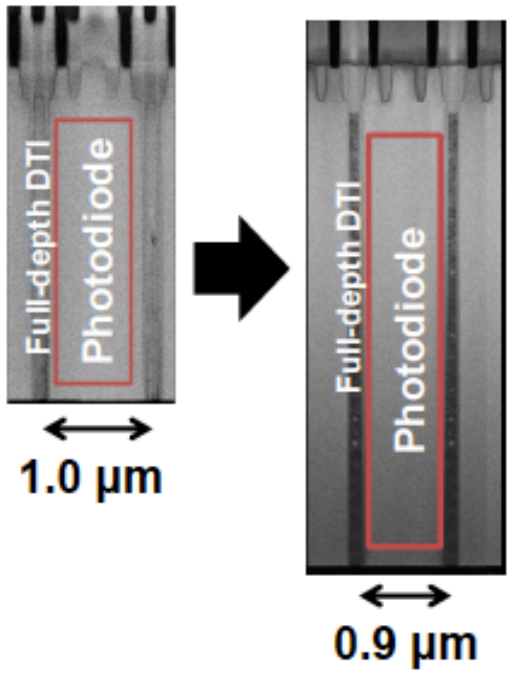
2-layer stacked structure
(BI-CIS)

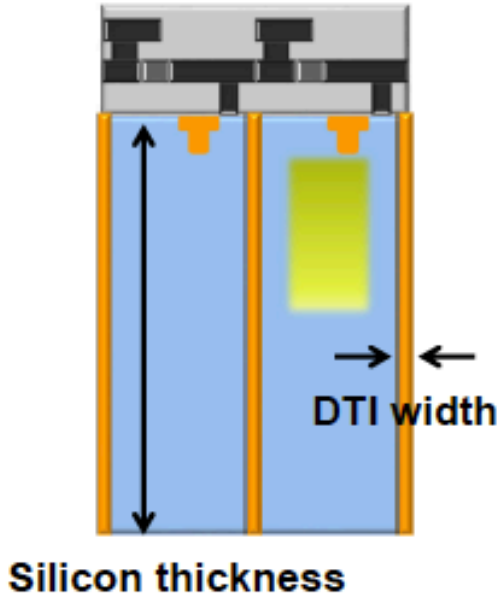
Top layer : 1.8V
- Low-Voltage Pixel

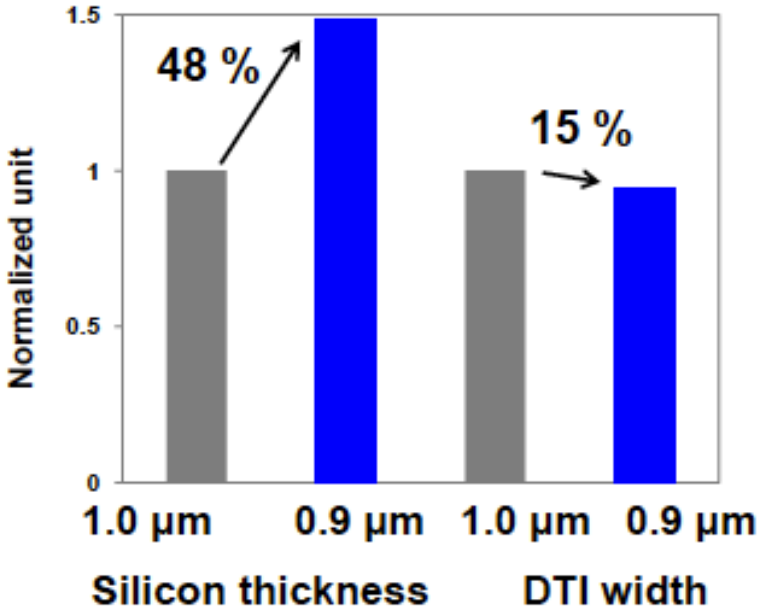
Bottom layer : 1.8V/1.0V
- PLL/MIPI D-PHY
- Column ADCs
- DAC/BIAS
- Row Decoder/Drivers
- Motion Detection
- Optical Detection

Samsung submicron imager with deep-etched separation

*1st gen 1.0 um pixel







'thick' Si : now 4μm instead 2.7μm to improve signal in red

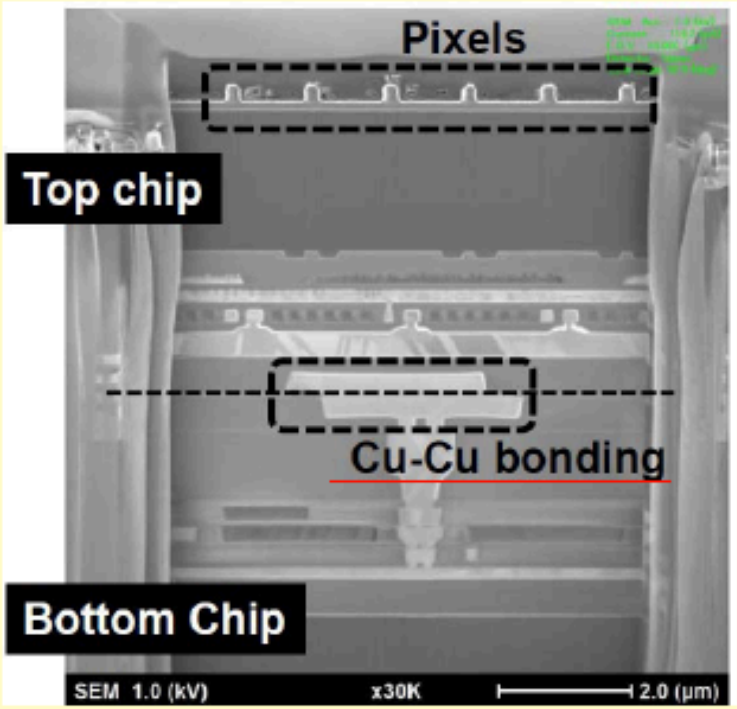
Stack (4). Wafer–to–Wafer Hybrid Direct Bonding

- **Oxide bonding**
  + TSV(Through silicon via)

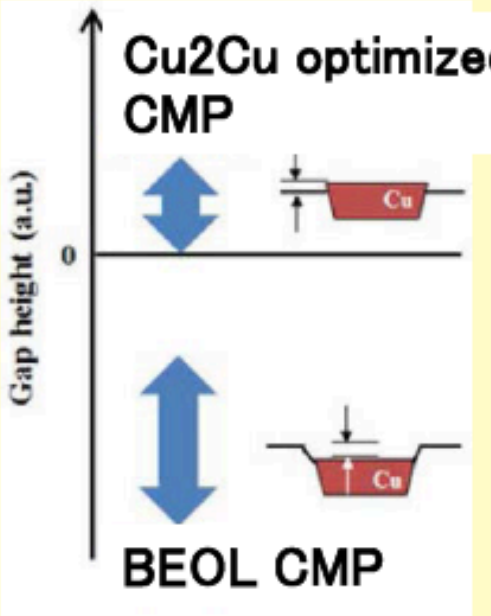
Interconnections are limited at only peripheral.

- **Hybrid bonding**

Interconnection can be located at pixel array also.



K. Shiraishi et al. (Toshiba), ISSCC 2016

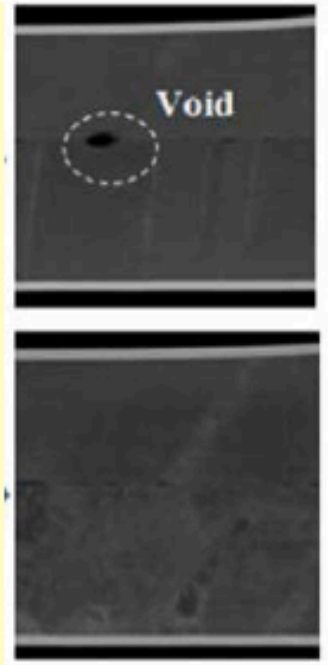


CMP optimization

Y. Kagawa et al. (Sony), IEDM 2016

< 150 ℃

400 ℃



Post–bond annealing

- **2 um pitch interconnection**

E. Beyne (IMEC), 2018

Future particle imagers at colliders

technical/electronics possibilities
- smaller/thinner pixels and more layers

advantages for the physics?
- increase number of points along tracks
- improve precision on momentum measurements
- disentangle composition of jets
- more complete image of the interaction products

+ operational advantages

IMPORTANCE OF Q/C

Often thermal noise from the input transistor dominant, in that case:

$$\frac{S}{N} \sim \frac{Q/C}{\sqrt{gm}} \sim \frac{Q}{C}\sqrt[m]{I} \sim \frac{Q}{C}\sqrt[m]{P} \; with \; 2 \le m \le 4$$

m = 2 for weak inversion
m = 4 for strong inversion

For constant S/N: $$P \sim \left[\frac{Q}{C}\right]^{-m} \; with \; 2 \le m \le 4$$

Collected charge Q over sensor/input capacitance C ratio:

- Determinant for analog power consumption
- Very important figure of merit for a particle sensor
- Want SMALL collection electrode for low C
- Interest of sensor segmentation

fundamentals from Walter Snoeys

for mip's
smaller capacitance allows
larger S/N
& lower power

aim at pixel 3x3x3 μm^3
voxel
even smaller is possible

capacitance ~0.3fF
noise <15 e^- rms (?)
mip signal ~150 e^-

11 million cells/cm^2

Future particle imagers at colliders

advantages for 3μm pixels in multiple layers

track vector parameters locally available

possibility to determine primary vertex at 1st level

<< ns signal collection improves timing precision

short signal path improves radiation hardness

reduced carrier trapping probability

high field possible even at low voltage

reduction of coordinate corruptions by delta electrons

....

ISSCC developments to be exploited in experiments

Size reduction and 3D stacking
lower power more functionality
picosecond domain and faster processing accessible

Data transmission
increase speed and data volume, better drivers
new ideas ? use RF besides cables and fibers?

Memory developments (now main drivers of technology)
shift the balance between local or distant processing

GaN and SiC in power conversion circuits

Imagers move to 3D hybrid
even in the low-cost, visible applications
...

Progress

needs

which performance can more advanced technologies achieve

good knowledge of their details

building up of practical insight and expertise

cleverness in circuit design

intensive contacts about commercial practices

study of our special environment: radiation and magnetic field

how to convince our own community of the obvious advantages

Thank You