Discharge protection of CMOS pixel chips in Micromegas MPGDs

Nikhef
MESA+
University of Bonn
IZM-Berlin Fraunhofer
CEA- Saclay
Neuchatel EPFL-LMTS

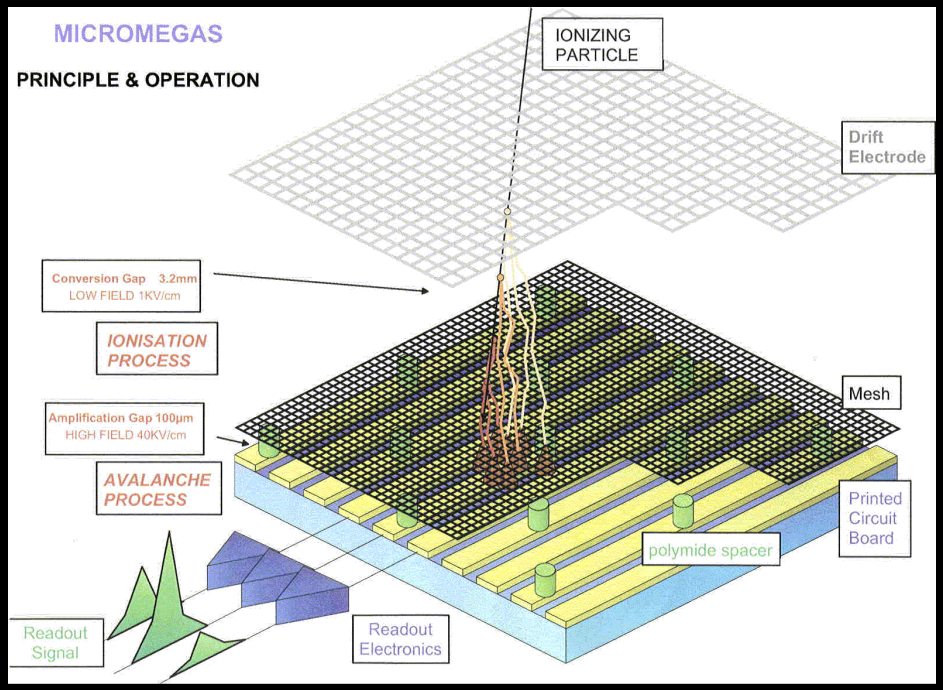
Re-presented by Harry van der Graaf

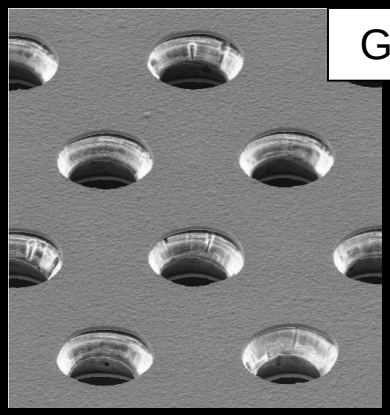
RD 51 MPGD Stability Workshop, Munich
Munich, June 21, 2018

Micro Patterned Gaseous Detectors (MPGDs)

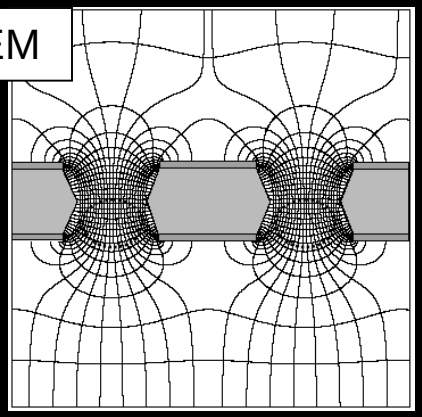
1995

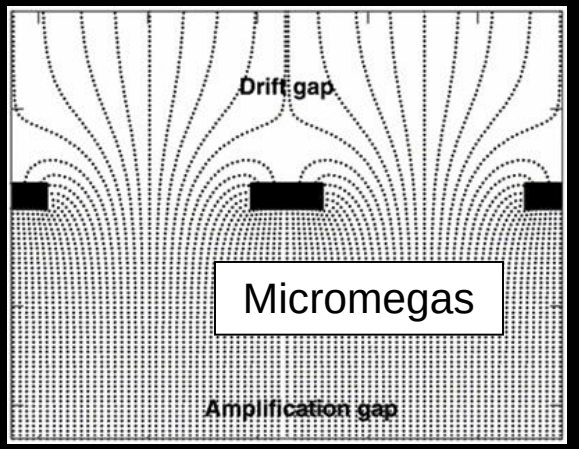
- High field created by Gas Gain Grids
- Most popular: GEM & Micromegas





GEM





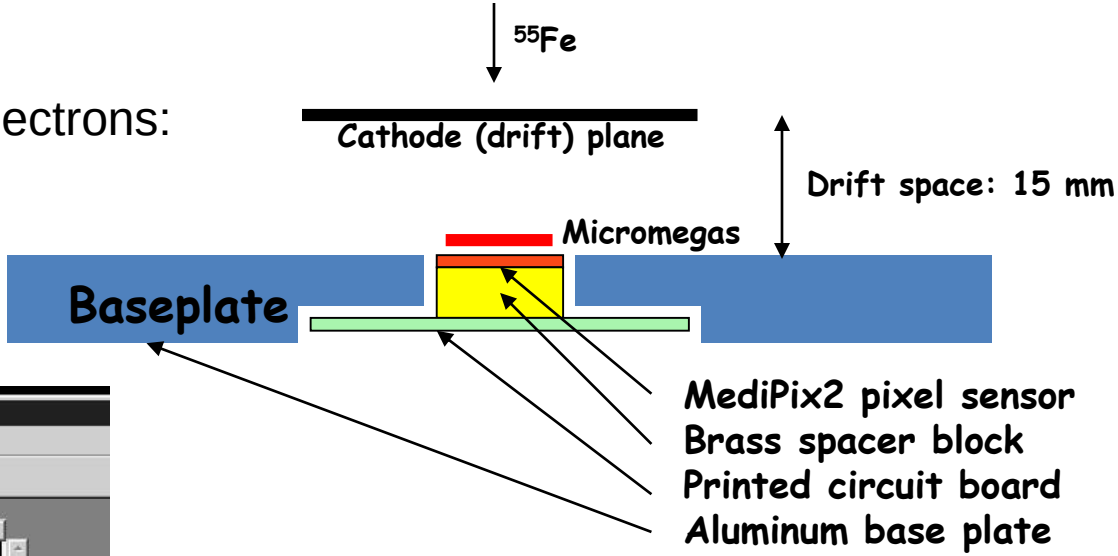
improved granularity : wire chambers react on COG of many electron clouds/clusters

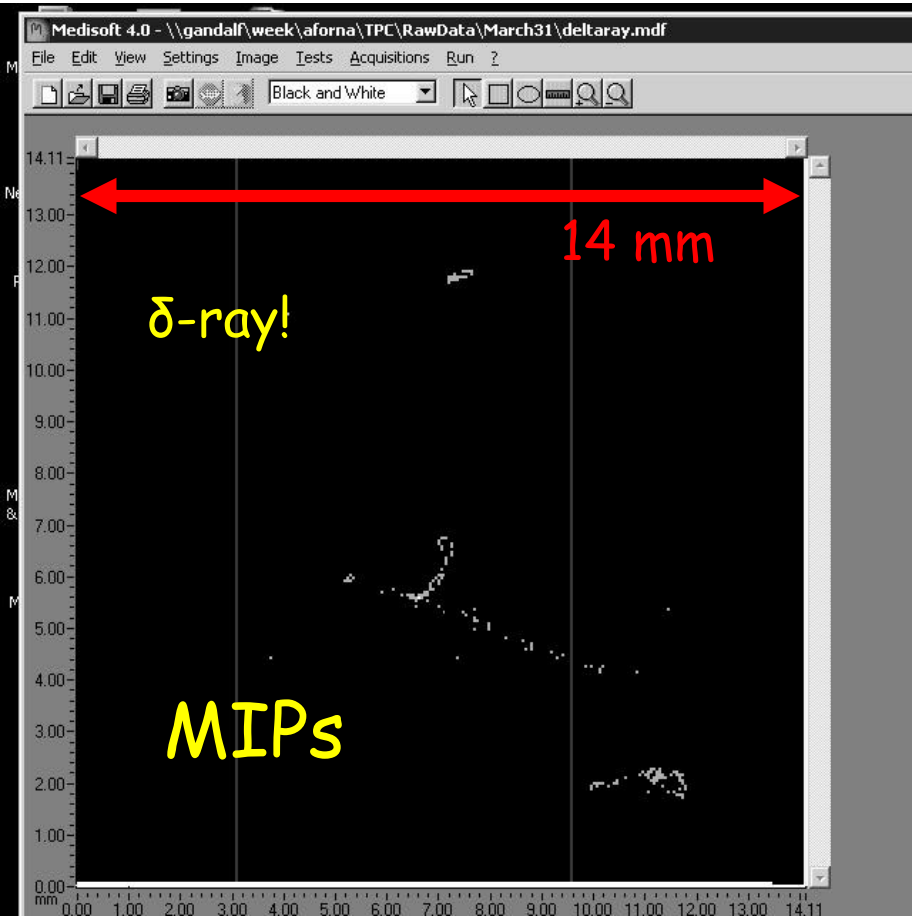
2D detector

April 2004 Micromegas + MediPix 2

NIKHEF/Saclay/Univ. Twente

enough gas gain to see individual electrons:
MIP tracking





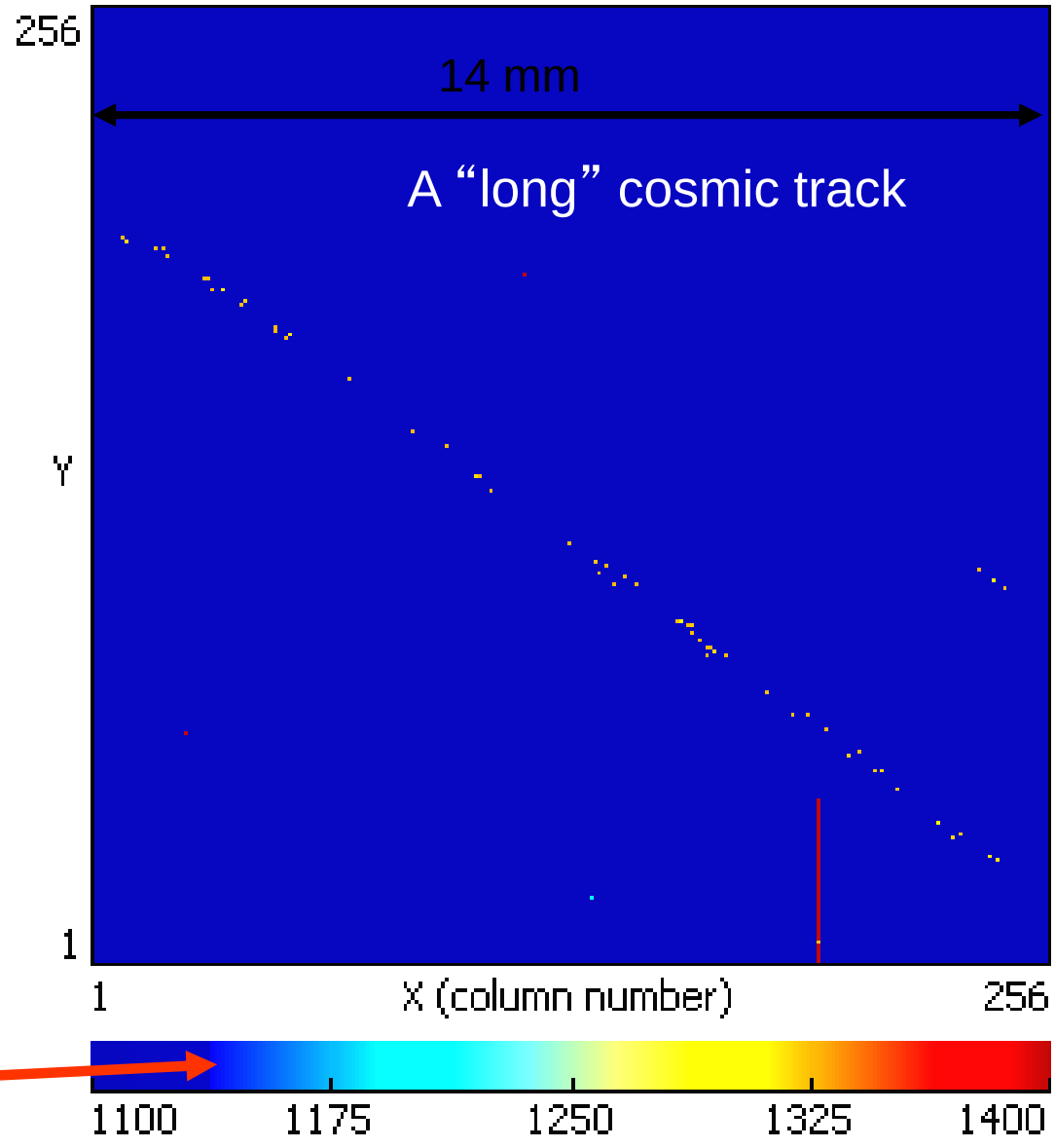
He/Isobut
80/20
Modified MediPix

Paul Colas, Yannis Giomataris

cathode @ - 1500 V

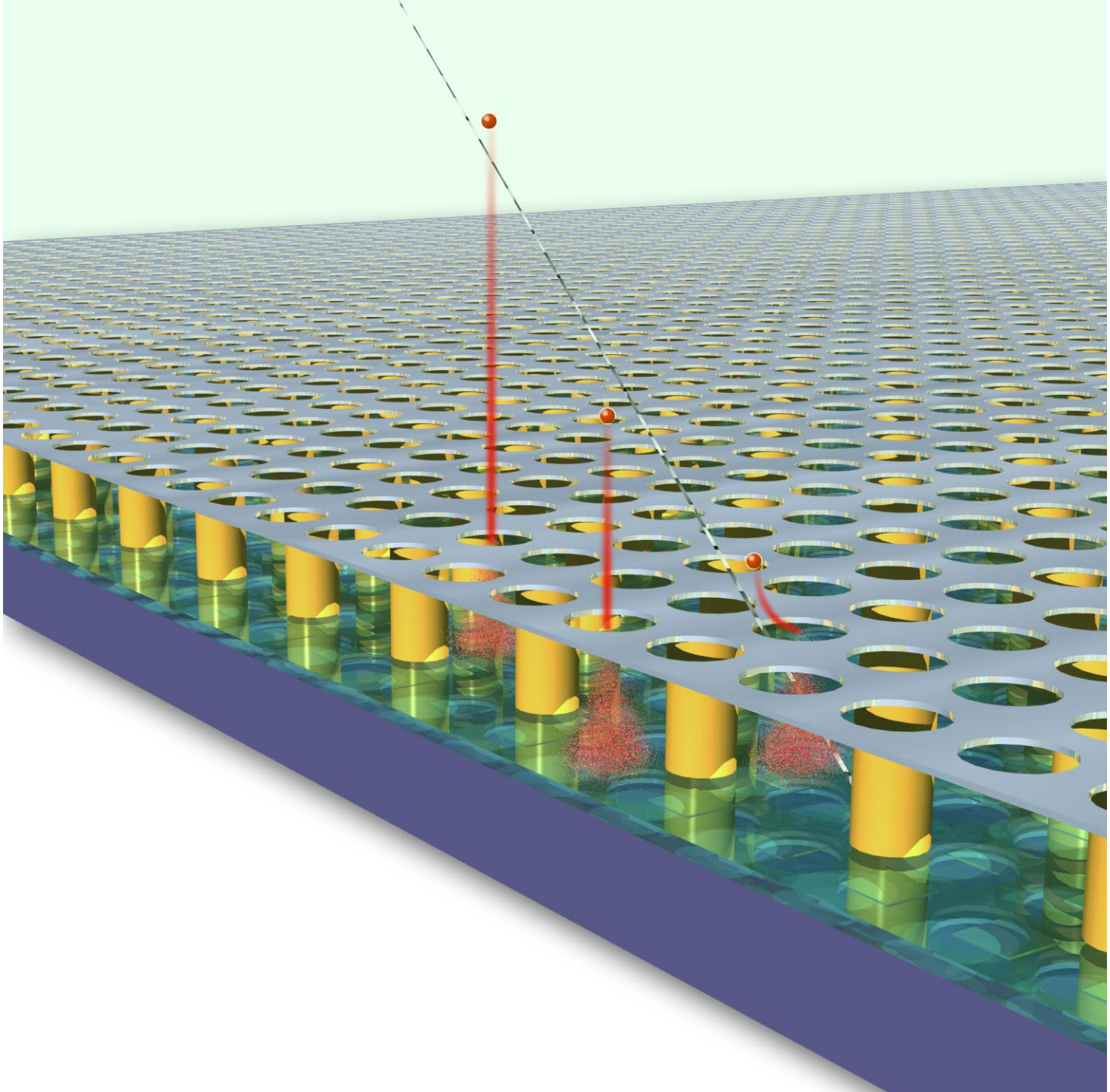
10 mm

Timepix
+
20 µm thick Siprot
+
Ingrid



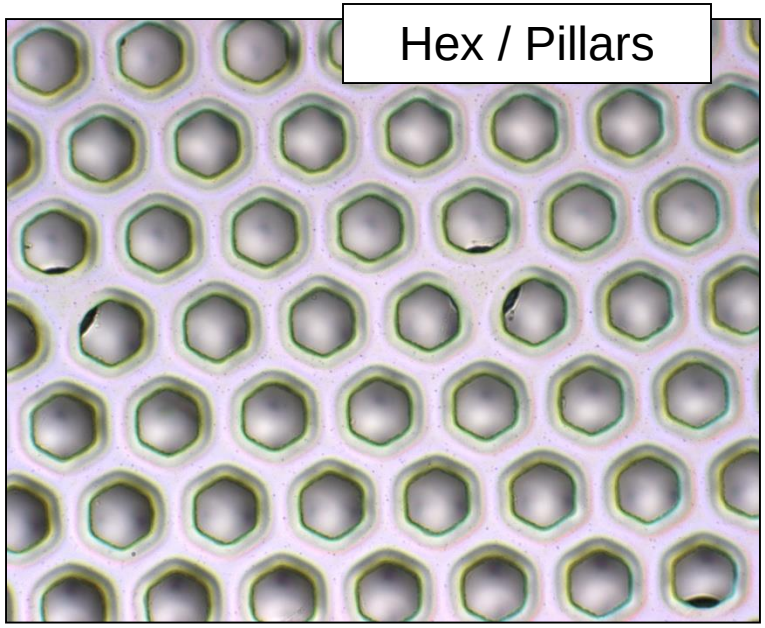
Drifttime (bin = 10 ns)

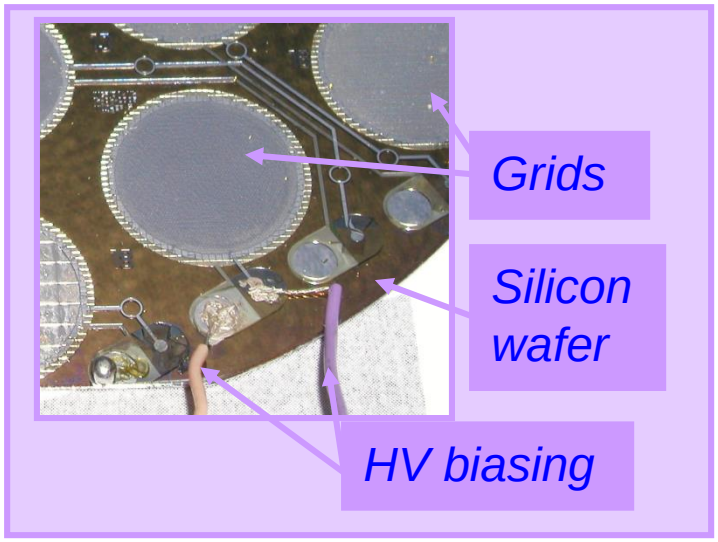
Stable operation in He iC4H10



2006 – 2007

Wafer post-processing: InGrid





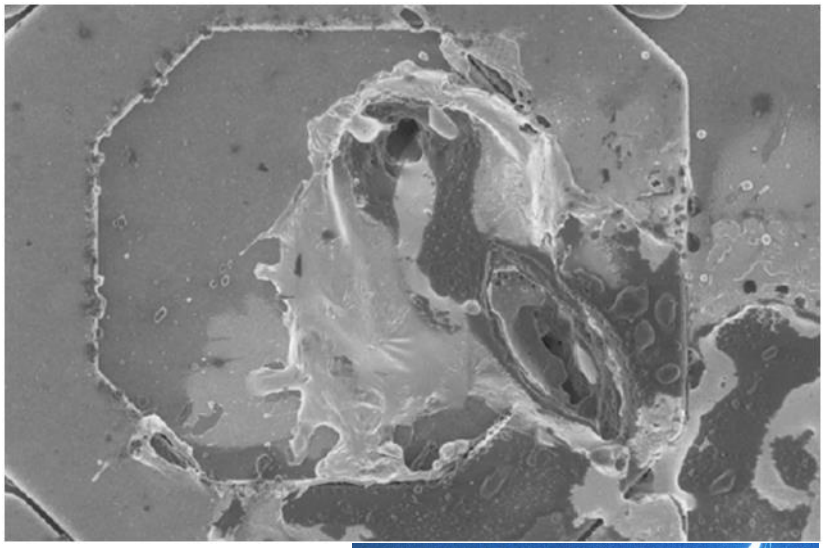
InGrid: an Integrated Grid on Si (wafers or chips)

- perfect alignment of grid holes and pixel pads
- small pillars Ø, hidden pillars, full pixel area coverage
- Sub-micron precision: homogeneity
- Monolithic readout device: integrated electron amplifier

Max Chefdeville, Victor Blanco Carballo

Discharge (spark) protection

2006-2007 dead chips everywhere
2007-2008 spark protection and Ingrid
2008-2009 characterizing performance
of GridPix

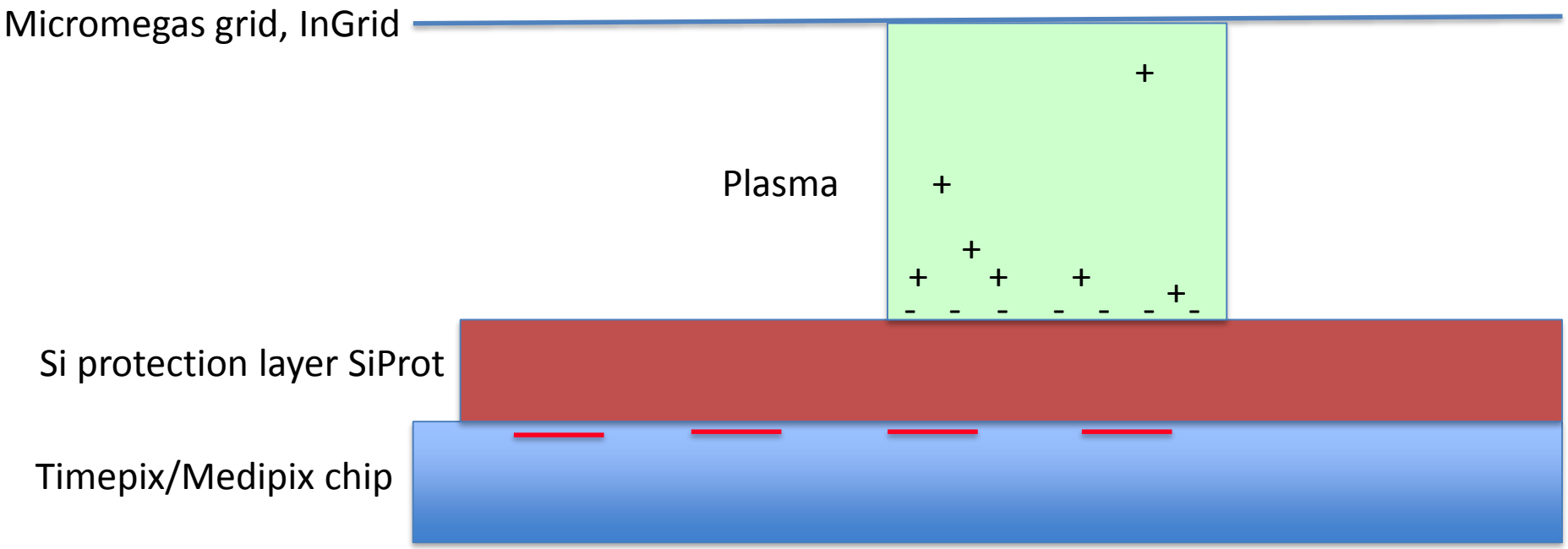


Apply principle of Resistive Plate Chamber (RPC):
quench discharge before completion
by covering the chip with a high-resistivity
protection layer

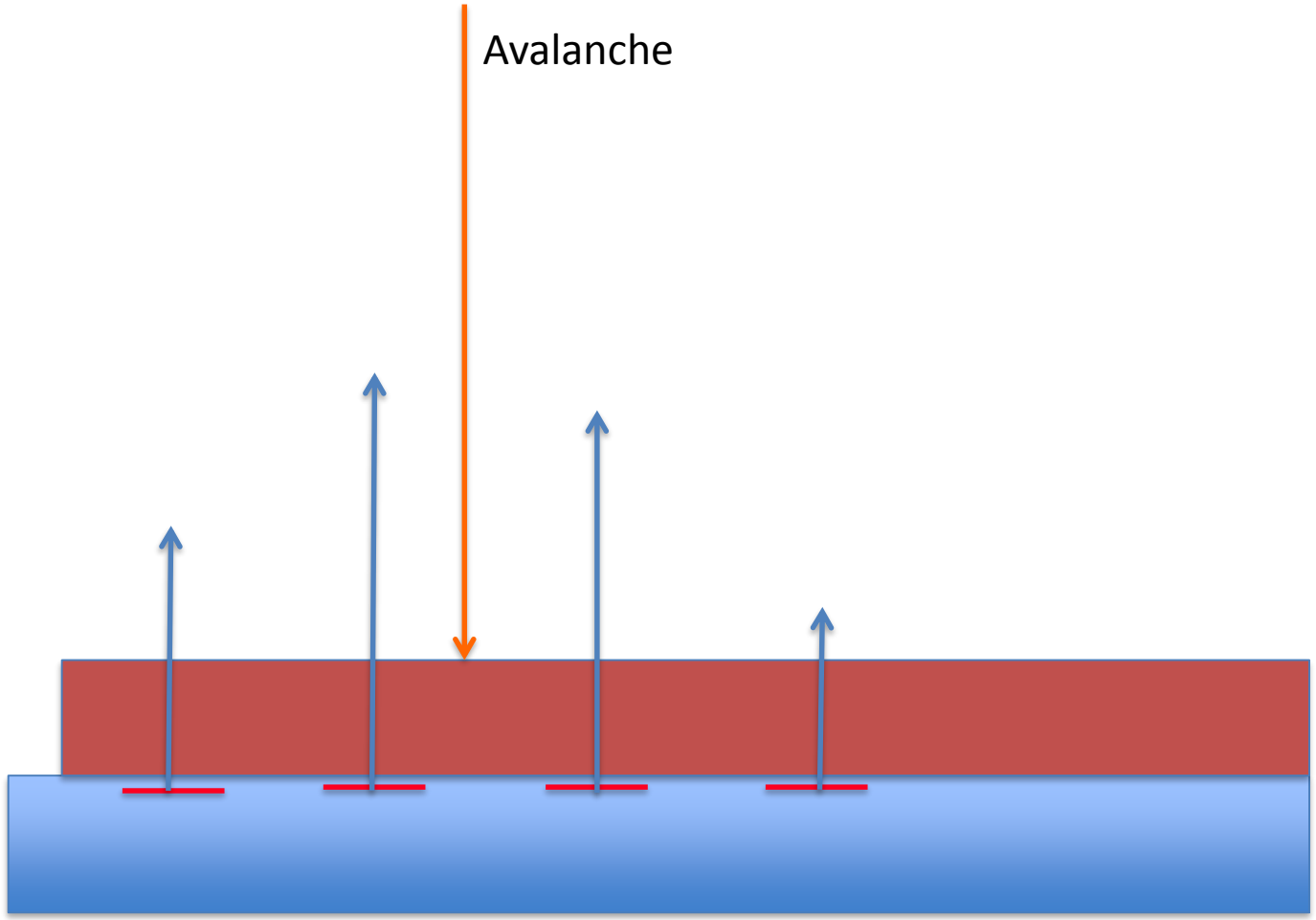
Pierre Jarron: pioneered H-Si layer on Medipix as direct X-ray convertor

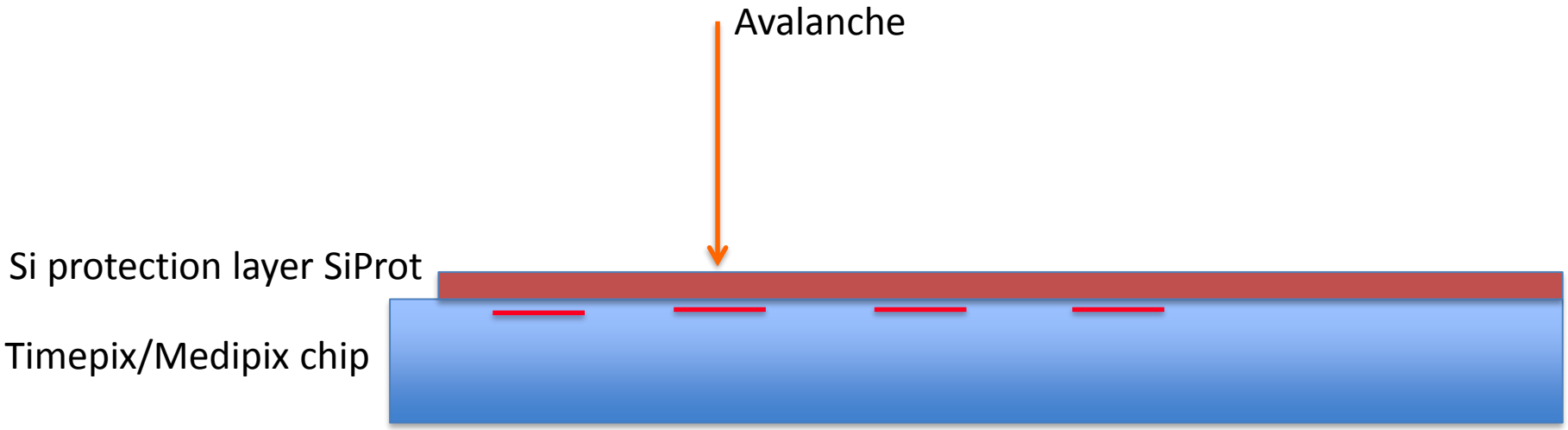
Nicolas Wyrsch: (IMT Neuchatel, now EPFL-Neuchatel): Solar panel studies using (low cost) H-Si layer on glass/foil substrate

1) Quenching: surface charge reduces E-field in plasma area
2) Protection of pixel chip surface area against hot plasma



This is NOT related to charge spreading (enabling interpolation of digital charge info)





Normal (avalanche signal): induced charge almost equal to avalanche (electron) charge as long as layer thickness is small with respect to pixel input pad diameter.
True for Medipix and TimePix -1
TimePix 3 has 10 micron diameter input pads: some signal loss.

Specific resisitivity ρ of SiProt

Virtual time constant τ of layer-on-conducting substrate:
Assuming equipotential at layer top surface

capacitor: $C = A\varepsilon_0 k/D$ resitivity: $R = \rho D /A$, so $\tau = RC = \rho \varepsilon_0 k$

Time constant associated with discharges (streamers) pico-seconds:sets lower limit on ρ.
Normal signal current reduces potential of upper layer surface: sets upper limit
Resistance between two input pads must be high enough (avoiding input noise). Sets upper limit.

… discharges are observed !

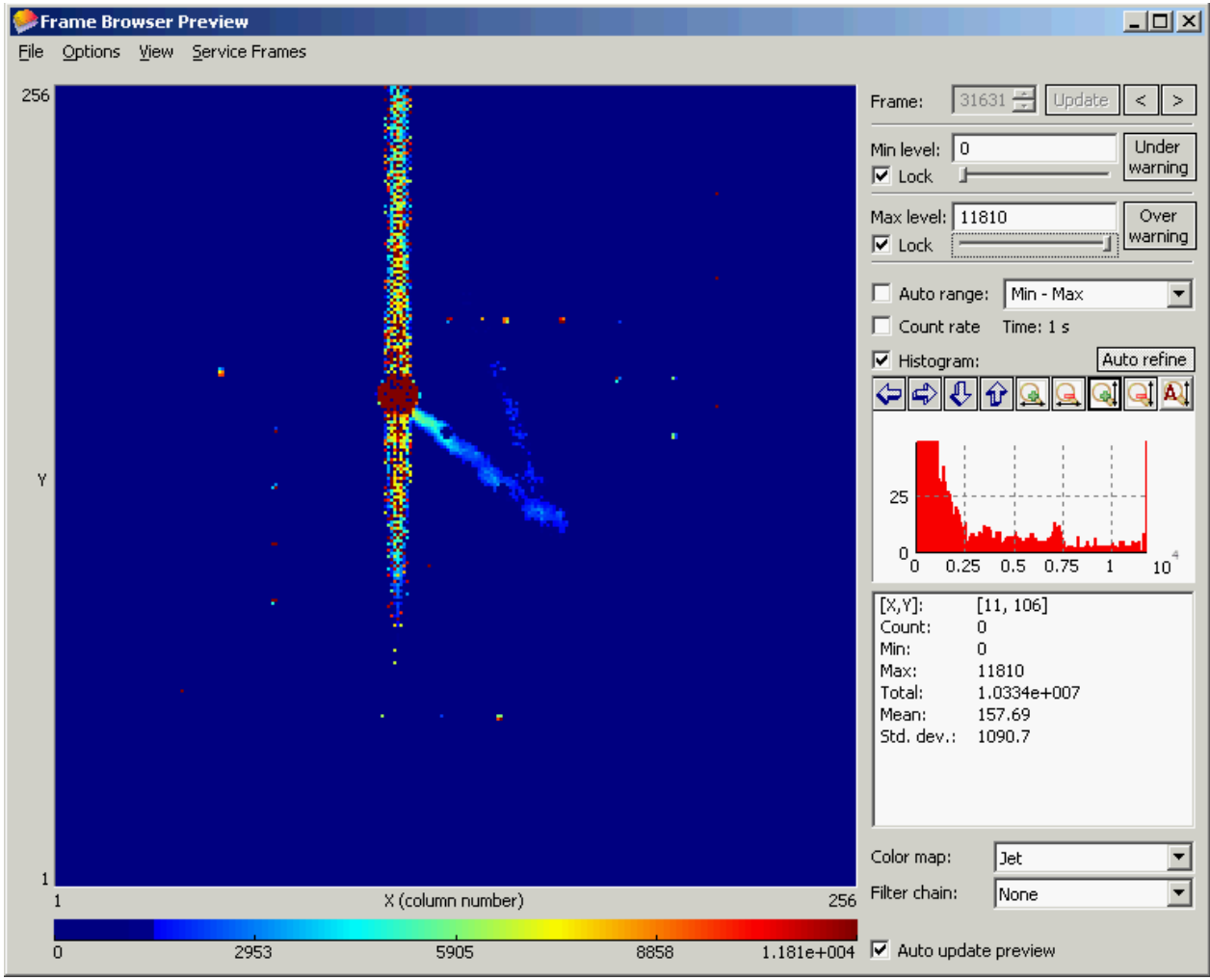
initiated by 2.5 MeV alpha's from Thorium/Radon in gas

For the 1st time: image of discharges are being recorded

Round-shaped pattern of some 100 overflow pixels

Perturbations in the concerned column pixels
- Threshold
- Power

Chip keeps working



2007 Protection layer of amorphous silicon

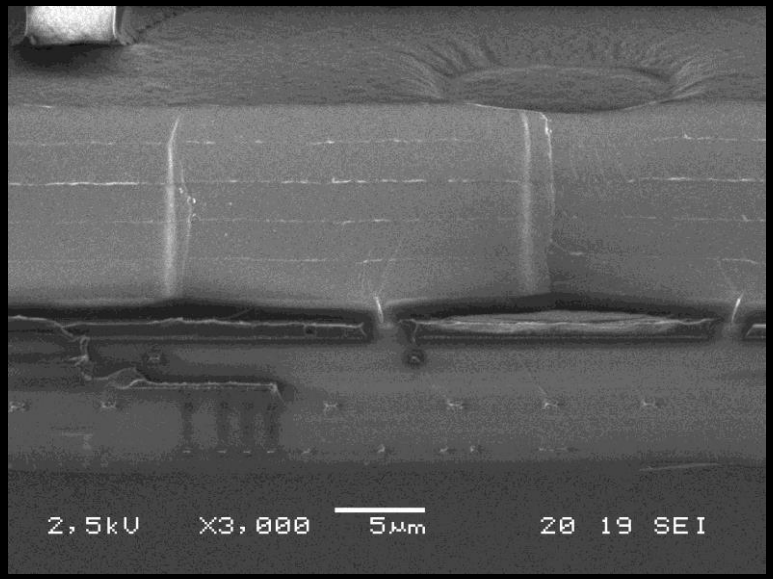
Nicolas Wyrsch

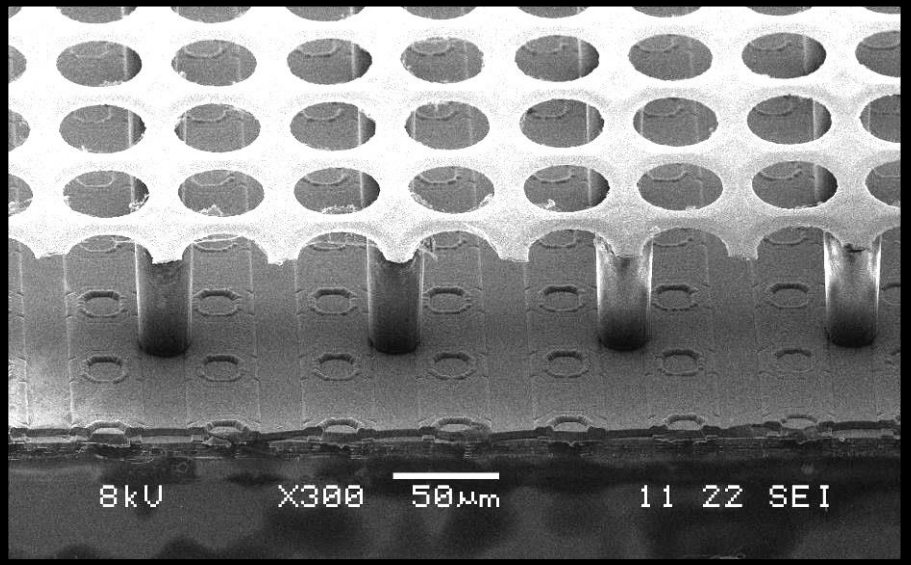
$3\ SiH_4 + 4\ NH_3 \rightarrow Si_3N_4 + 12\ H_2$

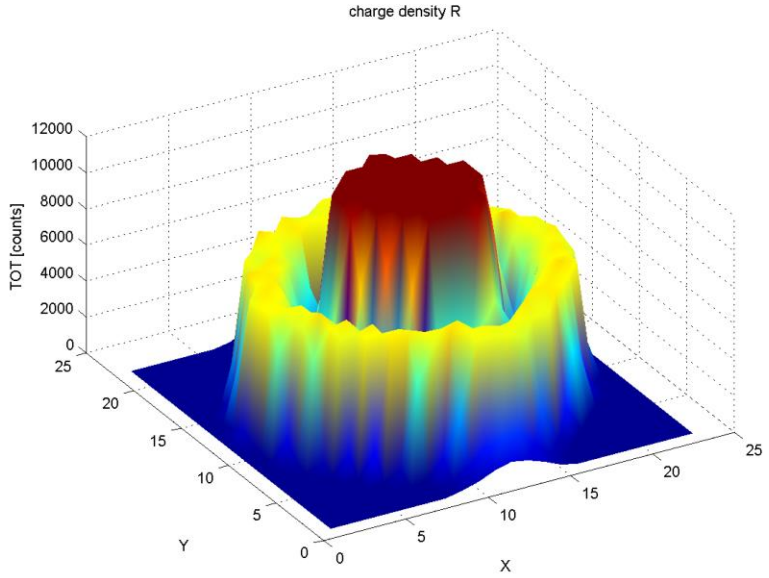
- Silicon Nitride is often applied as passivation layer:
  top finish of chips.

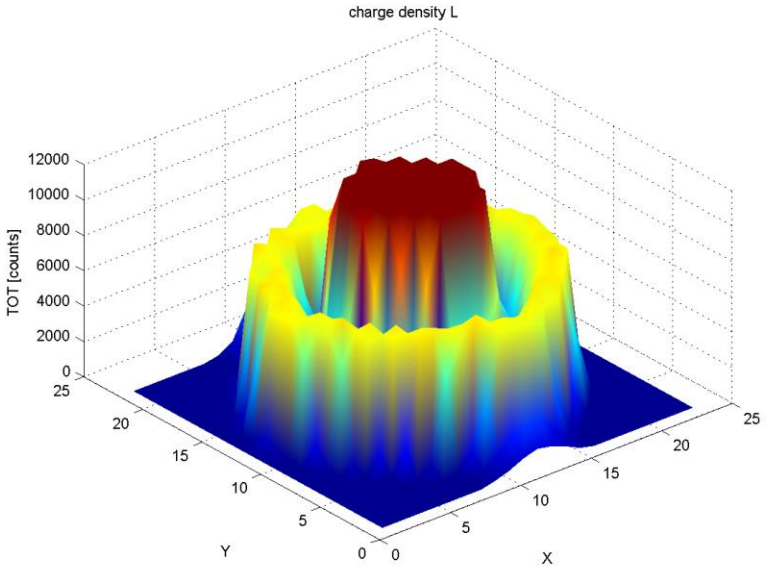
- With overdose of SiH_4:conductivity: high resistivity bulk material

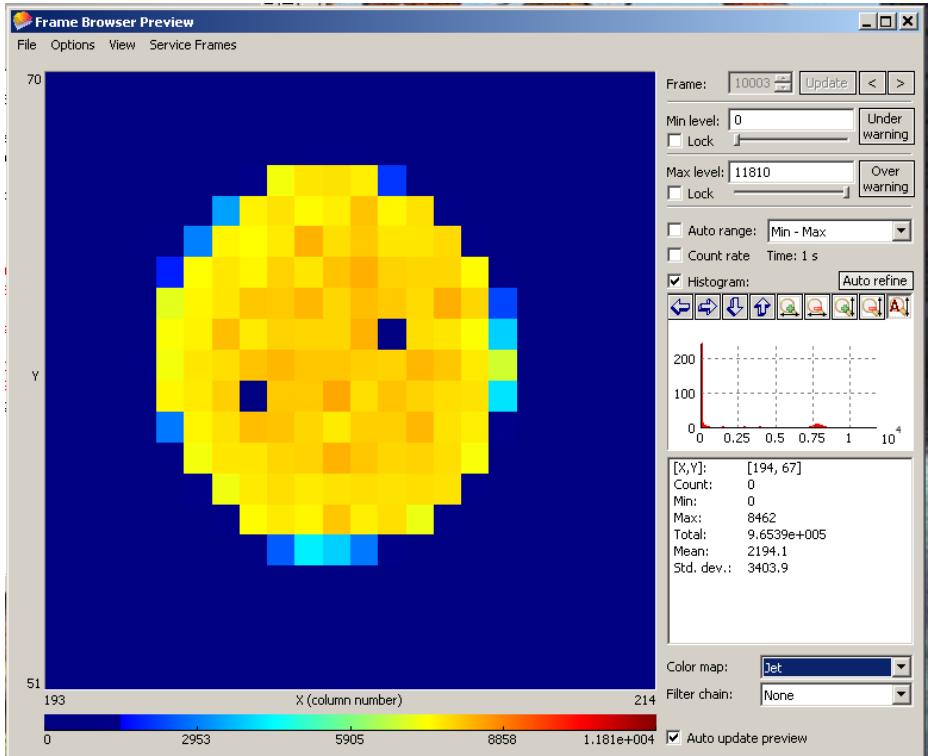
- Favored material for bearings in turbo chargers, jet engines



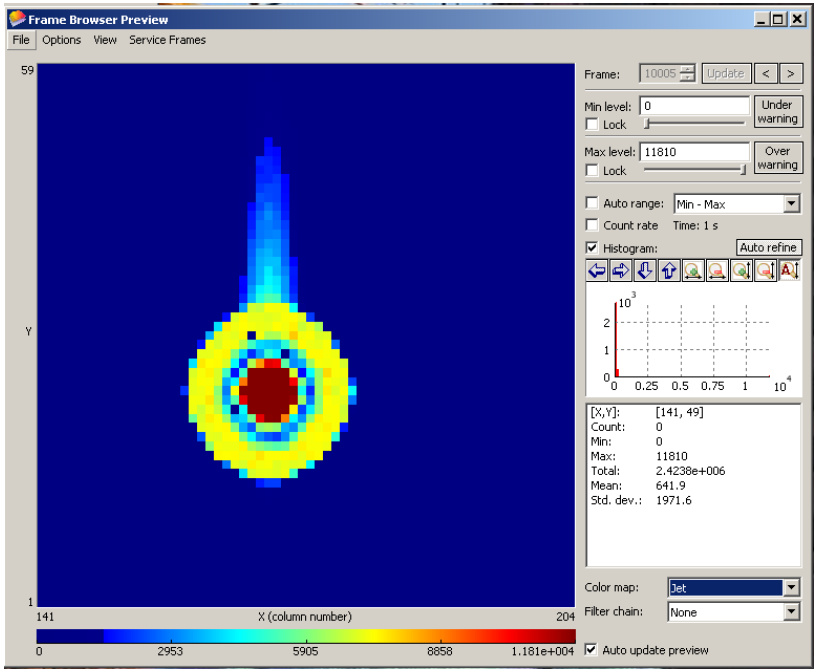


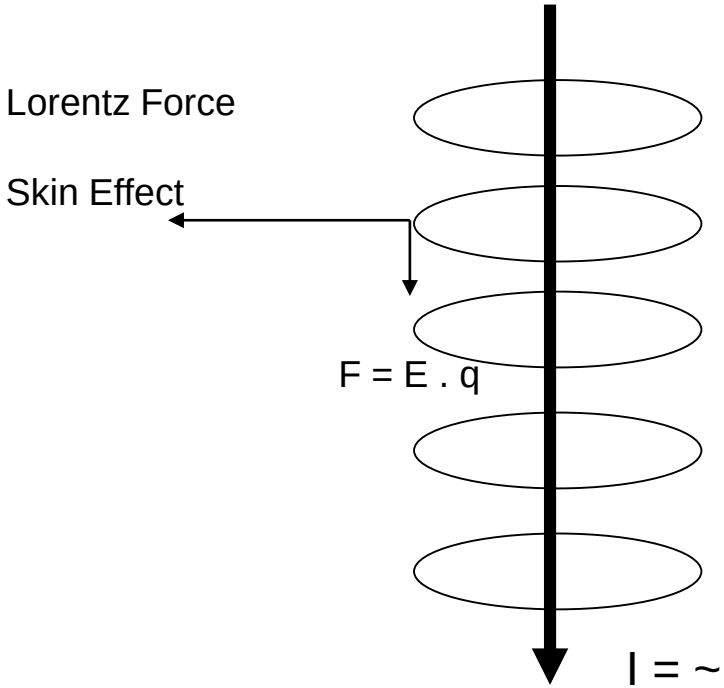




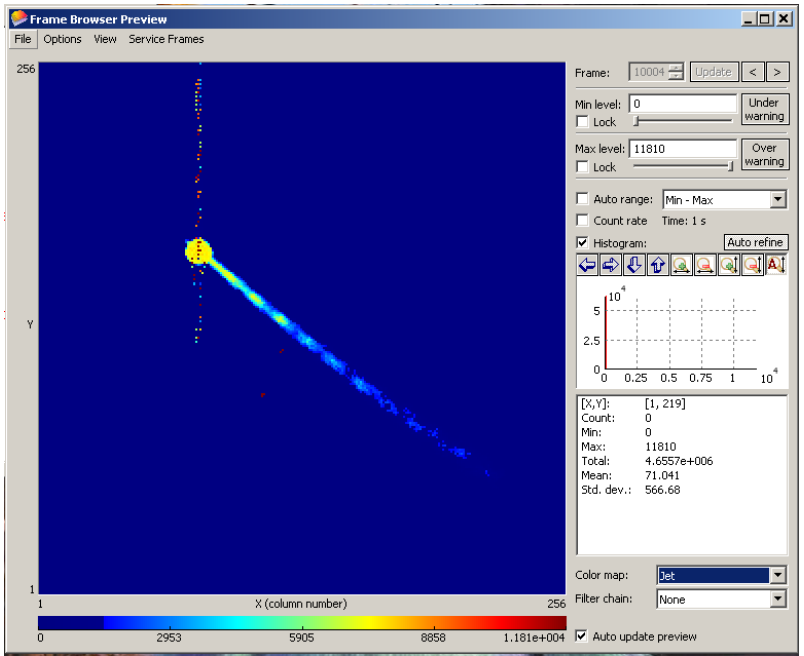


Discharge (protection) studies:
Martin Fransen



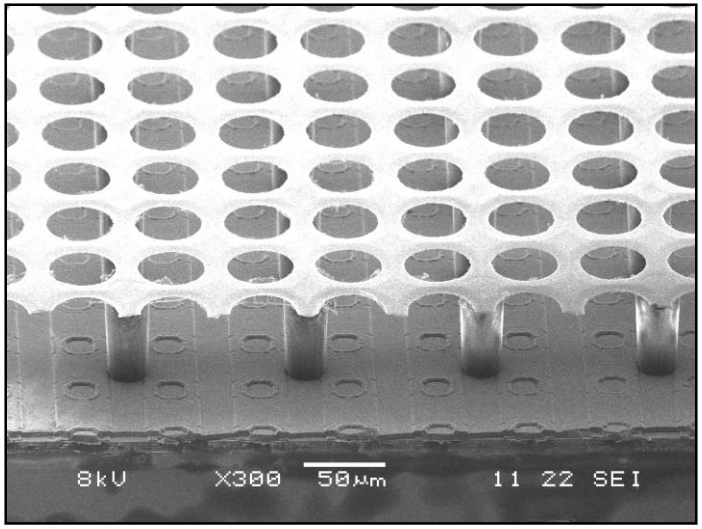


Improvement with Si Nitride

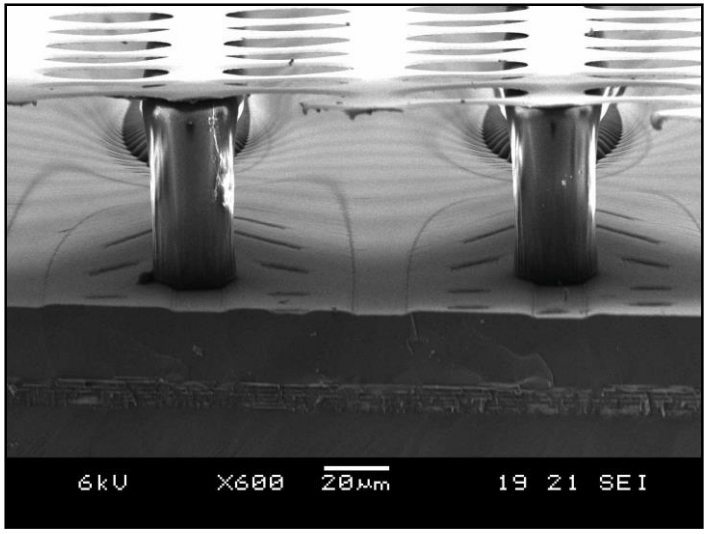


Full post-processing of a TimePix

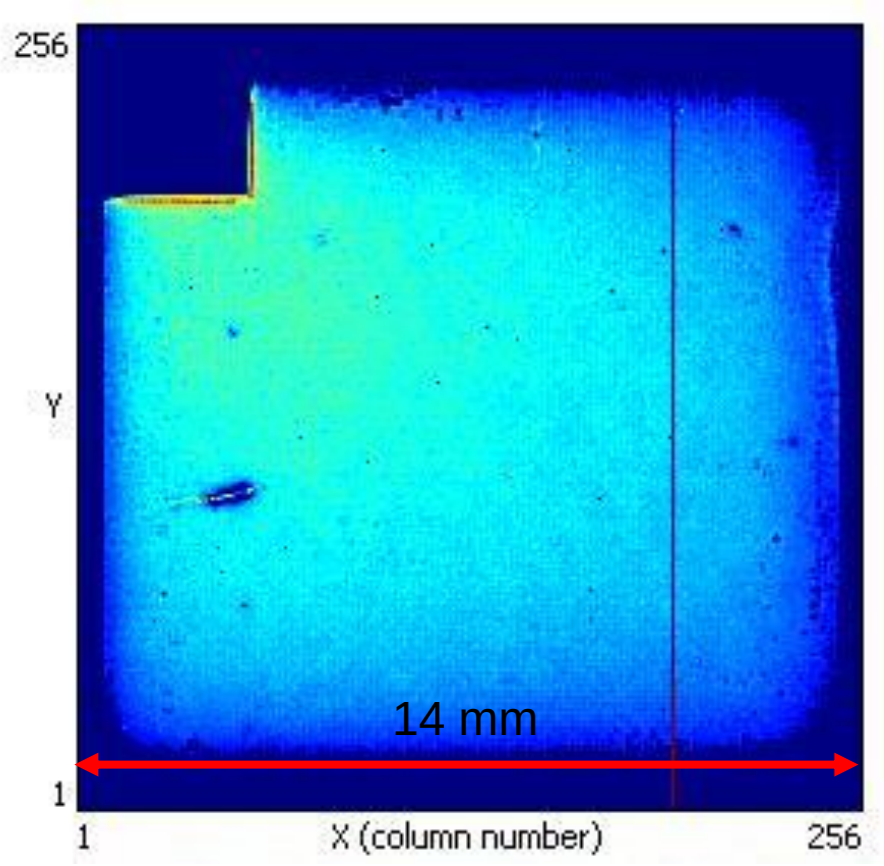
- Timepix chip + SiProt + Ingrid:



MESA+

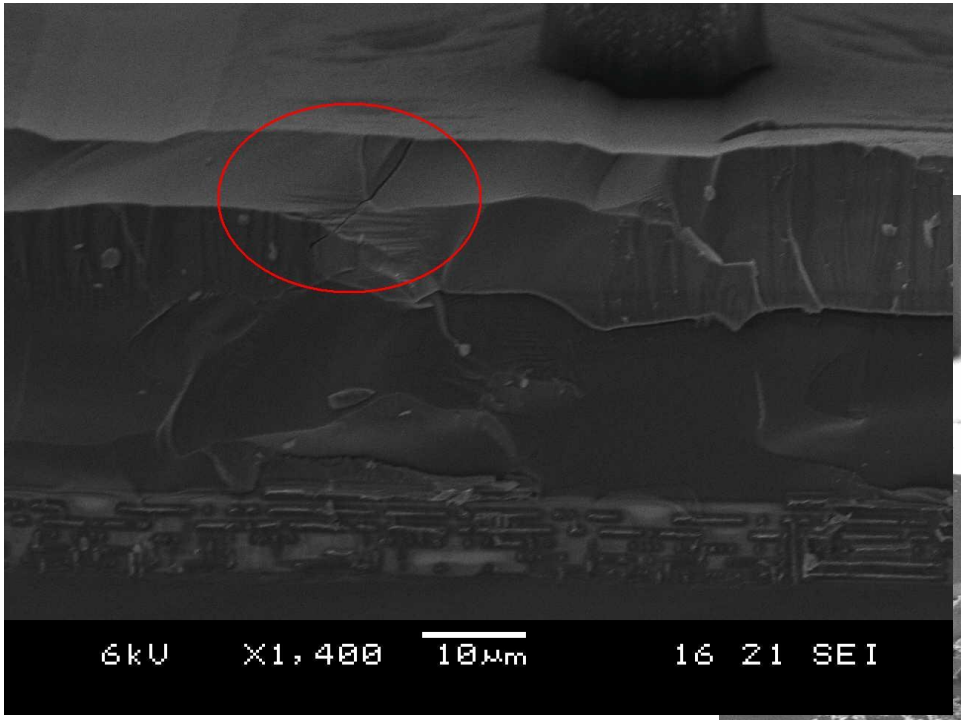


IMT Neuchatel



"Uniform"

Charge mode



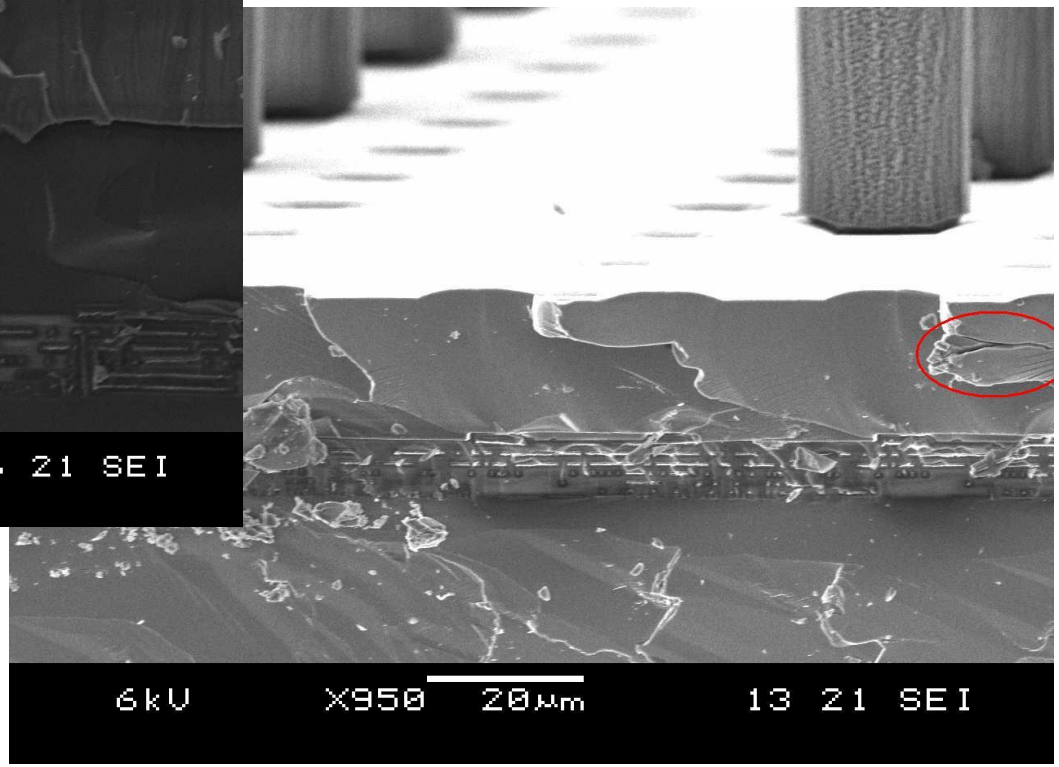
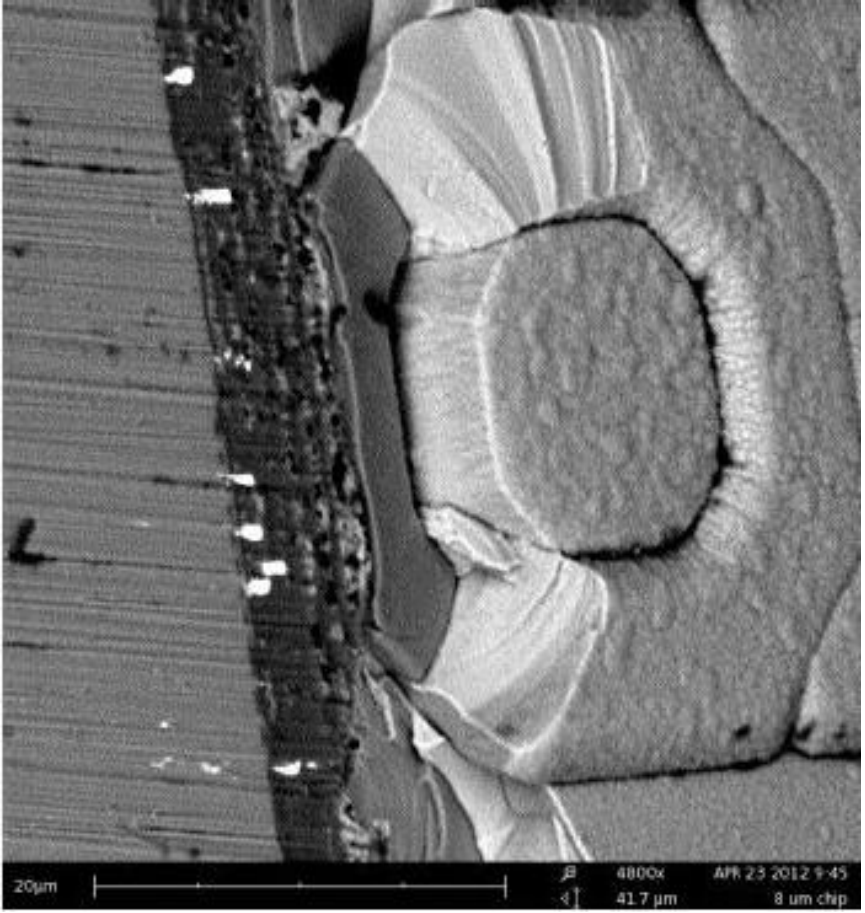


Fig 6. SEM images of a cut-open GridPix chips, clearly showing the SiNitride protection layer on top of the chip, of which its metal layers are well visible. A fault in the form of a cavity is identified and indicated.



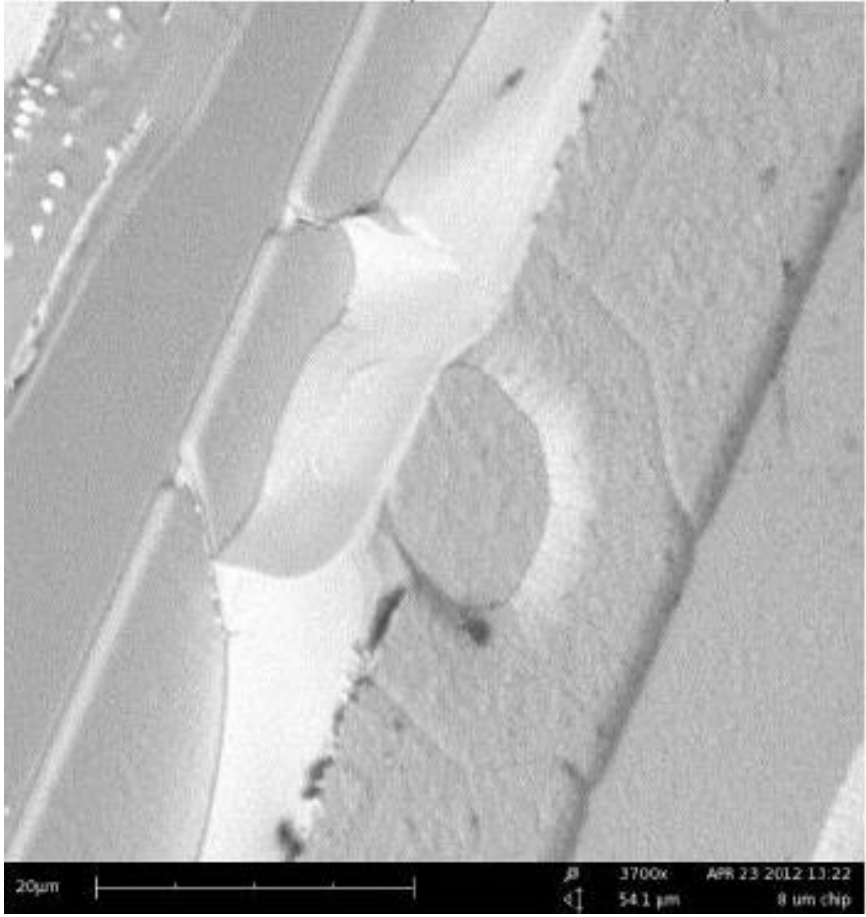
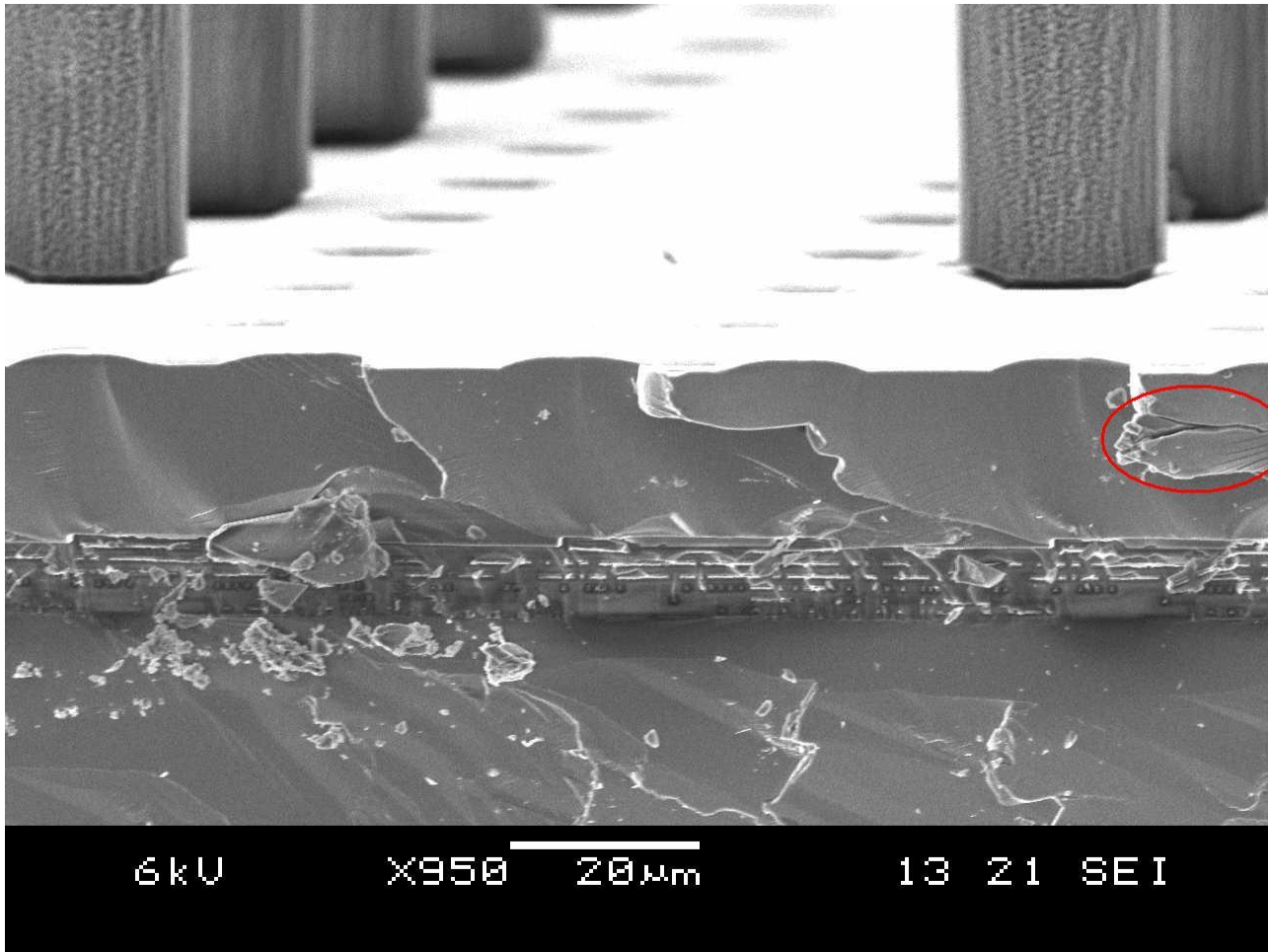
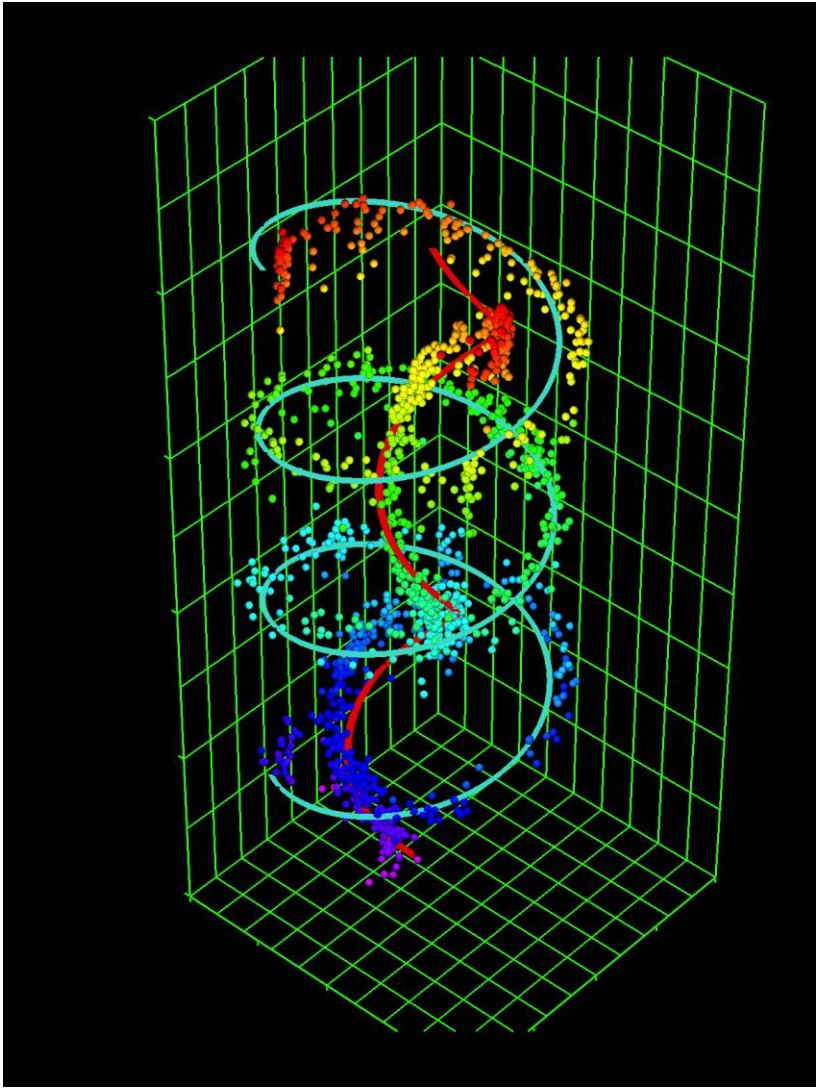


Fig 7. The pixel input pads of the TimePix 1 chip cause a well-known irrigularity acting as seed for a cavity (defect) in a protection layer to be deposit. Left: edge variation seeds cavity, right: no problem

MEMS Technology

- May 2010: 18 pcs GridPix (= TimePix + SiNProt + InGrid) made
    - quite good sparkproof!
- weak spots in protection layer found: future: all ceramic InGrid





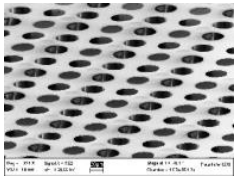
2007: GridPix with functioning protection layer
the ultimate TPC detector:

- single electron sensitive
- extract ALL info of primary electrons in gas
- only gas diffusion limits TPC performance
- (and pixe lsize)

2007 – 2016:

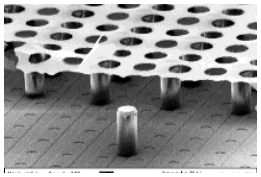
1. attempt GridPix mass production on wafers: wafer post processing (InGrid)
2. Improve protection layer: no faults permitted

GridPix production at IZM-Berlin

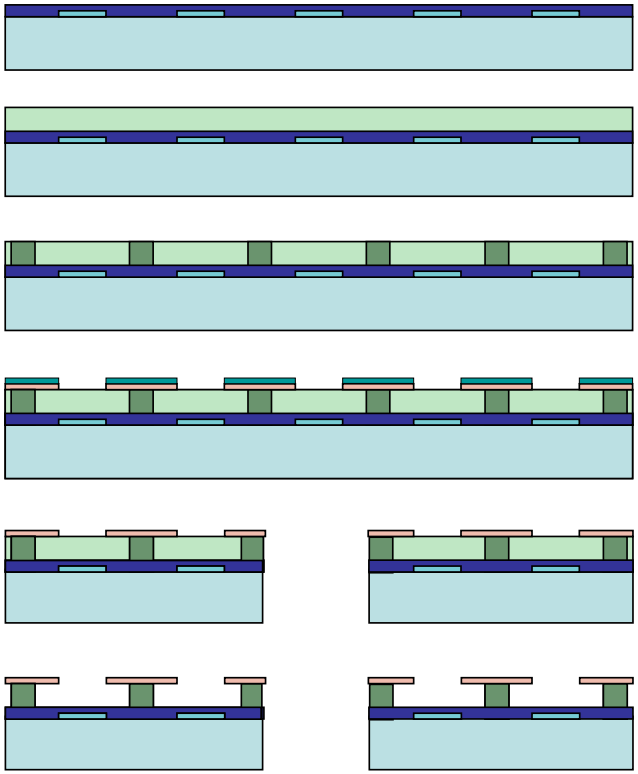


Wafer-based Production

Fraunhofer IZM



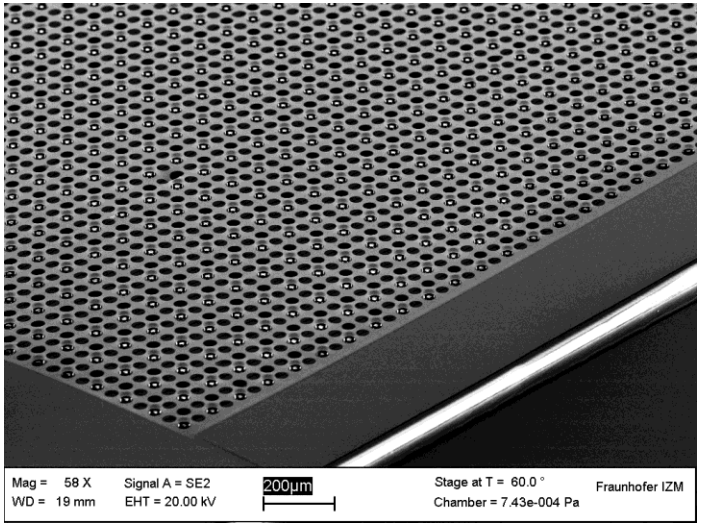
Production at Twente was based on 1 - 9 chips process.
New production set up at the Fraunhofer Institut IZM at Berlin.
This process is wafer-based → 1 wafer (107 chips) is processed at a time.

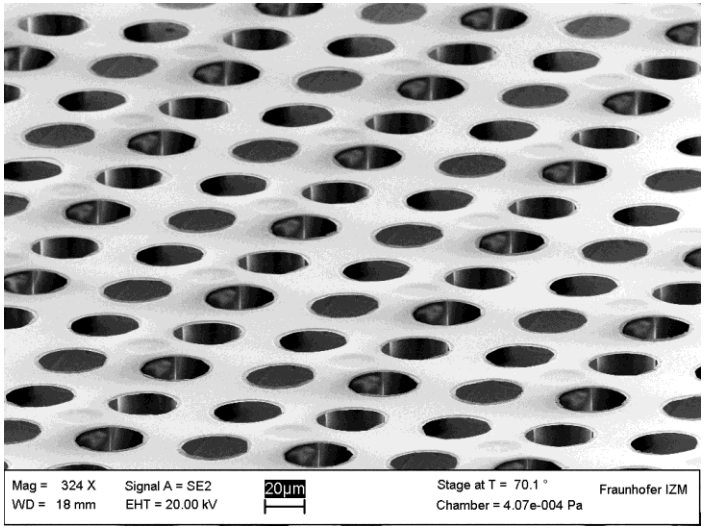


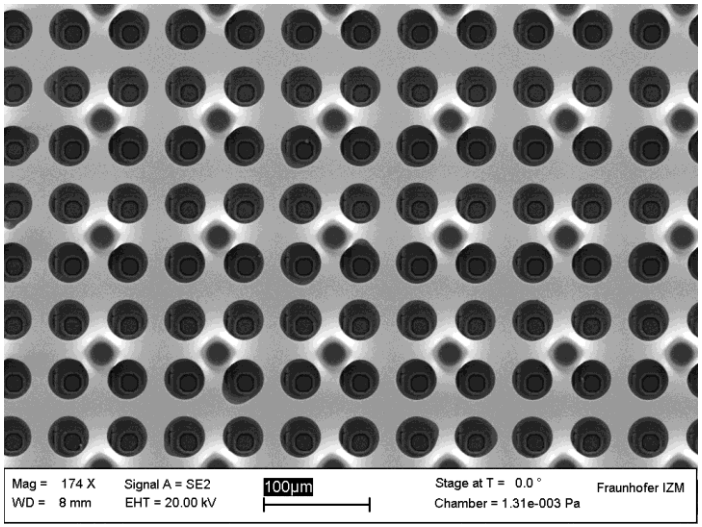
1. Formation of Si_xN_y protection layer
2. Deposition of SU-8
3. Pillar structure formation
4. Formation of Al grid
5. Dicing of Wafer
6. Development of SU-8

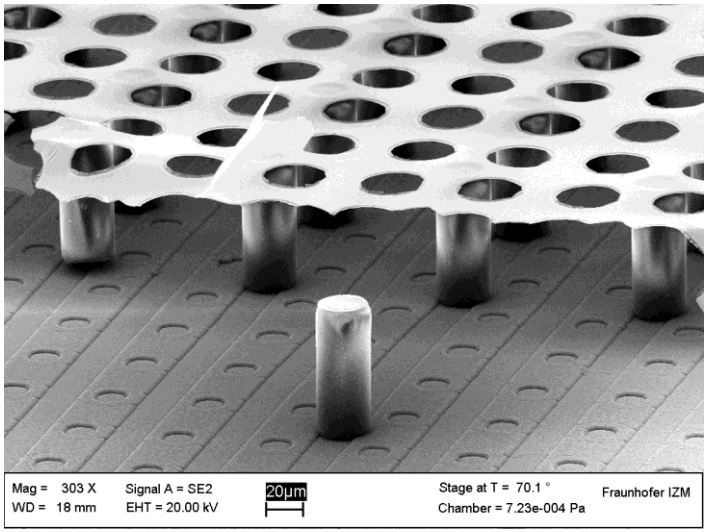
SEM Pictures

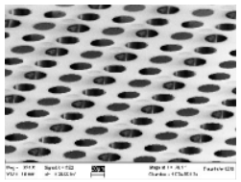
Fraunhofer IZM

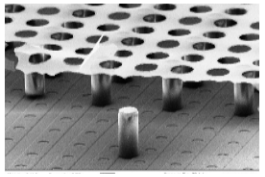




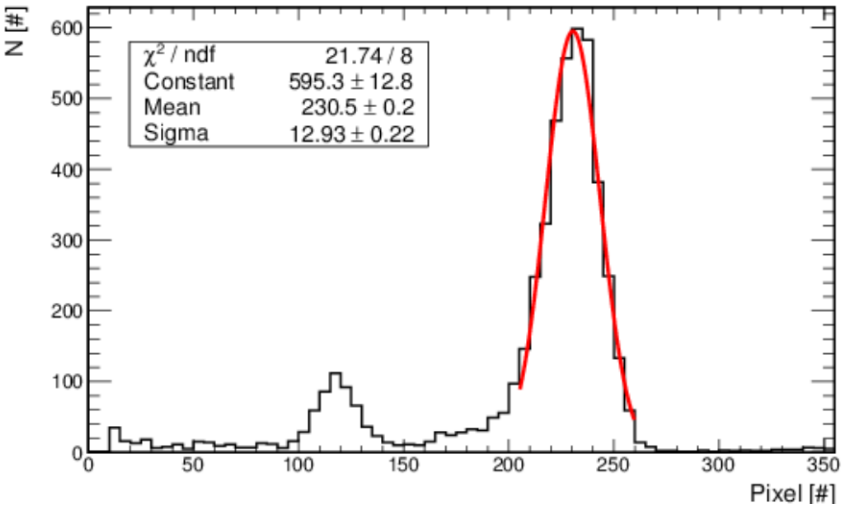


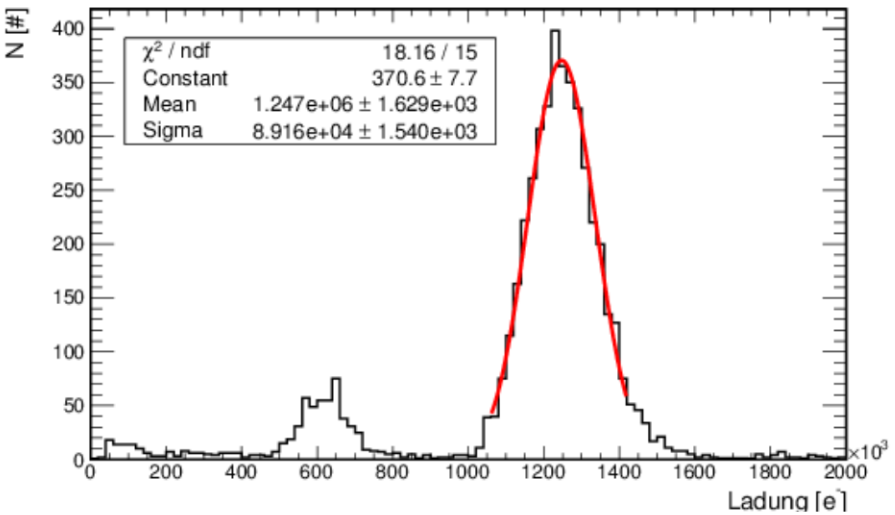


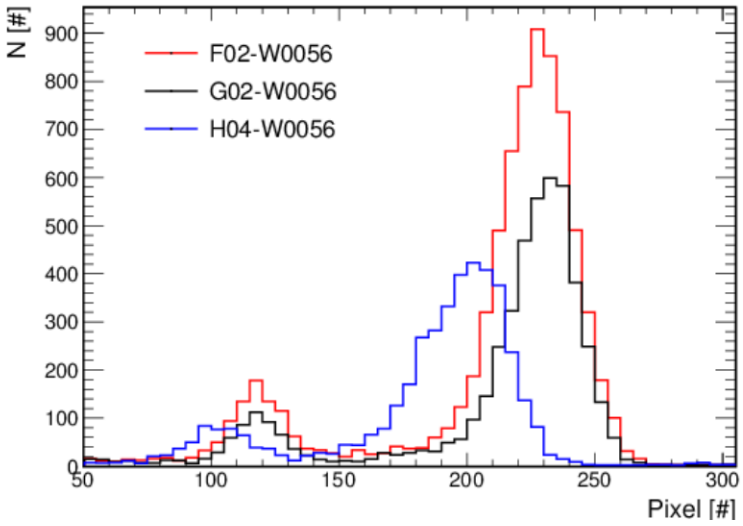




Some results of IZM-3: ^{55}Fe energy spectra







Voltage on grid 350 V (gain: 5500)

G02-W0056 pixels: $\sigma_N/N = 5.6\%$

charge: $\sigma_Q/Q = 7.2\%$

F02-W0056 pixels: $\sigma_N/N = 6.1\%$

charge: $\sigma_Q/Q = 7.2\%$

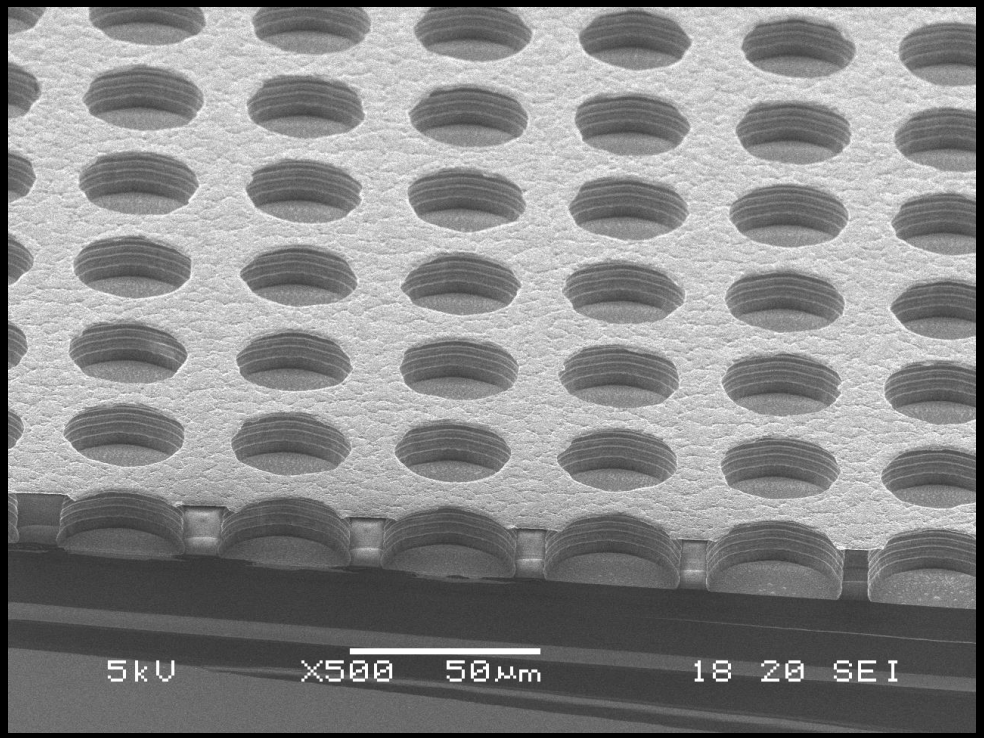
H04-W0056 pixels: $\sigma_N/N = 8.3\%$

charge: $\sigma_Q/Q = 11.2\%$

New R&D: the all-ceramic GridPix:

- Si TimePix chip
- SiNitride protection layer
- SiNitride InGrid

➔common thermal expansion coefficient: 6 x 10^{-6} K^{-1}



First GEMGrid with SiO2 as insulating spacer between grid and substrate
Victor Blanco Carballo, MESA+/Nikhef

Why Ceramic?

- Outgassing of the SU-8 pillars
- Application in cold (cryogenic) environments
  DBD, DarkMatter

Material	**Coefficient of thermal expansion (10^{-6}/ºC)**
Silicon	2.6
Silicon Nitride	3.2
Silicon Oxide	2.3
Aluminum	22
SU-8	102

- Double Spark protection (like a RPC)

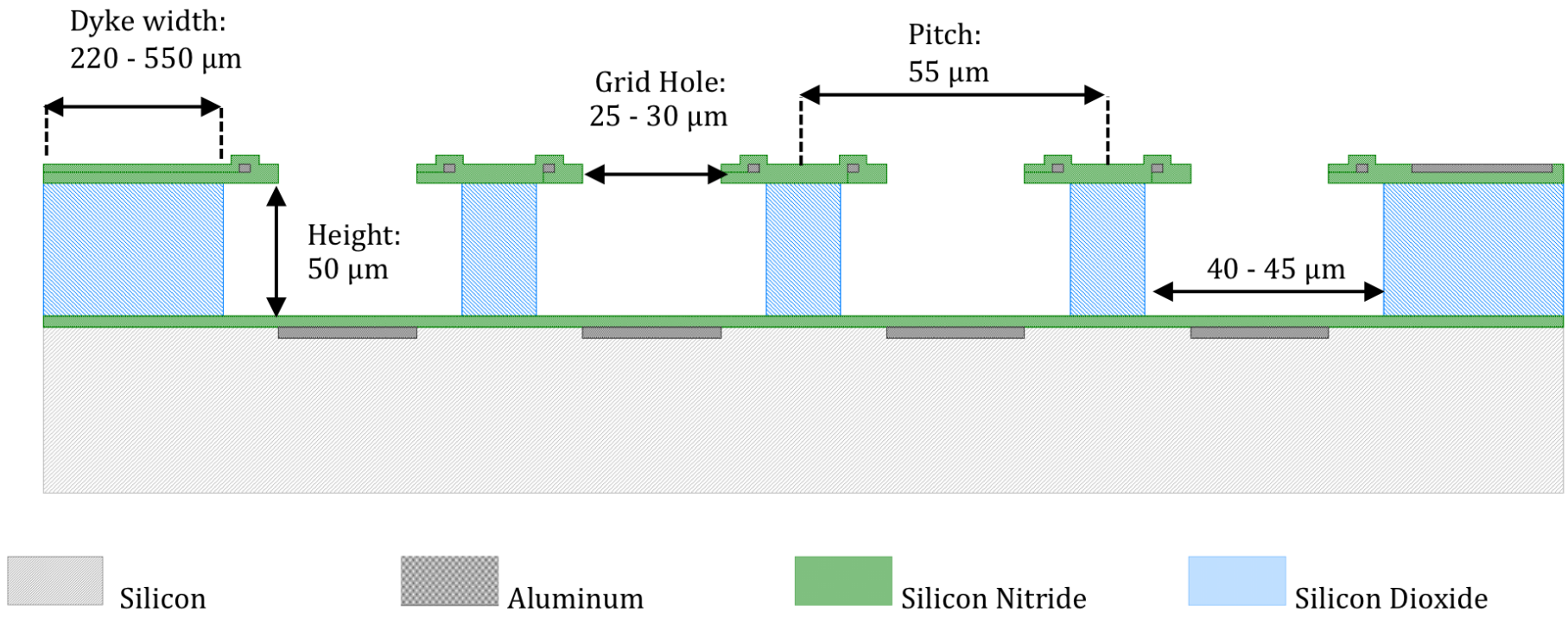


Figure 1 All-Ceramic InGrid

a.) Deep Reactive Ion Etching

b.) Wet Thermal Oxidation

c.) LPCVD TEOS

d.) Temporary wafer bonding to carrier wafer

e.) Wafer thinning

f.) Glass frit bonding to TimePix Wafer

g.) Carrier wafer removal

h.) Silicon dioxide removal (Plasma etch)

i.) PECVD Silicon Nitride

j.) Aluminum sputtering

k.) Aluminum Patterning

l.) PECVD Silicon Nitride

m.) Opening grid holes (Plasma etch)

n.) Silicon removal (DRIE + plasma etch)

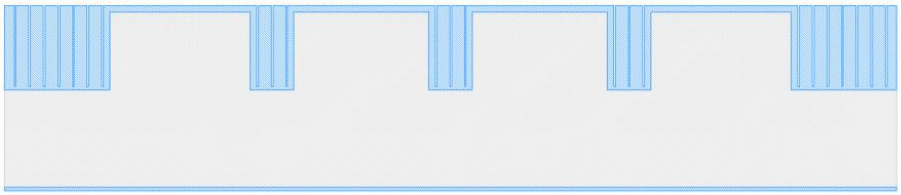
Silicon

Aluminum

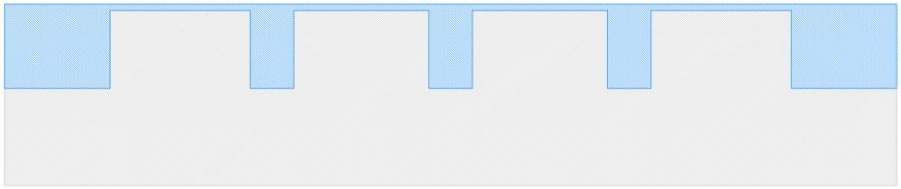
Silicon Nitride

Silicon Dioxide

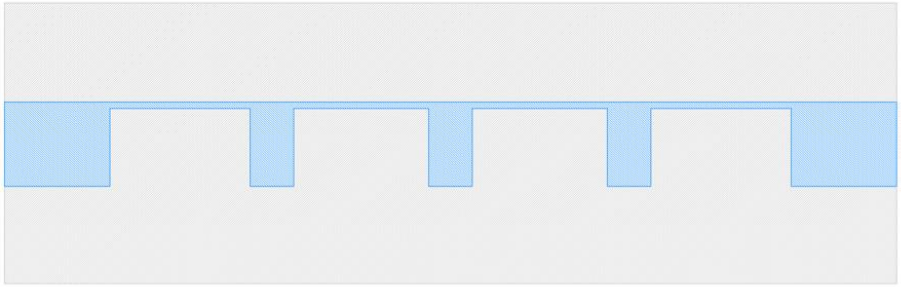
a.) Deep Reactive Ion Etching



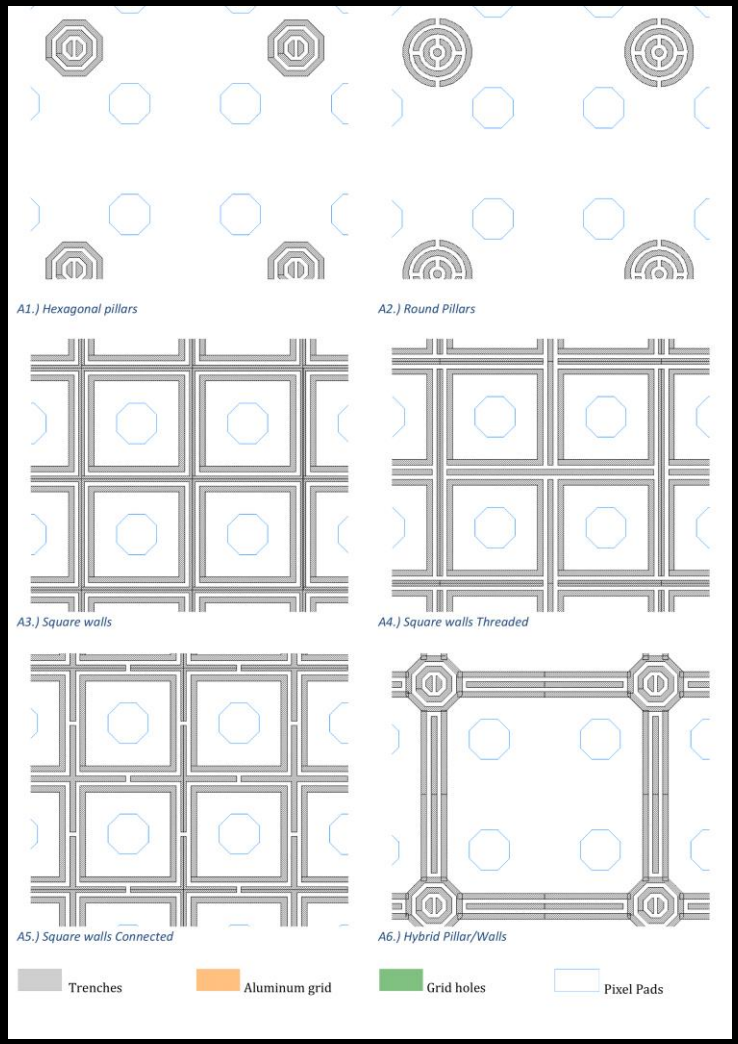
b.) Wet Thermal Oxidation



c.) LPCVD TEOS



d.) Temporary wafer bonding to carrier wafer



Development of All-Ceramic InGrid in progress at
IZM-Berlin Fraunhofer and EKL/Delft University of Technology

Hong Wah Chan & Yevgen Bilevych

The GridPix Quad General Purpose readout unit

- A GridPix/TimePix-3 is the best possible readout of TPCs, providing full 3D info of all individual primary electrons
- one unit includes 4 TimePix-3-based InGrids
- units can be placed against one another, forming an arbitrarely large TPC readout area
- Spidre readout: 2.2 Gb/s hit pixel data (no frame readout!)
- Version 1.0 operational: version 2.0 awaits new badge of IZM TPX-3/InGrids
- Production ASI/Nikhef/Bonn may become true in 2019