



# Characterization and first field results of TIGER ASIC for the readout of GEM detectors

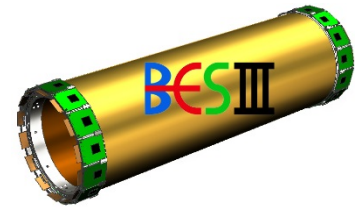
RD51 Collaboration Meeting and the "MPGD Stability" Workshop

Munich 18-22 June 2018

**Fabio Cossio**

CGEM-IT Group

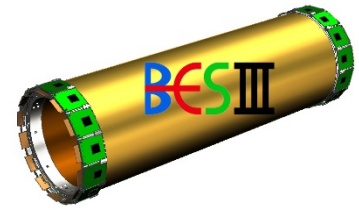
# Outline



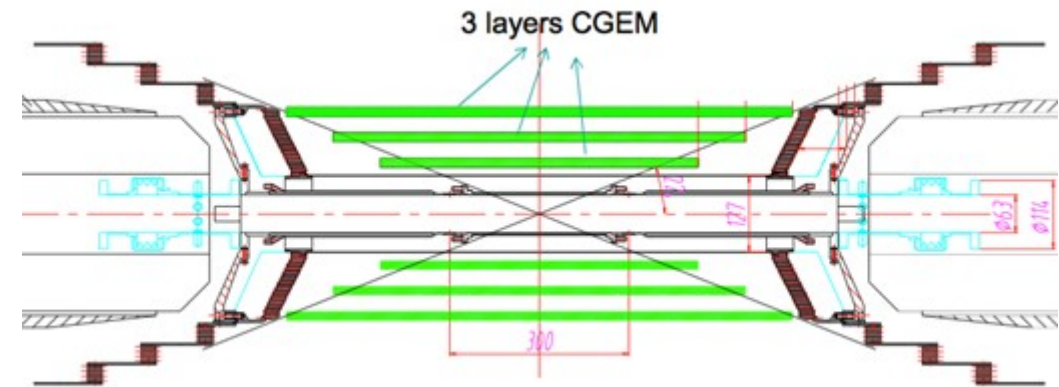
- Introduction
- TIGER ASIC architecture
- TIGER ASIC performance
- Results from tests with GEM detectors
- Summary and outlook



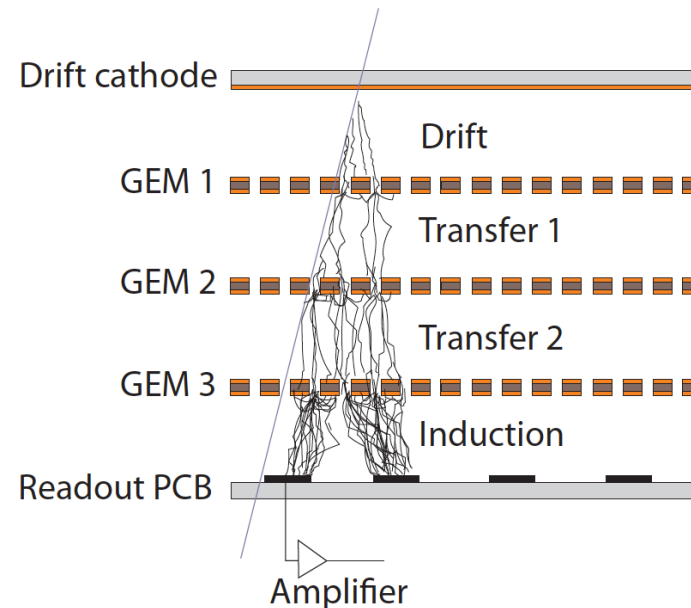
# CGEM Inner Tracker for BESIII



- BESIII Experiment 2018-2019 upgrade
- New Inner Tracker: 3 layers of **Cylindrical Gas Electron Multiplier (CGEM-IT)** detector
- Each layer: triple GEM with charge collected at the anode by 2D segmented readout strips



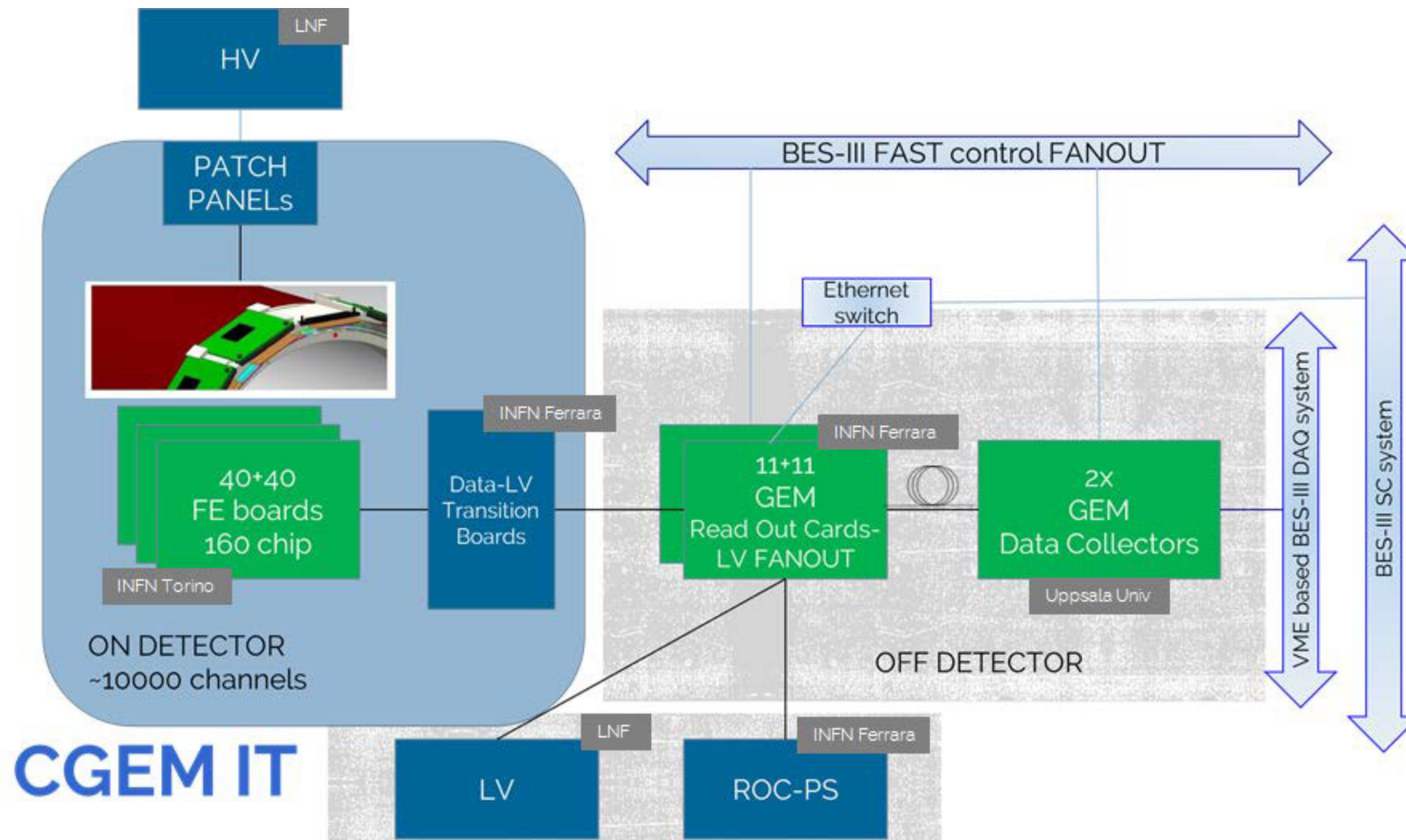
- **TIGER (Turin Integrated Gem Electronics for Readout)** dedicated 64-channel readout ASIC
- Must provide **charge** and **time measurement** for the analogue readout of the CGEM
- This enables **charge centroid** and **micro-TPC** algorithms to improve resolution and reduce the number of channels



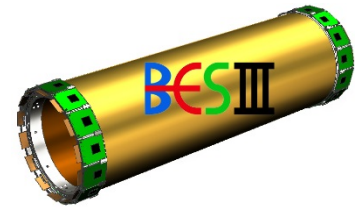
Readout	Analogue
Spatial resolution	130 $\mu\text{m}$
Pitch strip	650 $\mu\text{m}$
# channels	$\sim 10\ 000$
Sensor capacitance	100 pF
Channel rate	60 kHz
Collected charge	3 – 50 fC



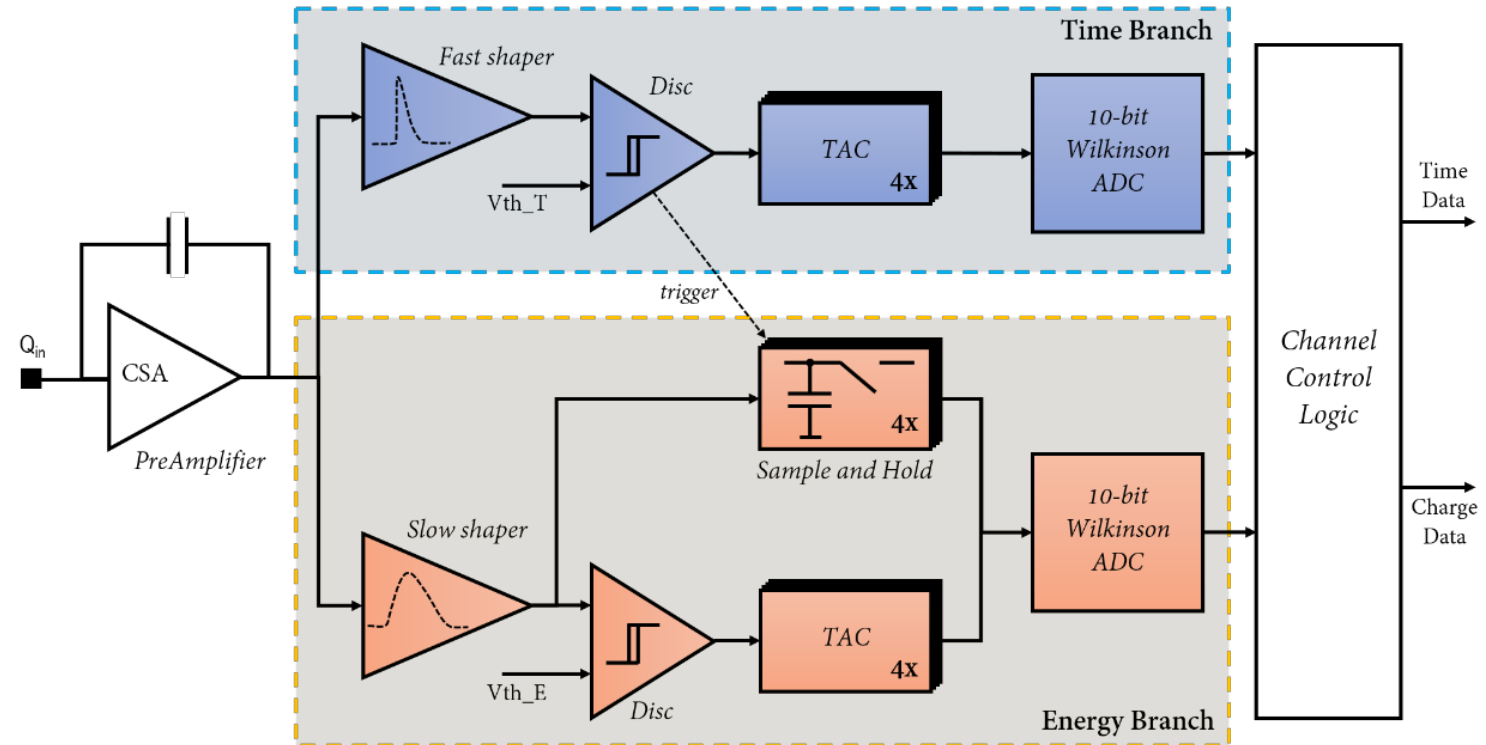
# Overview of CGEM readout electronics



# TIGER channel architecture



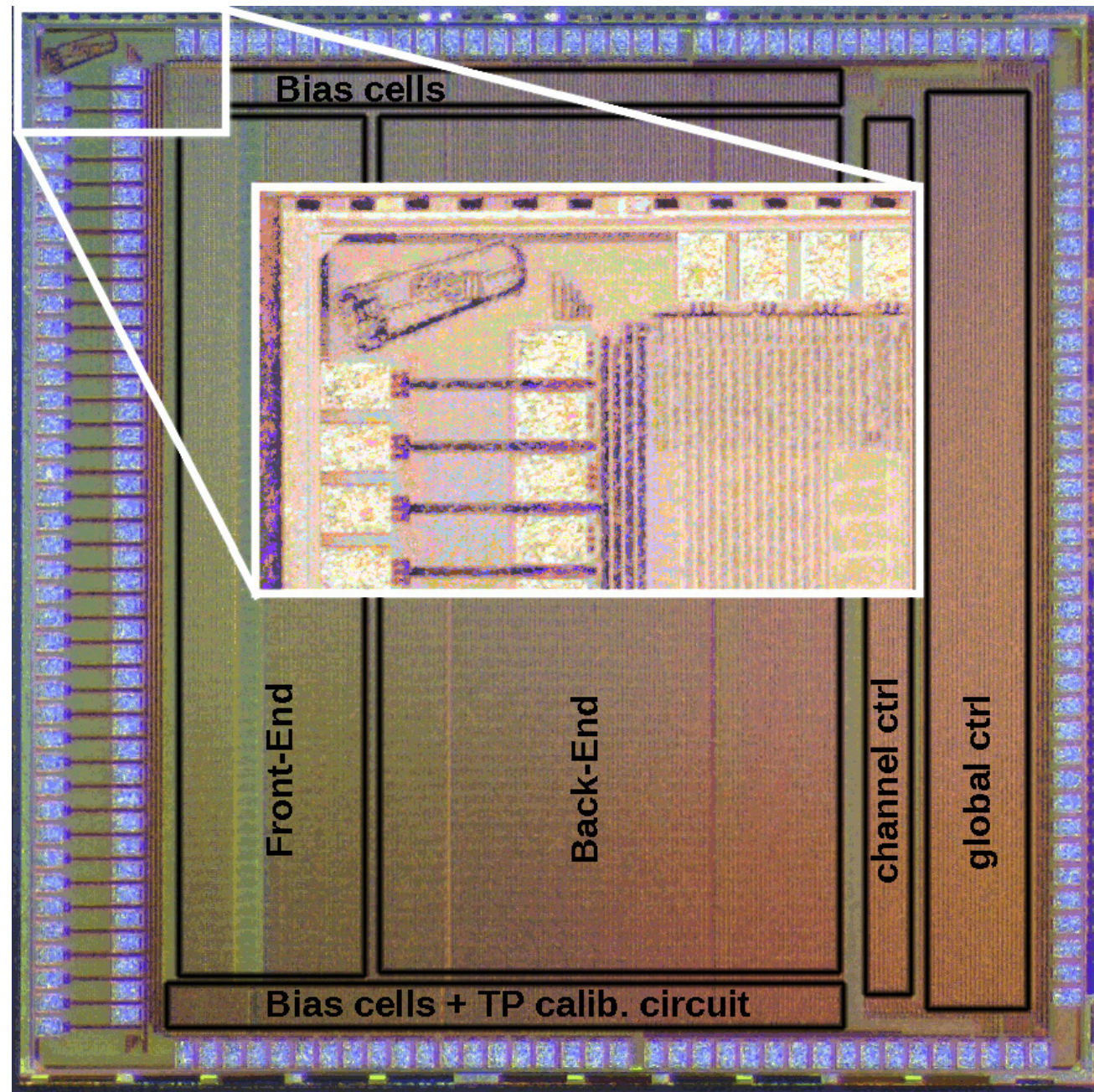
- Analogue Front-End:
  - Charge Sensitive Amplifier
  - **Dual-branch** shaper
  - Gain  $\approx 11$  mV/fC
  - Input dynamic range = 3 – 50 fC
  - ENC < 2000 electrons ( $C_{in} = 100$  pF)
- **Timestamp** on rising edge of fast branch
  - Time resolution < 5 ns
- **Charge** measurement:
  - **ToT**: timestamp on rising/falling edge (sub-50 ps binning quad-buffered TDCs based on analogue interpolation)
  - **S/H**: slow shaper output sampled and digitized with a 10-bit Wilkinson ADC
- Power consumption  $\approx 12$  mW/ch





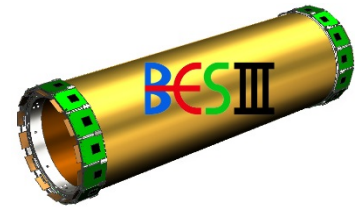
# TIGER: Turin Integrated Gem Electronics for Readout

- 5 x 5 mm<sup>2</sup> 110nm CMOS technology
- 64 channels: preAmp, shapers, TDC/ADC, local controller
- Digital backend inherited from TOFPET2 ASIC (SEU protected)
- On-chip bias and power management
- On-chip calibration circuitry
- Fully digital output
- 4 TX SDR/DDR LVDS links, 8B/10B encoding
- Nominal 160 MHz system clock
- 10 MHz SPI configuration link
- Sustained event rate > 100 kHz/ch





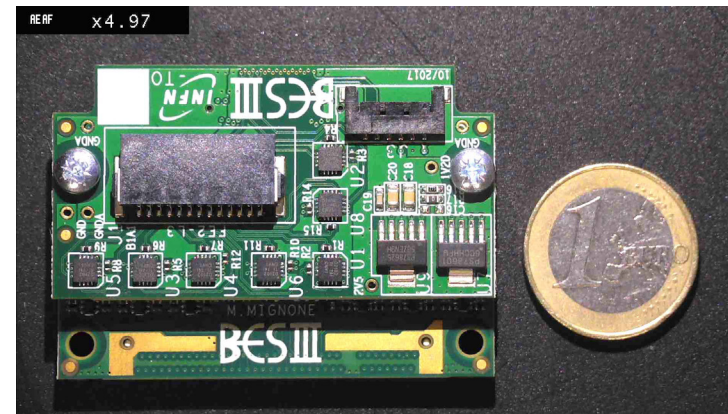
# TIGER characterization



- Tapeout of first silicon: MPW May 2016
- Tests of prototype from Nov 2016 to Apr 2017
- Engineering run with different design flavours and minor design revisions (Aug 2017)
- Test and characterization of final version from Jan 2018



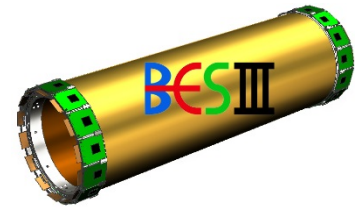
*2 TIGER ASICs wire-bonded on the Front-End Board (FEB)*



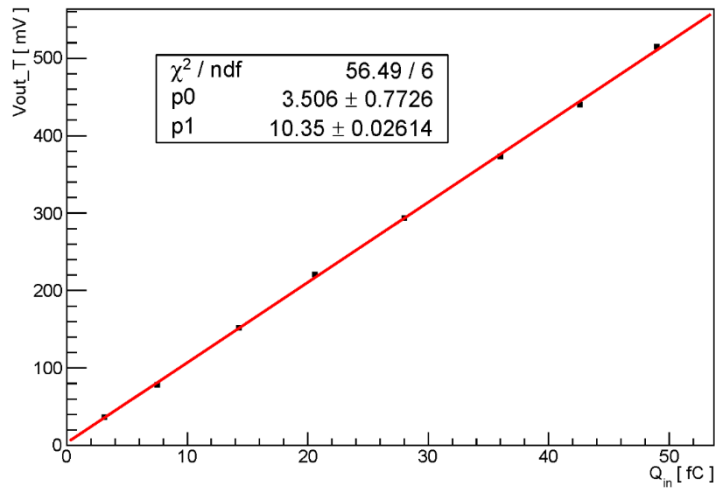
*Layer-3 Front-End Board (FEB)*



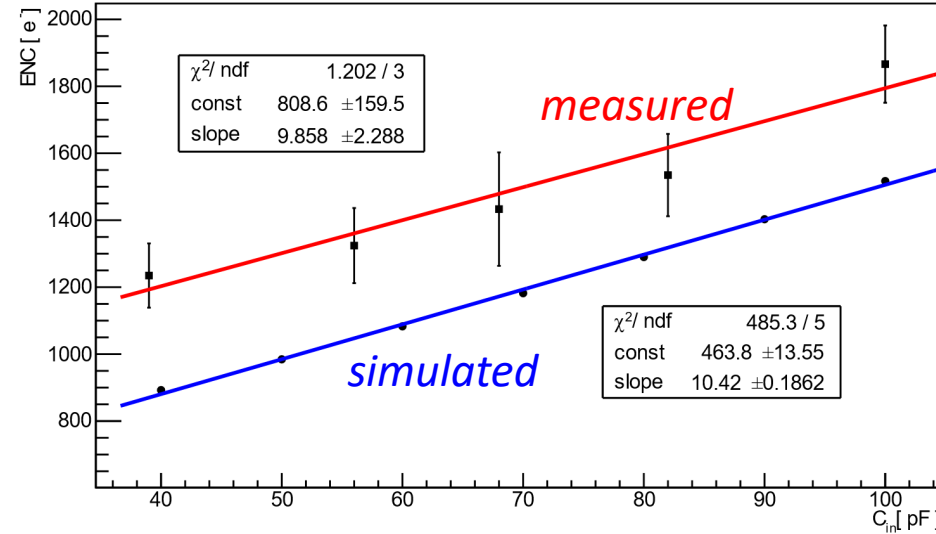
# Gain and Noise performance



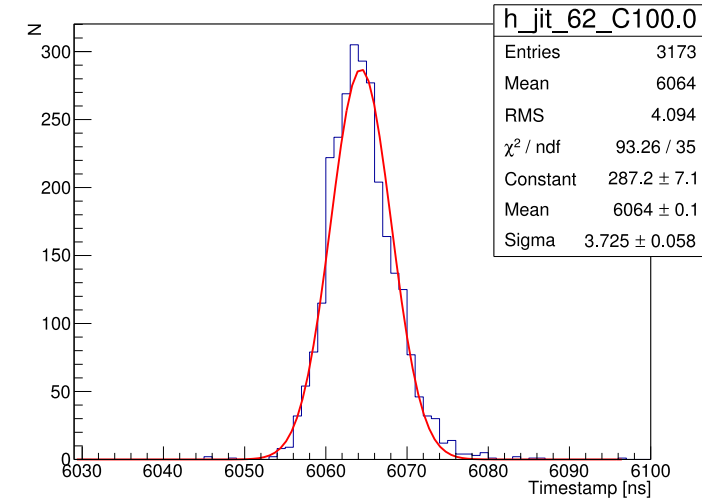
T-branch gain



Noise vs  $C_{in}$



T-branch jitter ch = 62, C = 100.0



## GAIN

- External charge injection (1 channel)
  - **Gain  $\approx 10.35$  mV/fC**  
(expected 11 mV/fC from simulation)
- Injection of  $Q_{in} = 8$  fC with internal TP (all channels)
  - **Average gain  $\approx 10.75$  mV/fC** with 3.5% RMS dispersion

## NOISE

- E-branch RMS noise for  $C_{in} = 100$  pF
  - **ENC  $\approx 1800 e^-$**  (measured) vs  $1500 e^-$  (simulated)
  - Large contribution from resistor in ESD protection circuit of the Test Board
  - Removed in the final **Front-End Board**

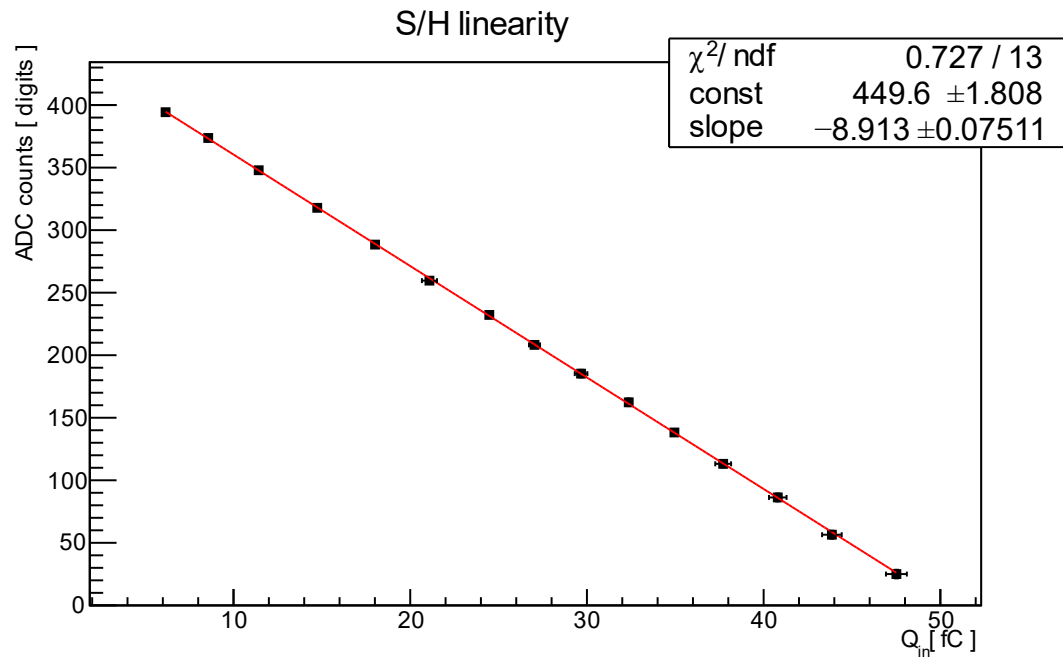
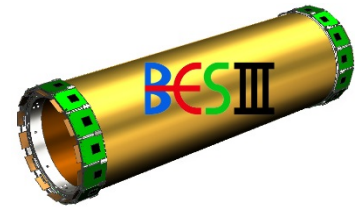
## JITTER

- $Q_{in} = 3$  fC,  $C_{in} = 100$  pF
  - T-branch RMS jitter  $\approx 3.7$  ns



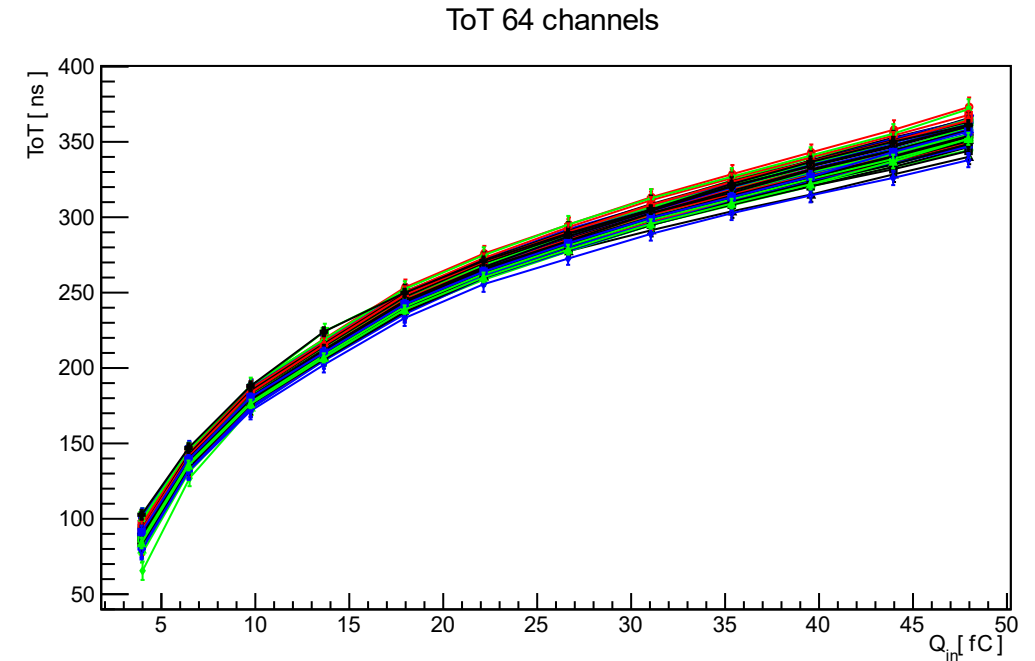


# Charge measurement



## Sample-and-Hold

- Linear up to  $\sim 50$  fC
- Saturation for  $Q_{\text{in}} > 50$  fC



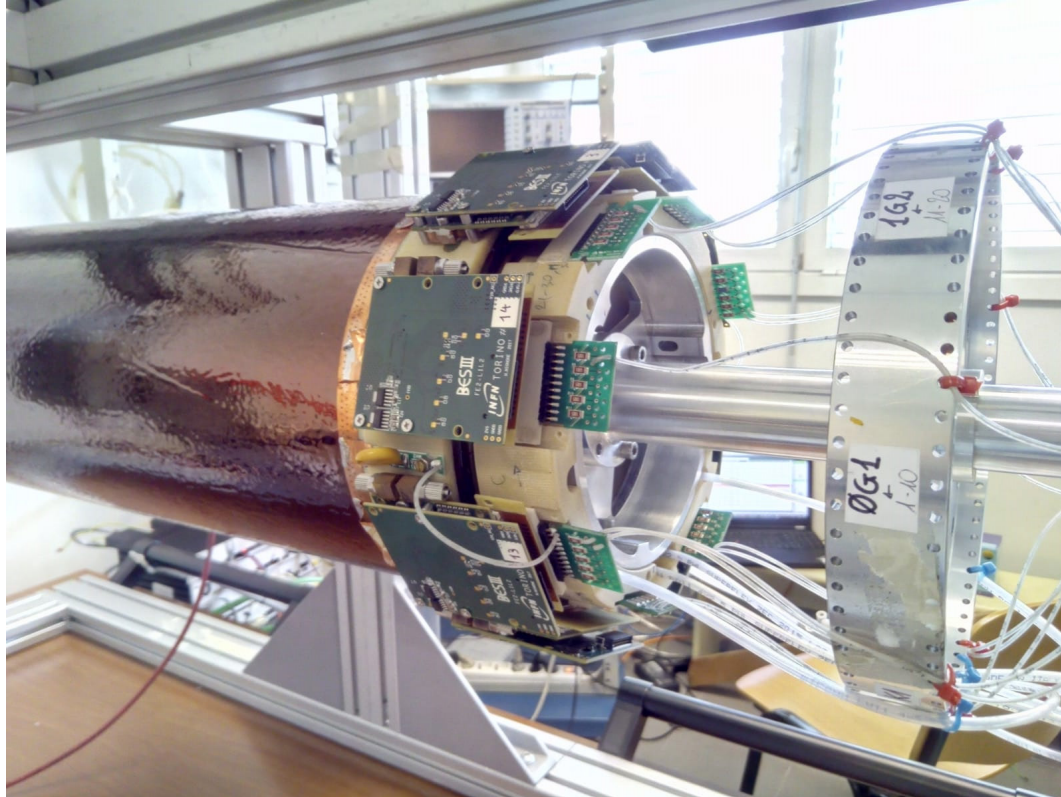
## Time-over-Threshold

- ToT curve due to the intrinsic non-linear pulse duration of CR-RC<sup>n</sup> shapers

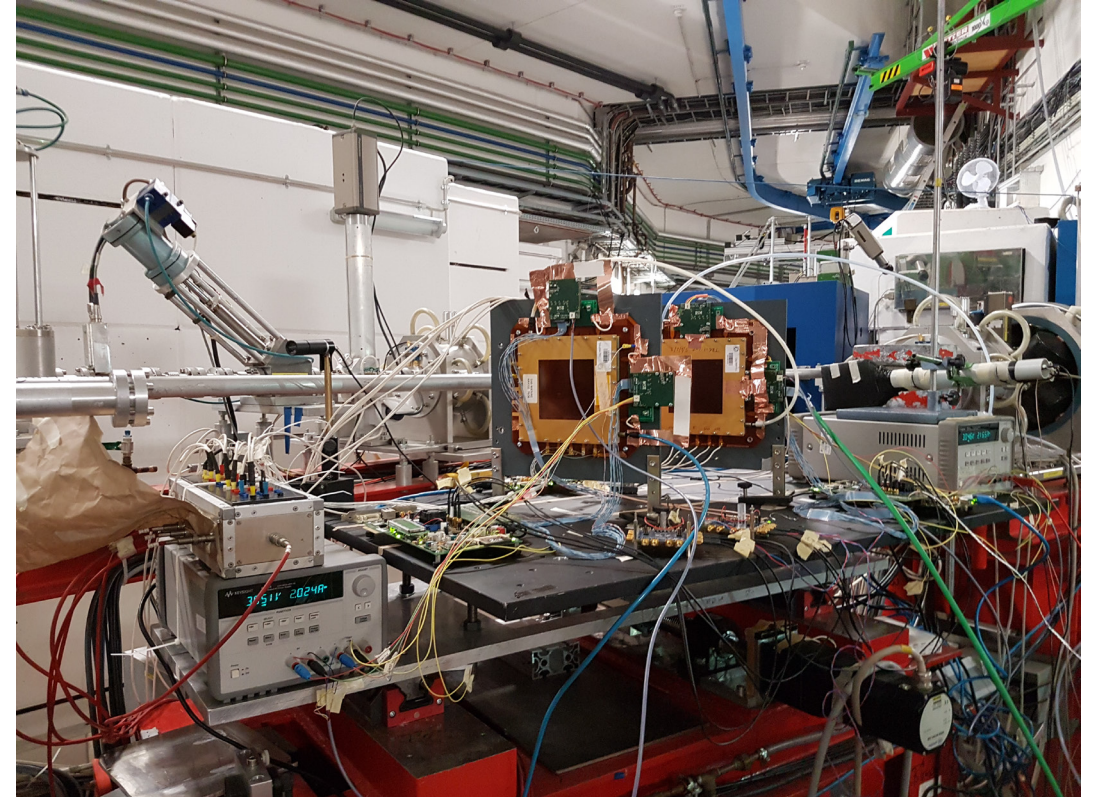
Calibration curves to compensate channel-by-channel offsets



# Results from test with GEM detectors



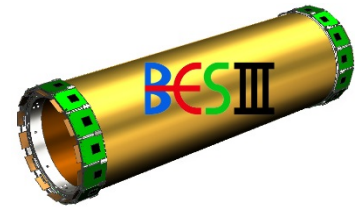
*CGEM Layer-1 fully instrumented*



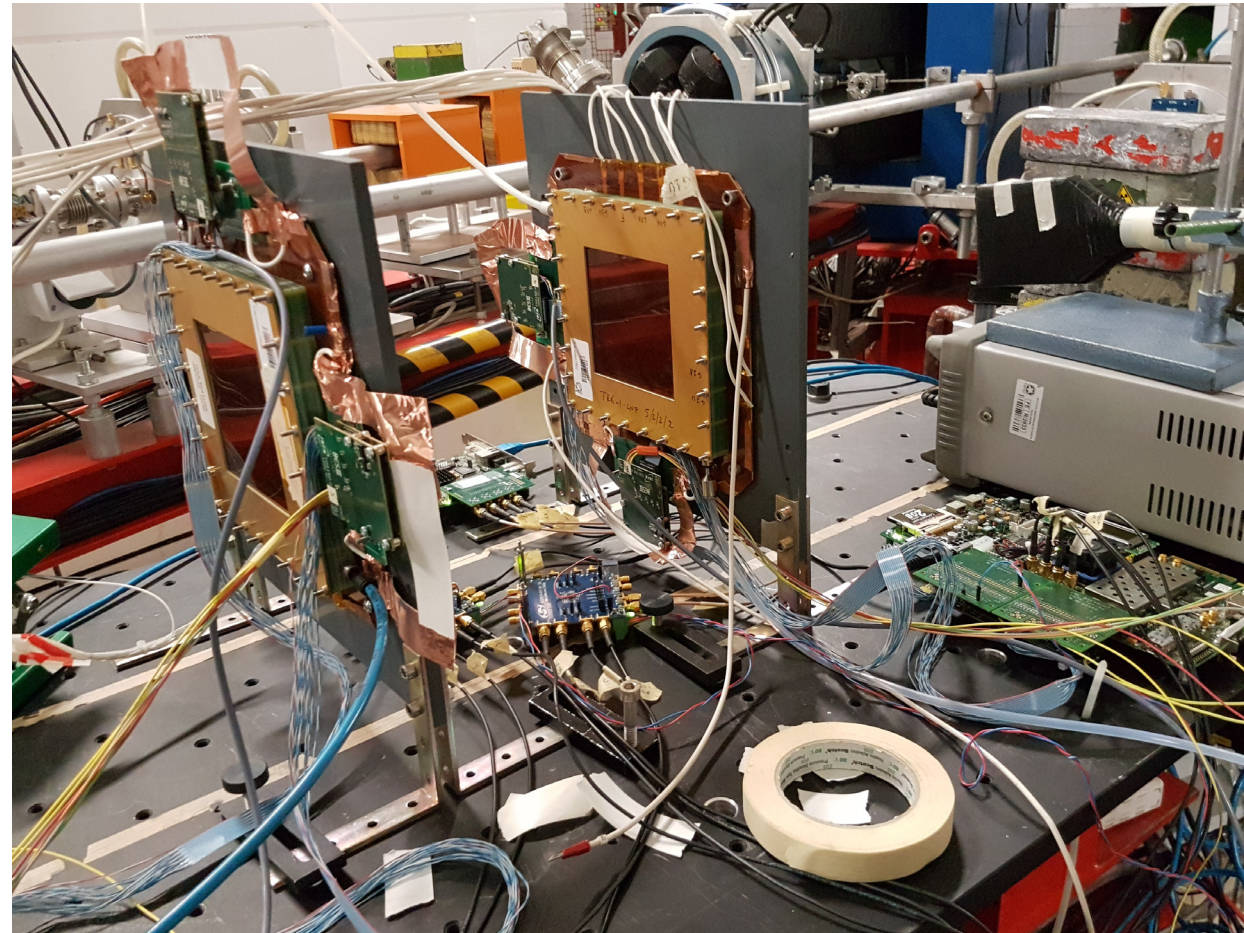
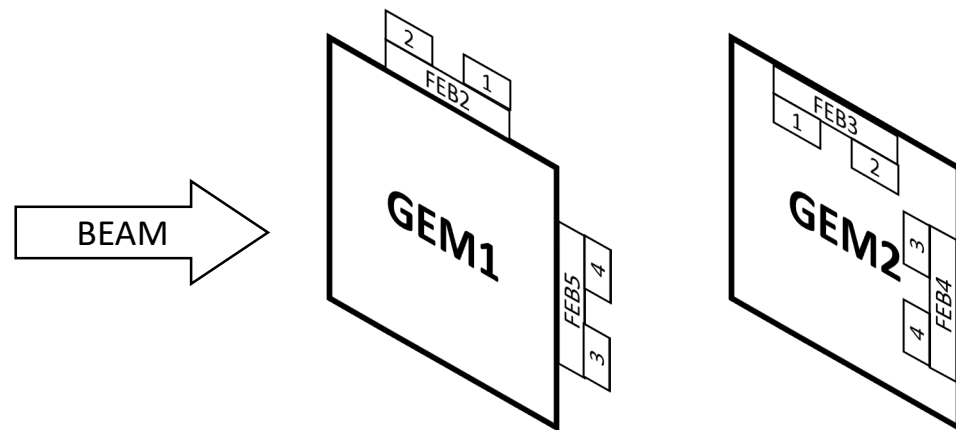
*Test beam at Mainz with planar GEMs*

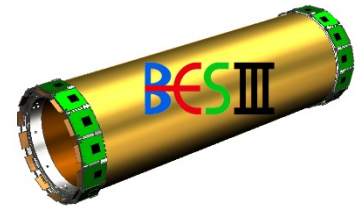


# Mainz Test Beam

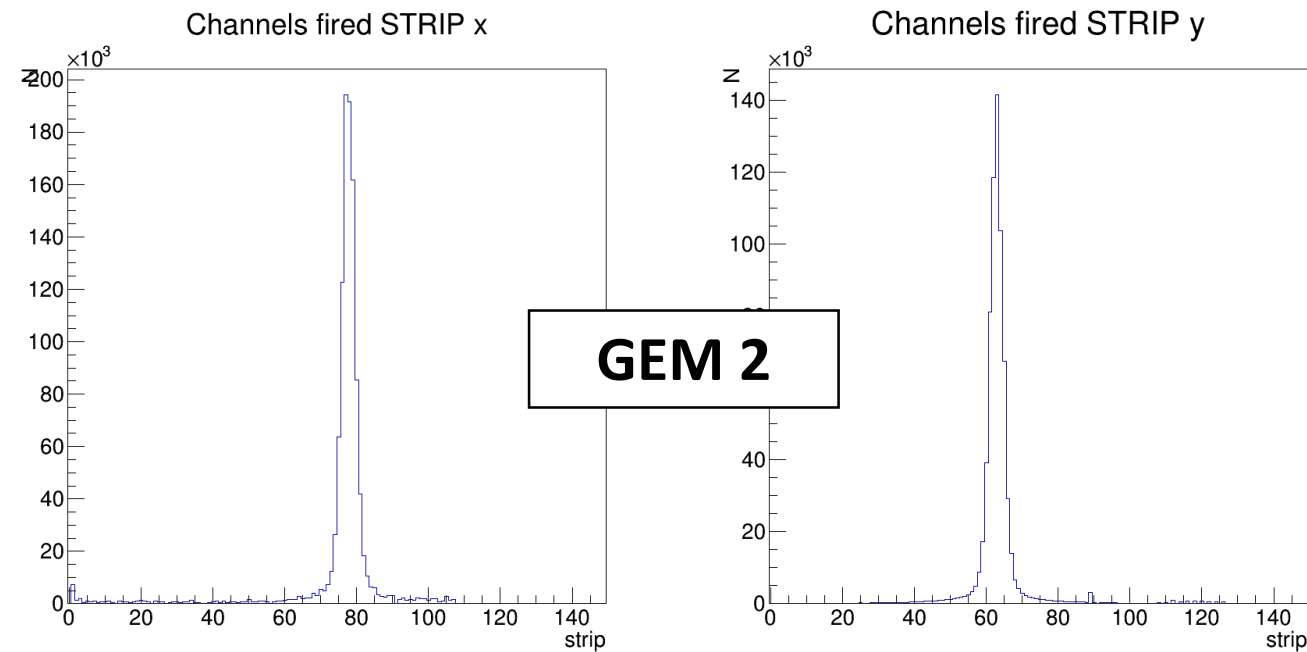
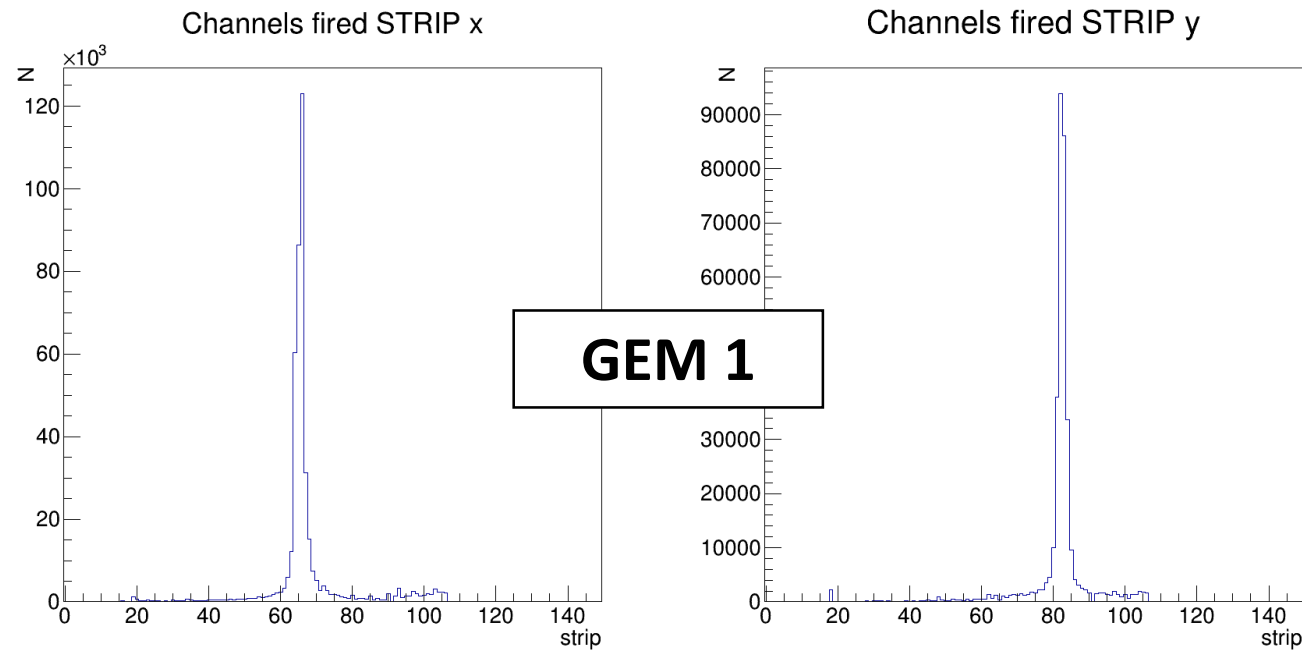


- MAMI (MAInz MIcrotron), Nov 13-16
- Test detector (planar GEMs) + electronics (TIGERv0) to fully validate the system
  - 2 planar GEMs
  - 4 FEBs = 8 TIGER (2 FEBs for each GEM)

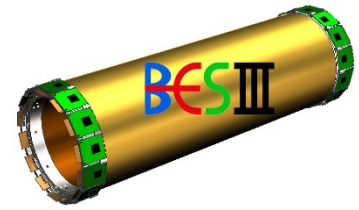




# Beam profile







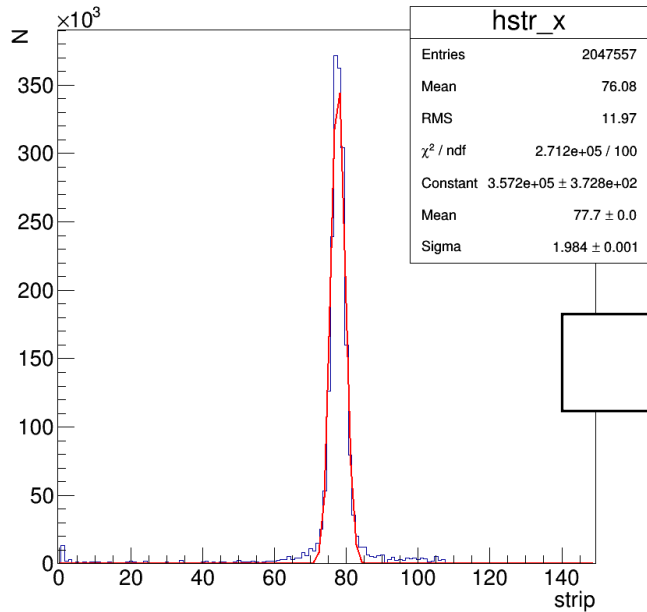
# Beam profile

GEMs rotated 30° along the X-axis to replicate the conditions in BESIII Experiment

- enlarged X-strip profile
- same Y-strip profile

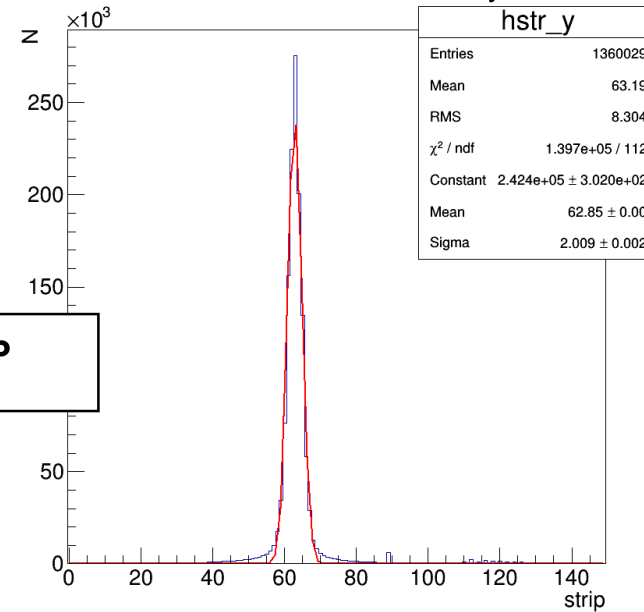


Channels fired STRIP x

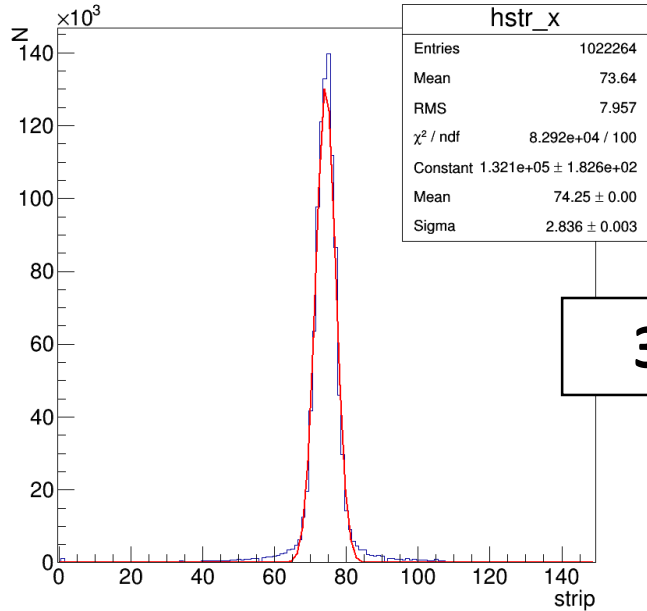


0°

Channels fired STRIP y

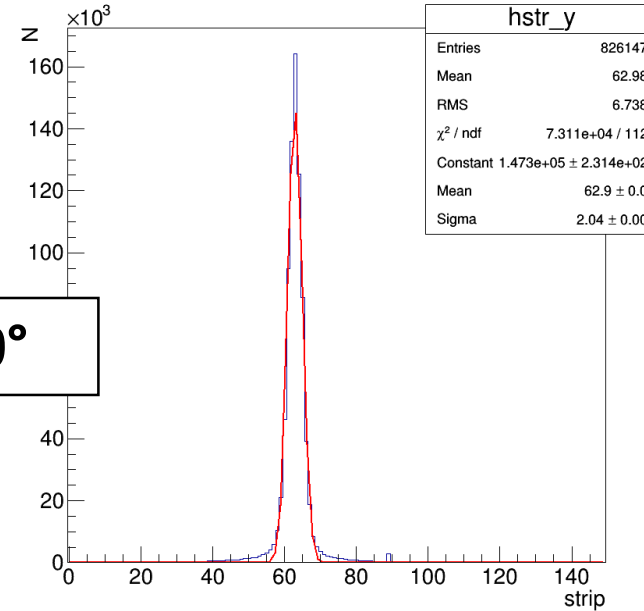


Channels fired STRIP x

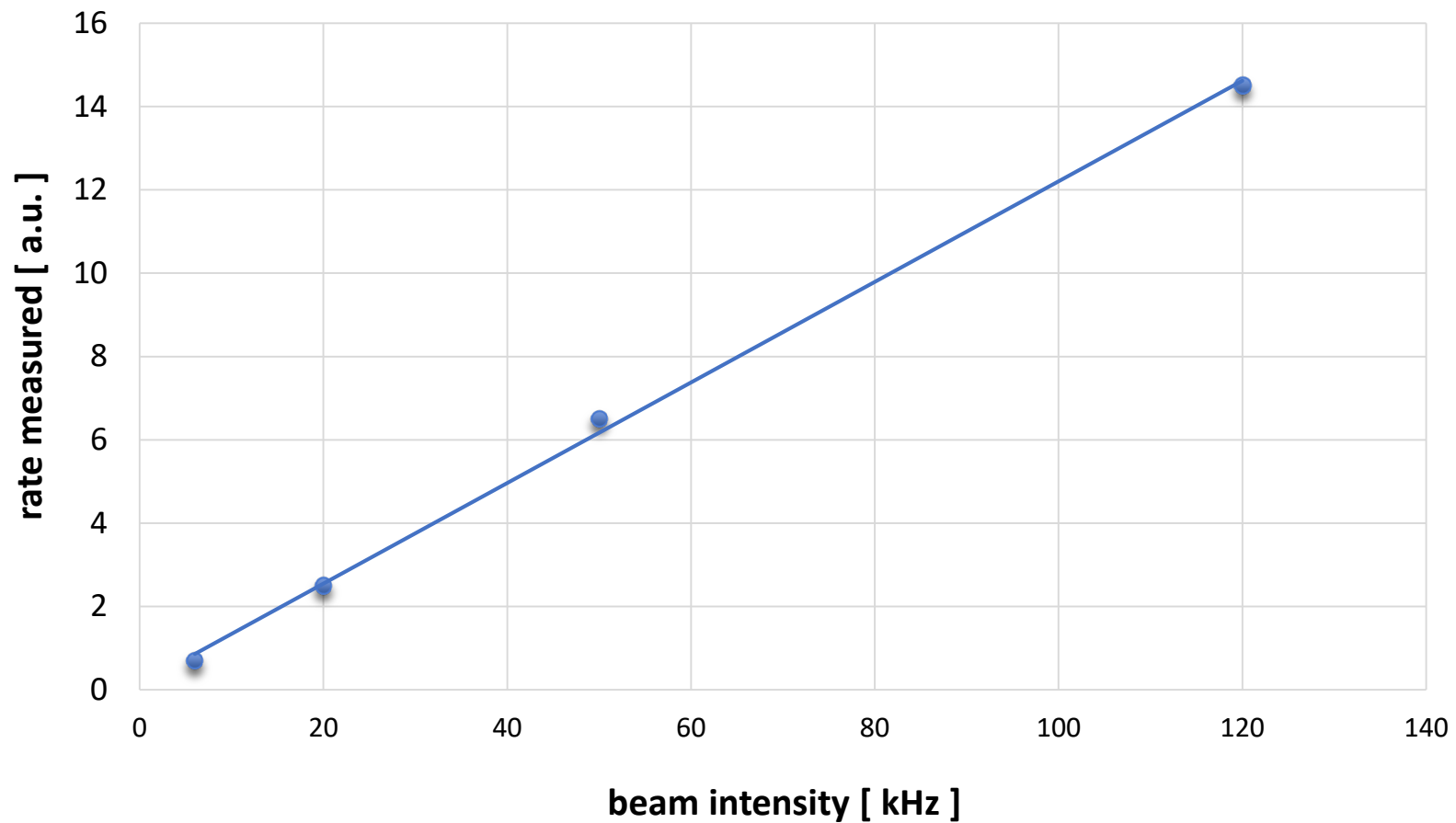


30°

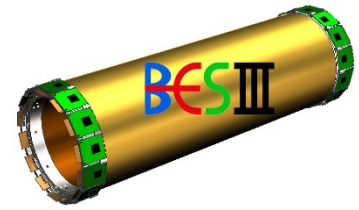
Channels fired STRIP y



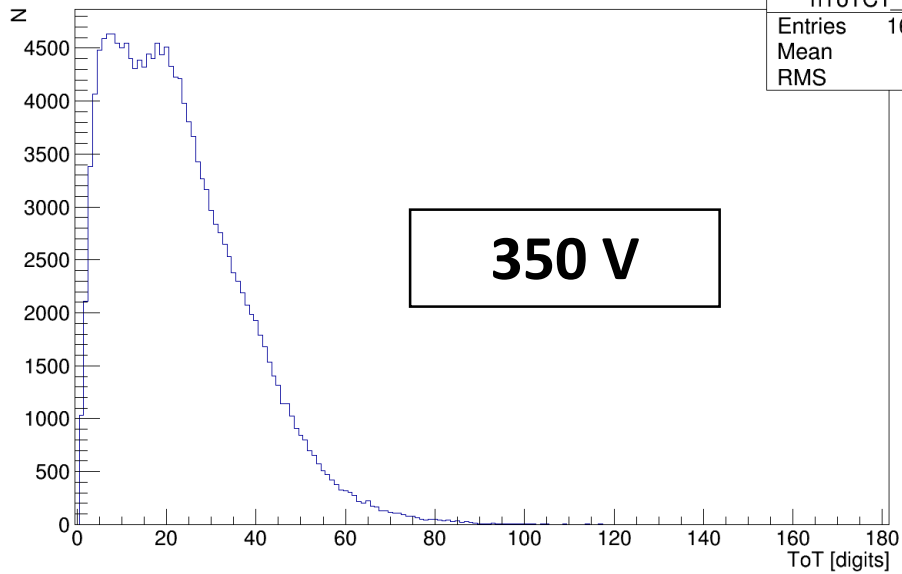
# Rate capability



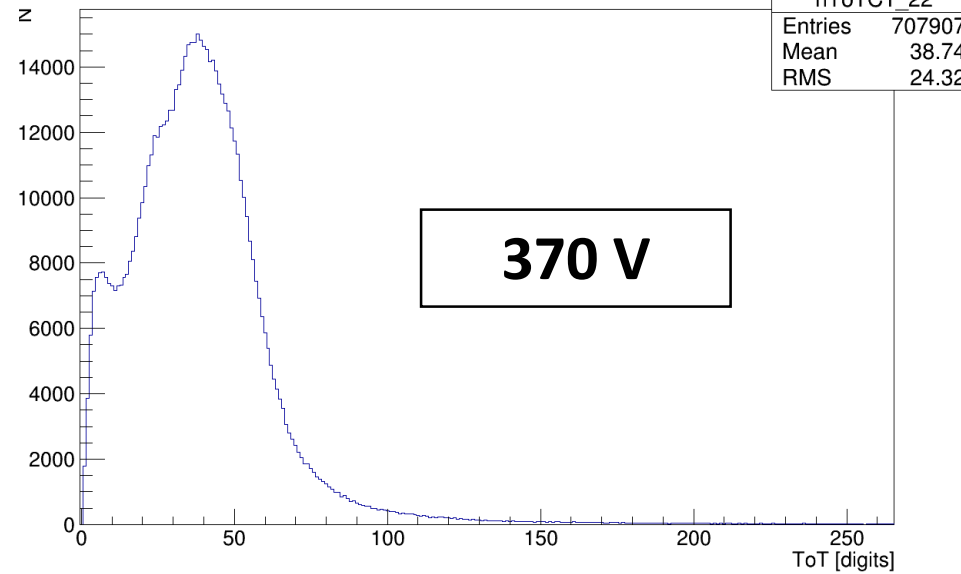




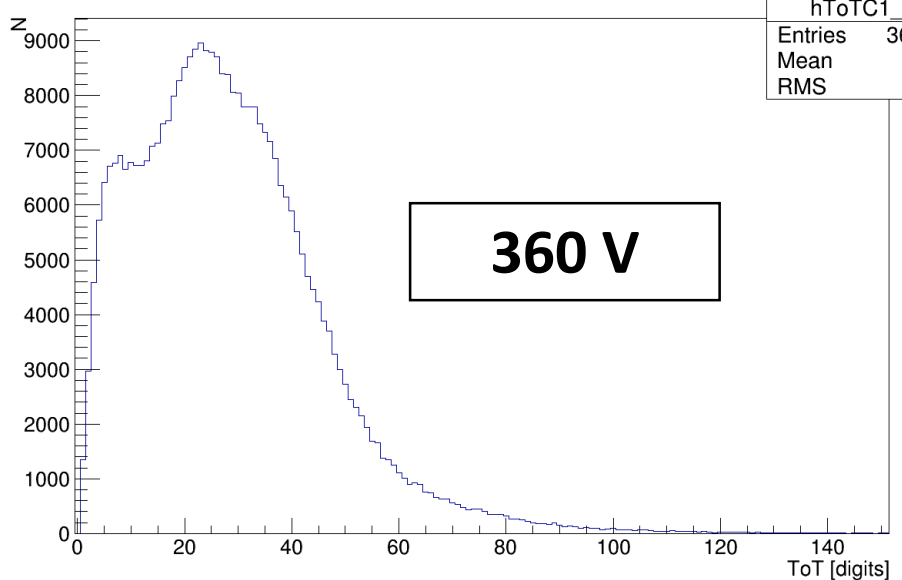
CHIP 1 ToT channel 22



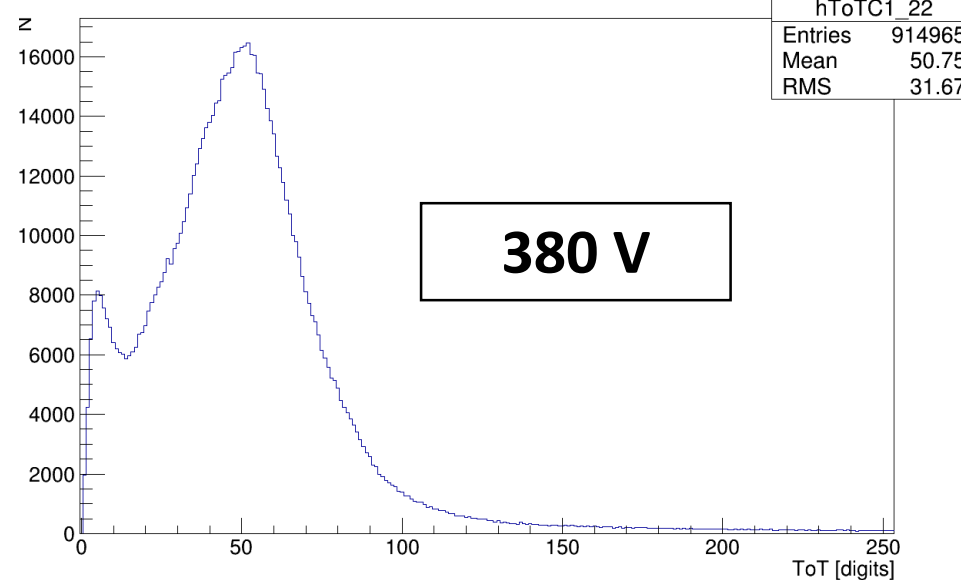
CHIP 1 ToT channel 22



CHIP 1 ToT channel 22



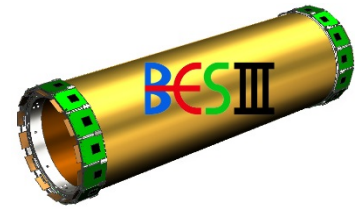
CHIP 1 ToT channel 22



# HV scan



# Summary and Outlook



- ASIC fully functional and validated
  - Time-based readout working properly
  - Charge measurement: good linearity with S/H
  - Successful validation of a fully-equipped double planar GEM setup with 8 TIGER chips (~512 channels)
- FEB production for all layers completed
  - Layer-1 FEBs test and calibration completed, installed on detector
  - Layer-2/3 FEBs characterization ongoing (installation expected by mid July)
- Tests with cylindrical GEMs ongoing
  - signals from cosmic rays and  $^{90}\text{Sr}$
- In situ (BESIII @ IHEP) commissioning of fully instrumented BESIIICGEM-IT (Autumn 2018)







Istituto Nazionale di Fisica Nucleare  
SEZIONE DI TORINO

## Torino TIGER WG

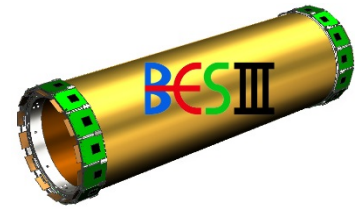
M. Alexeev, A. Bortone, J. Chai, W. Cheng, F. Cossio, M. D. Da Rocha Rolo, G. Giraud, M. Greco, M. Maggiora, S. Marcello, M. Mignone, A. Rivetti, R. Wheadon



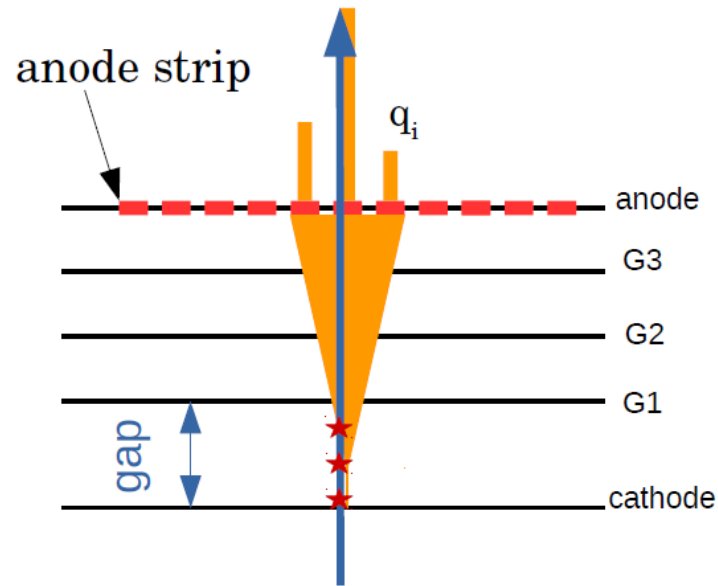
*The BESIII CGEM project has been funded by European Commission within the call H2020-MSCA-RISE-2014*

# Backup Slides

# Why an analogue readout?

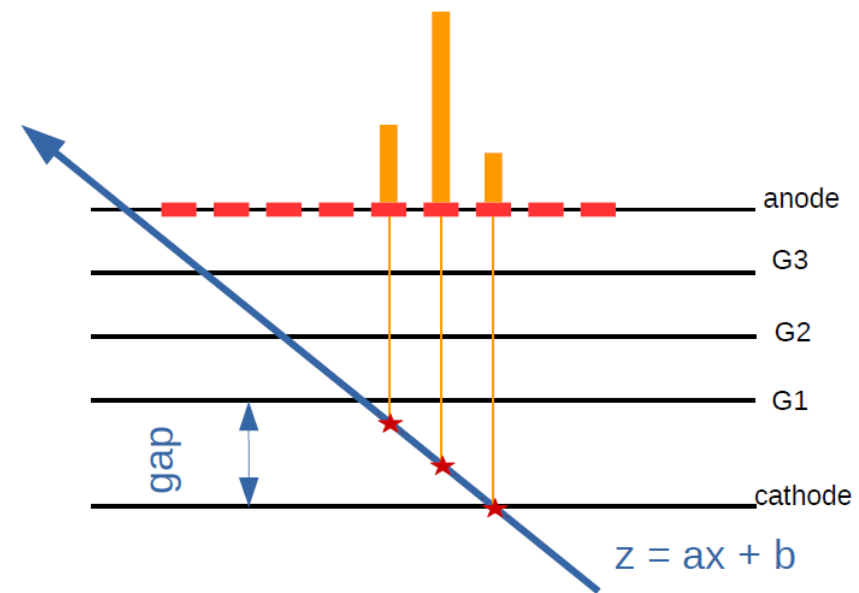


## Charge Centroid algorithm



- Weighted average position from fired strips
- Improve spatial resolution vs digital readout (constrained to the strip pitch)

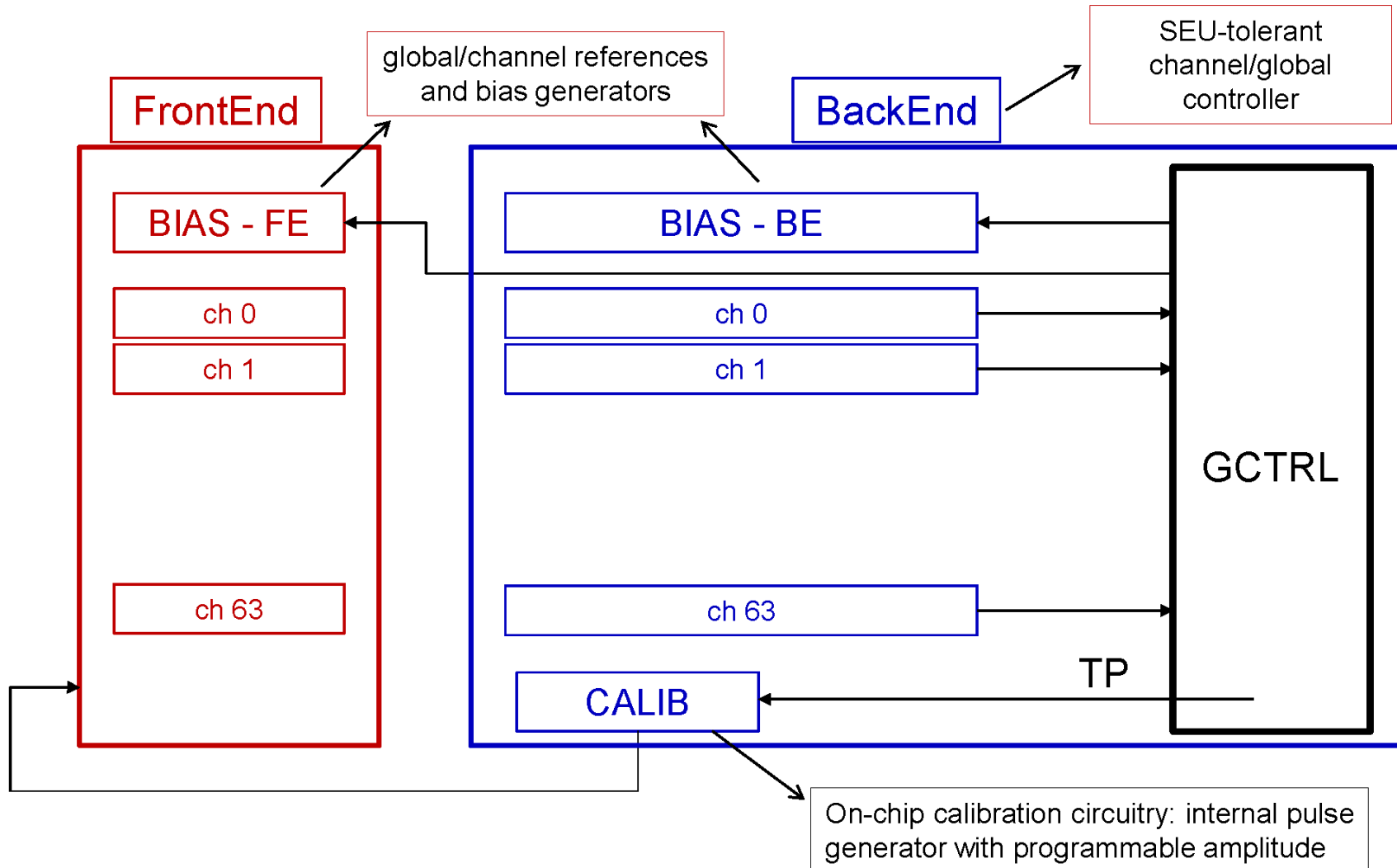
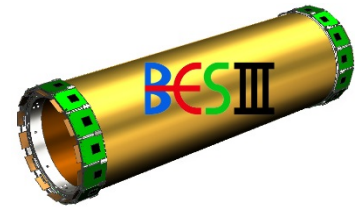
## $\mu$ -TPC mode



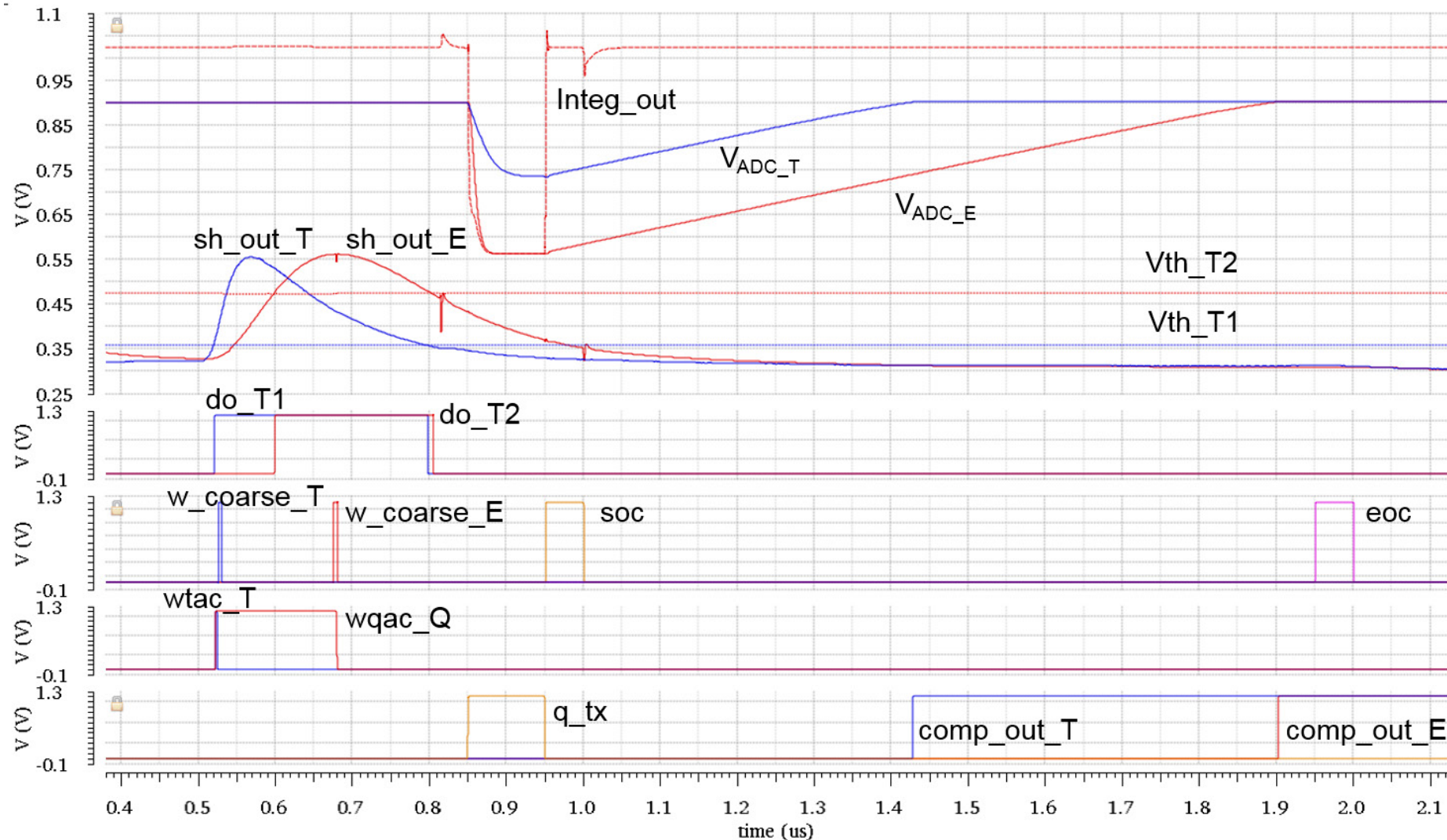
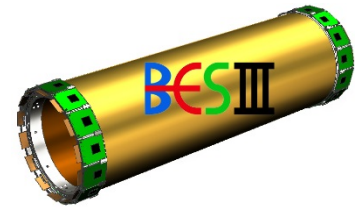
- Known the drift velocity, use time information to assign to each fired strip a 2D point
- Reconstruct the particle track from these coordinates
- Improve the spatial resolution in magnetic field, especially for angled tracks



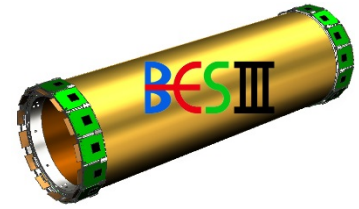
# Overview of the chip architecture



# Simulation of one event



# TIGER v2



- **TIGER Versatile Digitizer**
  - Alternative design, shared engineering run
  - Versatile front-end, can be used for readout of GEM or other sensors
- RGC (common-gate with gm-boosting) input-stage
  - Current-mode amplification
  - Low configurable input impedance
  - Programmable gain: 3-bit DAC, range 50-300 fC Input

