VMM and the SRS - update

Michael Lupberger (CERN)

Outline

ASIC implementation – an overview

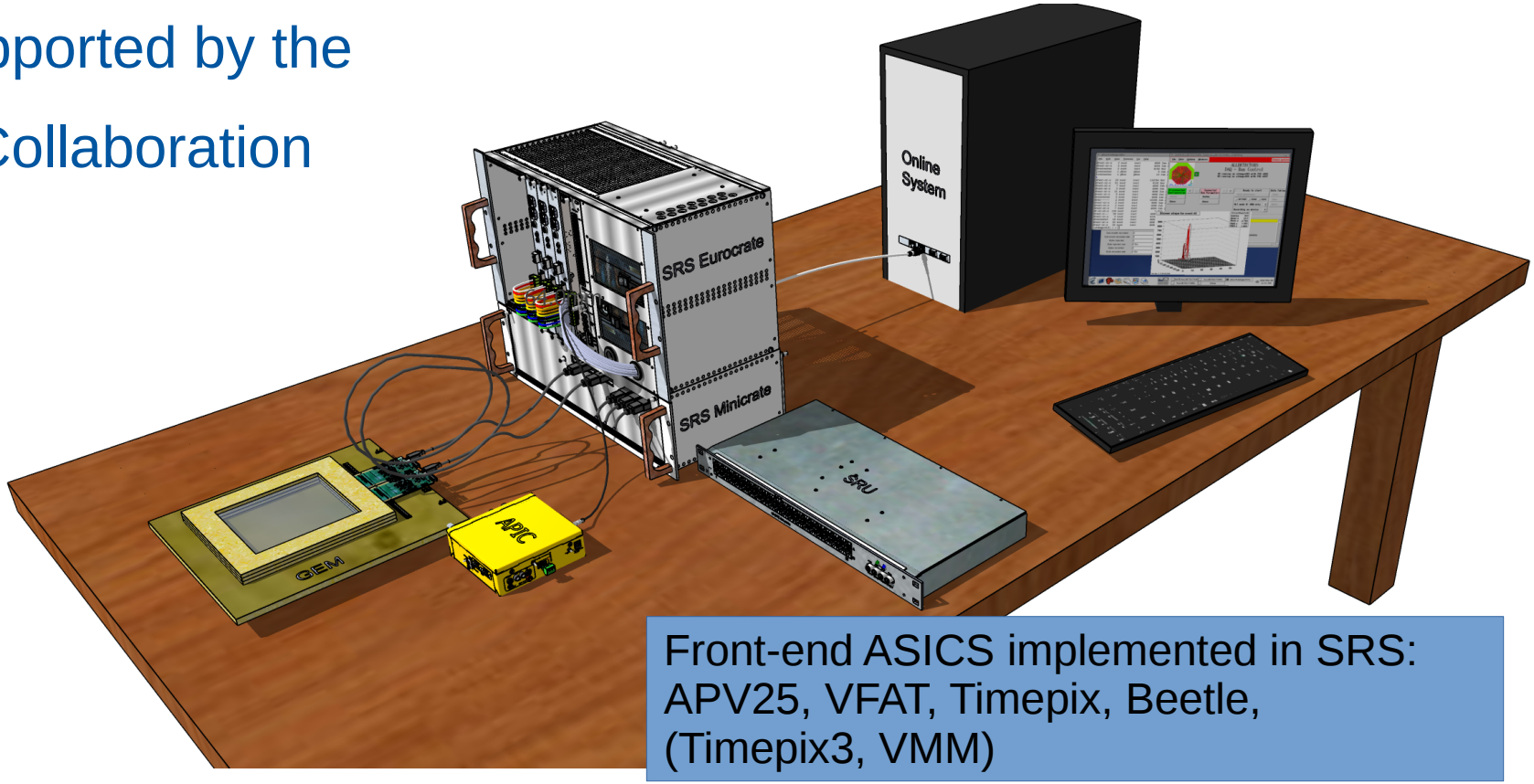
What happened since the last Mini week in February

Future SRS VMM users

Outlook into the near future

SRS

A generic readout system for laboratory and detector instrumentation developed and supported by the RD51 Collaboration



Front-end ASICS implemented in SRS:
APV25, VFAT, Timepix, Beetle,
(Timepix3, VMM)

VMM ASIC

130 nm CMOS technology

64 input channels, each w/ preamplifier, shaper, peak detector, several ADCs

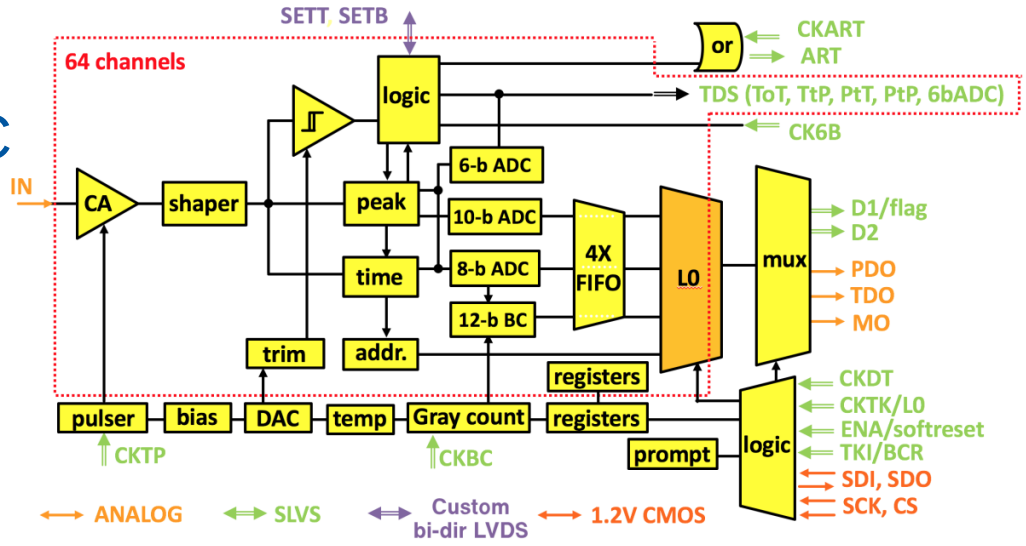
Pos. & neg. polarity sensitive

Digital block w/ neighbouring logic, FIFO, multiplexer

Adjustable gain 0.5 – 16 mV/fC

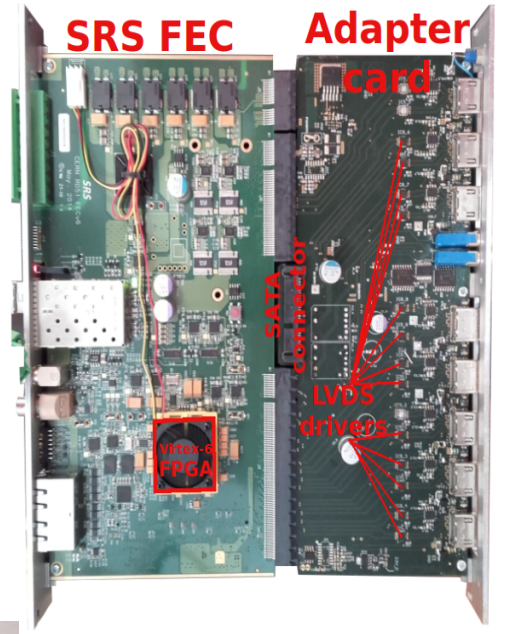
Adjustable shaping time from 25 ns – 200 ns

Input capacitance from few pF – 1 nF



ASIC implementation – an overview

Current status of hardware



SRS FECv6

Available and working fine – as it is general SRS hardware

Adapter Card

3 older versions working

PCB design of final version ongoing, schematics completed

Hybrids

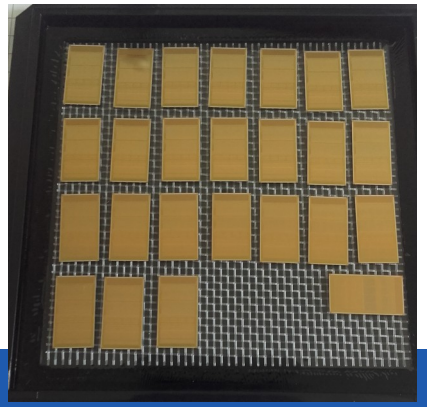
Some VMM2 hybrids → not used any longer

4 first VMM3 prototype hybrids died after intense testing for about 1 year

3 new VMM3 prototype hybrids (not final version) for testing

1 new VMM3a prototype hybrid (not final version) just in from bonding lab

28 final version hybrids PCBs in production, expected this week:
- 24 will go to a company for component placing and VMM3/3a bonding,
- 4 will go the CERN SMD lab and CERN bonding lab for VMM3a bonding



ASIC implementation – an overview

Current status of firmware

SRS FECv6

Working good, but optimisation ongoing → see Yan's presentation

Hybrids

Working good, but optimisation ongoing:

Freddy was again at CERN for 7 weeks, improving readout speed of VMM to Spartan FPGA

- readout clock 40 MHz → 160 MHz, configurable readout clock (10, 20, 40, 80, 160) MHz
- all tested and working reliably in both single and double data rate
- theoretical maximum 200 MHz not achieved. Some bit errors at about 180 MHz
  could be due to VMM2, which was used for tests

BCID reset by user configuration implemented

BCID reset at start of each measurement ongoing

I2C ADC readout for new final hybrid ready

Big project still to do on both FEC and hybrid: Master/Slave

ASIC implementation – an overview

Current status of software

News: collaboration with CERN EP-DT-DI for development and long term support → DAQ discussion in this session

Slow control

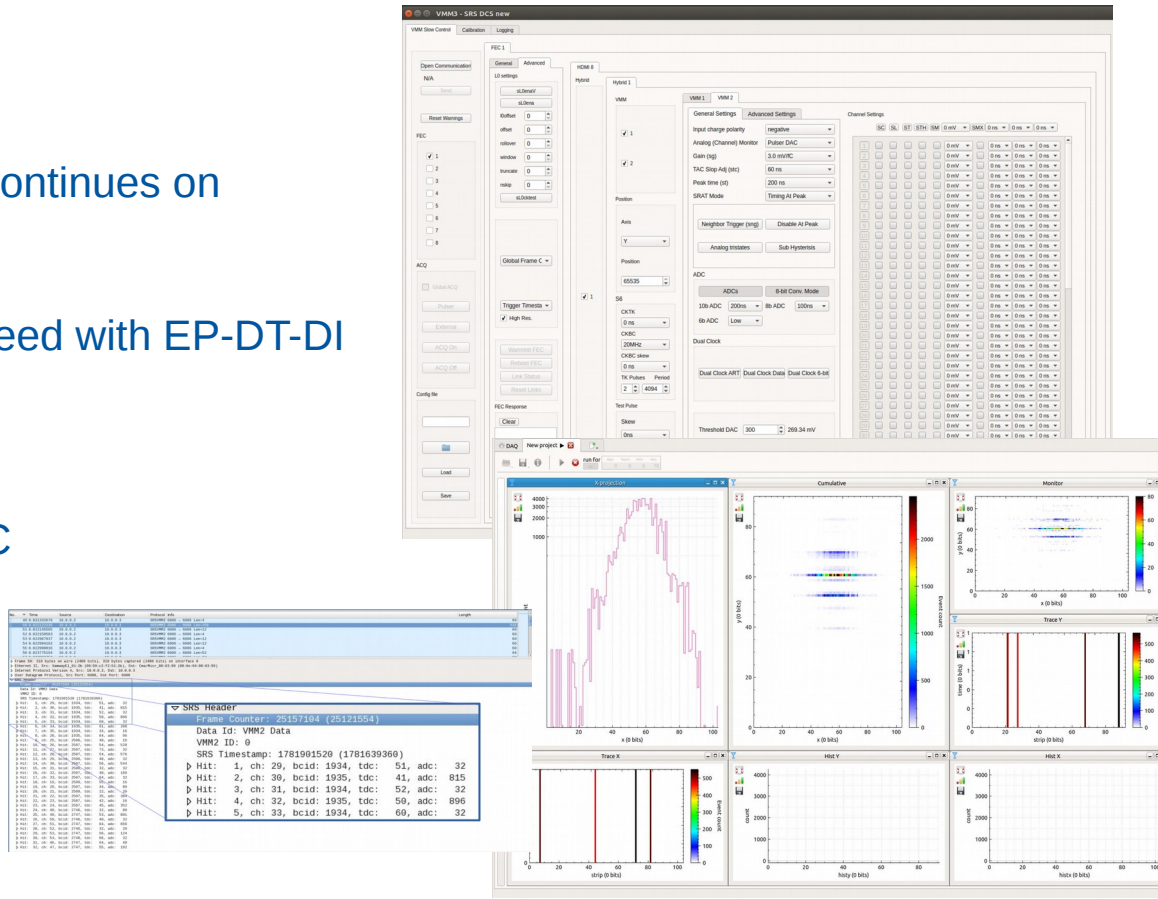
New CERN summer student (Usman) continues on current version (by Manuel)
- implement automated calibration
- convert to web based interface as agreed with EP-DT-DI

Online monitoring

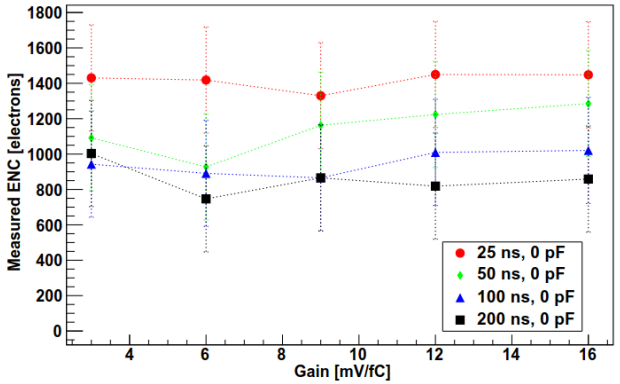
- Martin's tool developed by ESS DMSC
- Graphana
- Wireshark with plugin

Data acquisition (storing)

- Morten's tool



What happened since February 2018



VMM3 hybrid noise test

→ completed, publication in preparation

RD51 test beam in March/April

→ no participation due to lack of VMM hybrids and delayed production

Preparation for the future

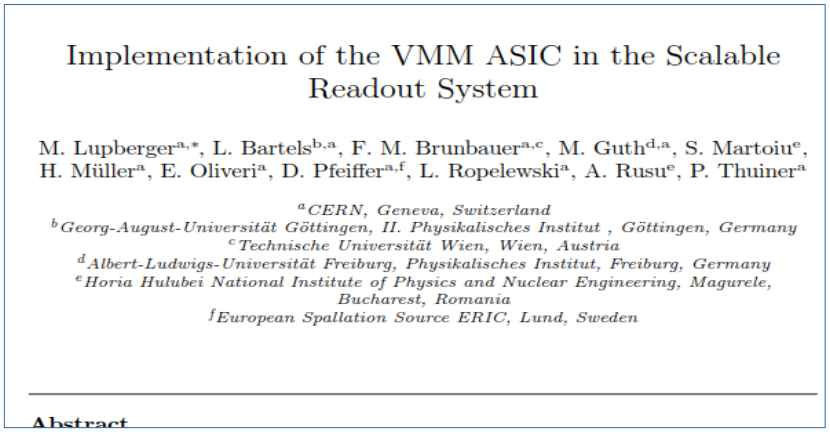
→ Publication “Implementation of the VMM ASIC in the Scalable Readout System”
→ work on grant applications to secure further developments

Firmware developments

→ Hybrid: BCID reset
→ FEC: see Yan’s presentation

Software

→ see discussion



Implementation of the VMM ASIC in the Scalable Readout System

M. Lupberger[a,*], L. Bartels[b,a], F. M. Brunbauer[a,c], M. Guth[d,a], S. Martoiu[e], H. Müller[a], E. Oliveri[a], D. Pfeiffer[a,f], L. Ropelewski[a], A. Rusu[e], P. Thuiner[a]

[a] CERN, Geneva, Switzerland
[b] Georg-August-Universität Göttingen, II. Physikalisches Institut , Göttingen, Germany
[c] Technische Universität Wien, Wien, Austria
[d] Albert-Ludwigs-Universität Freiburg, Physikalisches Institut, Freiburg, Germany
[e] Horia Hulubei National Institute of Physics and Nuclear Engineering, Magurele, Bucharest, Romania
[f] European Spallation Source ERIC, Lund, Sweden

Abstract

Future SRS VMM users

Group	Application	VMM hybrids	Contact
ESS Lund / BrightnESS	NMX instrument @ ESS	164	Dorothea PFEIFFER
University of Science and Technology of China	RICH R&D for future colliders in China (CEPC and STCF)	156	LUI Jianbei
Bonn University	BASTARD neutron detector	71	Jochen KAMINSKI Markus KÖHLI
Mainz University	MAGIX experiment @ MESA	211	Stefano CAIAZZA
Budker Institute of Nuclear Physics, Novosibirsk	μWell MPGD R&D	22	Lev I. SHEKHTMAN
INFN Tieste	Generic R&D	10	Silvia DALLA TORRE
Tsukuba University	ALICE FoCal, Si Pads	50	CHUJO Tatsuya
GDD group CERN	Generic R&D	16	Eraldo OLIVERI
Peking University	CMS GEM upgrade	52	Dayong WANG
LMU Munich	Ion Tomography with Micromegas	16	Felix KLITZNER
LMU Munich	Medical physics with MPGDs, Si	48	Jona BORTFELDT
ETH Zurich	GBAR experiment @ CERN	≈40	Gianluca JANKA
CERN	BGV(Beam Gas Vertex) beam monitor*	200	Robert KIEFFER
University of Virginia, Charlottesville	EIC tracker @ RHIC*	Not known yet	Kondo GNANVO

Outlook into the future

What will/should happen until the end of this year

Highest priority: Users need hardware asap

→ complete adapter card design and produce PCBs
→ equip the 28 hybrids with components and VMMs and learn from this test production
→ secure VMM supply for all the user projects
→ help users to get first test systems
→ documentation and training

Continue development, system will still be in a prototype state

→ possibly master/slave option will not be implemented in firmware yet
→ not critical, it should be clear to all users that SRS is not (never) a finished product
→ further development will also rely on users

BrightnESS (funding for SRS VMM developments) will end in Sept

→ ESS supports the project until end December

RD51 needs to prepare for after 2018 now in order to continue SRS VMM

→ **Discussion at the end of this session**

Conclusion

Implementation of VMM in SRS is advancing well

→ All aspects as software, hardware firmware and production are treated

→ Call as always: SRS lives on users! If you have a student you can send, please tell us

Major advancements since last Mini week

→ First articles for publication

→ SRS FEC firmware data though improved significantly

→ Readout speed of data from VMMs improved significantly

→ We can be lucky to have (had) two students with excellent FPGA programming skills

Preparing for the future

→ More and more groups want to use SRS VMM

→ The collaboration undertakes efforts to assure the continuation of these developments