Future of SRS system: Hardware and Firmware – my ideas

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Outlook into the future

What will/should happen until the end of this year

Highest priority: Users need hardware asap

→ complete adapter card design and produce PCBs
→ equip the 28 hybrids with components and VMMs and learn from this test production
→ secure VMM supply for all the user projects
→ help users to get first test systems
→ documentation and training

Continue development, system will still be in a prototype state

→ possibly master/slave option will not be implemented in firmware yet
→ not critical, it should be clear to all users that SRS is not (never) a finished product
→ further development will also rely on users

BrightnESS (funding for SRS VMM developments) will end in Sept

→ ESS supports the project (e.i. my position at CERN) until end December
My fellowship at CERN will then definitely and and I will move to Bonn for private reasons

→ **RD51 needs to prepare for after 2018 now in order to continue SRS VMM**

Outlook into the future

What will/should happen after this year

SRS VMM will replace SRS APV and become THE readout option in RD51 and even projects outside our collaboration

→ continued development and support needs to be guaranteed
→ new funding for a person working on electronics at CERN is not yet assured (EP R&D outcome)
→ manpower with knowledge and experience is leaving CERN

Proposal: Optimum solution for RD51 and myself:

→ I propose to continue my work on SRS in Bonn
→ RD51 would like me to continue working on SRS
→ a central SRS group would help the whole collaboration
→ additional funds would help SRS to develop further

→ I intend to set up my own group (or at least my own position) in Bonn and hence apply for several grants with support of RD51

⇒ Continuation of SRS VMM developments would be secured for the next years at no additional costs to the collaboration with the same or even more manpower than currently.

Outlook into the future

What will/should happen in the next years

SRS VMM will replace SRS APV and become THE readout option in RD51 and even projects outside our collaboration

→ the system shall be further developed to fully exploit the capabilities of the VMM and current SRS hardware (highest priority).
→ SRS users and developers groups shall continuously improve the system such that can be operated reliably in the lab and at experiments
→ the supply with hardware, firmware, software, training and know how is organised
→ more and more users (also running experiments or such in the design phase) will join

SRS core hardware needs refreshment (FECv6 is from 2013)

→ By learning from other system in HEP (like CaRIBOu, FELIX, PCIe40, USBpix, SPIDR, RCE…) a new FEC shall be designed. Current ideas:
- Go from pure FPGA to System on Chip (combined FPGA and CPU)
- Significantly improve output bandwidth to handle data from larger system and cope with high data rates of VMM (up to 800 Mb/s/VMM) and recent ASICs in general (e.g. Timepix3: 5.12 Gb/s), optimum would be 100 Gb/s Ethernet output at new FEC
- Valencia group could help (Curro offered support)

Outlook into the future

What will/should happen in the next years (continued)

Implement new ASICs in SRS

→ VMM implementation most advance (BrightnESS and AIDA2020)
→ Timepix3 and GEMROC ongoing (AIDA2020)
→ future candidates: SAMPA, an ASIC of the SiPixel community

Use new SRS hardware to enter new dimension of application

→ SHIP experiments also plans VMM based tracker readout
→ almost half of the instruments at ESS will use VMM
→ new ASICs will open up new fields of application e.g. SiPixel community or allow for an SRS based readout for several subdetectors in an experiment

Establish a standard in our field

→ proper documentation and a common database with firmware and software coding blocks

→ the effort of common readout electronics for a whole community is unique
→ other communities could profit from similar effort
→ propagate this idea (and propose SRS as a starting point)