



Детекторы нового поколения

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Outline



1. Silicon Detectors for HEP experiments
2. Pixel detectors:
 - a) Now
 - b) Future
3. ALICE Inner Tracking System: current status and upgrade strategy
4. ALICE Pixel Detectors (ALPIDE family)
5. The ALPIDE characteristics studies
6. Detectors in Future Experiments
7. Industrial applications
8. Next planes
9. Conclusions

Silicon Detectors for HEP experiments



ALICE Pixel Detector

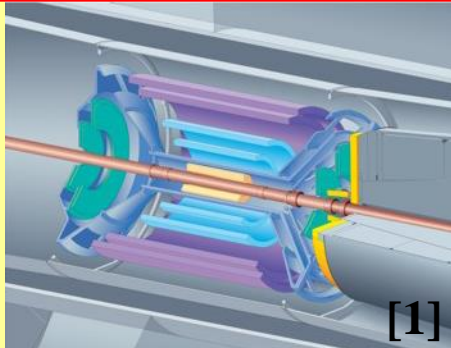
first two layers: tracking

ALICE Drift Detector

two middle layers: tracking+PID

ALICE Strip Detector

two outer layers: tracking+PID



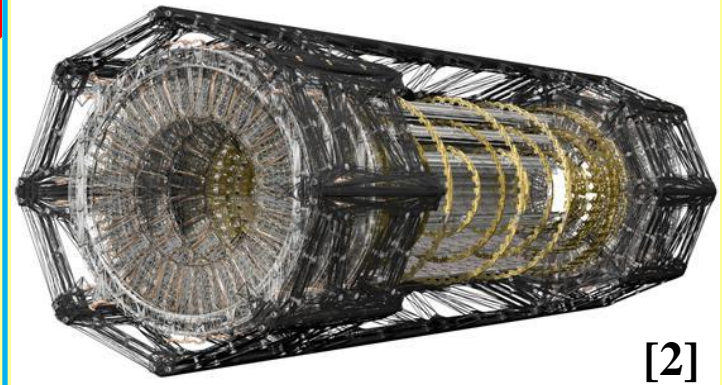
ATLAS Pixel Detector

80 million pixels

area: 1.7m²

15 kW power consumption

Pixel size: 50 x 400μm²



CMS Pixel Detector

65 million pixels.

Pixel size: 100×150 μm²



CMS Strip Tracker IB

First 4 layers (strips)

10 cm x 180 μm,

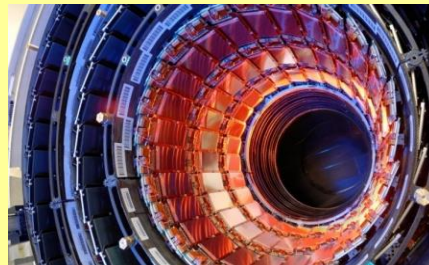
Next 6 layers (strips)

25 cm x 180 μm

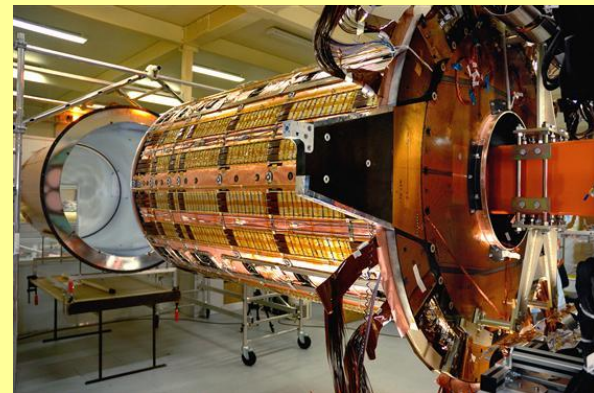
[4]

10 million strips

The largest Si detector in the world. More 200 m²



ATLAS Semiconductor Tracker (SCT)



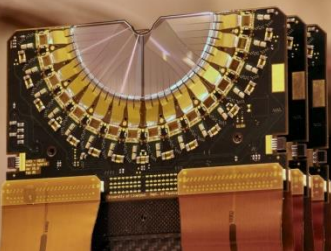
A silicon microstrip tracker : 4,088 two-sided modules and over 6 million implanted readout strips

LHCb VELO

VERTex LOcator

[5]

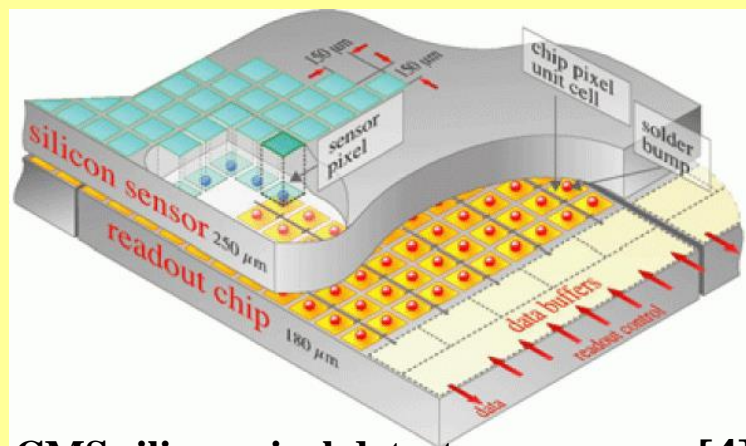
silicon microstrip detector



Pixel detectors: Now

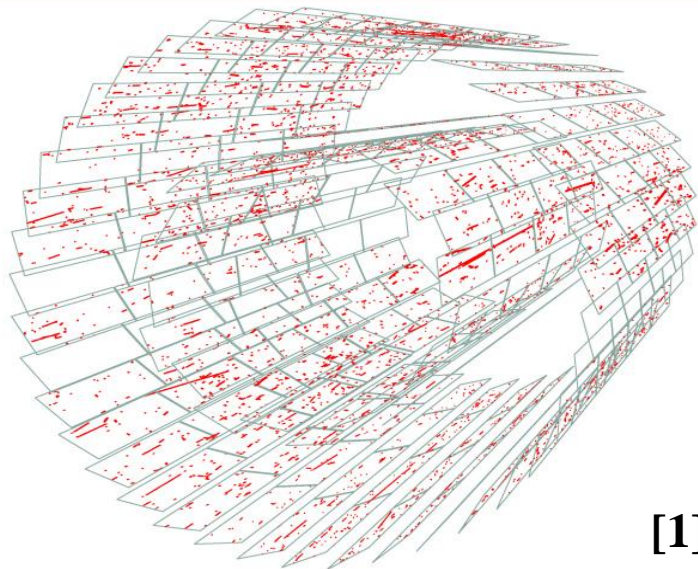
Hybrid Pixel Detectors in LHC:

- ATLAS
- CMS
- ALICE



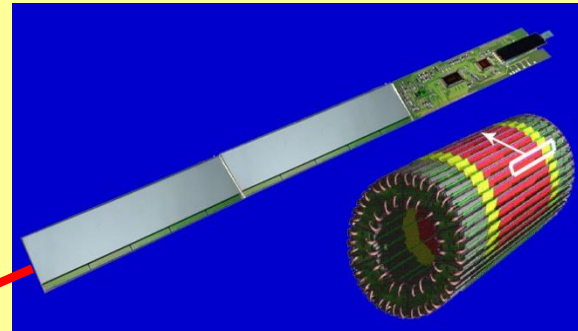
CMS silicon pixel detector [4]

- Good position resolution: Smaller pixels, Higher integration
- Small pixels - low capacitance - better S/N - smaller analog power
- More pixels – More logic per pixels – high integration
- Work at higher rates and high radiation level

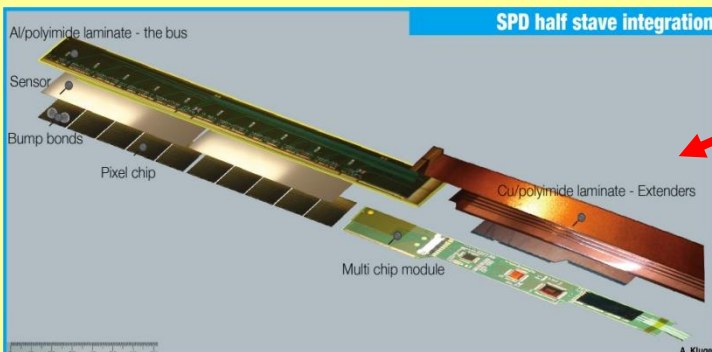
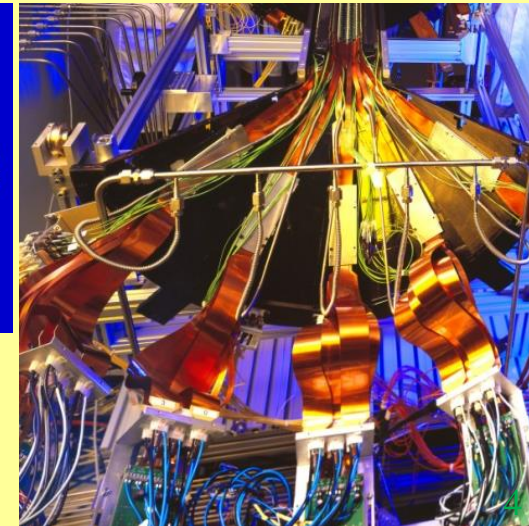


[1]

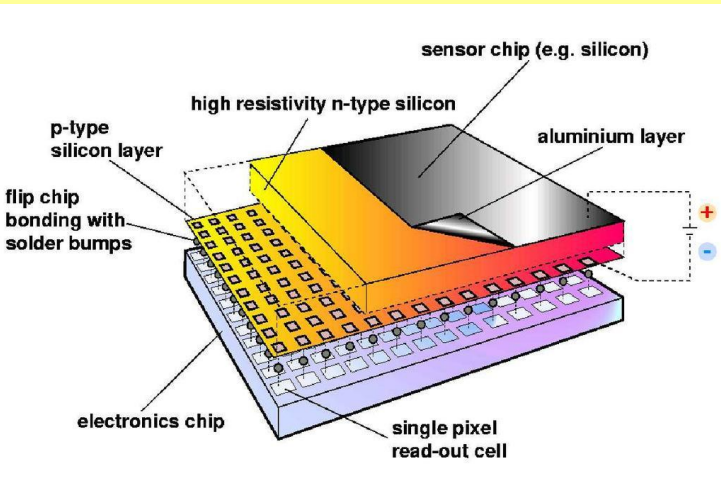
June 2008, ALICE Silicon Pixel detector registered muon tracks produced in the beam dump near Point 2 of the LHC



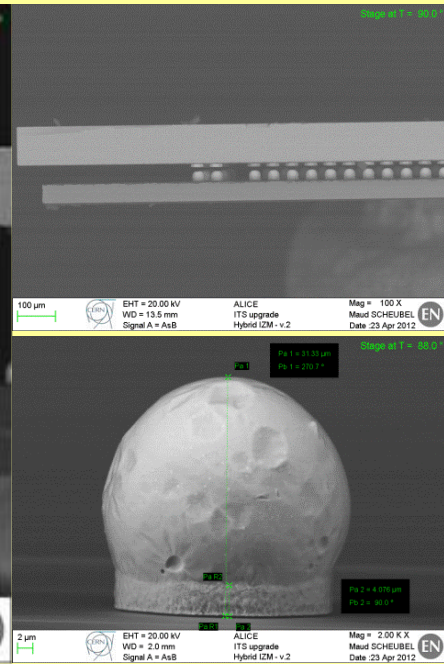
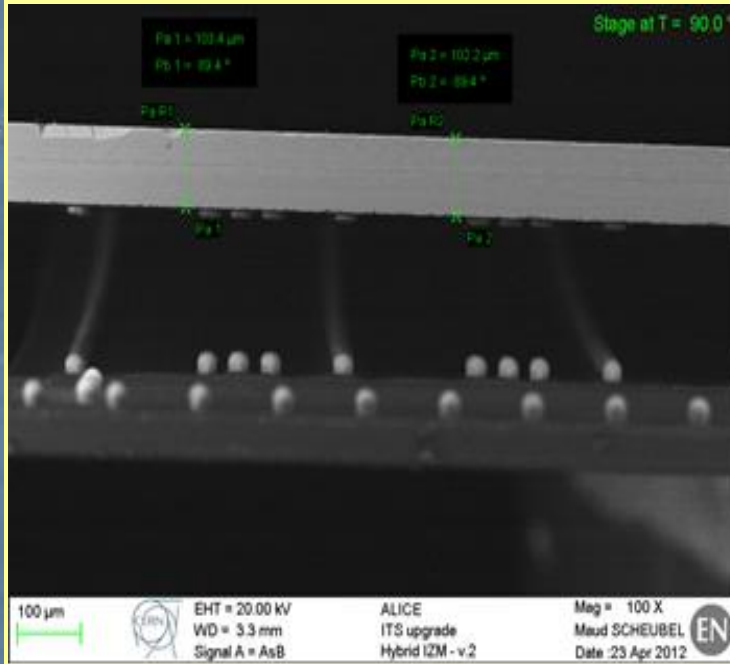
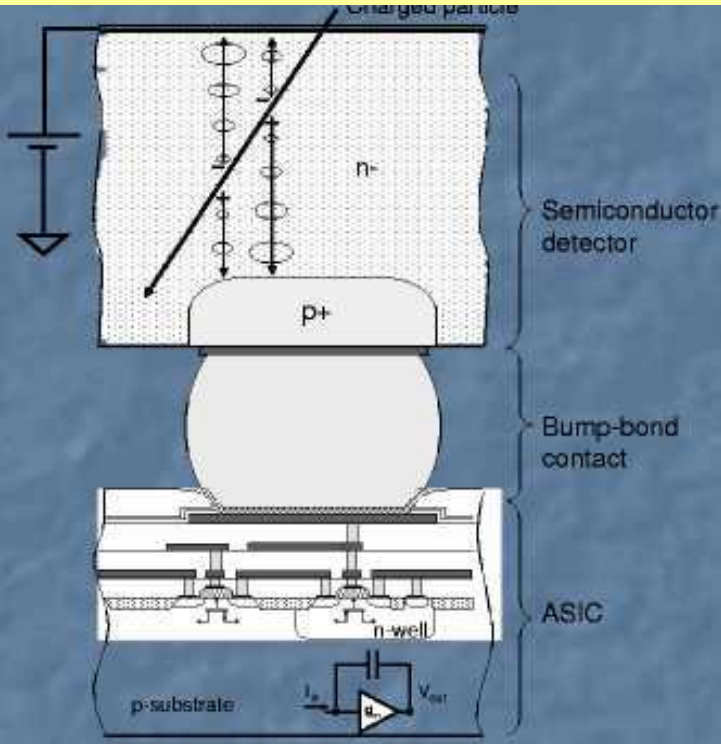
ALICE silicon pixel detector [1]



Pixel detectors: Now. Hybrid Pixel Detectors



1. Sensor and readout chip (ASIC) are independent modules
2. Interconnection needed to connect each pixel in the sensor to a readout cell in the ASIC - Bump bonding ASIC and detector (very complicated technologies)
3. Thick detector units: radiation length $1 - 3 \% X_0$
4. Sensor and electronics optimized for very high radiation (hit rate)



Chip 50 μm and sensor 100 μm ; sensor matrix 256x160 cells; pixel size: 50 μm x 425 μm [6] 5

Pixel detectors: Future



For HEP experiments. For future trackers

Excellent resolution - More channels - Higher integration

Low mass tracking system – Minimum materials (cables, cooling, services) - Low power consumptions

Radiation tolerance – work at high radiation doses

For electronics: acquire more data at higher rate - high speed data processing, low error rates (FPGA based trigger systems, CPU based DAQs)

**We will built Large and complicated systems
acceptable cost!**

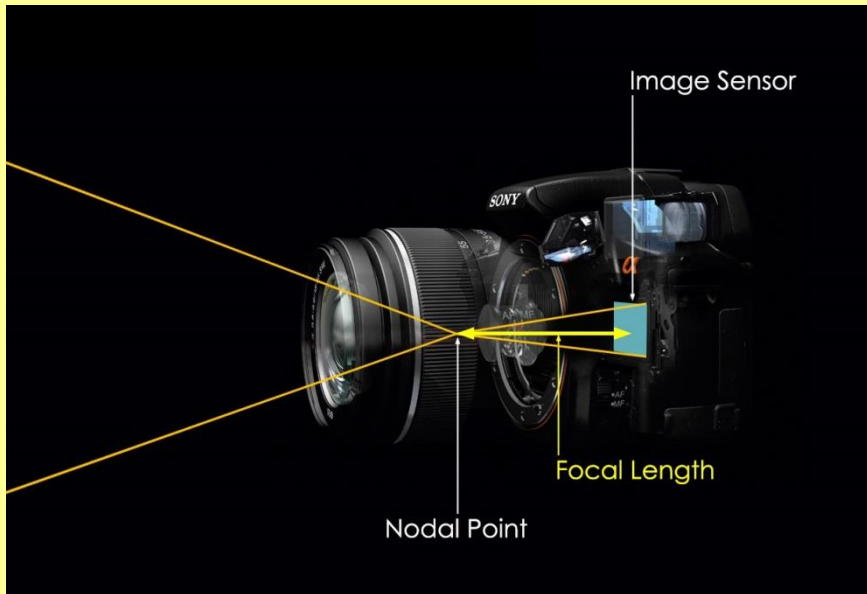
Pixel detectors: Future



Monolithic Active Pixel Sensors (MAPS)

Idea from CMOS Active Image Pixel Sensors

Advantages of CMOS imaging sensors (camera-on-chip) in industry: low power, compact devices (digital cameras) due to electronics – on a chip, reduced the number of components



Era of digital photography



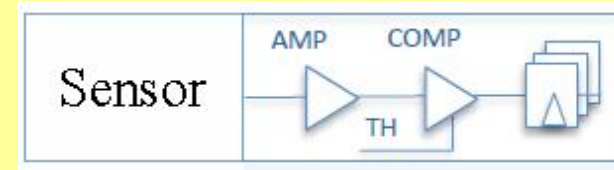
Era of mobile photography

Pixel detectors: Future

Monolithic Active Pixel Sensors (MAPS)

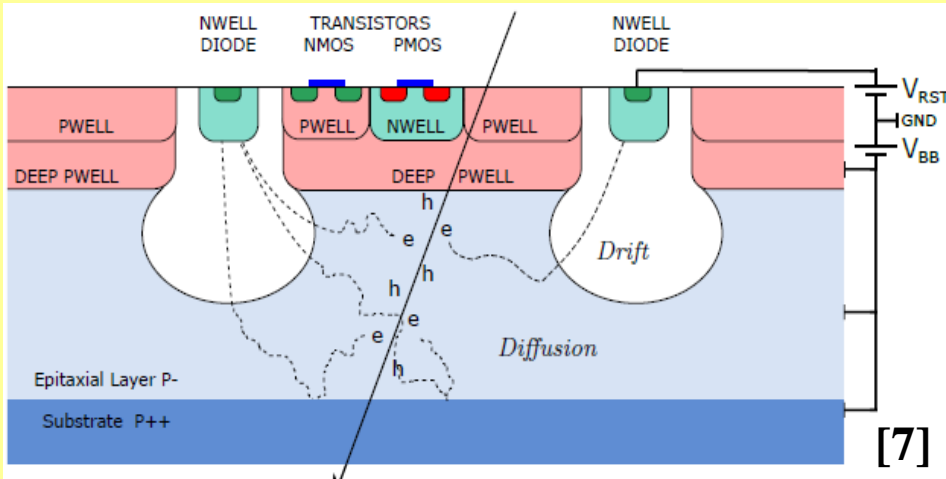


Active volume of the detector integrated into the ASIC
In one pixel we have detector + front-end electronics



Thin monolithic CMOS sensor, on-chip digital readout architecture

Optimized for highest hit rates and also work in high radiation environment

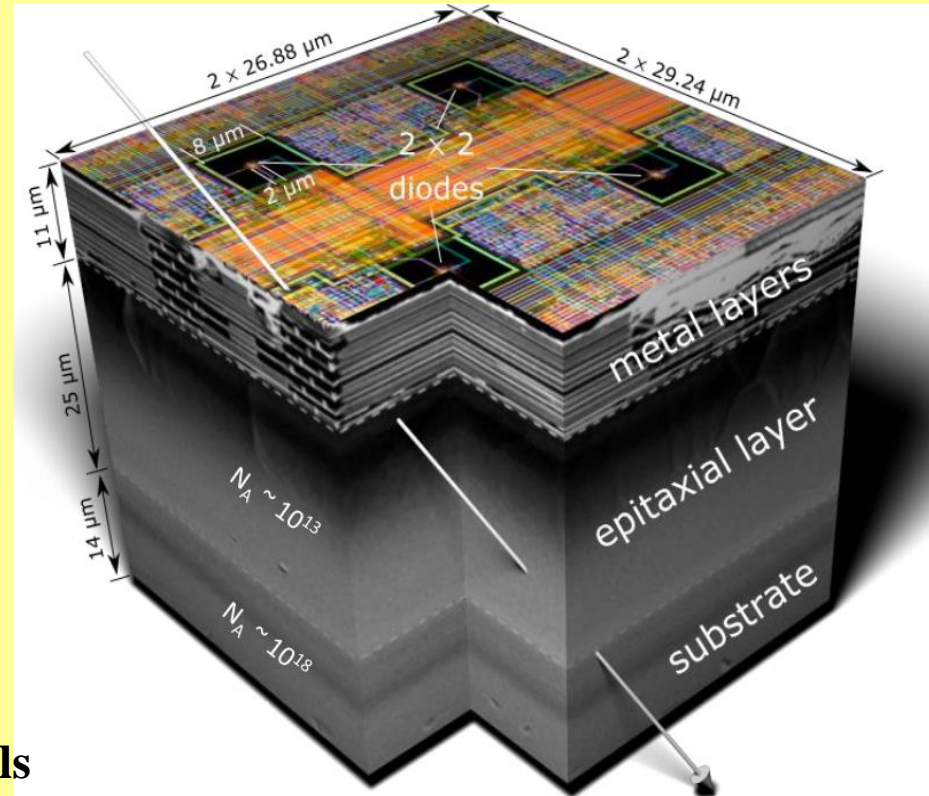


Small pixel and thin detectors: for new ALICE ITS size of one pixel is $28 \times 28 \mu\text{m}^2$ and total radiation length of 0.3% X0 per layer

Cost: cheaper than other.

Example: new ALICE ITS

1. Option 1: 7 layers of MAPS – 14 000 kCHF
2. Option 2: 3 innermost layers of hybrid pixels and 4 outermost layers of strips - 20 000 kCHF [8]



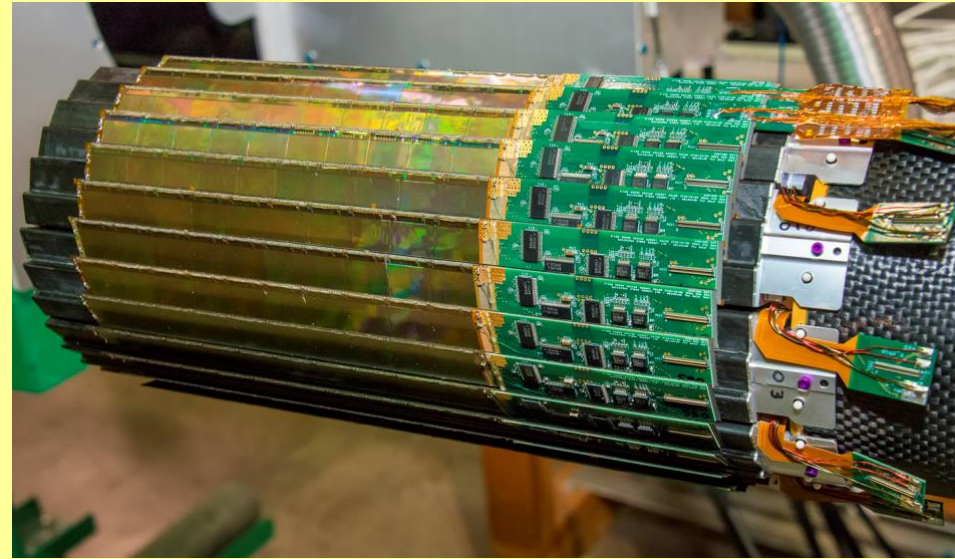
Pixel detectors: Future. Monolithic Active Pixel Sensors (MAPS)



First using: **STAR Heavy Flavour Tracker.**

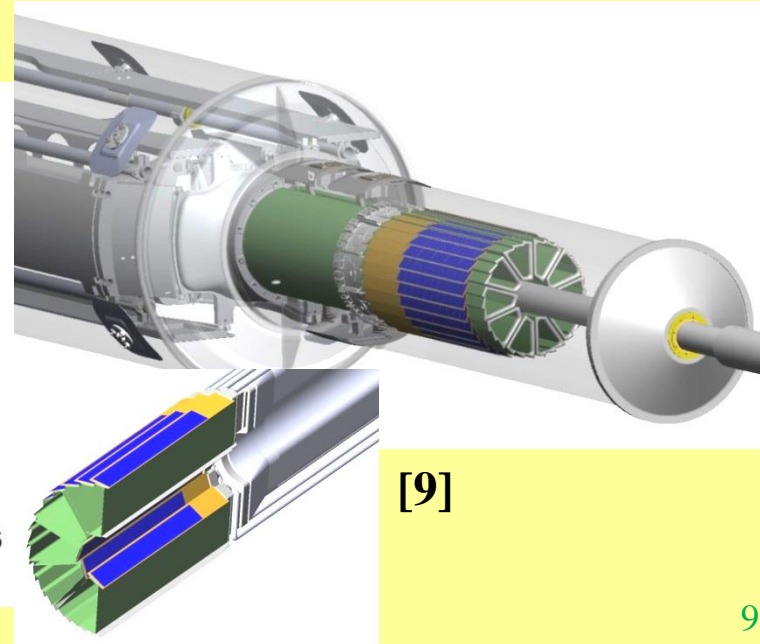
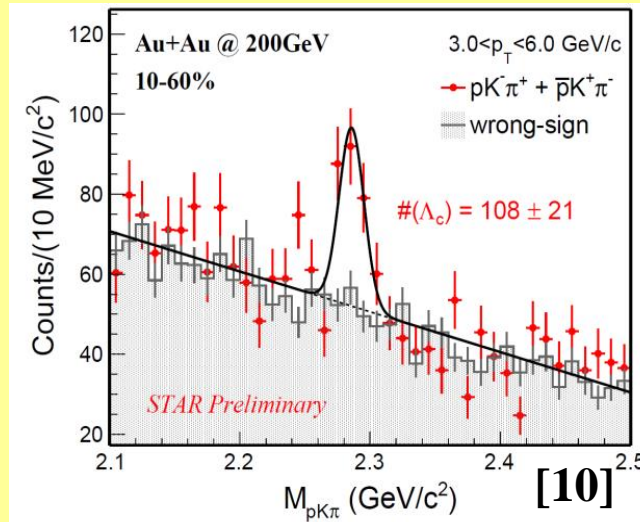
First MAPS based vertex tracker at a collider experiment.

1. Two layers of detectors
2. Pixel size - 20.7 x 20.7 μm
3. Radiation length - $\sim 0.5\%$ X0 **350 nm CMOS technology**
4. Number of pixels - 360M
5. Integration time 185.6 μs
6. Radiation dose: 20 to 90 kRad / year



First measurements of Λ_c production in central Au+Au collisions at $\sqrt{s_{NN}} = 200$ GeV. The invariant yield of Λ_c for $3 < p_T < 6 \text{ GeV}/c$ was measured in 10-60%.

Invariant mass spectra of $K\pi$ pairs. The data points are the Λ_c signals. The grey histogram depicts the background distribution (scaled by 1/3)



[9]



Limitation:

1. Read-out capabilities limited at 1kHz for Pb-Pb collisions;
2. Pointing resolution of the present ITS restricts the range of measurements.
It is adequate for the study of charm and beauty mesons at $p_T > 1 \text{ GeV}/c$, but at lower p_T the statistical significance becomes insufficient for currently achievable data sets;
3. Detection of charmed baryons is currently not feasible in Pb-Pb collisions.
The mean proper decay length $\sim 60 \mu\text{m}$, which is lower than the pointing resolution of the current ITS in the p_T range of most of the $\Lambda_c^+ \rightarrow p K^- \pi^+$ daughter particles ($< 1 \text{ GeV}/c$);
4. For the same reasons study of beauty mesons, beauty baryons, and of hadrons with more than one heavy quark is beyond reach of the current detector

Motivations for upgrade:

1. Increase vertex resolution
2. Improve tracking efficiency and p_T resolution at low p_T :
allow improvement of the resolution of the track impact parameter by a factor of three or better (at $p_T = 1 \text{ GeV}/c$) with respect to the present ITS
3. Increase readout rate capabilities:
readout Pb-Pb interactions at $> 100 \text{ kHz}$, readout p-p interactions at $> 400 \text{ kHz}$, (currently limited at 1kHz with full ITS)

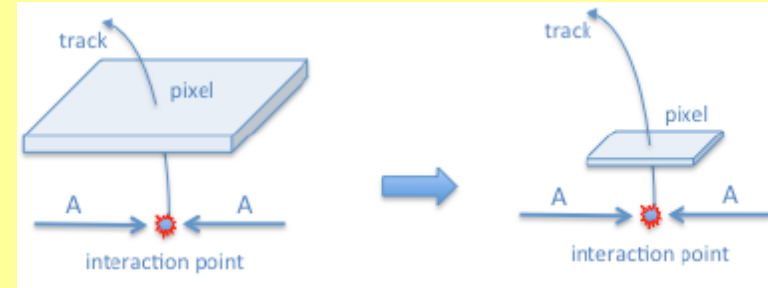
ALICE Inner Tracking System: current status and upgrade strategy



Upgrade strategy (main points):

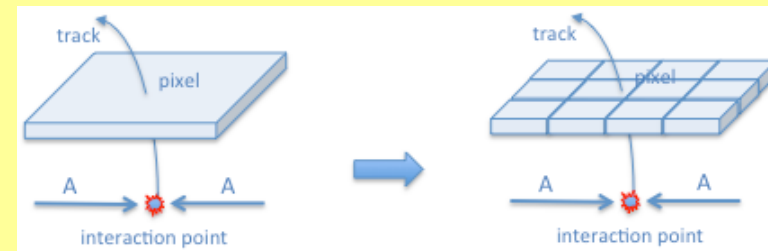
1. Improve impact parameter resolution by a factor of ~ 3

- First detection layer closer to the beam line: radius from **39mm** to **23 mm**
- Reduction of material budget: the radiation length per layer (for inner layer) **X** from **1.14** to **0.3 %X₀**
- Reducing pixel size: from **425x50** to **28x28 μm^2**



2. Improve tracking efficiency and p_T resolution at low p_T

- Increase in granularity (smaller pixels)
- number of layers (from 6 to 7)
- instead **silicon drift** and **strips** the **pixels** will be used



Also:

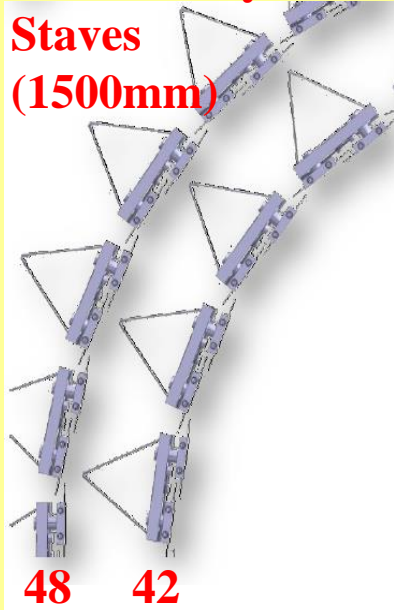
- lower power consumption and a highly optimized scheme for the distribution of the electrical power and signals
- mechanics, cooling and other detector elements will be also improved

ALICE Inner Tracking System: current status and upgrade strategy

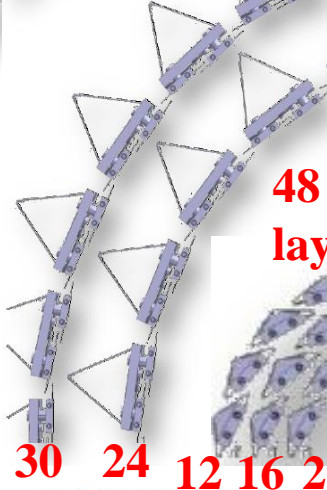


90 Outer layer

Staves (1500mm)



54 Middle layer Staves (900mm)



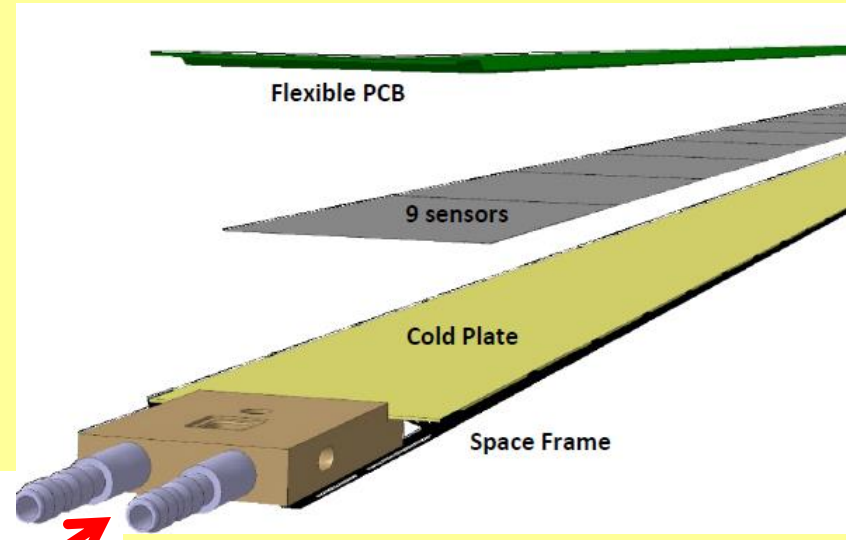
48 Inner layer Staves



290mm

48 42 30 24 12 16 20

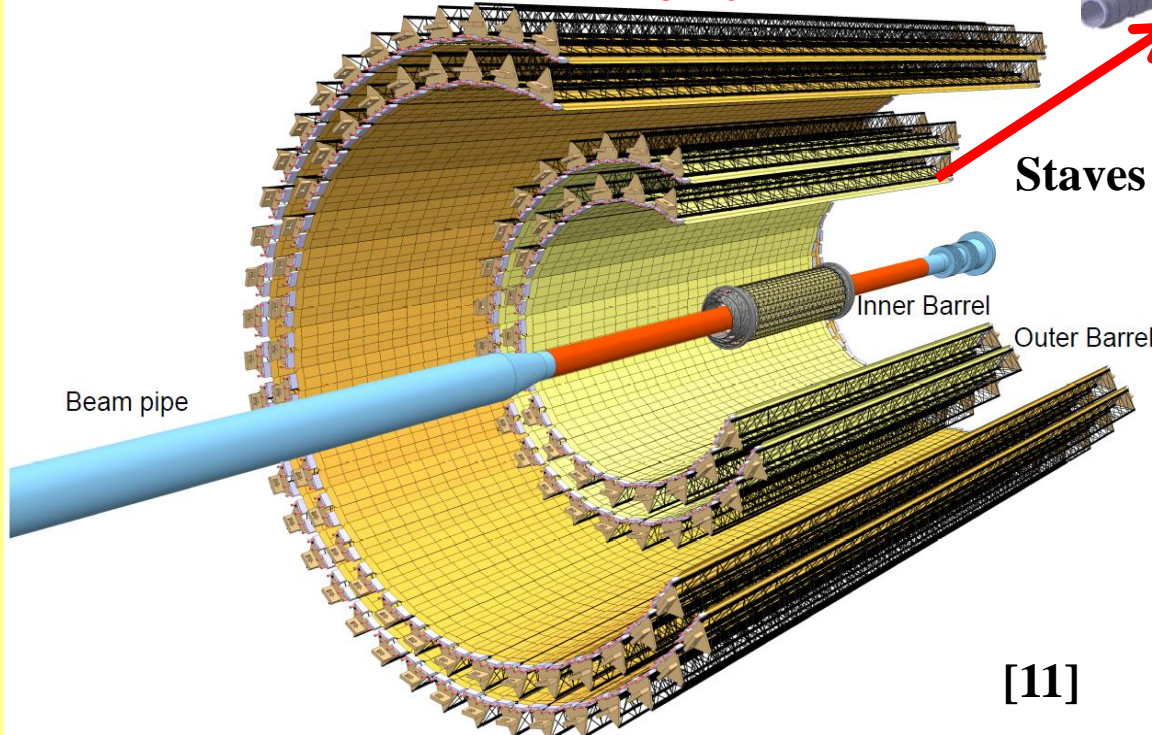
Inner Barrel Stave



Stave :

- 1. Hybrid Integrated Circuit (HIC)**
- 2. Cold plate**
- 3. Space frame**

**Barrel: 7 layers of MAPS
12.5 G pixels
~10m² total active area**



[11]



For the ALICE ITS upgrade TowerJazz technology is being explored by four different chip architectures

Architecture (discriminator, read-out)	Pitch ($r\phi \times z$) (μm^2)	Integration time (μs)	Power consumption (mW cm^{-2})
MISTRAL (IPHC) (end-of-column, rolling-shutter)	22×33.3	30	200
ASTRAL (IPHC) (in-pixel, rolling-shutter)	24×31 IB 36×31 OB	20	85 60
CHERWELL STFC-RAL in UK (in-strixel ^a , rolling-shutter)	20×20	30	90
ALPIDE (in-pixel, in-matrix sparsification)	28×28	4	< 50

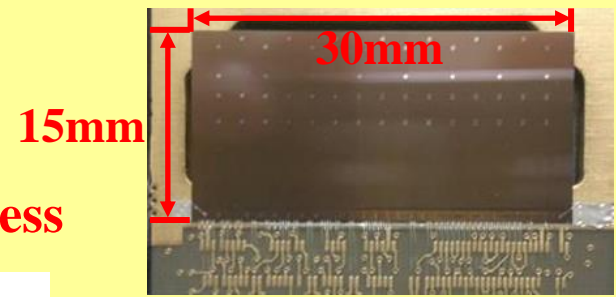
ALice PIxel DEtector

[11]

Main parameters of all chip architectures conform to the requirements of ALICE ITS upgrade.

ALICE Pixel Detectors (ALPIDE family)

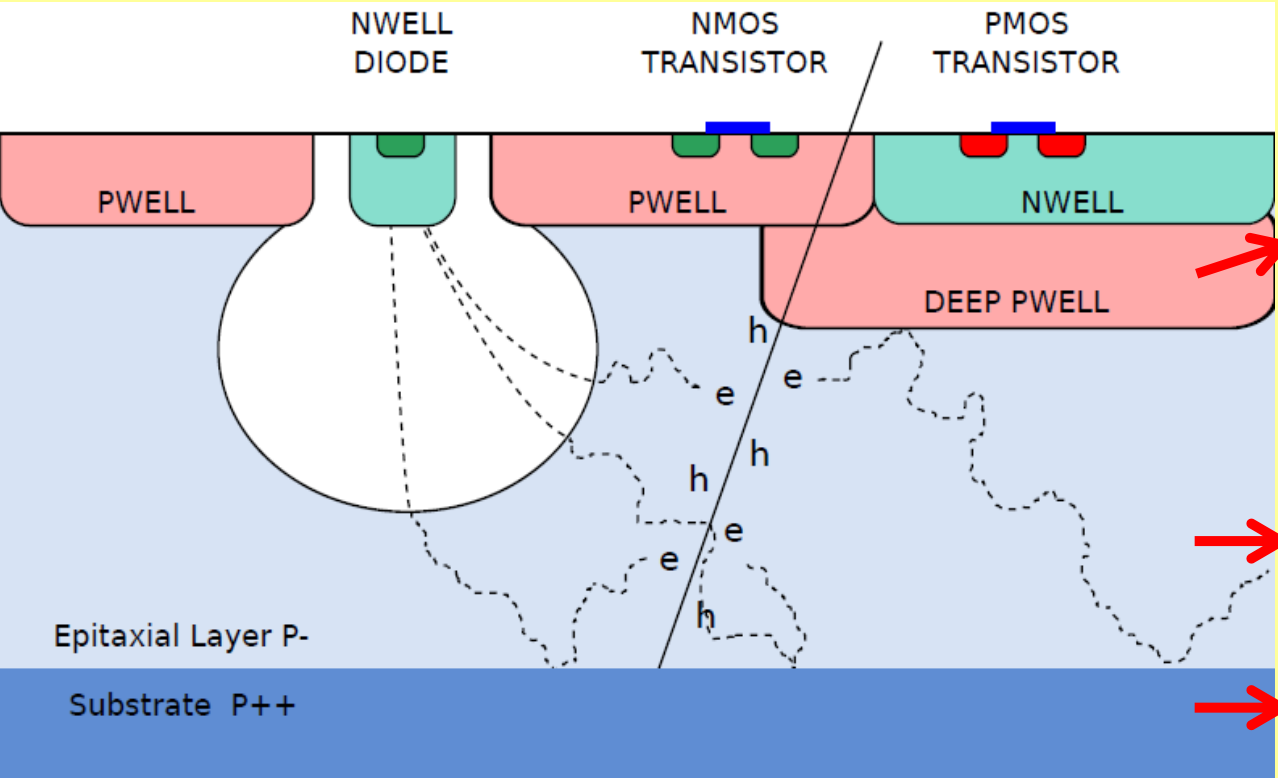
MAPS using TowerJazz 180nm CMOS Imaging Process



Shields the other **nwells** different from the collection electrode, preventing them from collecting signal charge which then would be lost for readout. Full CMOS within the pixel

High resistivity ($> 1\text{k}\Omega \cdot \text{cm}$) p-type epitaxial layer ($25\mu\text{m}$)

low-resistivity p-type substrate



Small n-well diode ($2\text{-}3\ \mu\text{m}$ diameter), ~ 100 times smaller than pixel \rightarrow low capacitance

The gate oxide thickness of $3\ \text{nm}$ \rightarrow robustness to Total Ionizing Dose

Possibility to apply back bias to the substrate can be used to increase depletion zone around NWELL collection diode: S/N ratio increases, higher efficiency

ALICE Pixel Detectors (ALPIDE family)

Pixel detector general requirements

(from Technical Design Report for the Upgrade of the ALICE ITS)

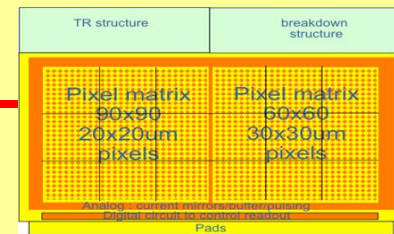


Parameter	Inner Barrel (IB)	Outer Barrel (OB)	ALPIDE Performance
Silicon thickness	50 μm	100 μm	
Chip dimension	15 mm x 30 mm	15 mm x 30 mm	
Spatial resolution	5 μm	10 μm	5 μm (IB), 5 μm (OB)
Power density	< 300 mW/cm ²	< 100 mW/cm ²	40 mW/cm ² (IB), 30 mW/cm ² (OB)
Max. integration time	30 μs	30 μs	10 μs
Detection efficiency	>99%	>99%	>99% Upper limit!
Fake-hit rate	<10 ⁻⁵ (TDR), <10 ⁻⁶ * /event/pixel for IB and OB		<<<10 ⁻⁶ /event/pixel
Total Ionizing Dose	270 krad 2.7 Mrad*	10 krad, 100 krad*	Up to 500 krad
Non-Ionizing Energy Loss (1 MeV n _{eq} /cm ²)	1.7 x 10 ¹² (TDR), 1.7 x 10 ¹³ *	1.7 x 10 ¹¹ (TDR), 1.7 x 10 ¹² *	Up to 1.7 x 10 ¹³

radiation load integrated over the approved program (~ 6 years of operation)

*revised numbers with respect to ALICE TDR (factor 10)

ALICE Pixel Detectors (ALPIDE family)



Two submatrices: 90x90 array of 20 x 20µm pixels and 60x60 array of 30x30µm pixels. Each sub matrices is divided in 9 sectors with one variant of collection electrode(analogue readout). Investigations: pixel geometry, starting material, sensitivity to radiation.

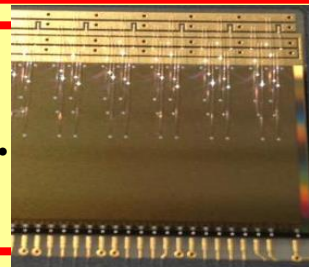
2012
Explorer
Explorer-1,2

2013
 pALPIDEss

Matrix with 64 columns x 512 rows of 22µm x 22µm pixels. (in-pixel discrimination and buffering). Study priority encoder and the front-end electronics

May-2014
 pALPIDE-1

Full-scale prototype to study system effects: 1024 columns x 512 rows of 28µm x 28µm pixels. Four sectors with different pixels.



May-2015
 pALPIDE-2

Four sectors with different pixels. Optimization of several circuit blocks. Allows integration into ITS modules

Oct-2015
 pALPIDE-3

Eight sectors with different pixels. Final interfaces, more features including 1.2 Gbit/s output serial link.

Jul - 2016
ALPIDE – Final Version



ALICE Pixel Detectors (ALPIDE family)



The chip measures **15 mm (Y) by 30 mm (X)**

Power consumption **40 mW/cm²**

Contains a matrix of **512 × 1024 sensitive pixels**

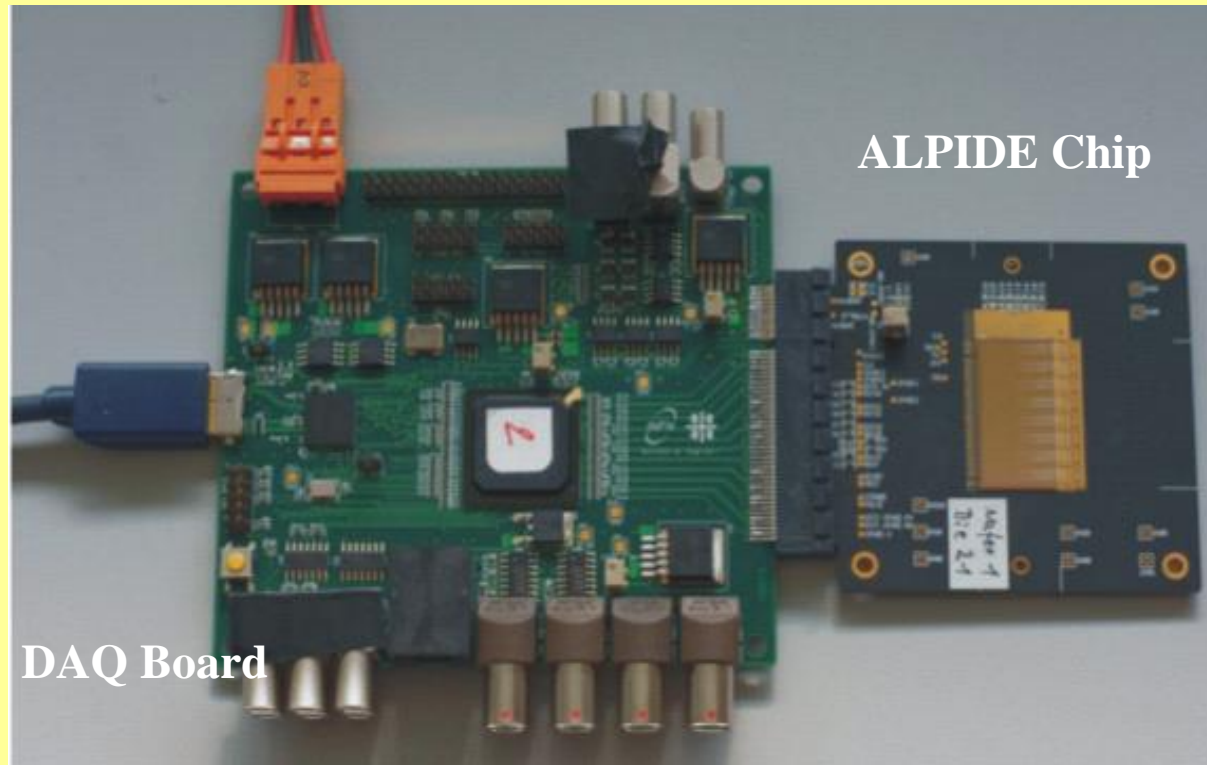
Full-scale Pixel Detector prototypes **pALPIDE-1,2**: pixel width is 28 μm and the pixel height is 28 μm. Four sub-matrices (sectors) of 512×256 pixels

Full-scale Pixel Detector prototype **pALPIDE-3**: pixel width is 29,24 μm and the pixel height is 26,88 μm. Eight sub-matrices (sectors) of 512×128 pixels

Sub-matrices (sectors) differing in charge collection diode geometry and in-pixel circuitry

pALPIDE-4 – ALPIDE
(final version) one sector

All the analogue signals → required by the front-ends are generated by a set of 11 (for pALPIDE-1,2) and 14 (pALPIDE-3) on-chip digital-to-analog converters (DACs).

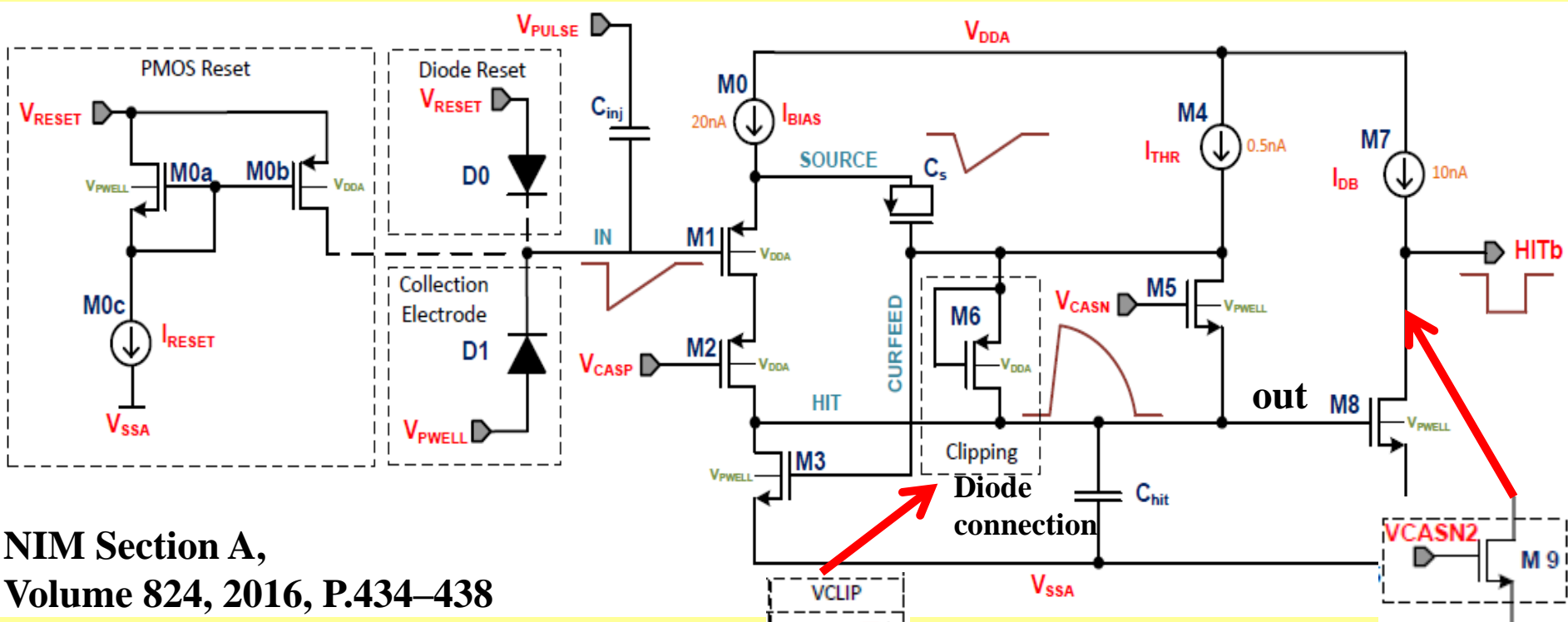


Full-scale Pixel Detector prototypes (pALPIDE -1,2,3)



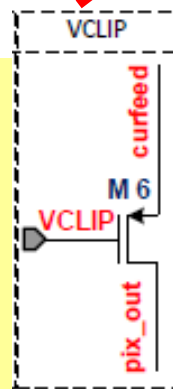
A comprehensive scheme for the pixel front-end circuit
Including all possible variations

For pALPIDE-1,2

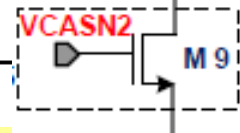


NIM Section A,
Volume 824, 2016, P.434–438

For pALPIDE-3
for sectors: 3,4,5,7
add VCLIP



For pALPIDE-3
for sectors: 0,3,4,5,7
add VCASN-2 (M9)



Full-scale Pixel Detector prototypes (pALPIDE -1,2,3)

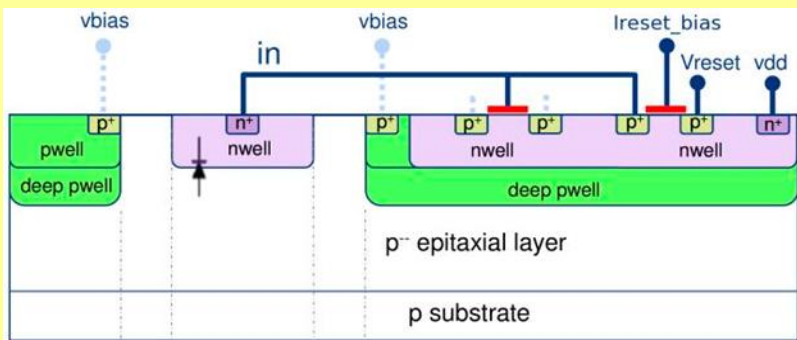


Each sector implements a different front-end electronics

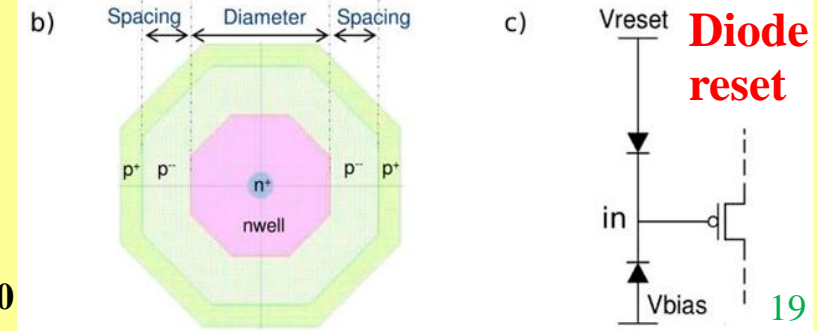
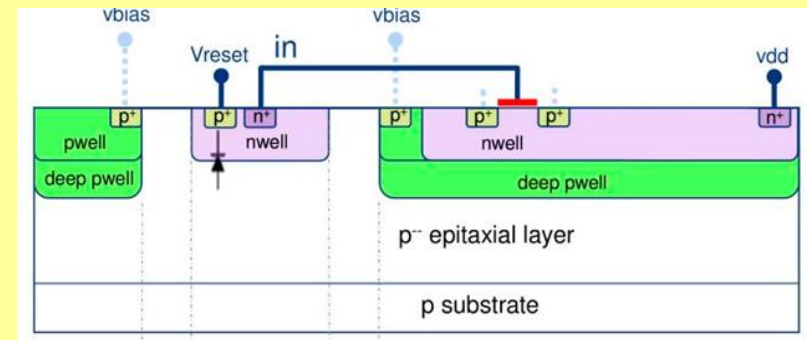
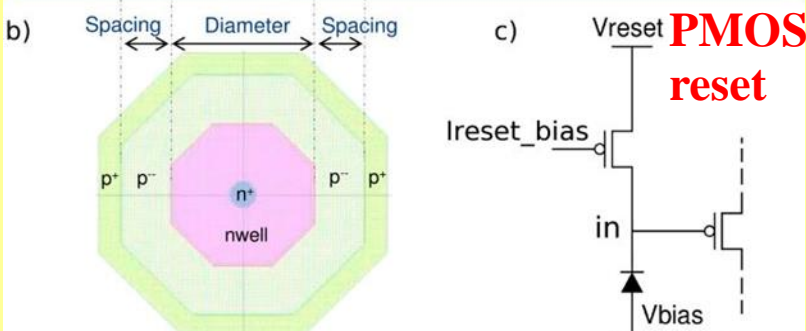
pALPIDE-1

pALPIDE-2

Sector	N-well diameter	Spacing	Reset type	Sector	N-well diameter	Spacing	Reset type
0	2 μm	1 μm	PMOS	0	2 μm	2 μm	PMOS
1	2 μm	2 μm	PMOS	1	2 μm	2 μm	PMOS
2	2 μm	2 μm	Diode	2	2 μm	4 μm	PMOS
3	2 μm	4 μm	PMOS	3	2 μm	4 μm	Diode



Collection electrode



JINST
doi:10.1088/1748-0221/10/03/C03030

Full-scale Pixel Detector prototypes (pALPIDE-1,2,3)

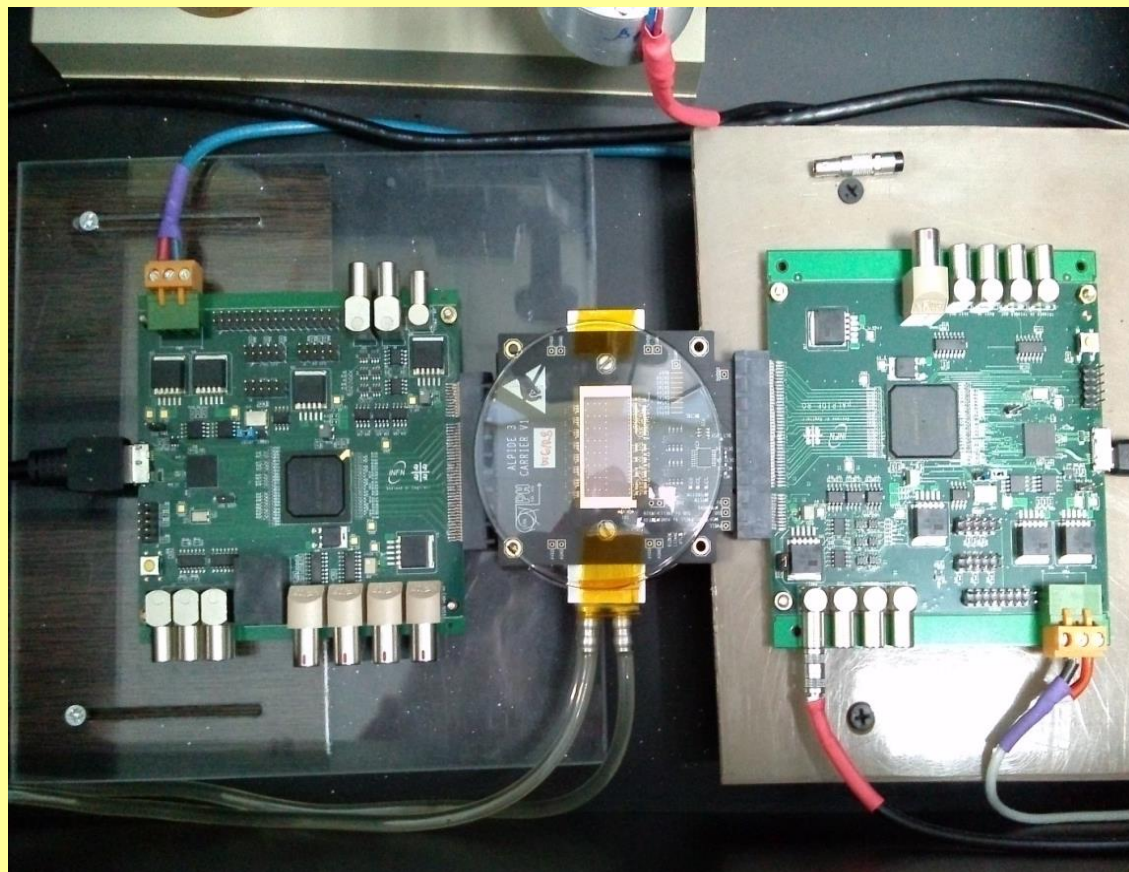


The front-end circuits in pALPIDE-3 are based on the pALPIDE-1, 2 circuit with step by step modifications in order to trace the effects on performance

Sector	M3, M5, M6, M8 (transistors)	Spacing	Reset type	Additional VCASN2 (M9)
0	optimized size	2 μm	Diode	Yes
1	optimized size	2 μm	Diode	No
2	as in pALPIDE-1/2	2 μm	Diode	No
3	optimized size	2 μm	Diode	Yes
4	optimized size	2 μm	Diode	Yes
5	optimized size	3 μm	Diode	Yes
6	as in pALPIDE-1/2	2 μm	PMOS	No
7	optimized size	2 μm	PMOS	Yes

For the characterization and tests of the ALPIDE prototypes, three experimental set-ups based on the test boards and software, which were **jointly developed within the ITS upgrade project**, have been constructed at **SPbSU**.

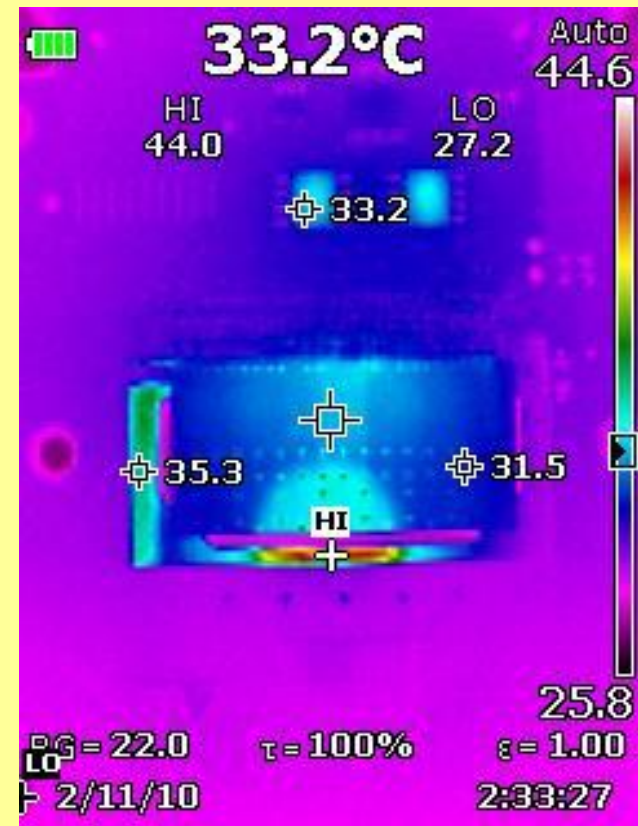
First Experimental Set-up



- 1.** Two different chip types (telescope geometry) with own DAQ boards have been installed.
- 2.** Dark box with electrical earthing inside needed for detector protection against light and electromagnetic interference. Temperature control inside the box is available.
- 3.** The water cooling (heating) system has been implemented.
- 4.** Radioactive source ($\gamma\beta$) positioning system. One can move source in XYZ-directions. It includes also system for visualization of central area on detector surface.
- 5.** Detector Power supply(current control).

Second Experimental Set-up

The same as previous one but with additional system including thermo-camera for detector heating investigations .



Study of the characteristics of full-scale Pixel Detector prototypes



1. Cryo-box.
2. Irradiated ALPIDE chip + DAQ board.
3. Chip was mounted on cooled platform.
4. Three thermocouples (1 copper-constantan, 2 chromel-alumel) mounted on cooled platform. Each thermocouple has own controller and DAQ

Third Experimental Set-up with cryogenic module



5. Dewar vessel with heater system.
6. Source holder.
7. Analytical balance

Also some improvements for Vbb power supply have been done.



Study of the characteristics of full-scale Pixel Detector prototypes

Second Experimental Set-up with cryogenic module



Two different mode of the cooling process:

- 1. Cooling by the chiller (alcohol-containing mixture) – only up to $-20\text{ }^{\circ}\text{C}$.
To prevent a chip from the frost the nitrogen was supplied into a cryo-box.**
- 2. Cooling by cold nitrogen which evaporates from its liquid phase.
The liquid nitrogen was heated by nichrome heater putted into the Dewar vessel.
Then cold gas flowed through platform (inside platform).
We can regulate the nitrogen flow, powered nichrome heater (different currents up to 6 A).
Also we can control the volume of the liquid nitrogen weighing Dewar vessel.
Temperature control:
 - a) 3 thermocouples**
 - b) on-chip temperature sensor. This sensor works only up to $-80\text{ }^{\circ}\text{C}$.****

The temperature $-115\text{ }^{\circ}\text{C}$ has been reached

Characterization and tests

1. Electrical tests:

- a) **On-chip Digital-Analogue Converter Test.** The output of the on-chip DACs is connected to monitoring pins of the detector and measured by ADCs on the DAQ board.
- b) **Digital Scan.** Scan generates a digital pulse in a number of pixels and reads the hits out. The number of injections per pixel and the group of pixels can be set.
- c) **Analogue Scan.** A programmable charge is injected into the preamplifier. The values of the injected charge, as well as the number of injections per pixel and the groups of pixels can be set.
- d) **Threshold Scan.** Scan performs analogue injections, looping over the charge ranging from 7 to 350 electrons. The values of V_{CASN} and I_{THR} can be set.

2. Noise characteristics of the sensor and its temperature dependence were studied

The scan gives a selectable number of random triggers and returns the number of hits. The values of V_{CASN} and I_{TH} and also chip temperature can be set.

3. Studies with a variety of gamma and beta sources were carried out

The scan gives the number of hits using the selectable number of random triggers. Radioactive source measurements are needed to study the uniformity of hit-maps and to evaluate cluster shape and size. The noise mask is prepared before the scan and can be used then in measurements.

All results see in Back up slides

Investigations of the detector's characteristics for different temperatures

Detectors pALPIDE-4 – ALPIDE (final version)

Detectors were irradiated by:
X-rays



Chip W8R22 – 60 krad (low dose)

Chip W7R12 – 300 krad (high dose)

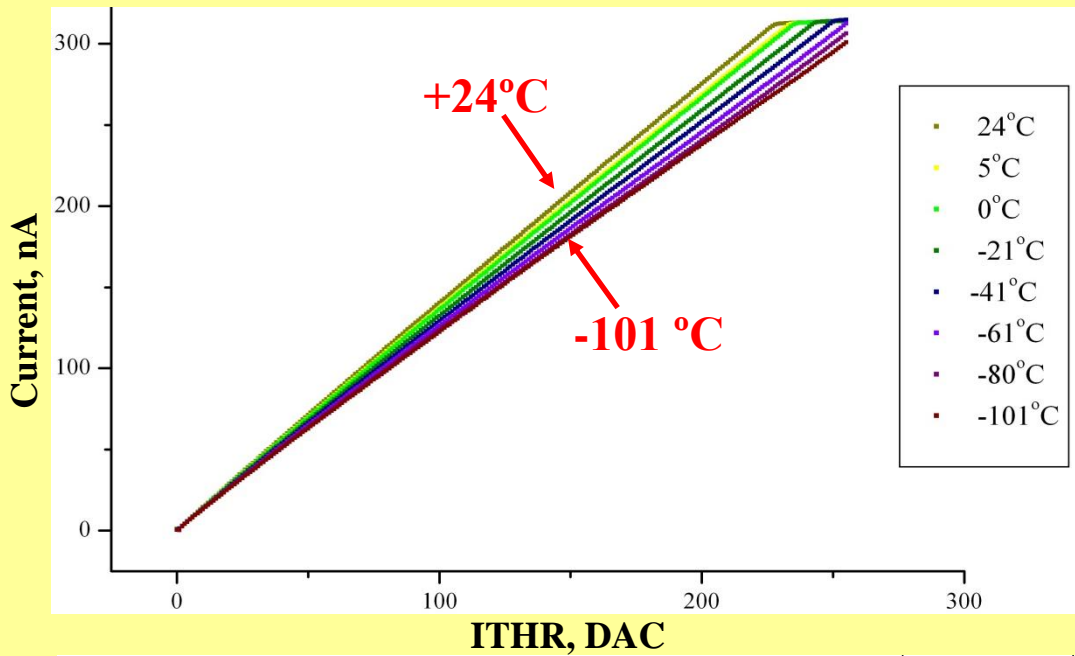


Before irradiation Chip W7R12 was measured at lab.

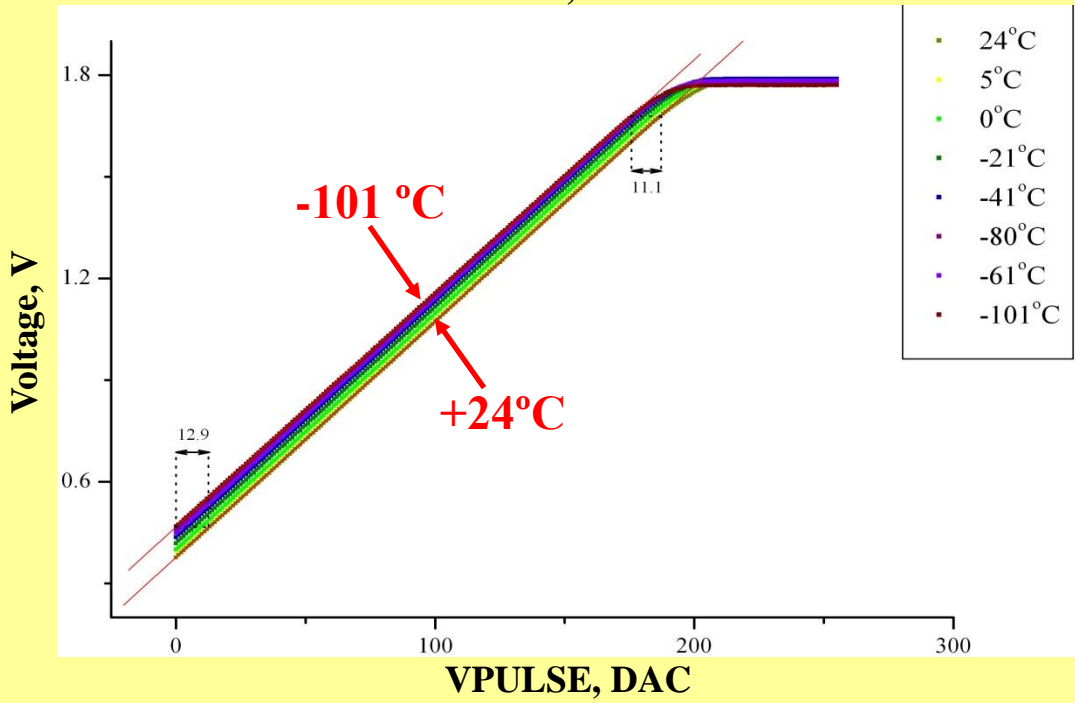
~ 5 month after irradiation

All measurements were done at **V_{bb} = -3V**

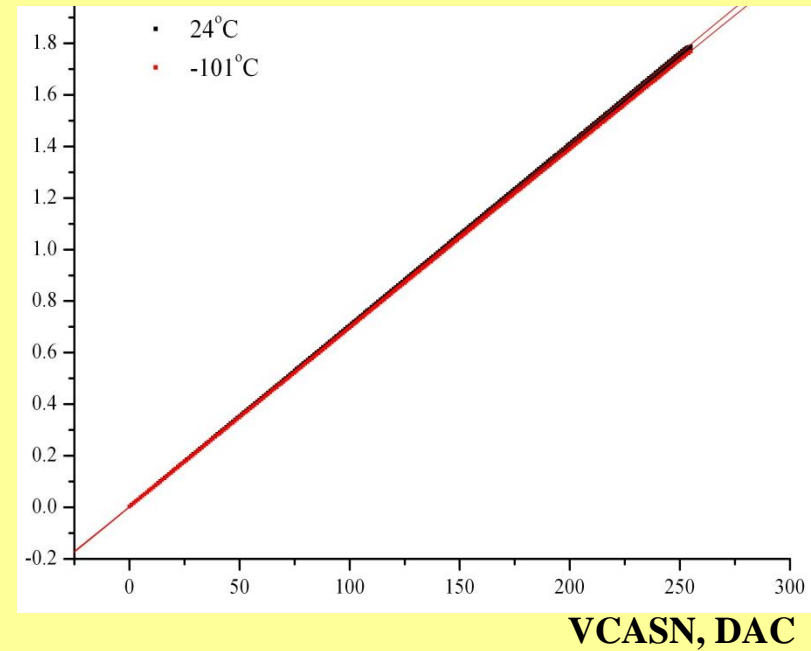
The ALPIDE characteristics studies



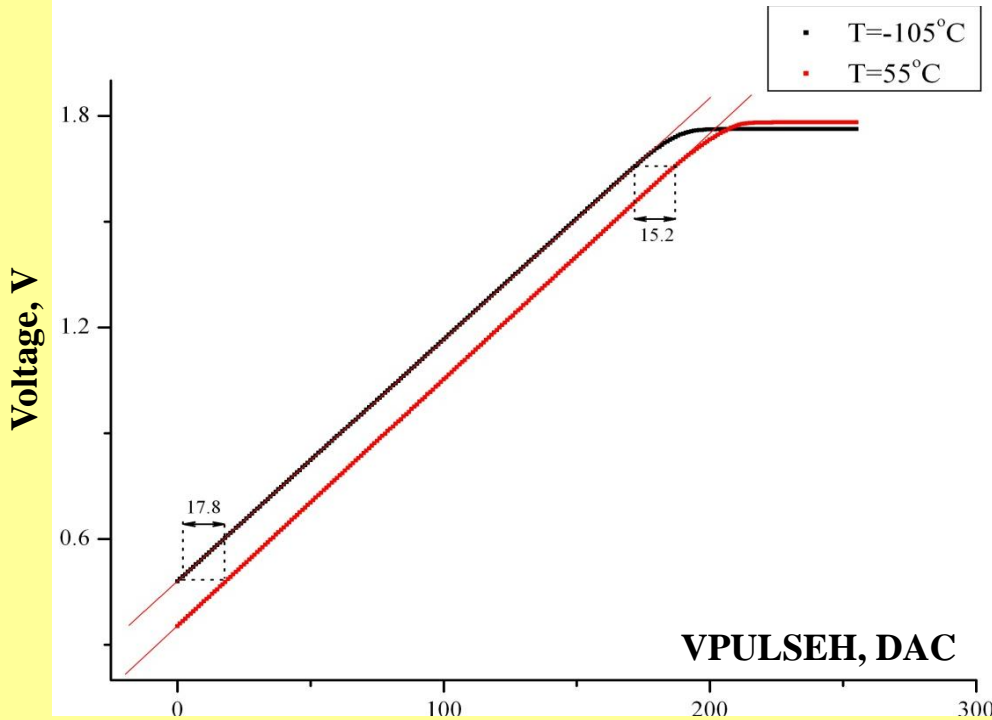
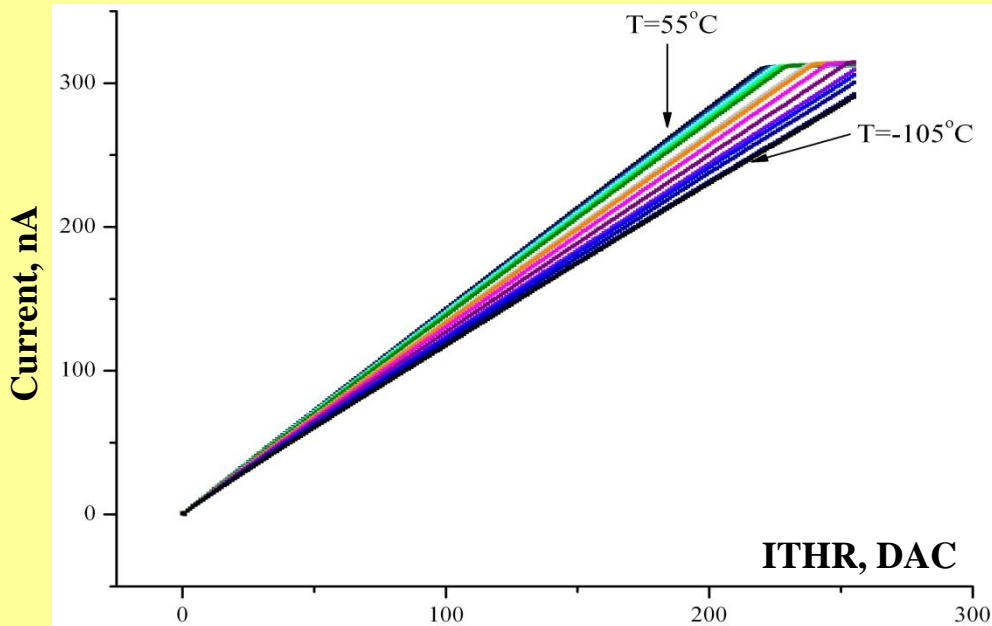
DAC Scan Chip W8R22



Voltage, V

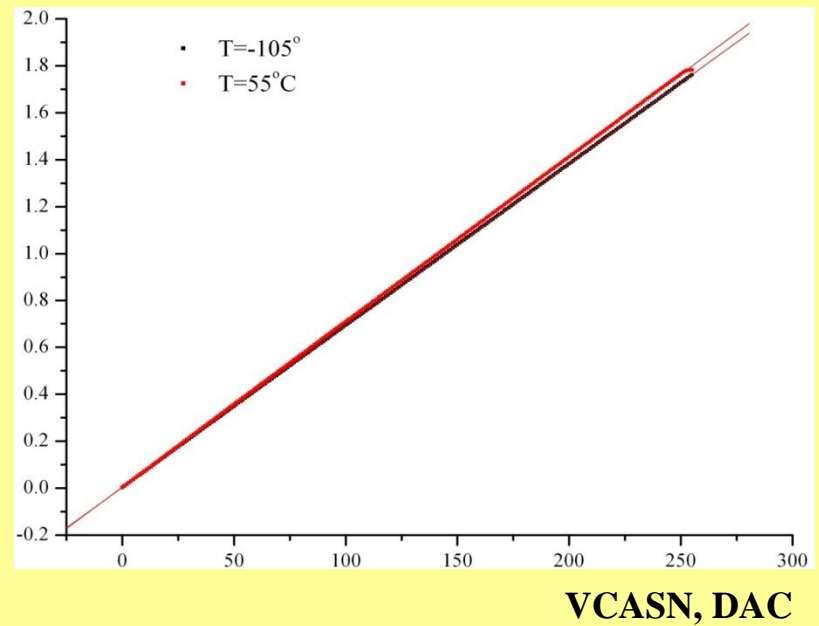


The ALPIDE characteristics studies

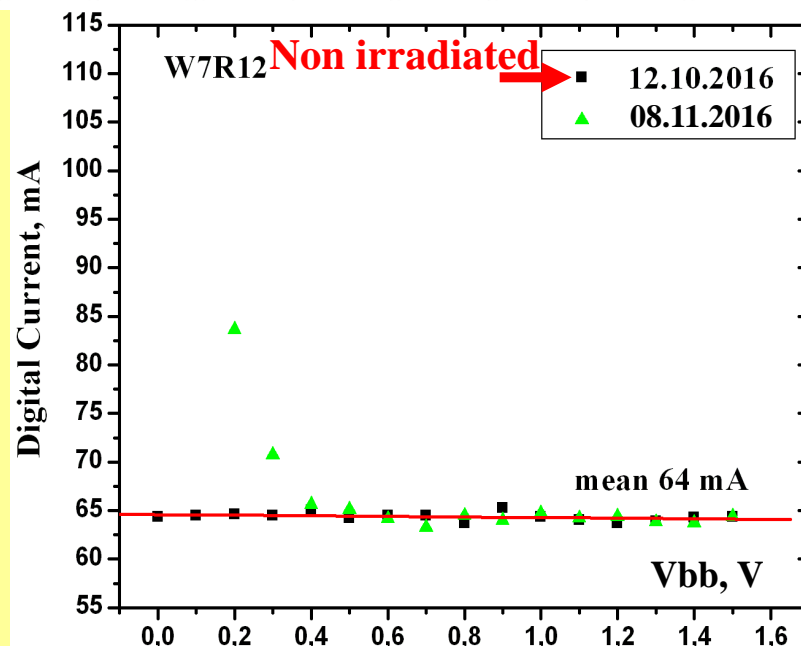
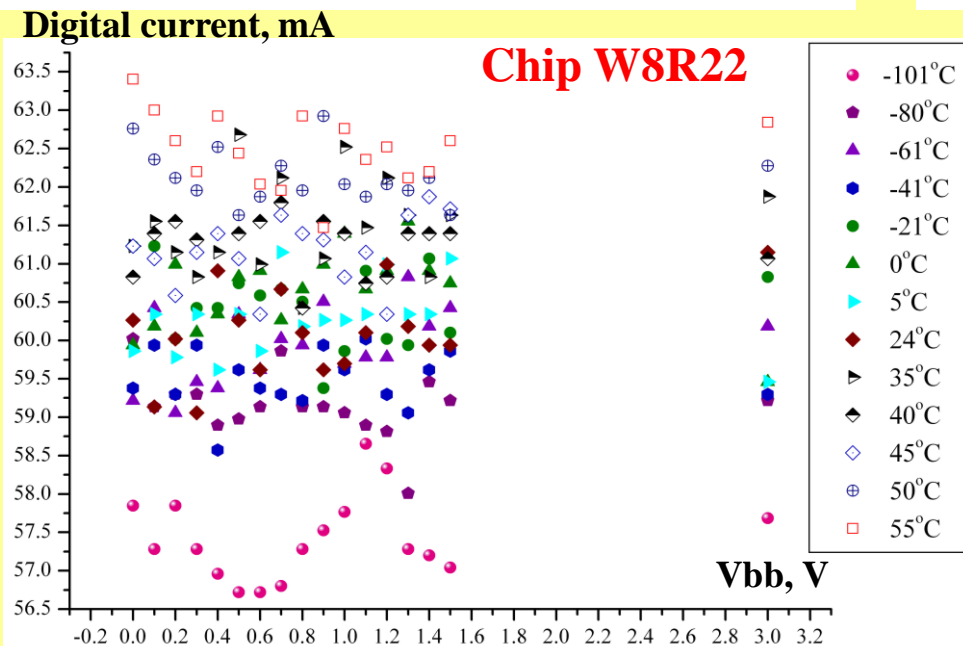
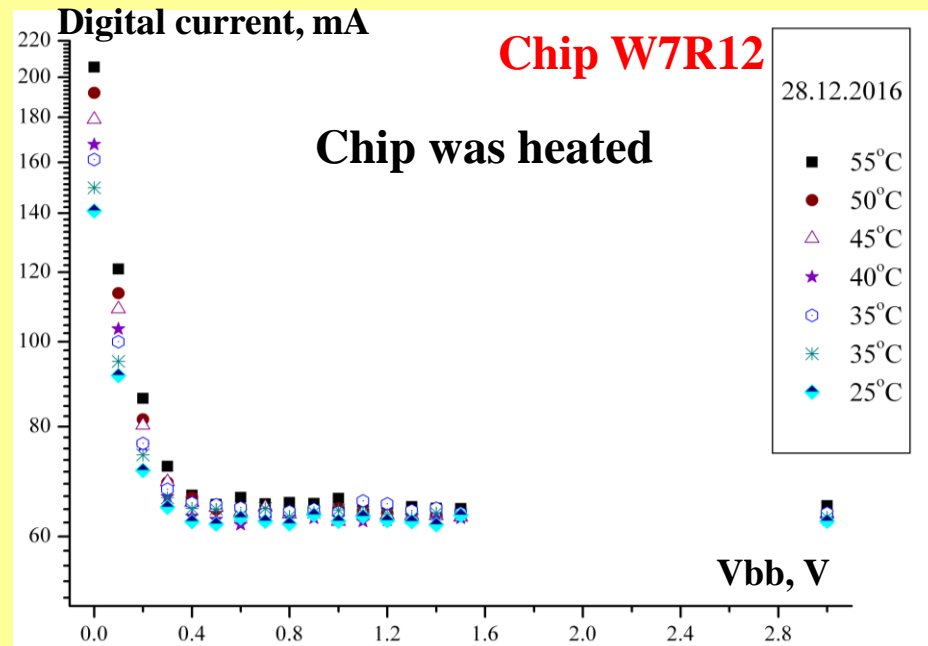
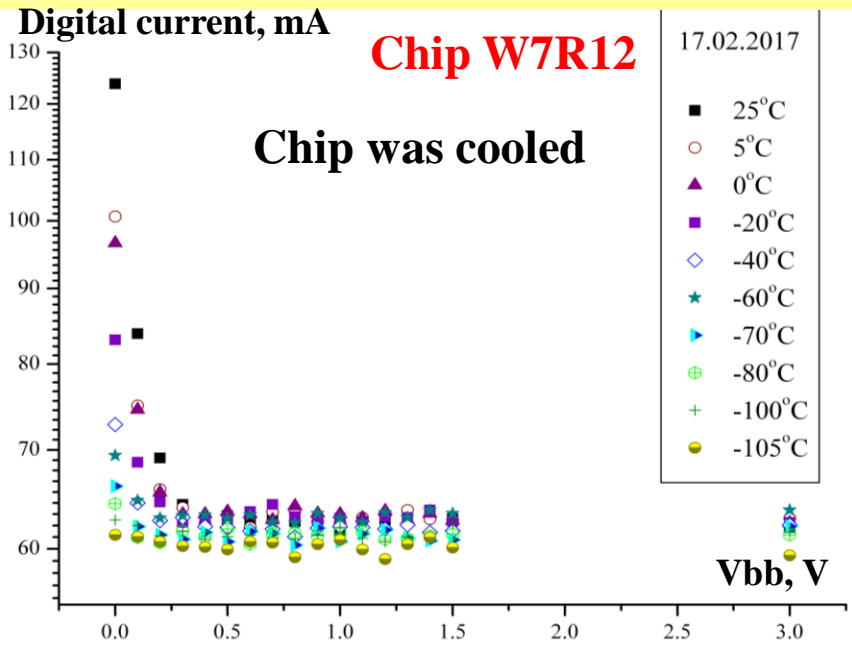


DAC Scan Chip W7R12

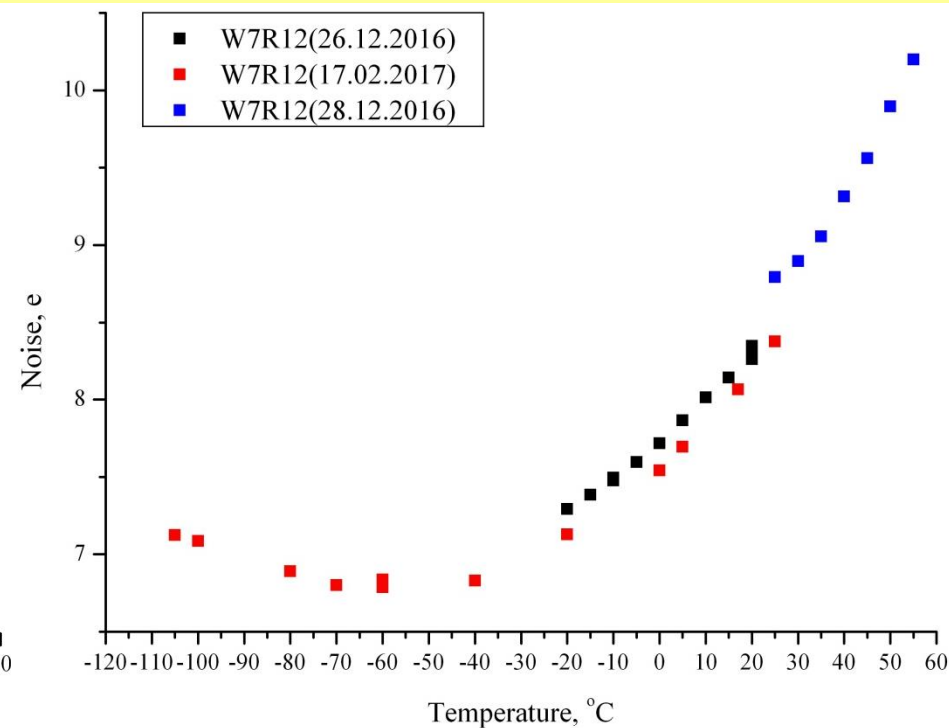
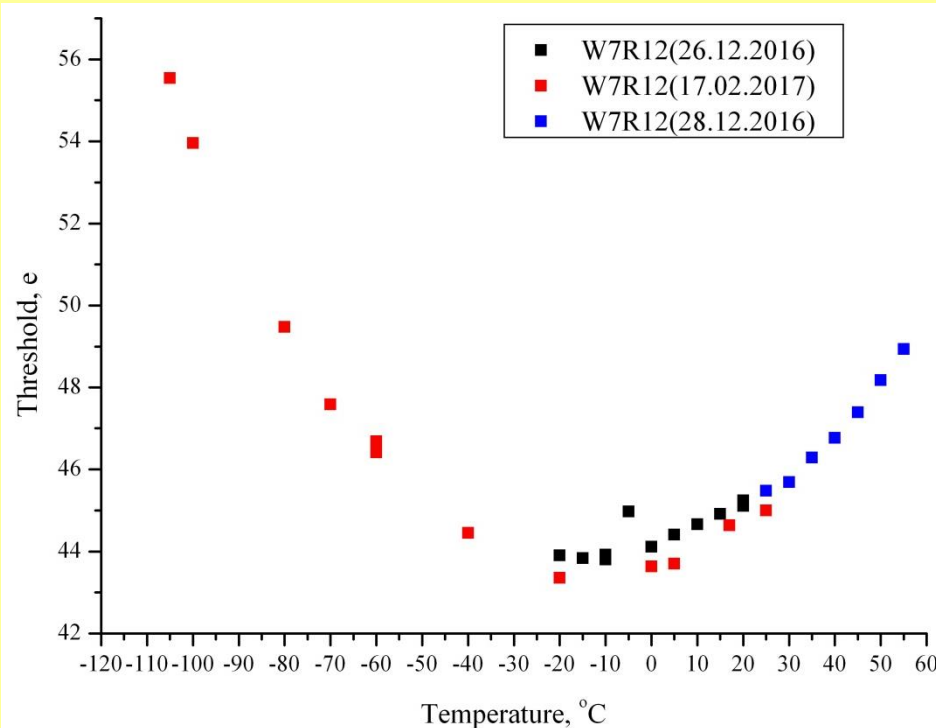
Voltage, V



**This chip was also heated to 55°C
(for annealing investigations)**



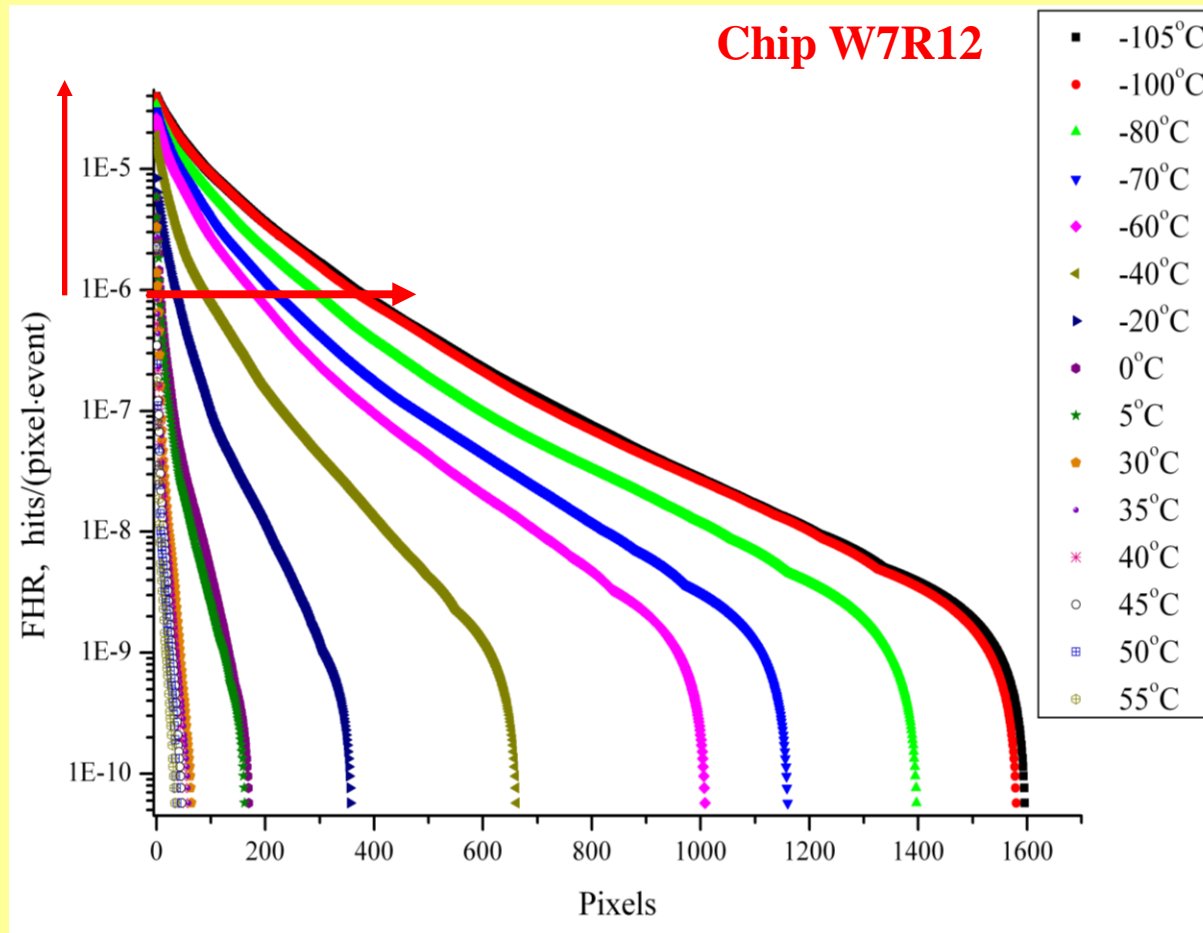
Chip W7R12



Before irradiation the threshold was ~ 85 e,
after irradiation (300 krad)
the threshold was ~ 45-50 e

Before irradiation the noise was ~ 6 e,
after irradiation (300 krad)
the noise was ~ 14 e

The threshold goes up both with increasing temperature and with lowering temperature, but initial value (before irradiation) of the threshold is not reached.



1. The number of pixels to be masked to achieve certain fake-hit rate increases with the lowering of temperature.
2. FHR also increases with temperature decreasing
3. The same results for low dose irradiated chip

The ALPIDE characteristics studies



Results for high dose irradiated chip

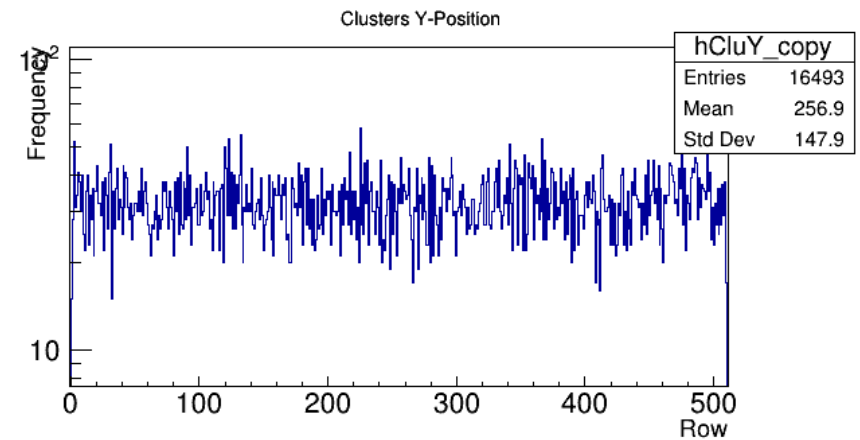
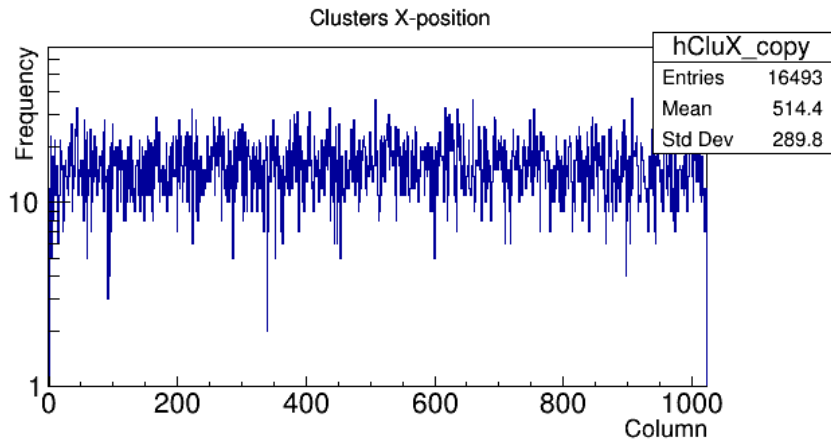
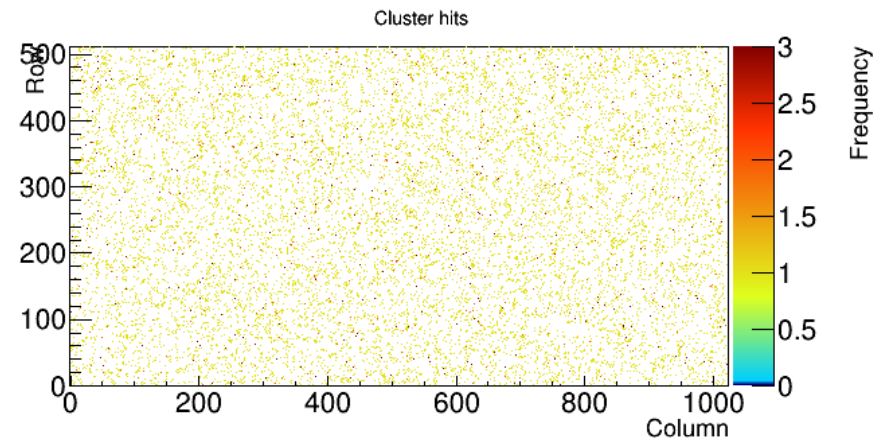
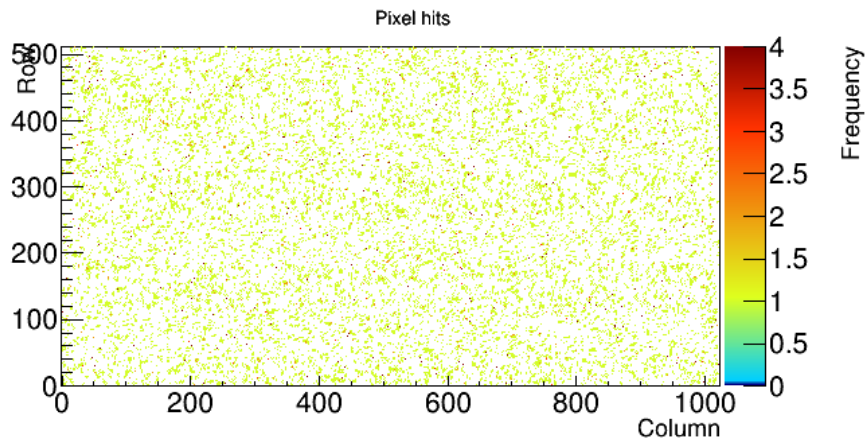
Source test + Cluster analysis

Triggers: 2000000

Vbb = -3V

Chip W7R12

Masked



Source: ^{133}Ba , chip temperature -115°C

The ALPIDE characteristics studies



Results for high dose irradiated chip

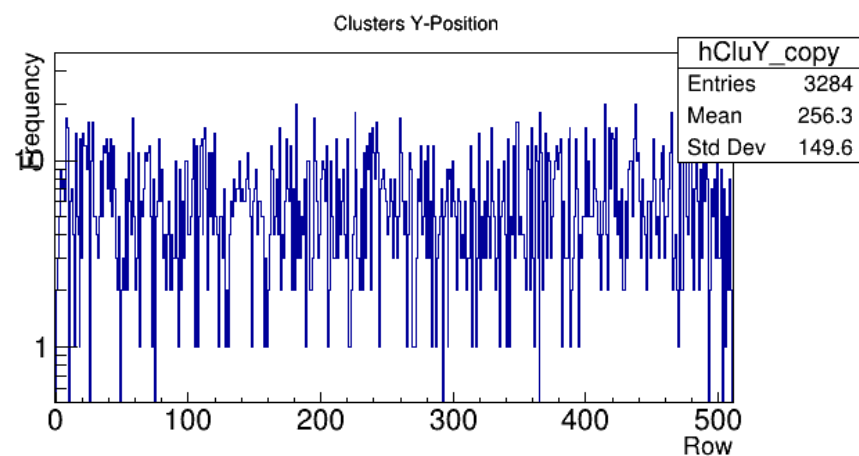
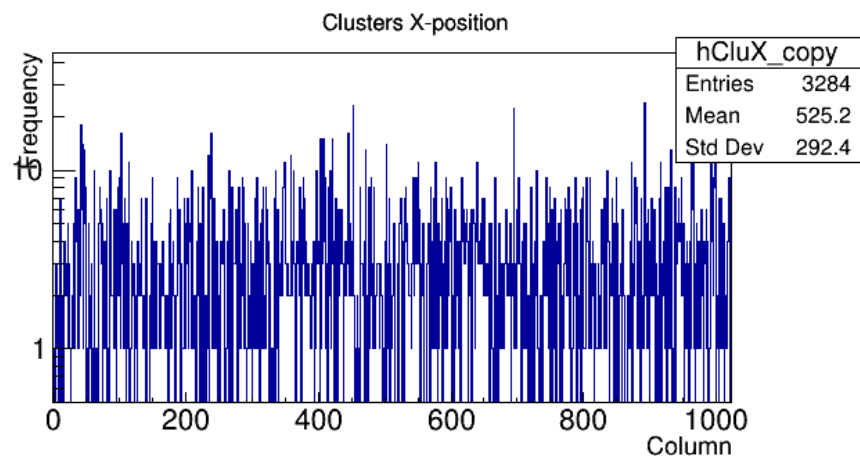
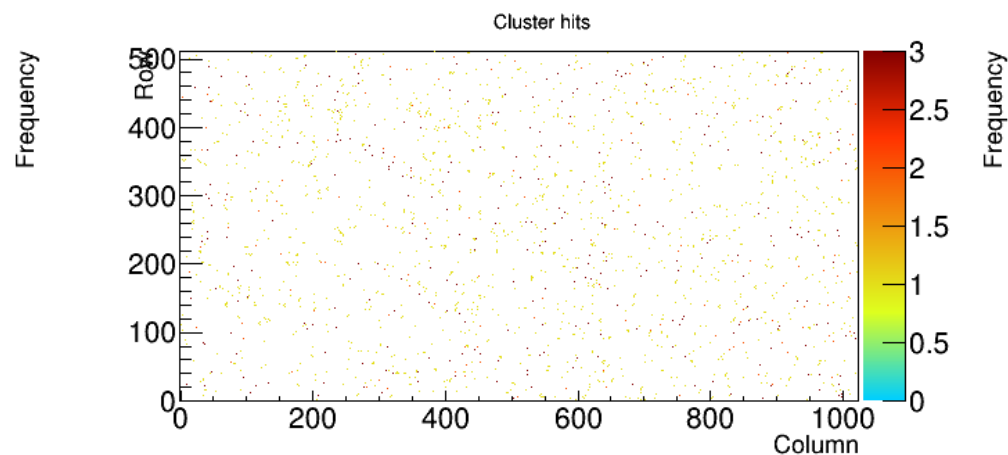
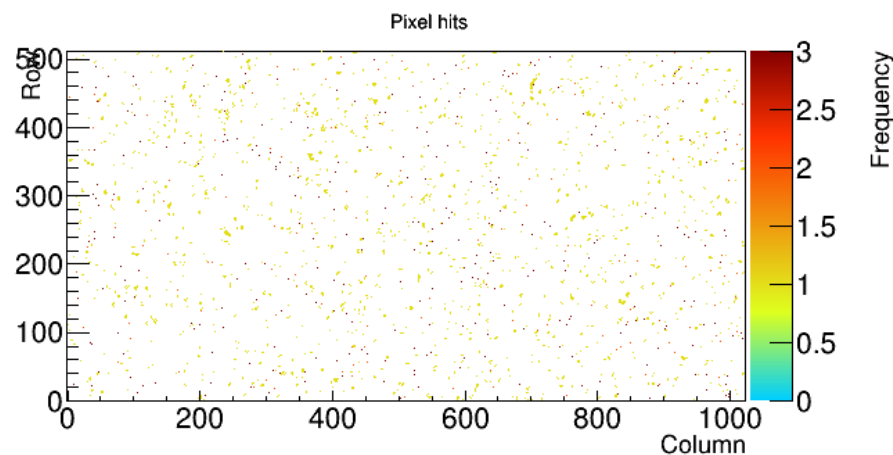
Source test + Cluster analysis

Triggers: 2000000

Vbb = -3V

Chip W7R12

Masked



Source: Sr-Y, chip temperature -100 °C

The ALPIDE characteristics studies



Results for high dose irradiated chip

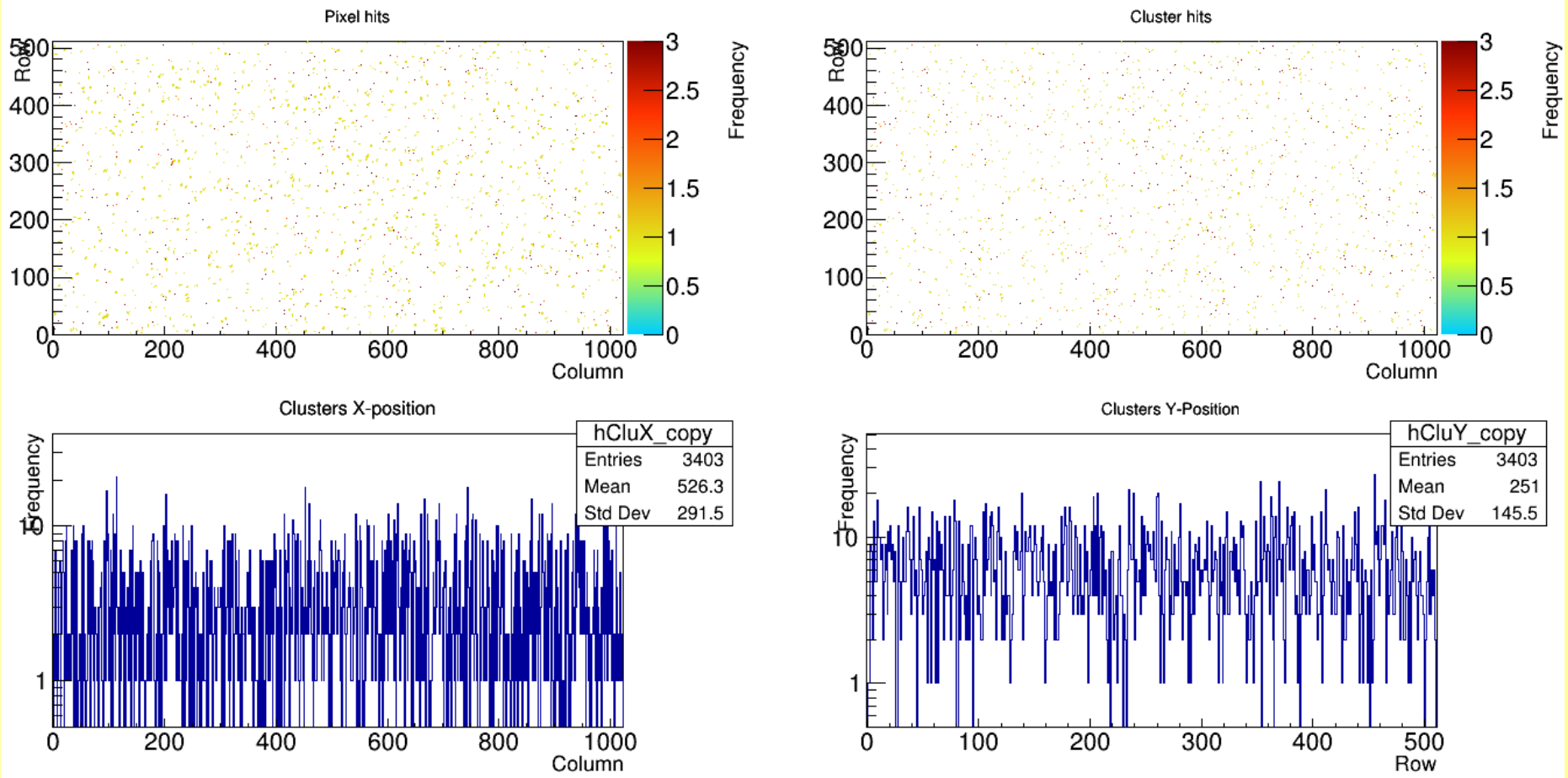
Source test + Cluster analysis

Chip W7R12

Masked

Triggers: 2000000

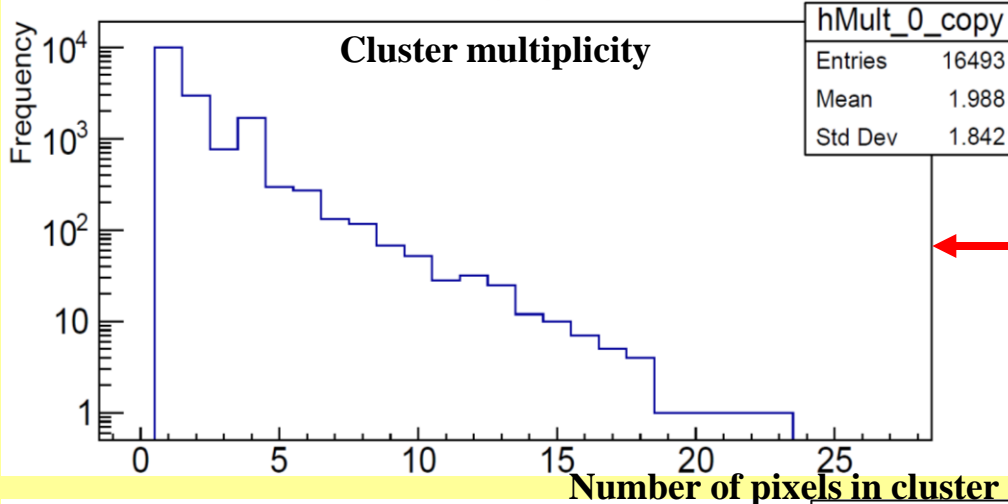
Vbb = -3V



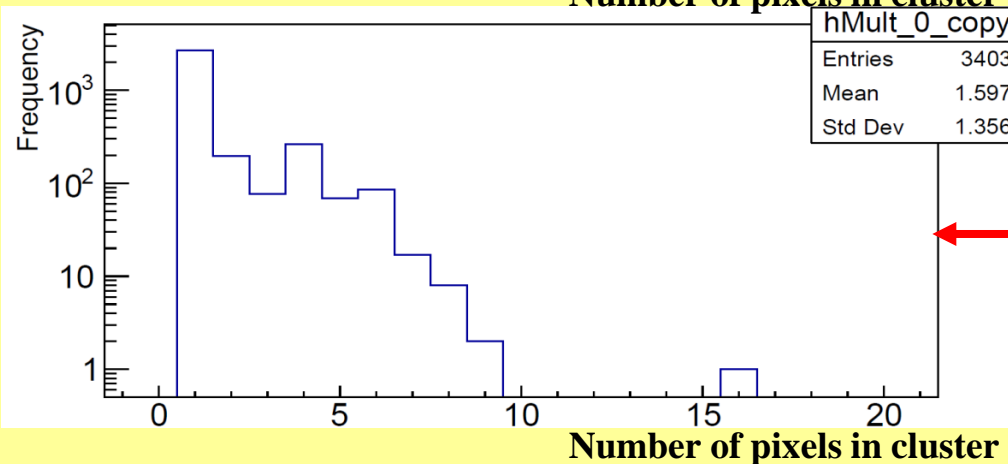
Source: 14C, chip temperature -100 °C

Source test + Cluster analysis

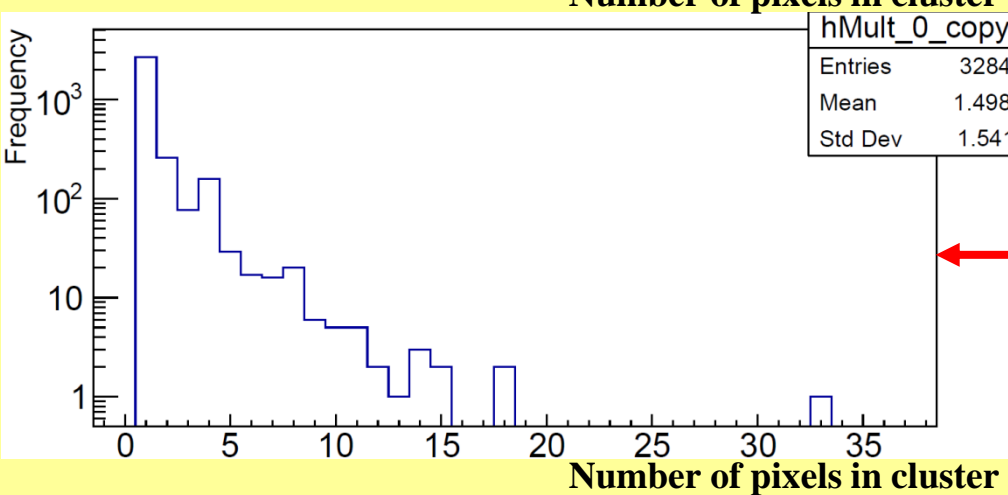
Chip W7R12



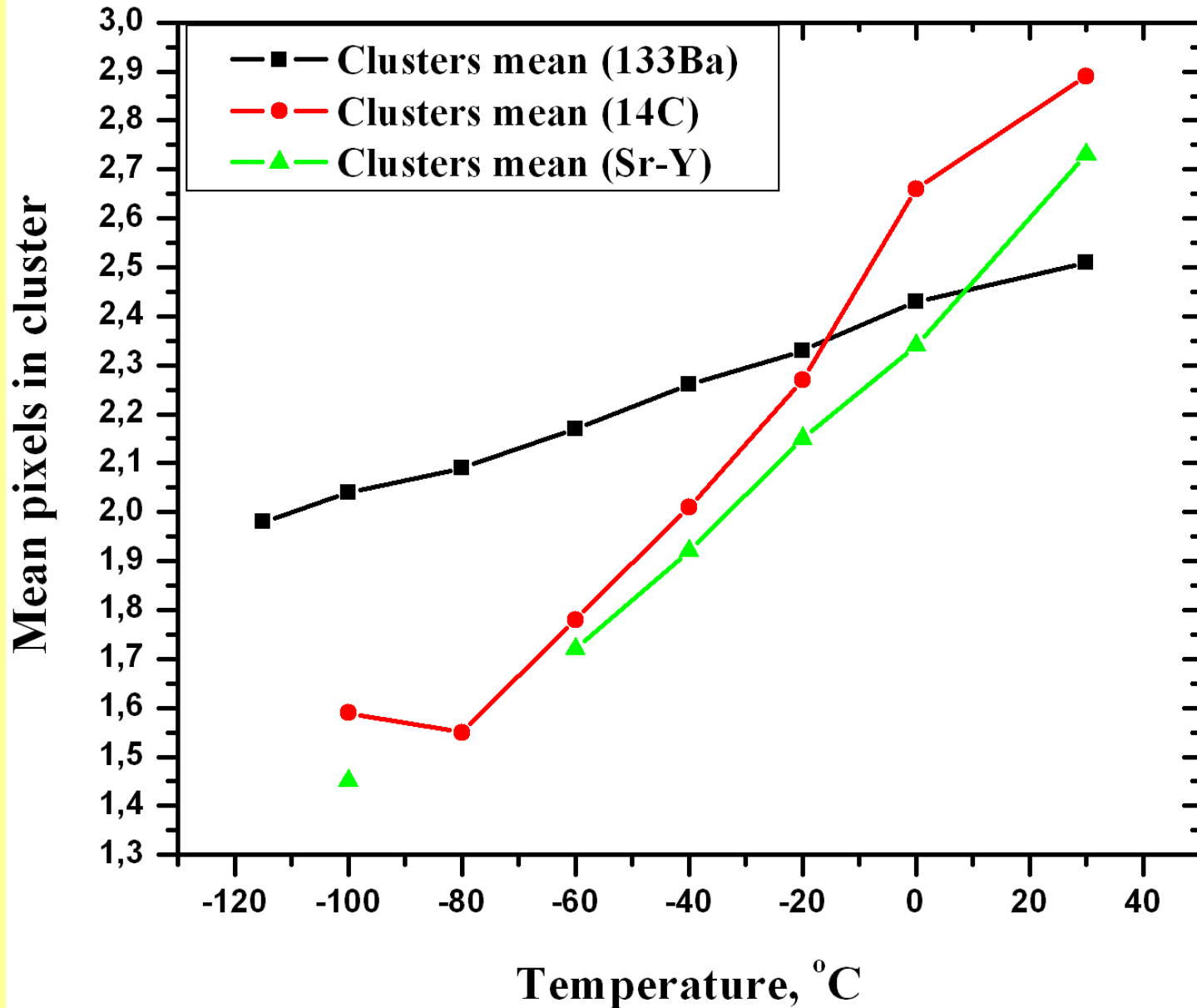
← 133Ba, chip temperature **-115 °C**



← 14C, chip temperature **-100 °C**



← Sr-Y, chip temperature **-100 °C**

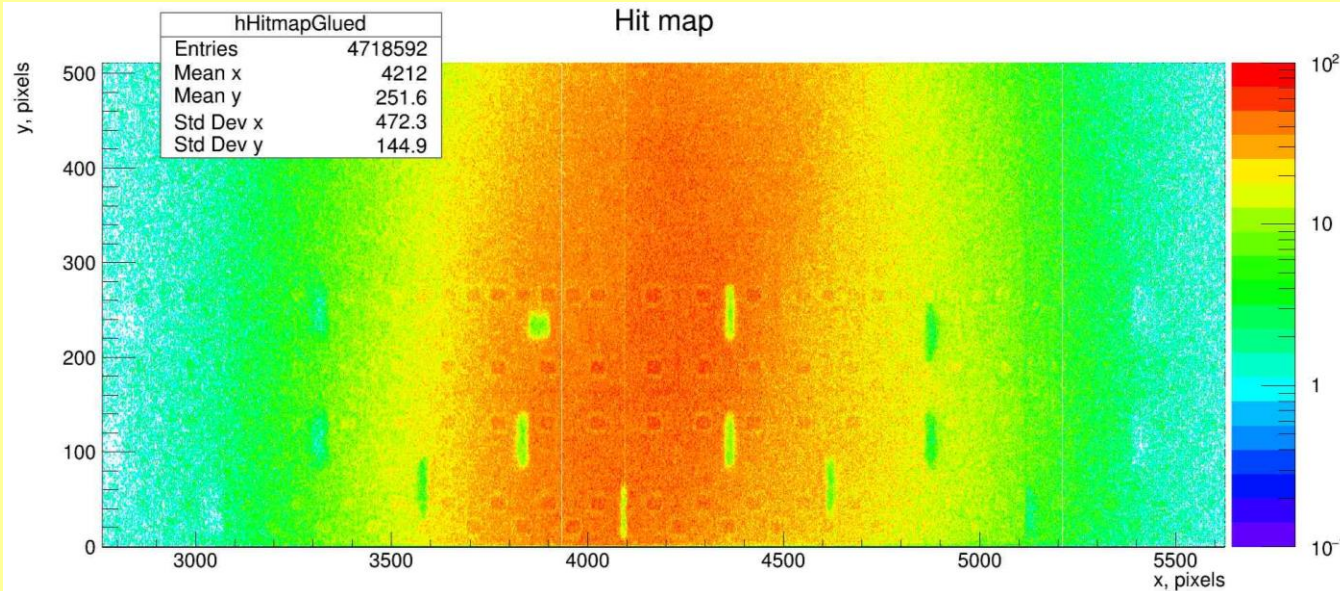
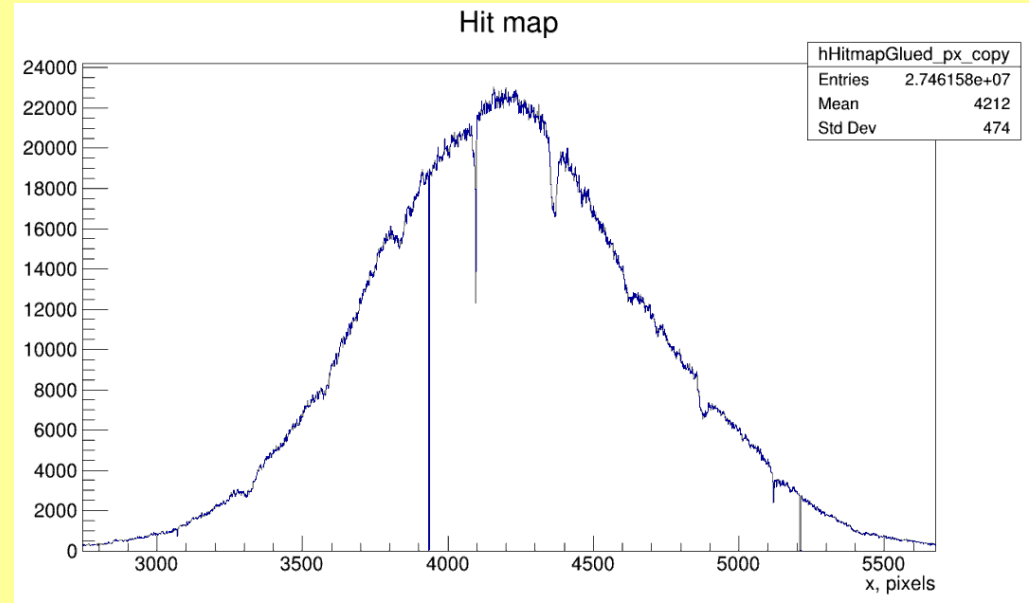
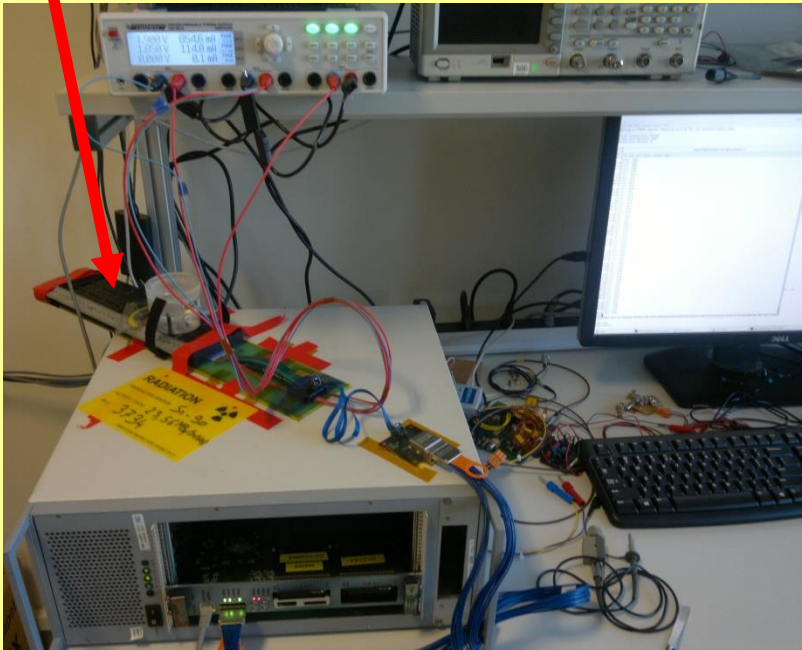


The ALPIDE characteristics studies

HIC – Hybrid Integer Circuit consist of 9 ALPIDE chips

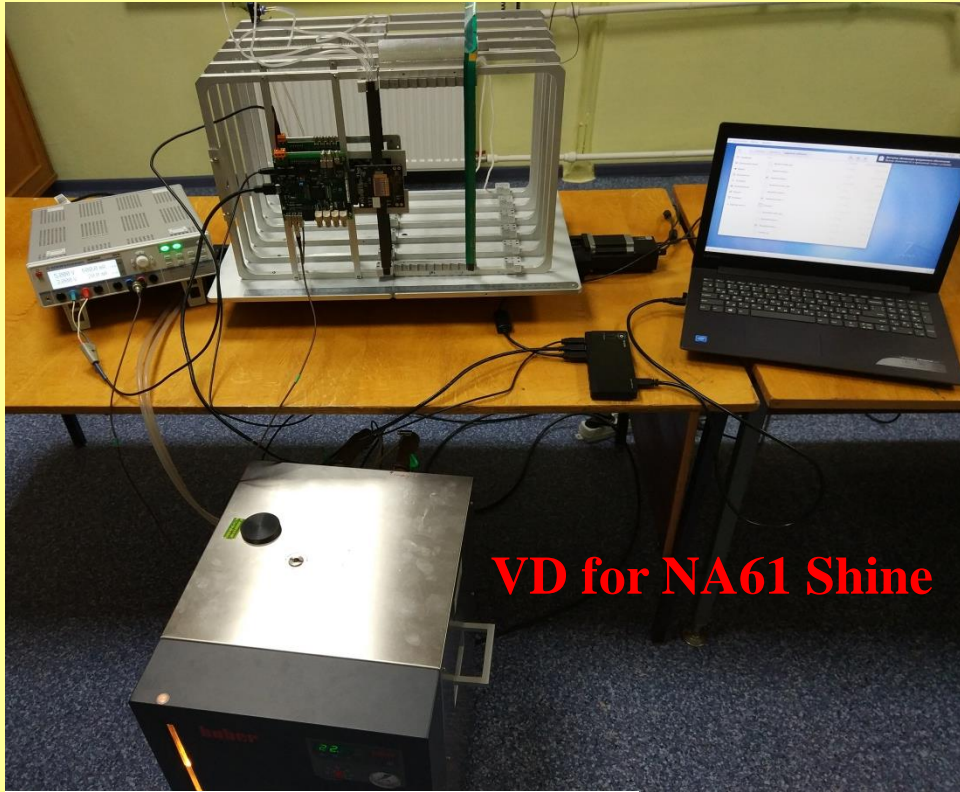


+ adapter IB FireFly-Eyespeed + VME

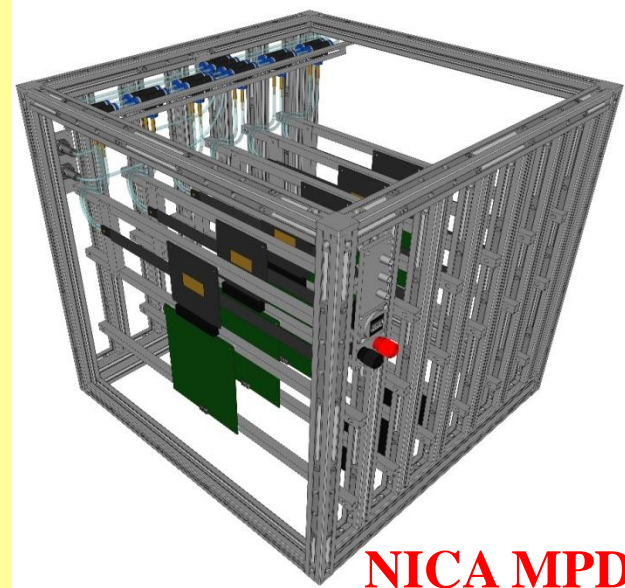


Sr-Y

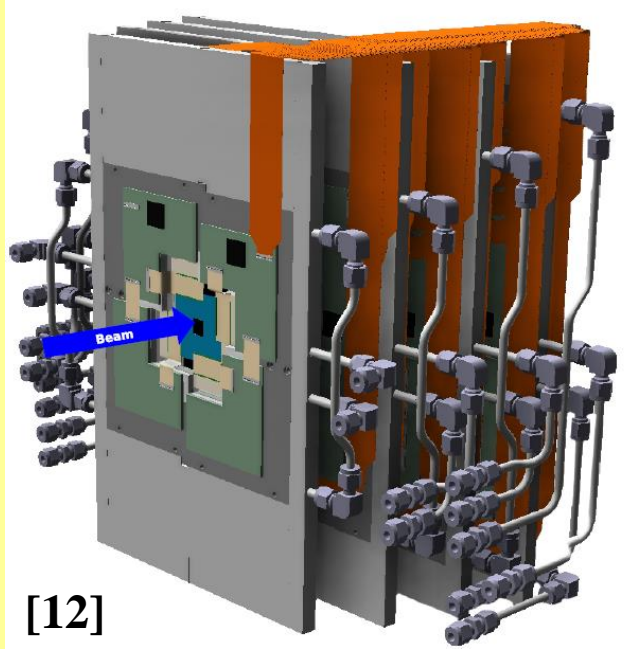
Detectors in Future Experiments



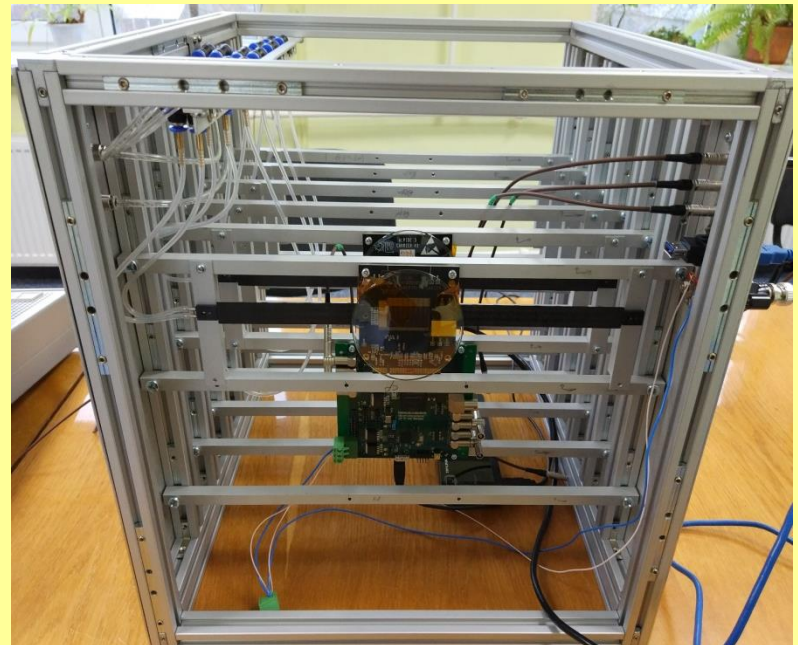
VD for NA61 Shine



NICA MPD

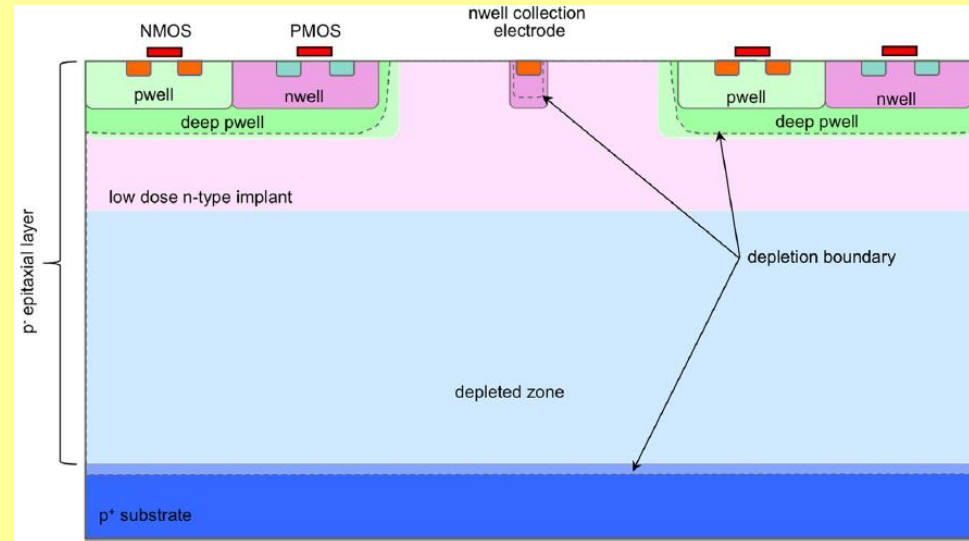
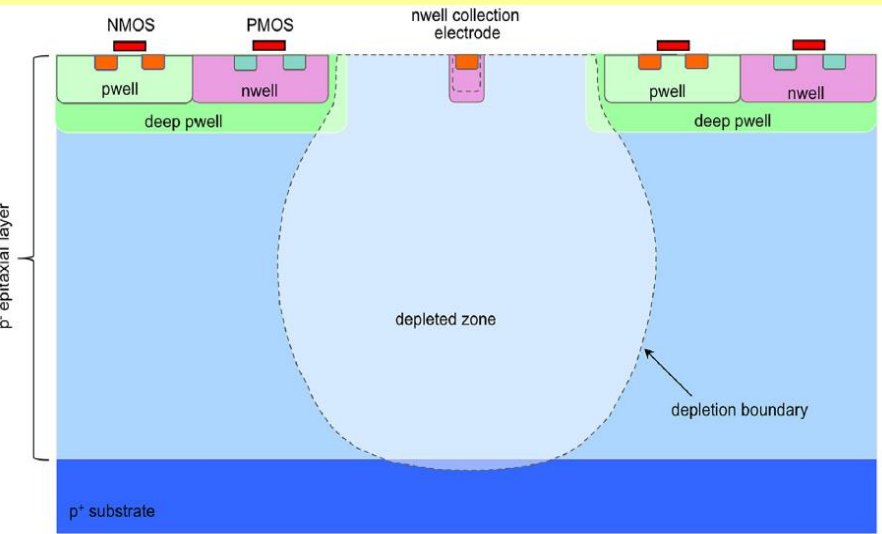


**CBM Micro Vertex
Detector
Chip MIMOSIS**



Detectors in Future Experiments

Modification for CMOS monolithic active pixel sensors



MAPS now. A deep pwell shields the nwells with circuitry from the sensor and allows full CMOS in the pixel. In the standard process it is difficult to deplete the epitaxial layer over its full width

[13]

MAPS future. Modification to fully deplete the epitaxial layer even with a small charge collection electrode. It uses a low dose blanket deep high energy n-type implant in the pixel array.

To improve NIEL tolerance up to 10^{15} 1 MeV n_{eq}/cm^2 , a drift field and hence depletion is required over the full sensitive layer. It reduce their collection time and hence the probability for them to be captured by radiation-induced defects or traps and be lost for readout.

Industrial applications



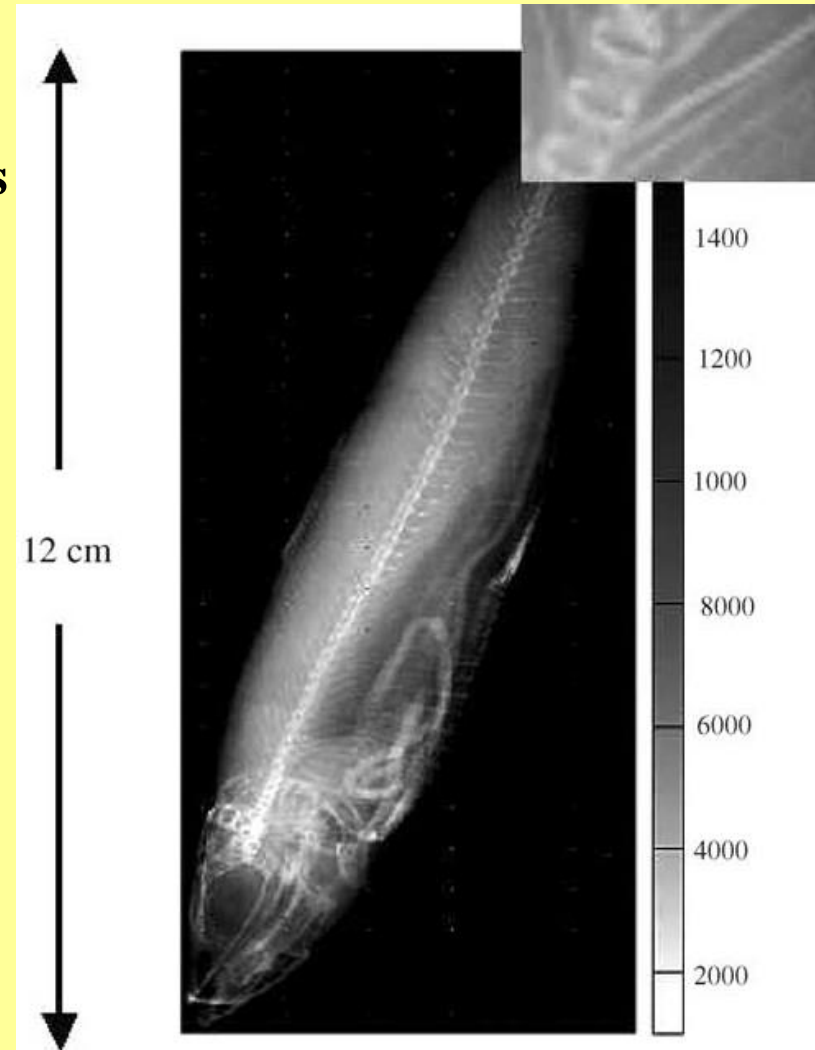
Medical: Scanners, Tomography, X-ray

Material science: Synchrotron, Xray detectors

Home security: Scanners, detectors


Space: rad tolerant electronics

Military

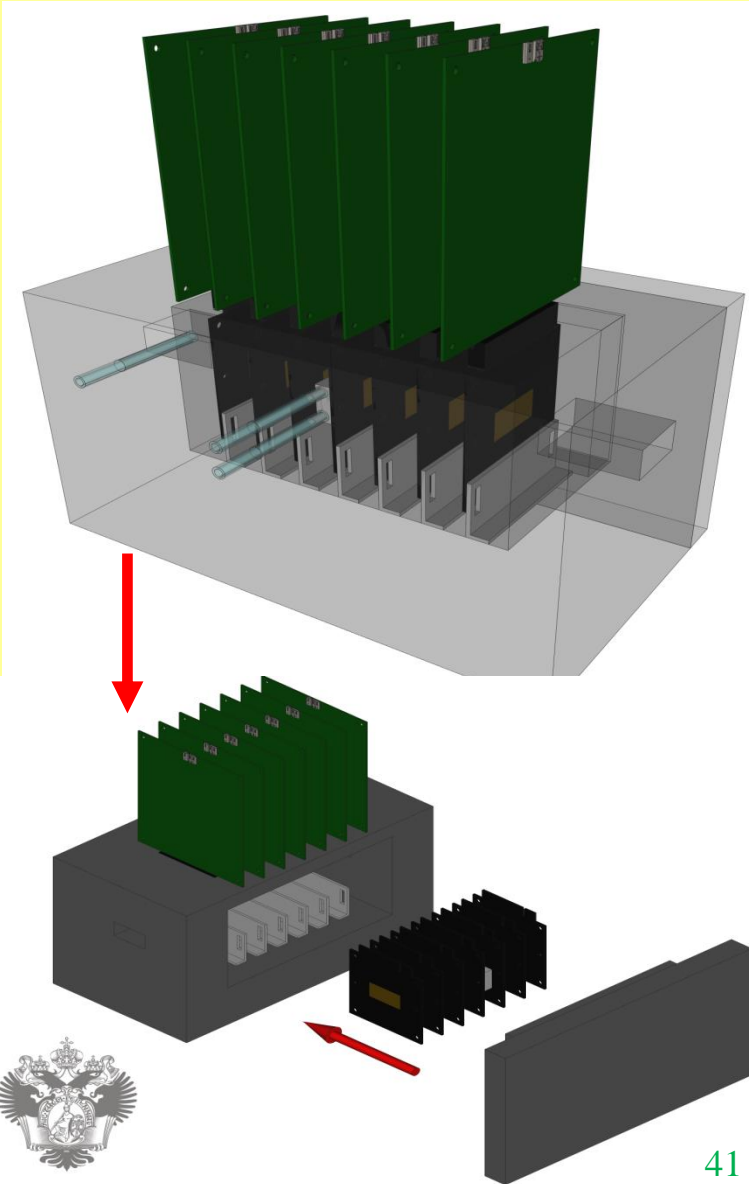


X-ray scan of a sardine with using the hybrid pixel detector MEDIPIX (64x64 pixels, 170 um x 170 um) from [14]

Next plans

1. Investigations of strongly irradiated ALPIDE – Final Version and Hybrid Integrated Circuit with 9 ALPIDE chips.
2. New experimental set-up for detector characterization: telescope + cooling. 
3. Constructing new VD prototype with ALICE inner barrel staves for NA61
4. New experimental set-up for detector tests with using Nuclotron beams in JINR for NICA MPD project.

New experimental setup for Beam Tests of Irradiated ALPIDE Chip equipped with cooling module



Conclusions



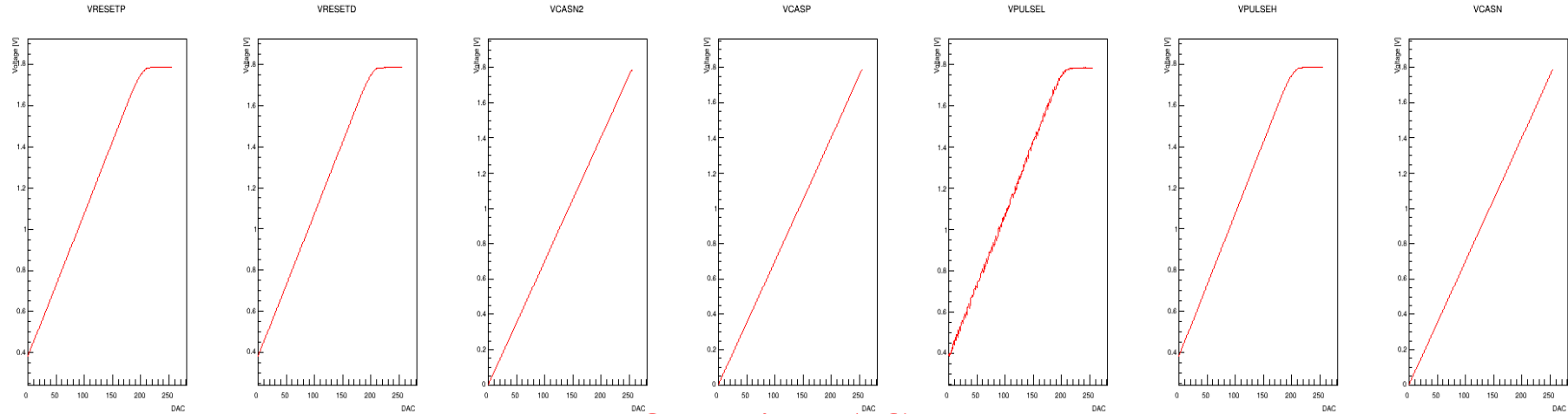
The development of MAPS have made significant progress in the last decade.

The big work is being done to make MAPS for using at high rate and high radiation environments in HEP experiments.

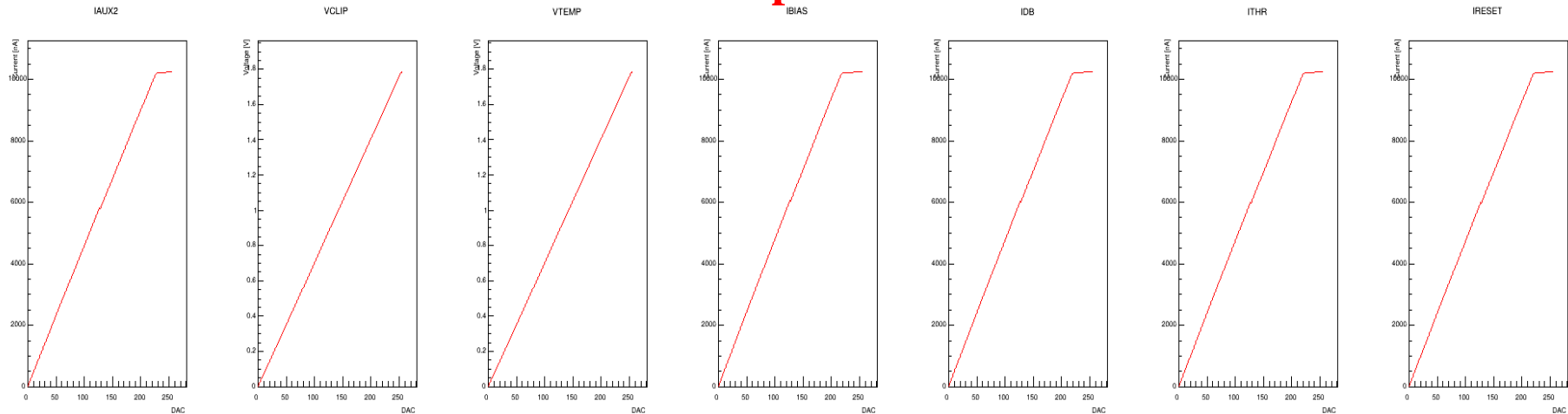
1. ALICE: <http://cdsweb.cern.ch/collection/ALICE%20Photos?ln=ru>
The ALICE experiment at the CERN LHC, 2008 JINST 3 S08002, doi:10.1088/1748-0221/3/08/S0800
2. ATLAS Experiment: <http://cds.cern.ch/record/1095925>
3. ATLAS Experiment: <http://cds.cern.ch/record/989408>
4. CMS: <http://cms.cern/detector/identifying-tracks>
5. LHCb: <http://cdsweb.cern.ch/search?cc=LHCb+Photos&ln=ru&p=subject%3A%22VELO%22>
6. V.Zherebchevsky «WG3 ITS upgrade meeting», CERN, 30.04. 2012: <https://indico.cern.ch/event/188015/>
7. Felix Reidt CERN-THESIS-2016-033
8. Conceptual Design Report for the Upgrade of the ALICE ITS
9. Flemming Videbaek For the STAR collaboration Brookhaven National Lab
<https://sss.slideserve.com/shaw/the-star-heavy-flavor-tracker>
10. Guannan Xie (for the STAR Collaboration). <https://arxiv.org/pdf/1704.04353.pdf>
XXVIth International Conference on Ultrarelativistic Nucleus-Nucleus Collisions/ (Quark Matter 2017)
11. The ALICE Collaboration. “Technical Design Report for the Upgrade of the ALICE Inner Tracking System”. In: J. Phys. G41 (2014), p. 087002.
12. CBM-MVD. <https://indico.gsi.de/event/6234/contribution/2/material/slides/0.pdf>
13. W. Snoeys et.al. Nuclear Inst. and Methods in Physics Research, A 871 (2017) 90–96
14. N. Wermes, Nuclear Instruments and Methods in Physics Research, A 512 (2003) 277–288

BACK-UP SLIDES

All next experimental results are presented for pALPIDE-3 chip



On-chip DAC Tests



Good linearity of voltage and current settings has been observed. The linear fit demonstrates the same slopes for all parameters for the present chip at different temperatures.

Study of the characteristics of full-scale Pixel Detector prototypes



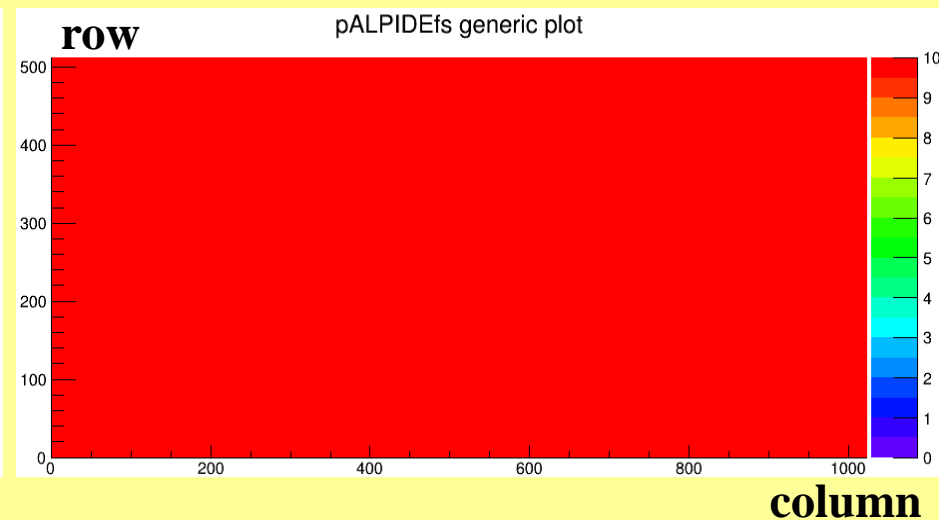
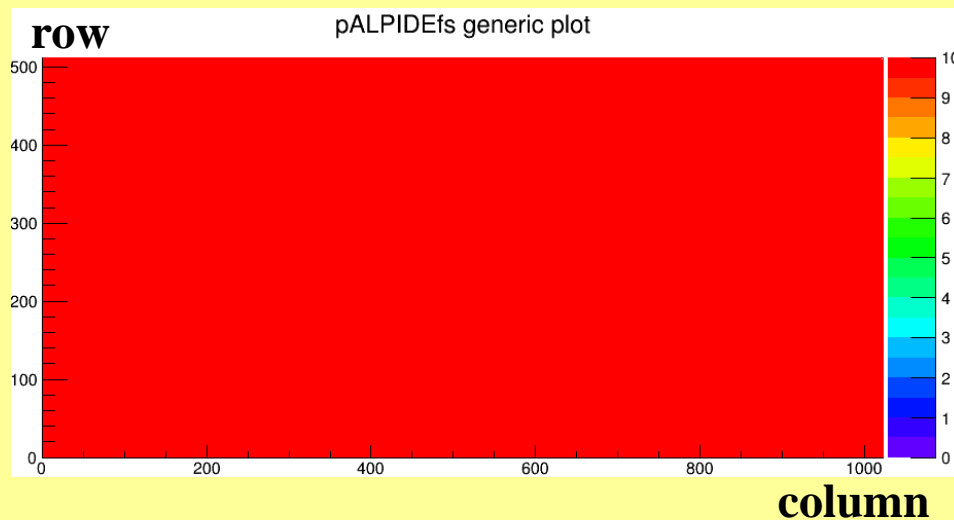
Digital and Analogue scans. Scans generate digital or analog pulses in a number of pixels and read the hits out

For both tests common parameters: 10 (number of injections per pixel) and test 100 % of the pixels

For analogue test an additional parameter the charge equal 350 e⁻ was used.

Digital Scan

Analogue Scan

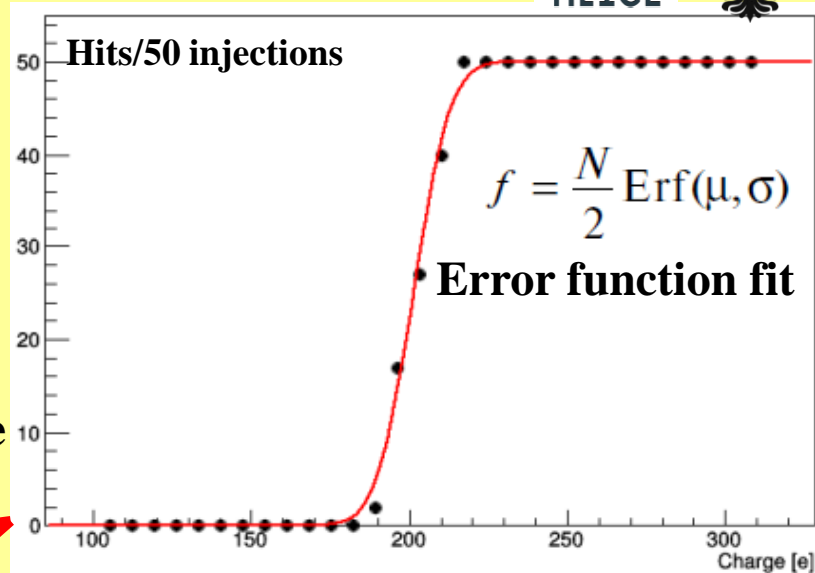


Good homogeneity of the pixel maps for both scans has been observed.

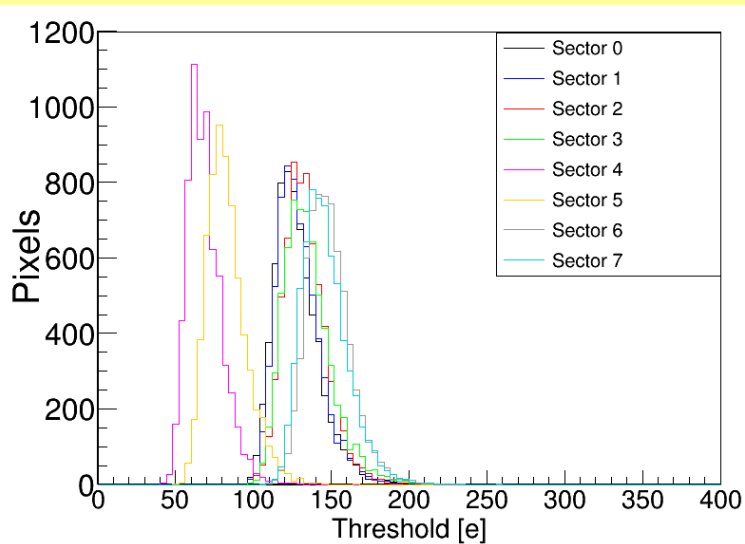
Threshold Scan

The operational thresholds for a certain set of detector's pixels depending on the charge delivered to the chosen pixels was determined

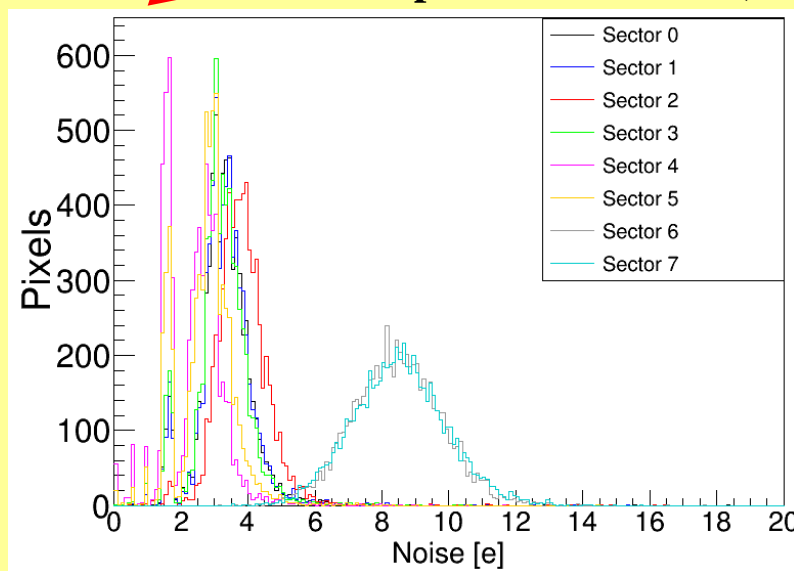
In order to extract threshold a number of charge injections with different amplitude are performed (50 points with 50 injections per point). A probability distribution of fired pixels measuring a pixel response (S-curve) has been obtained.



N - number of injections, μ - threshold value
 σ - temporal noise value (threshold dispersion)



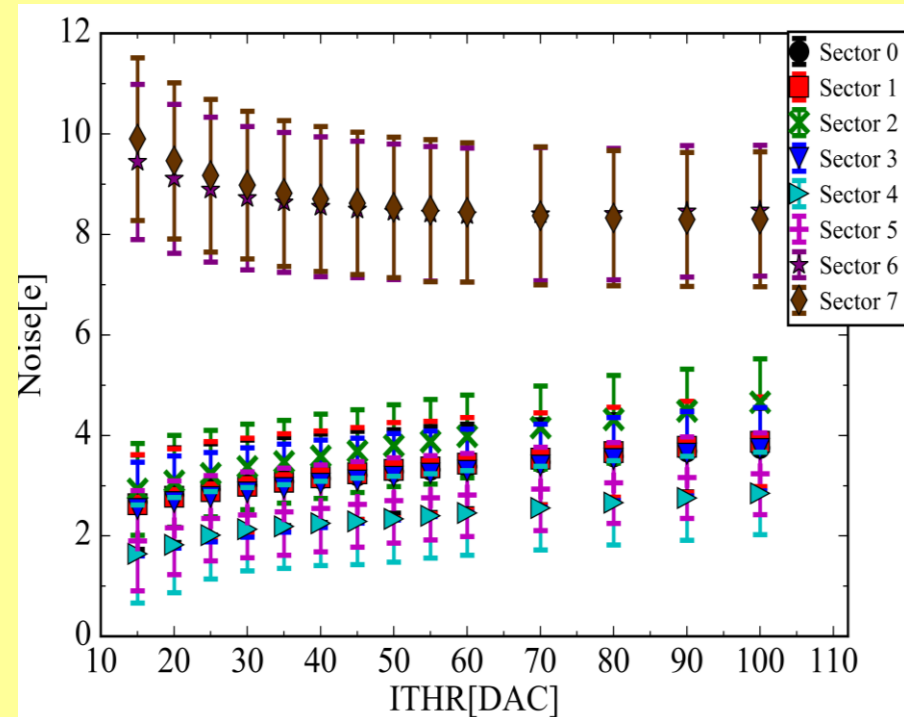
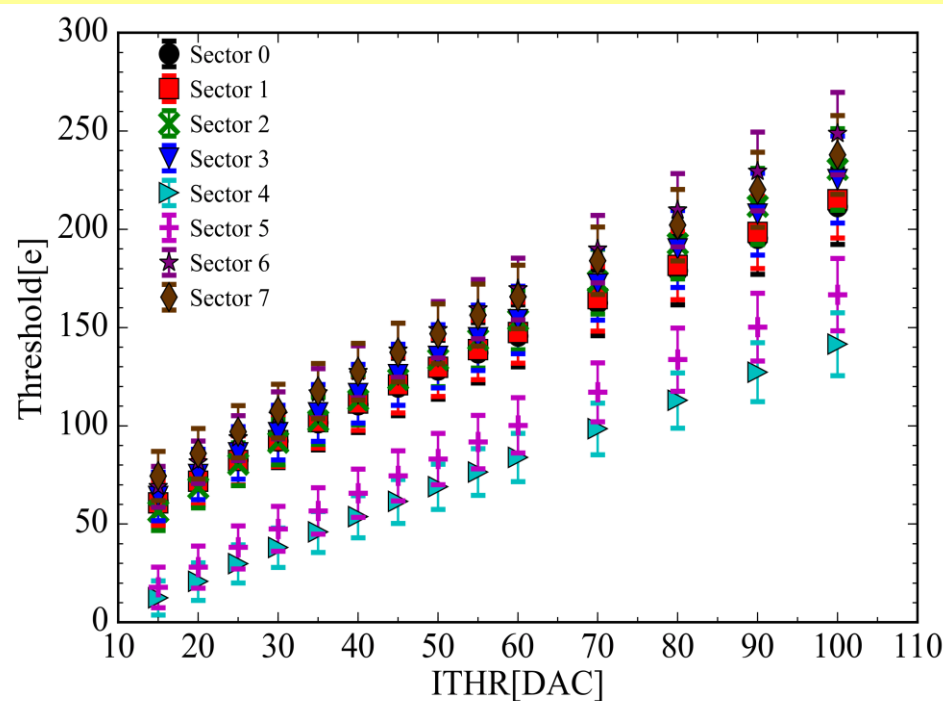
Pixel threshold distribution for 8 sectors



Temporal noise values for the pixels for 8 sectors

Threshold Scan

1. Investigations of threshold and noise, depending on the magnitude of the I_{THR} current fed to the control transistor of a sensor at a fixed VCASN value



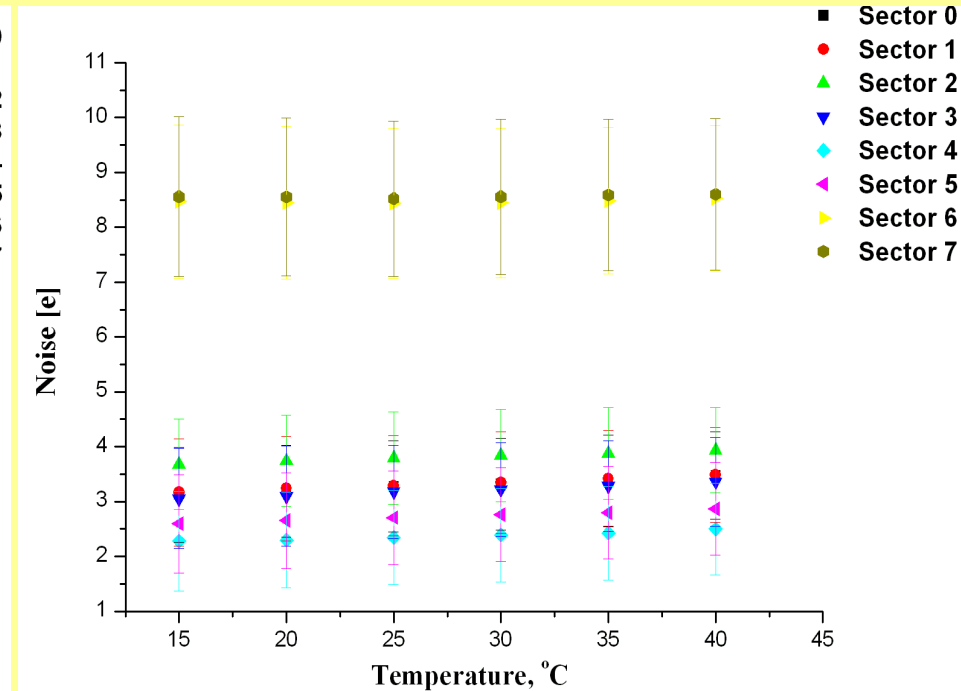
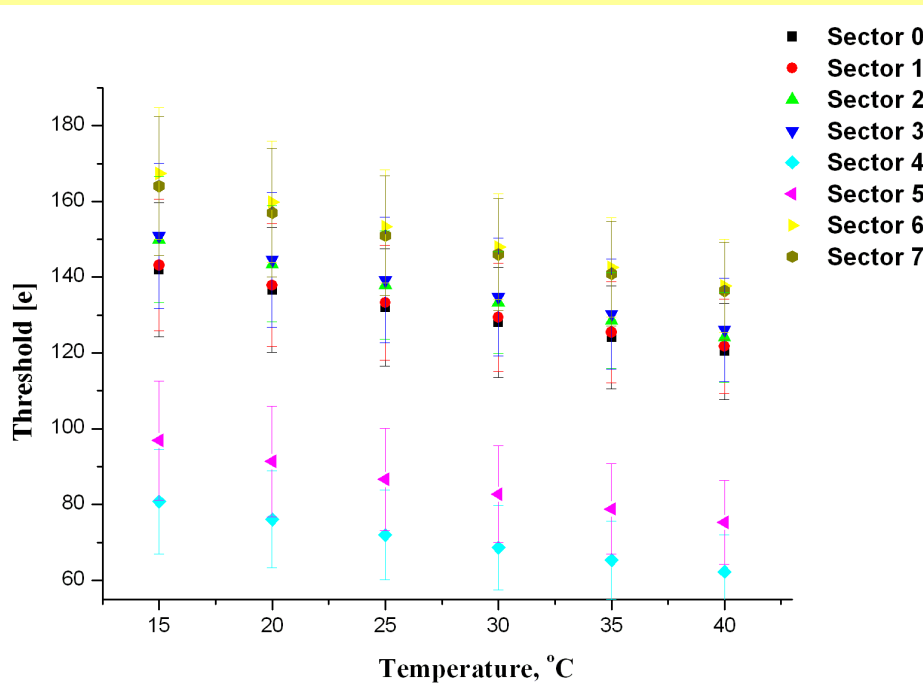
The linear dependence of the threshold values vs. Ithr has been observed for all sectors.

The threshold noise distributions are constant in the Ithr region: 40 - 60 DAC.

The thresholds in sectors 6-7 are bigger than in other sectors.

Threshold Scan

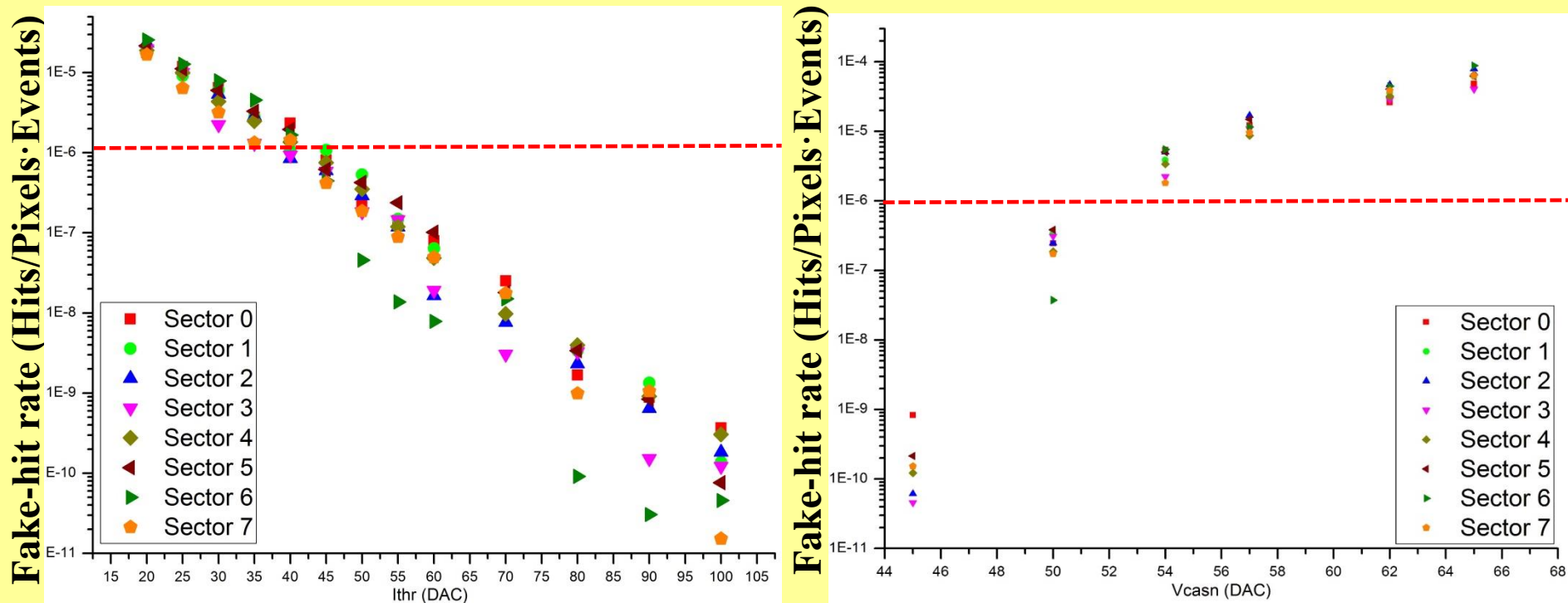
1. Investigations of threshold and noise, depending on chip temperature



The threshold goes down slowly with the increasing of **Temperature** for all sectors.

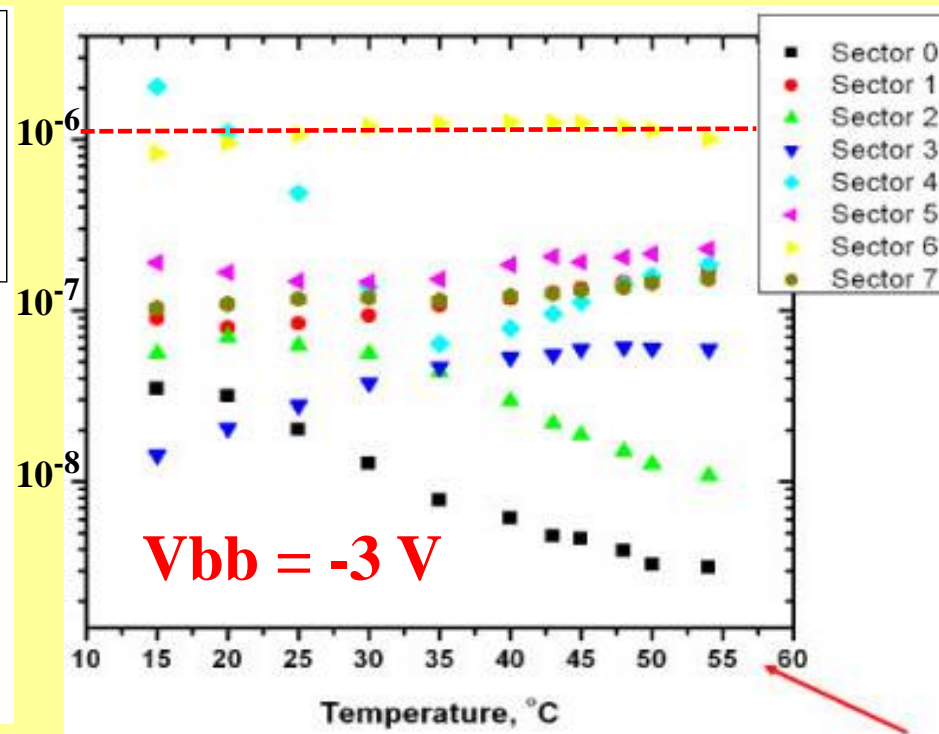
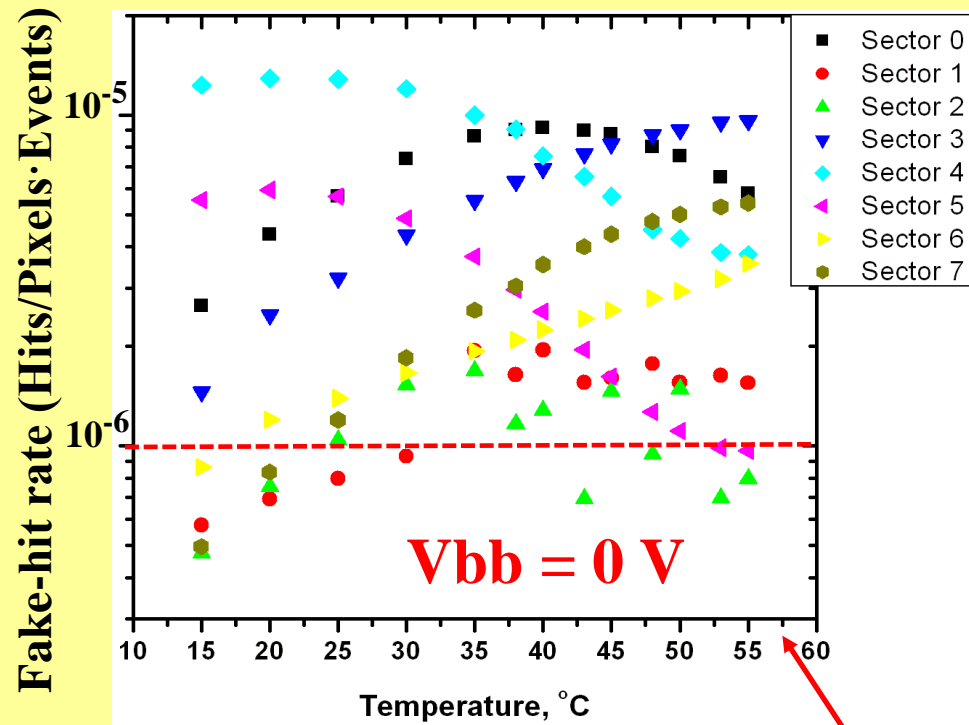
The threshold noise distributions are constant within the entire temperature range.

Noise characteristics of the sensor



Noise occupancy strongly depends on the main detector settings I_{TH} and V_{CASN} . The values of these parameters which does not exceed the acceptable level of Fake hits per pixel per event (upgrade requirements) have been found.

Noise characteristics of the sensor and its temperature dependence



Temperature limit has been reached: **56 °C**

Noise occupancy strongly depends on temperature

After applying V_{bb} the acceptable level of Fake hits per pixel per event (upgrade requirements) has been reached.

Studies with gamma and beta sources. Cluster analysis

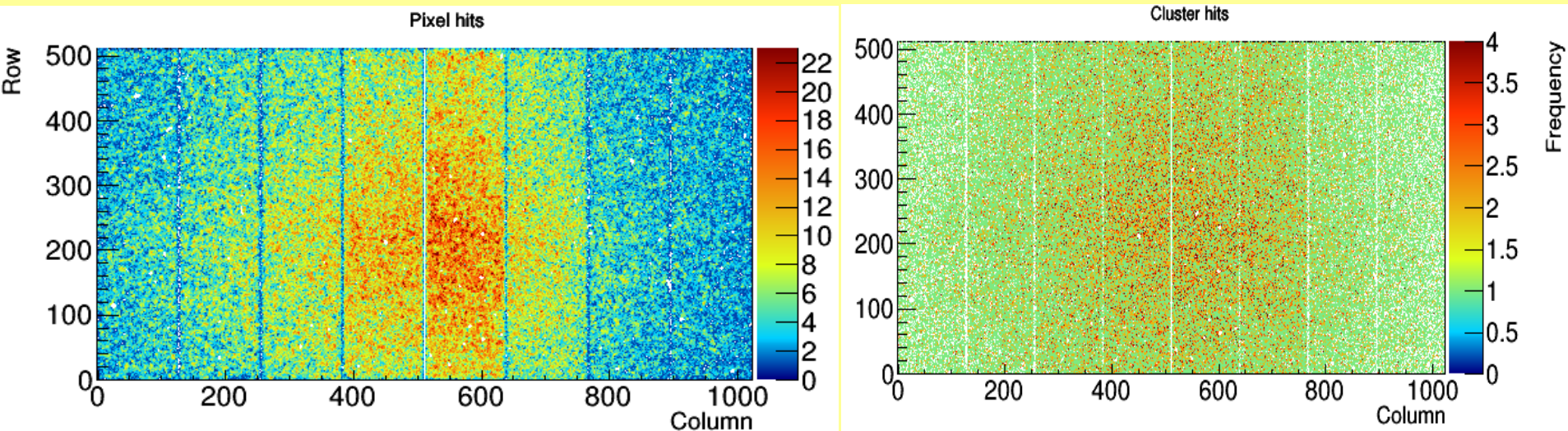
Gamma sources: ^{241}Am (13.9 keV), ^{133}Ba (5.64 keV), ^{152}Eu (4.29), ^{55}Fe (5.9 keV)

Beta sources: ^{14}C , $^{90}\text{Sr-Y}$

A cluster is considered to be an area of a pixel matrix with a certain number of neighboring fired pixels. The number of pixels determines the cluster size.

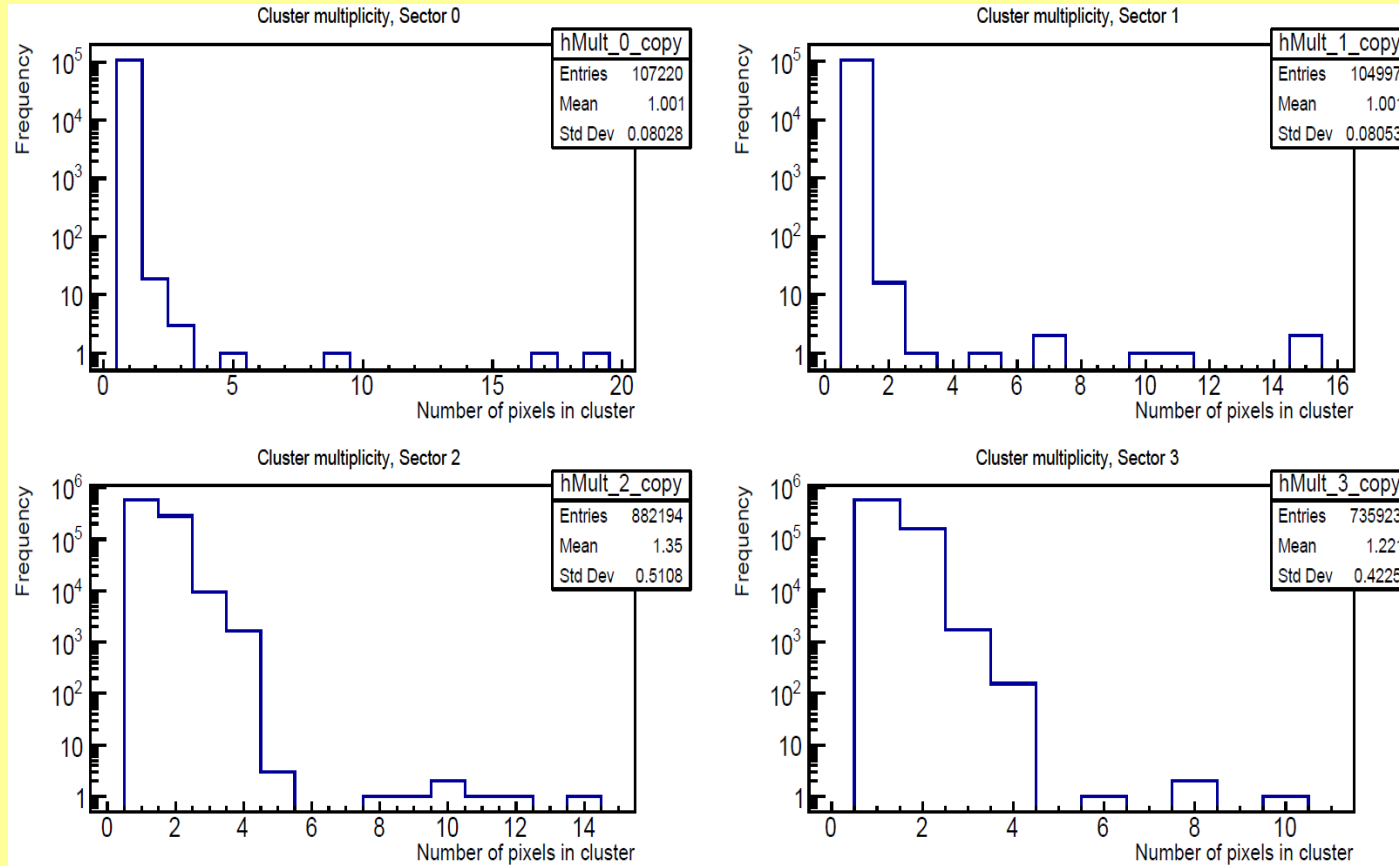
The clusters with cluster multiplicity = 1 have been included. Because in source test the noise mask (excluded hot pixels) has been applied.

Pixel and cluster hits for ^{152}Eu



Study of the characteristics of full-scale Pixel Detector prototypes

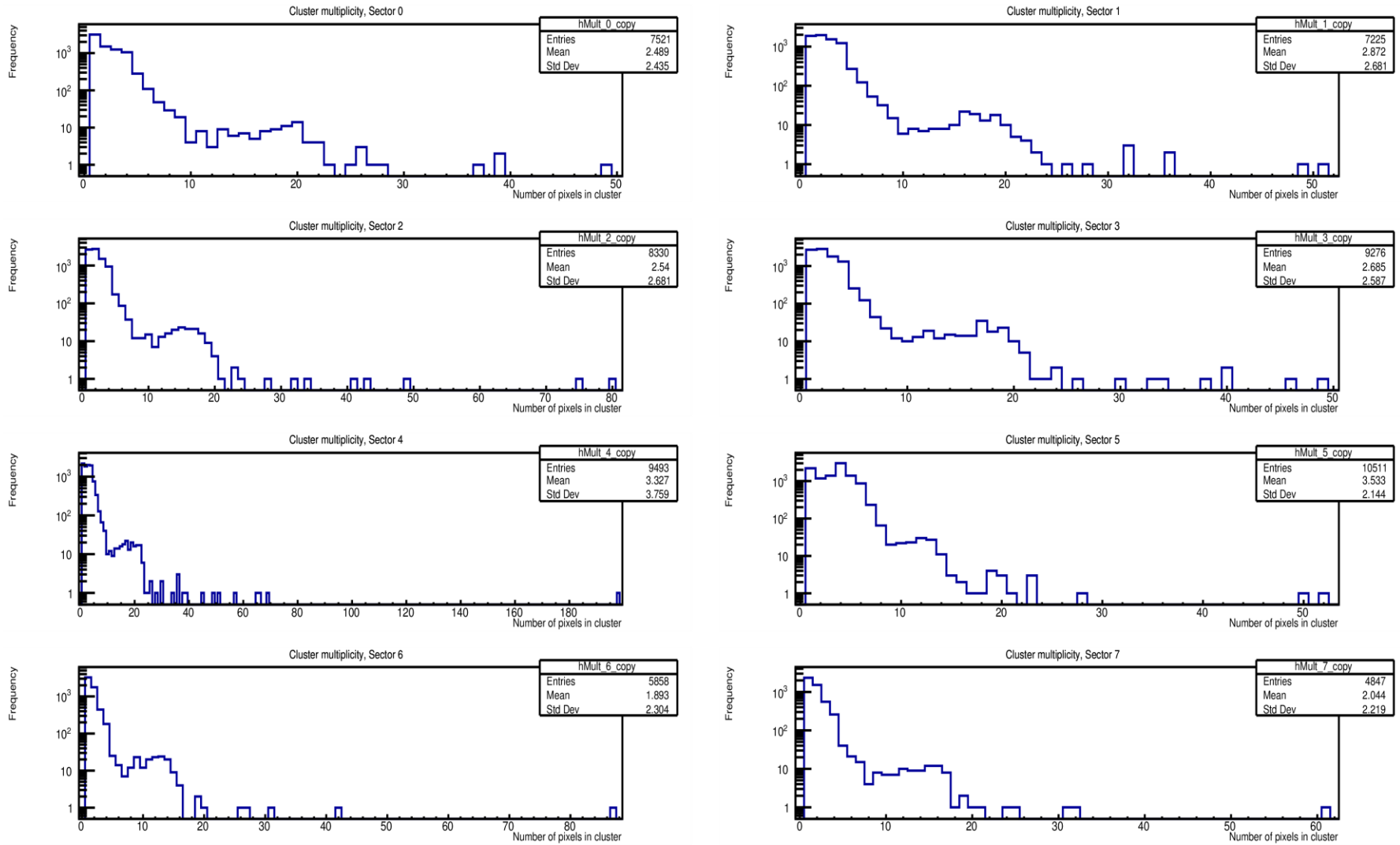
Cluster multiplicity in different sectors for 55Fe



No large clusters. Average cluster multiplicity no more 1.35

Cluster multiplicity in different sectors for ^{241}Am

The highest yield of large clusters in Sector 5 Occurrence of the large clusters could be explain by registration of the electrons emitted from these sources. For ^{55}Fe there is no large clusters (only gamma emits from source)



Study of the characteristics of full-scale Pixel Detector prototypes

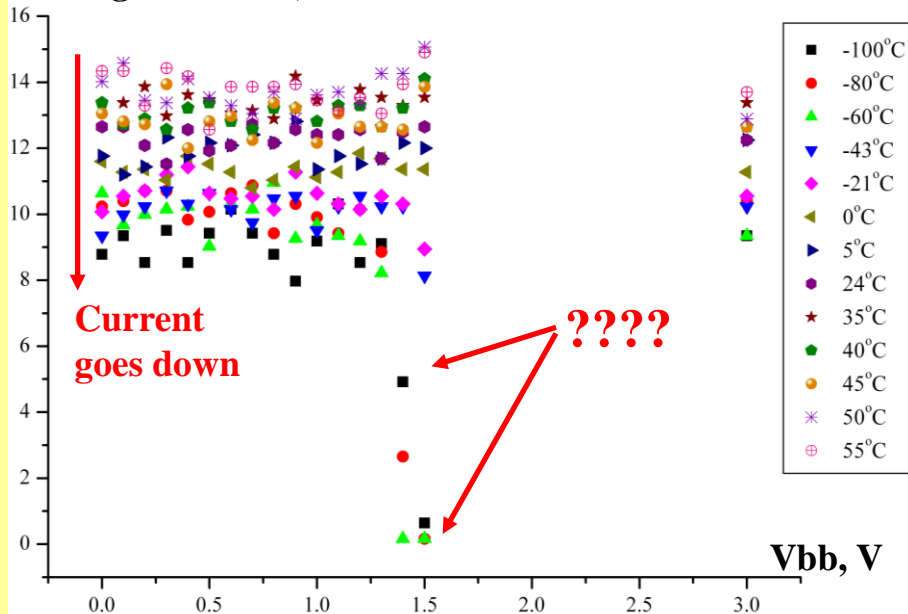
Analogue Currents



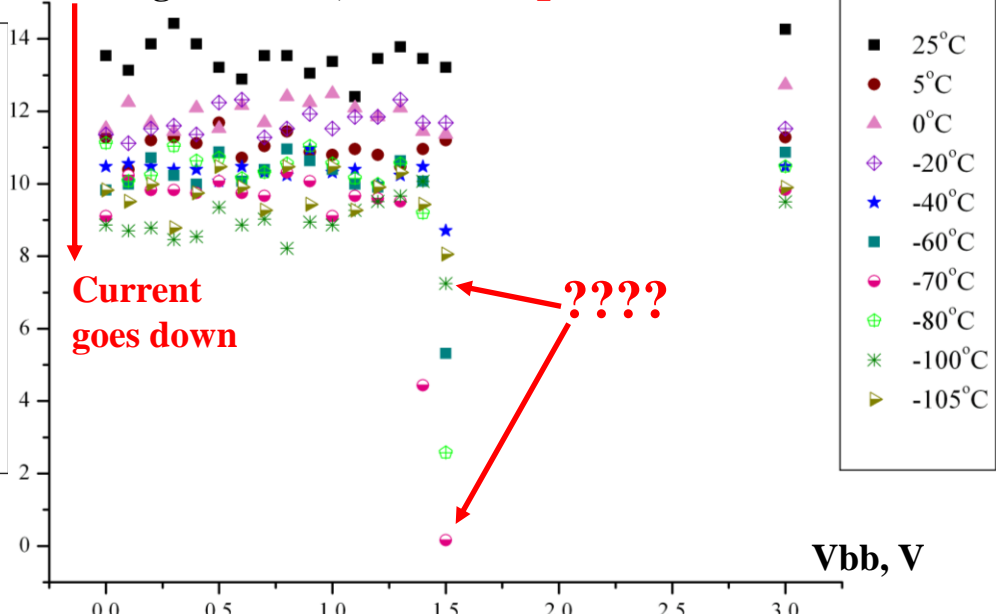
Chip W8R22

Chip W7R12

Analogue current, mA

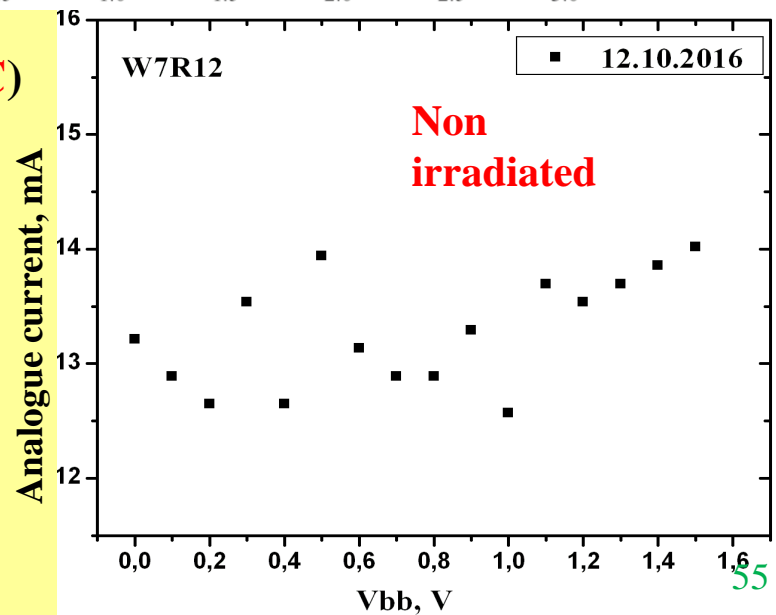


Analogue current, mA



1. With lowering temperature (from +24 °C to -105 °C) for both Chips analogue current goes down from 14 to 9 mA;

2. Strange current behavior for Vbb = 1.4-1.5 V has been observed for temperature range: -60 °C → -100 °C



ALICE Inner Tracking System (current status)

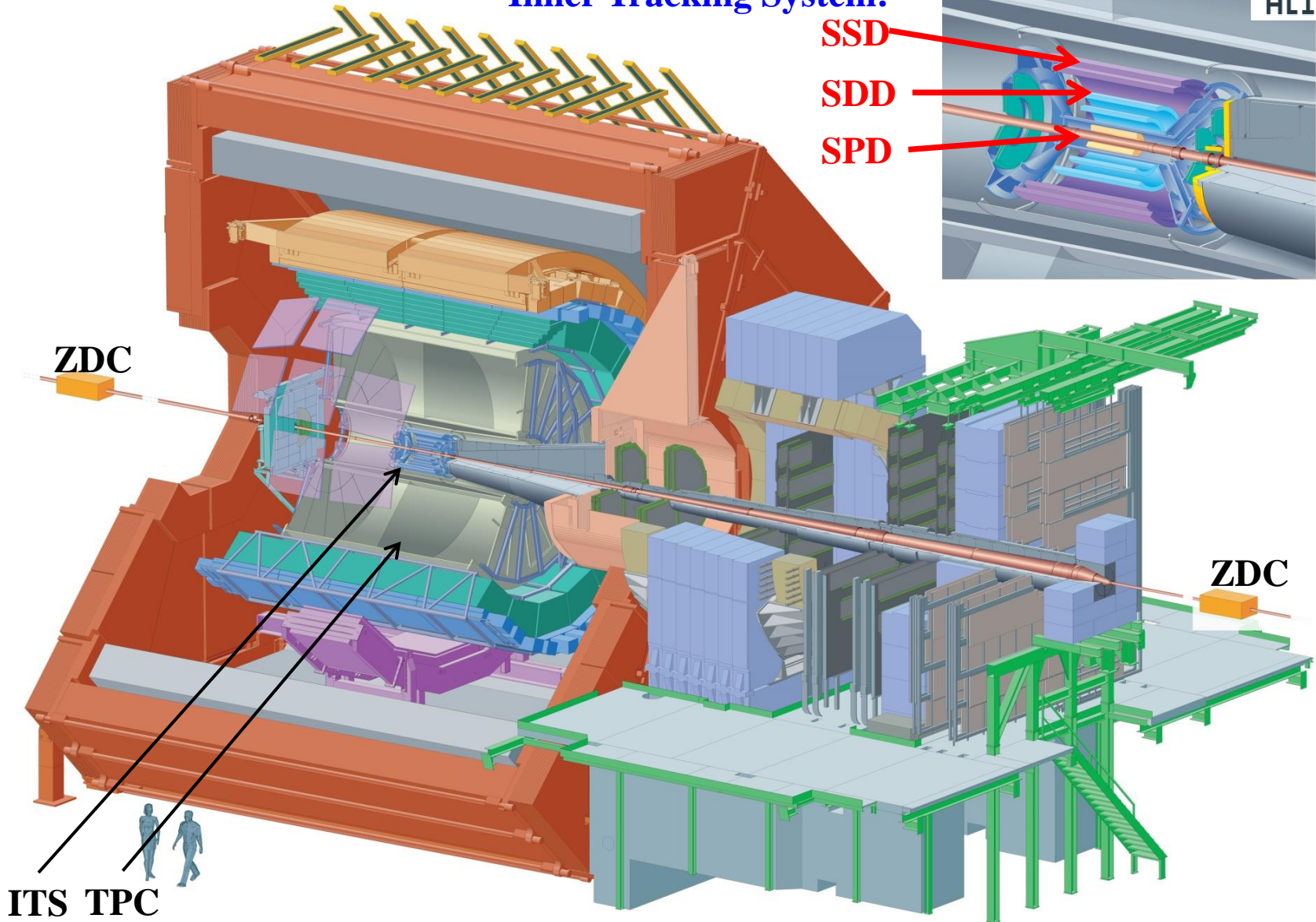
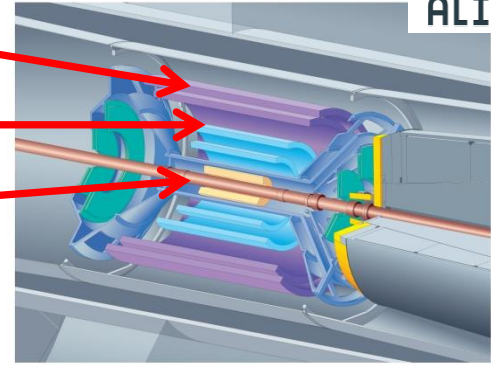


Inner Tracking System:

SSD

SDD

SPD



Current ALICE set-up with its main detectors [1]



Physics

Heavy- flavour measurements with largely improved tracking and read-out rate capabilities

Two main open questions concerning heavy-flavour interactions with the QGP medium are:

- 1. Thermalisation and hadronisation of heavy quarks in the medium. Measuring the heavy-flavour baryon/meson ratio, the strange/non-strange ratio for charm, the azimuthal anisotropy for charm and beauty mesons, and the possible in-medium thermal production of charm quarks**
- 2. Heavy-quark in-medium energy loss and its mass dependence.**

Also detailed measurement of low-mass dielectrons (low material budget and the improved tracking precision and efficiency of the new ITS):

Thermal radiation from the QGP, via real and virtual photons detected as dielectrons

Also production measurement of hypernuclear states

Physics

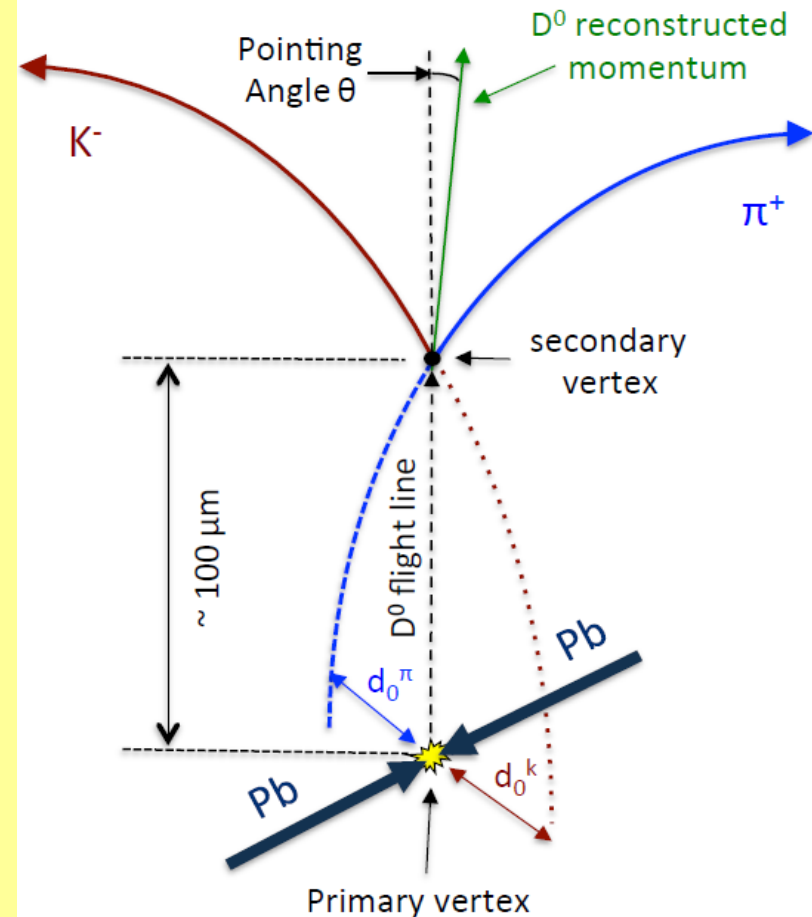
Improve primary vertex reconstruction, momentum and impact parameter Resolution

Resolution

Reconstruction of secondary vertices from c and b decays with high resolution

Secondary vertex determination

Example: D^0 meson

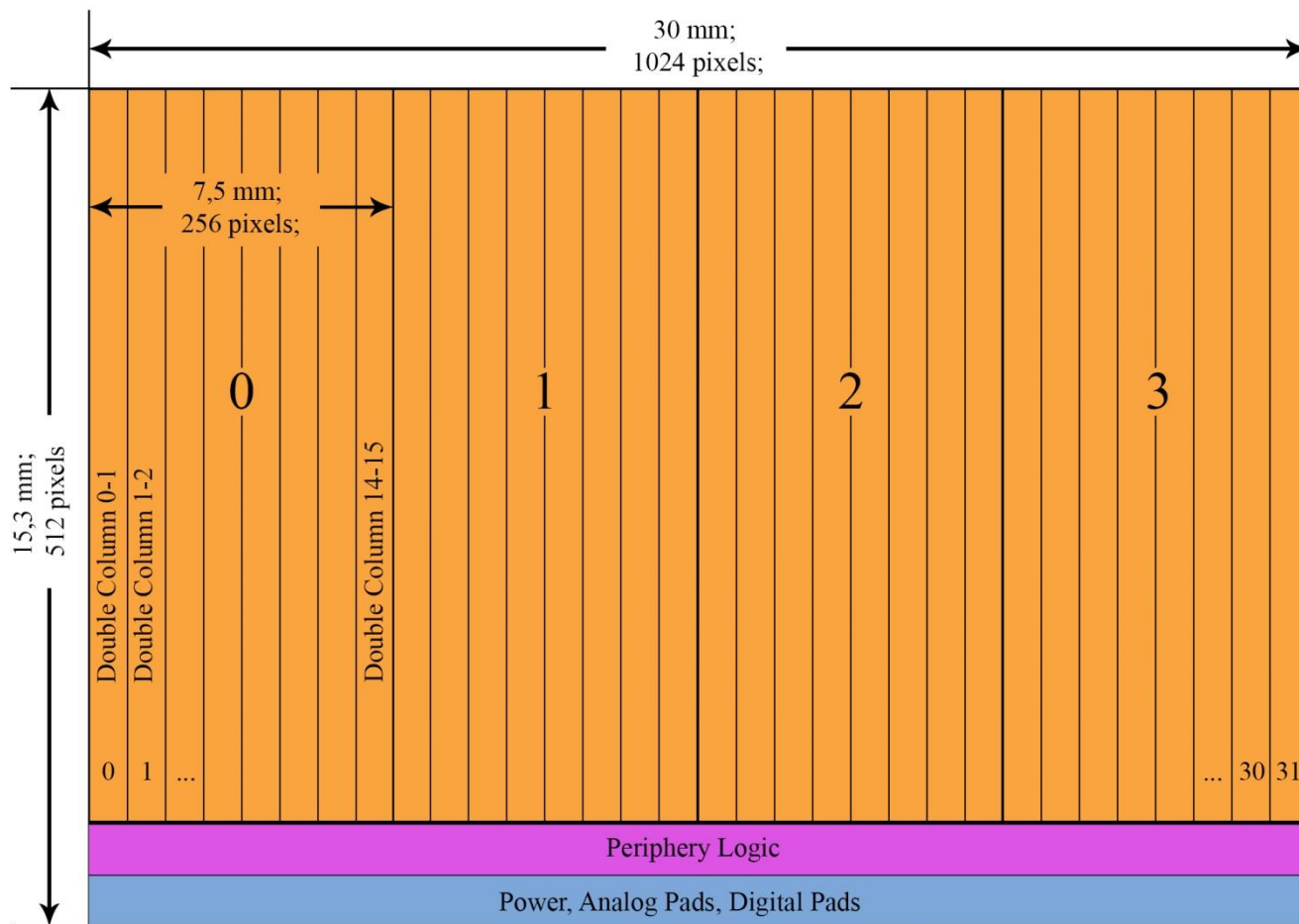


Particle	Decay Channel	$c \cdot \tau$ (μm)
Λ_c^+	$pK^-\pi^+$	60

Current ITS Impact Parameter Resolution $\sim 70 \mu\text{m}$ at $p_t=1\text{GeV}/c$

ALICE Pixel Detectors (ALPIDE family)

Pixel matrix of pALPIDE-1,2



The pixel matrix is divided into 32 regions arranged in sectors. Each sector includes 8 double columns (0, 1, 2..).

In the space between each pair of double columns is a priority encoder circuit (Address-Encoder Reset-Decoder) that performs the asynchronous reading of a signal from the pixels in these columns.

ALICE Pixel Detectors (ALPIDE family)



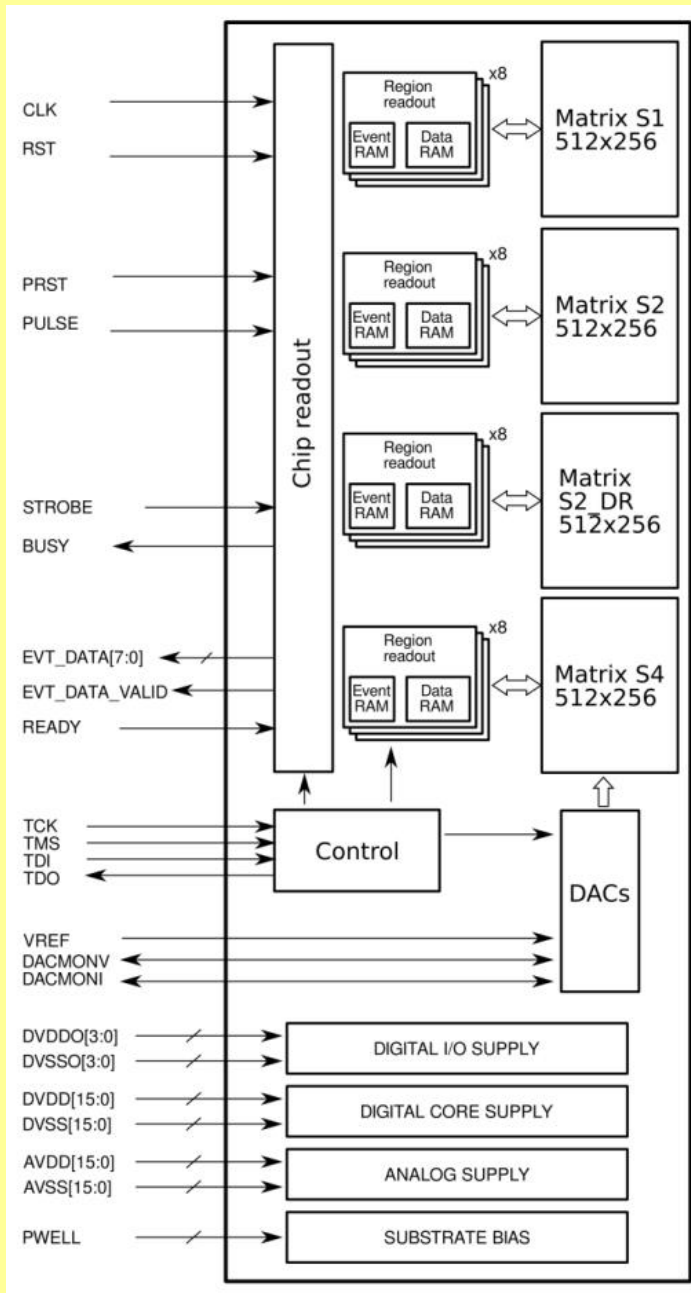
A general block diagram of pALPIDE-1,2

All the analogue signals required by the front-ends are generated by a set of 11 (for pALPIDE-1,2) and 14 (pALPIDE-3) on-chip digital-to-analog converters (DACs).

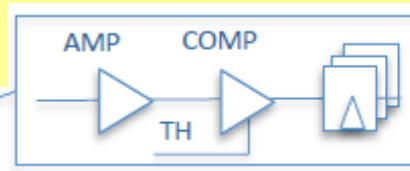
The region readout units contain multi-event storage SRAM memories.

Hit data from the 32 region readout blocks are combined and transmitted on a parallel 8-bit output data port.

A top-level Control block provides full access to the control and status registers of the chip.



ALPIDE chip architecture



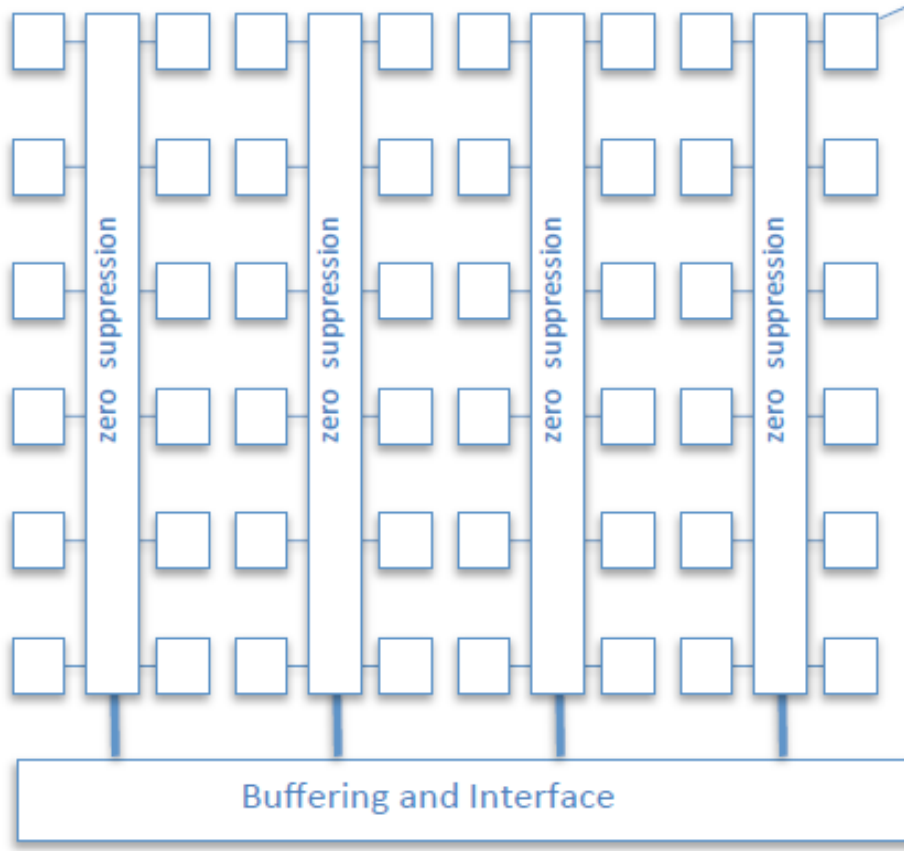
- In-pixel amplification**
- In-pixel discrimination**
- In-pixel (multi-) hit buffer**

Advantages

1. Analog signal is no longer driven over the column lines → reduce power consumption and increase readout speed.

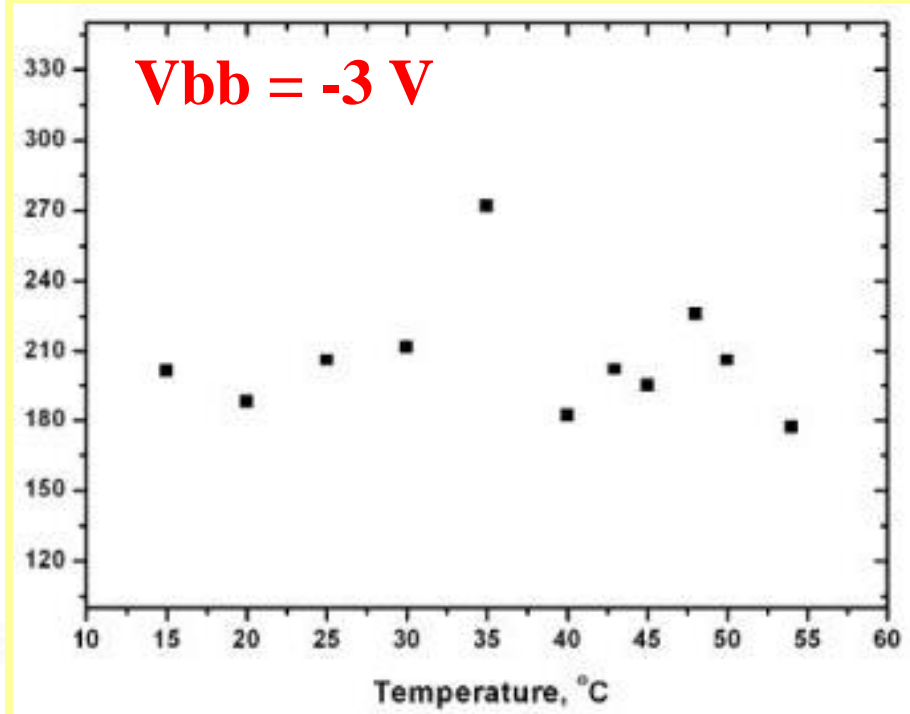
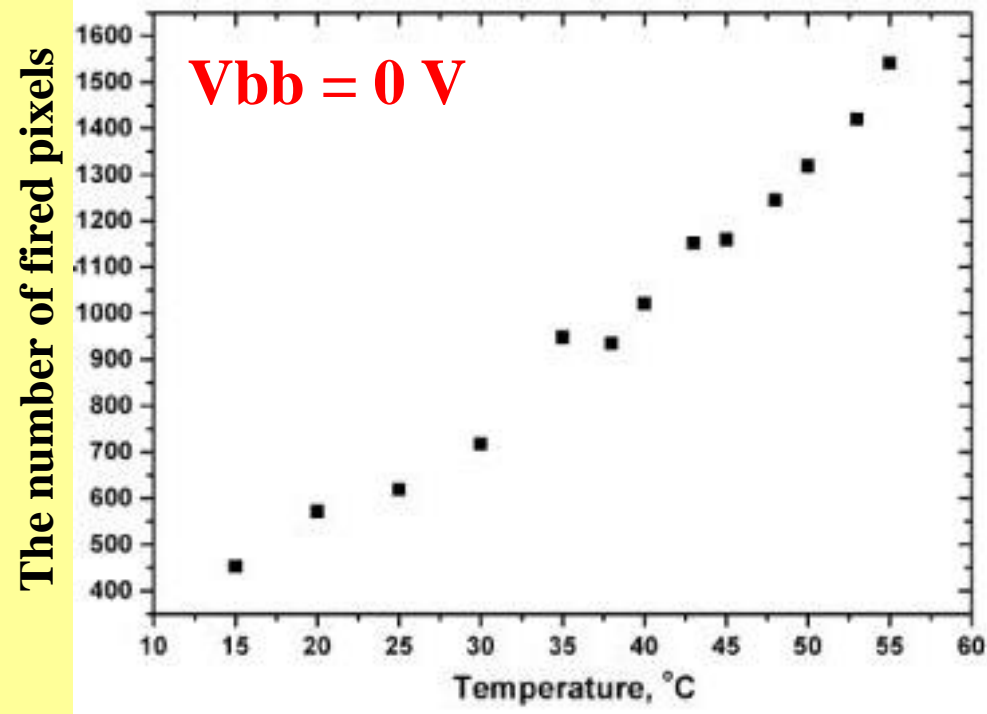
2. The realization of in-pixel discriminators: opportunity of readout, in which the digital outputs of the pixels are scanned by an encoder circuit that directly produces the address of hit pixels as output.

3. The circuit works in a way that the pixel hit register is reset after the read operation and the circuit will move on to the next hit pixel to encode its address. The procedure is iterated until the full pixel matrix is read out.



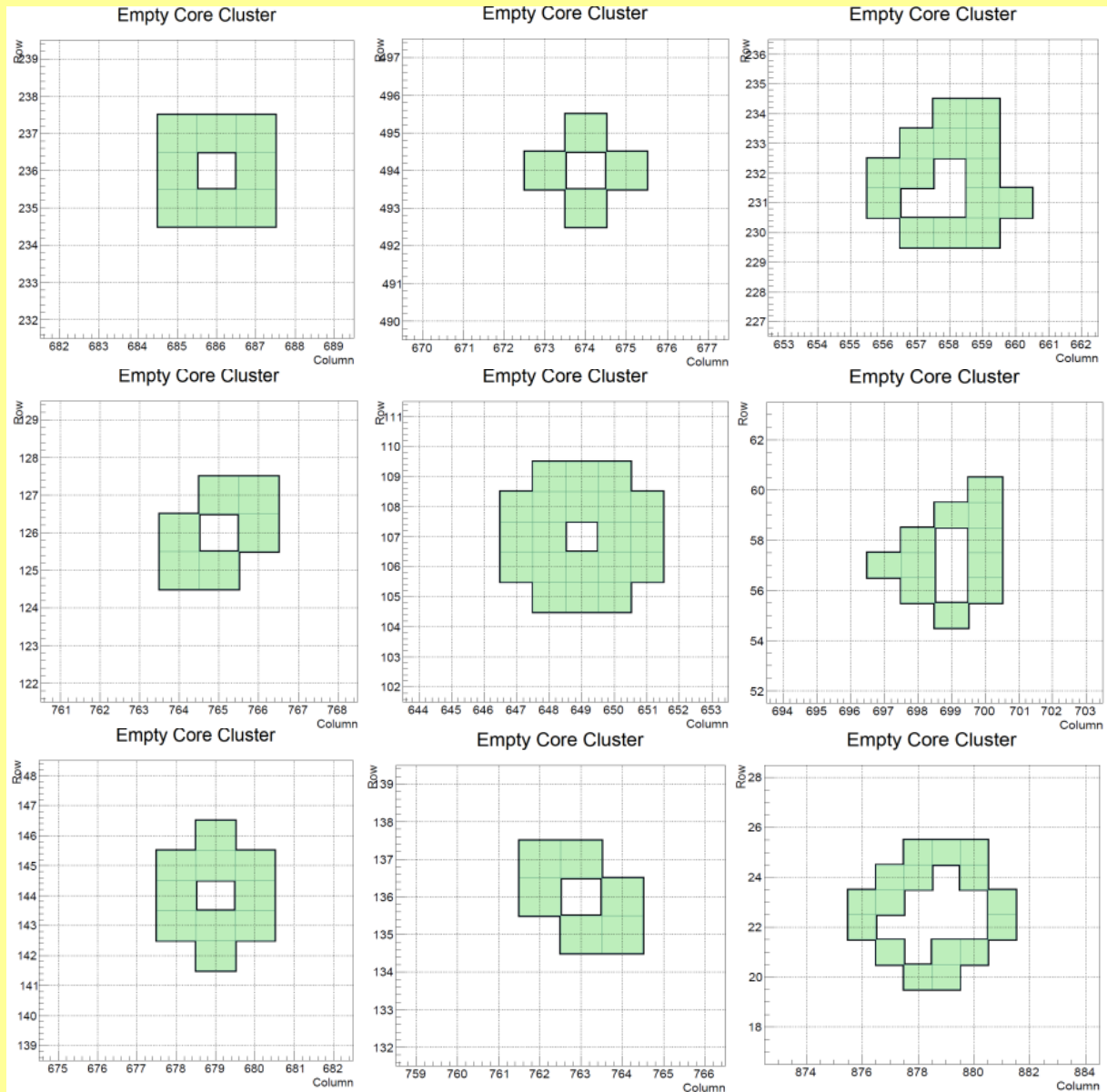
The zero suppression is performed within → the matrix. Address-Encoder Reset-Decoder circuit is employed. It can either be controlled by an **external trigger** signal or operated in **continuous acquisition mode**. ←

Noise characteristics of the sensor and its temperature dependence



The number of the fired pixels strongly depends on temperature
After applying V_{bb} the number of the fired pixels does not change.

Empty core clusters



The empty core cluster analysis has shown that form of such clusters don't depend on a source