Pixel detector for CMS upgrade

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CERN
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Outline

CMS Tracker Phase 2

Requirements, Layout & performance

Subsystems modules & mechanics

Novel technologies

Rad hard Sensors

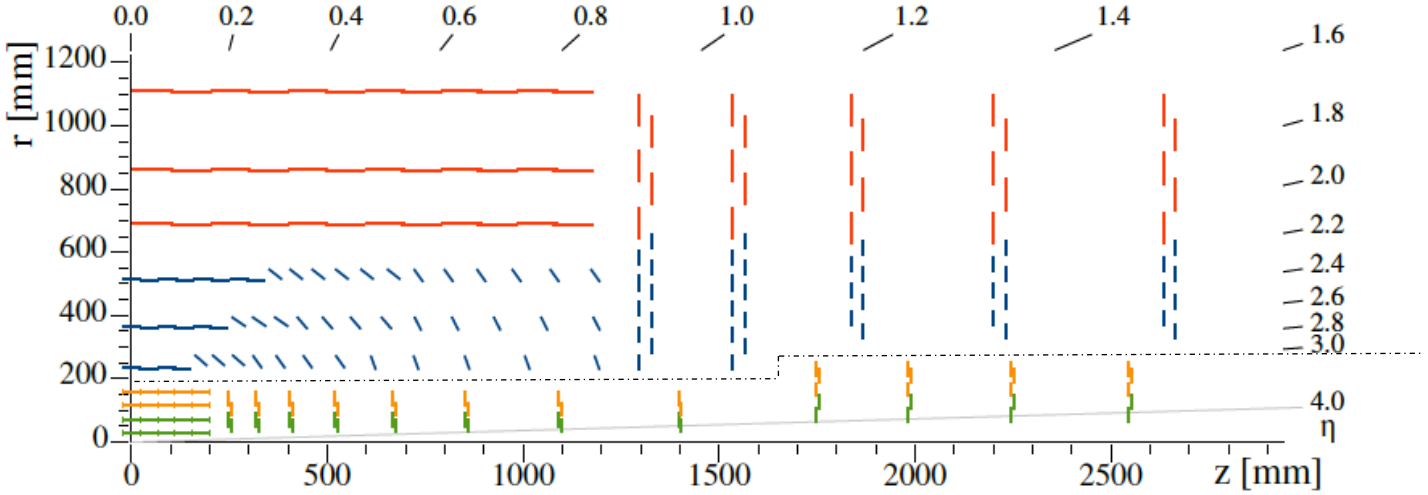
RD53 chip

Serial powering

Light mechanics & CO_2 cooling

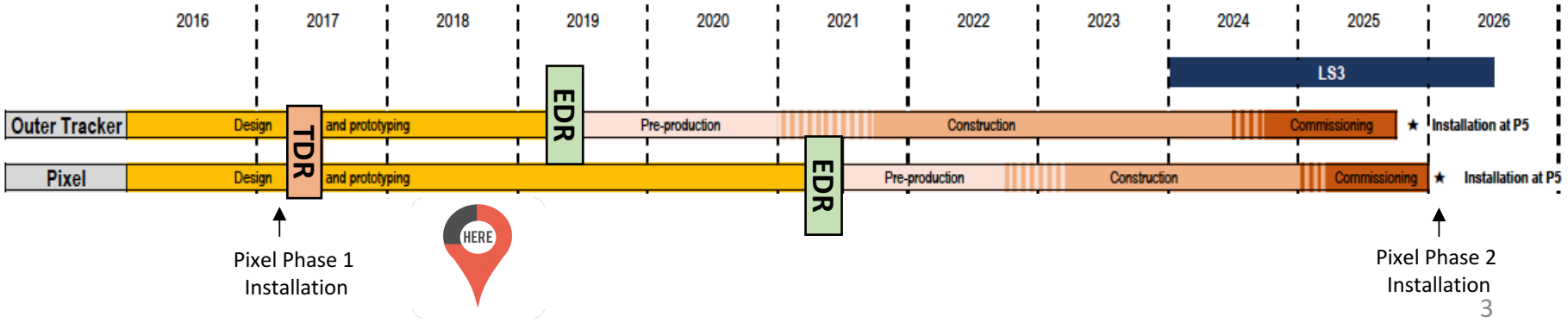
High b/w readout

Tracker Phase 2 Upgrade



Outer Tracker:
Strips
Macro pixels

Inner Tracker:
Pixels

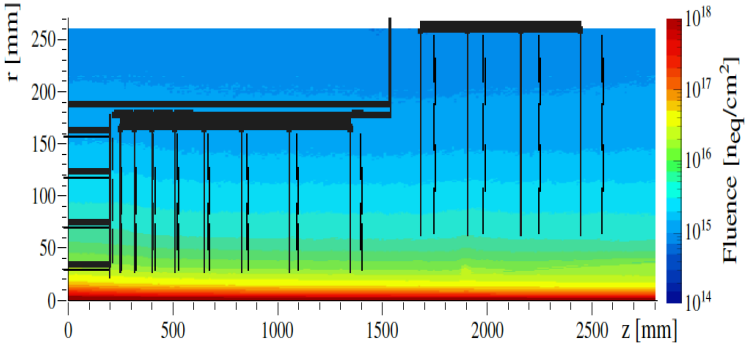


Inner tracker Phase 2 requirements

Objective:

Maintain or improve tracking capability with 200PU

- Increase granularity
- Reduce material
- Increase coverage



Innermost layer: 2.3x10^{16} n_{eq}/cm^2
Outer & Service cylinder: 10^{15} n_{eq}/cm^2

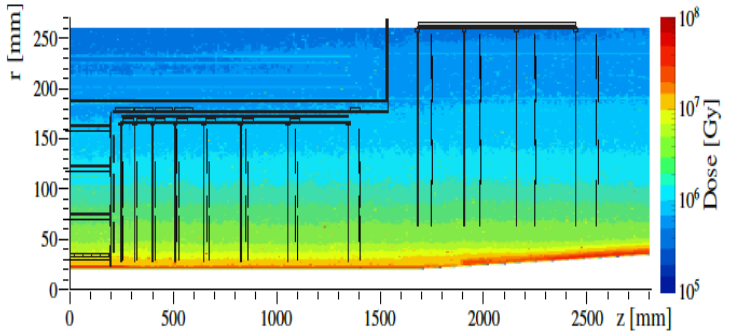
Challenges:

Unprecedented radiation levels for 3000 fb^{-1}

Increased hit rate (3.2 GHz/cm^2),

trigger rate 750 kHz & latency 12.5 us

- Multi-gigabit data transmission
- Large on chip buffering



Innermost layer: 1.2 Grad
Outer & Service cylinder: 100Mrad

Inner tracker Phase 2 requirements

Objective:

Maintain or improve tracking capability with 200PU

- Increase granularity
- Reduce material
- Increase coverage

Pixel Chip & Sensor 250 µm^2 : 2 billion pixels

Serial powering, CO_2 cooling, Light mechanics

New layout extended to |η|=4

Challenges:

Unprecedented radiation levels for 3000 fb^{-1}

10x Rad Hard Electronics & Sensors

Repairable/extractable detector

Increased hit rate (3.2 GHz/cm^2),

trigger rate 750 kHz & latency 12.5 us

- Multi-gigabit data transmission
- Large on chip buffering

RD53 Pixel Chip 65 nm

Light Fast Readout Links

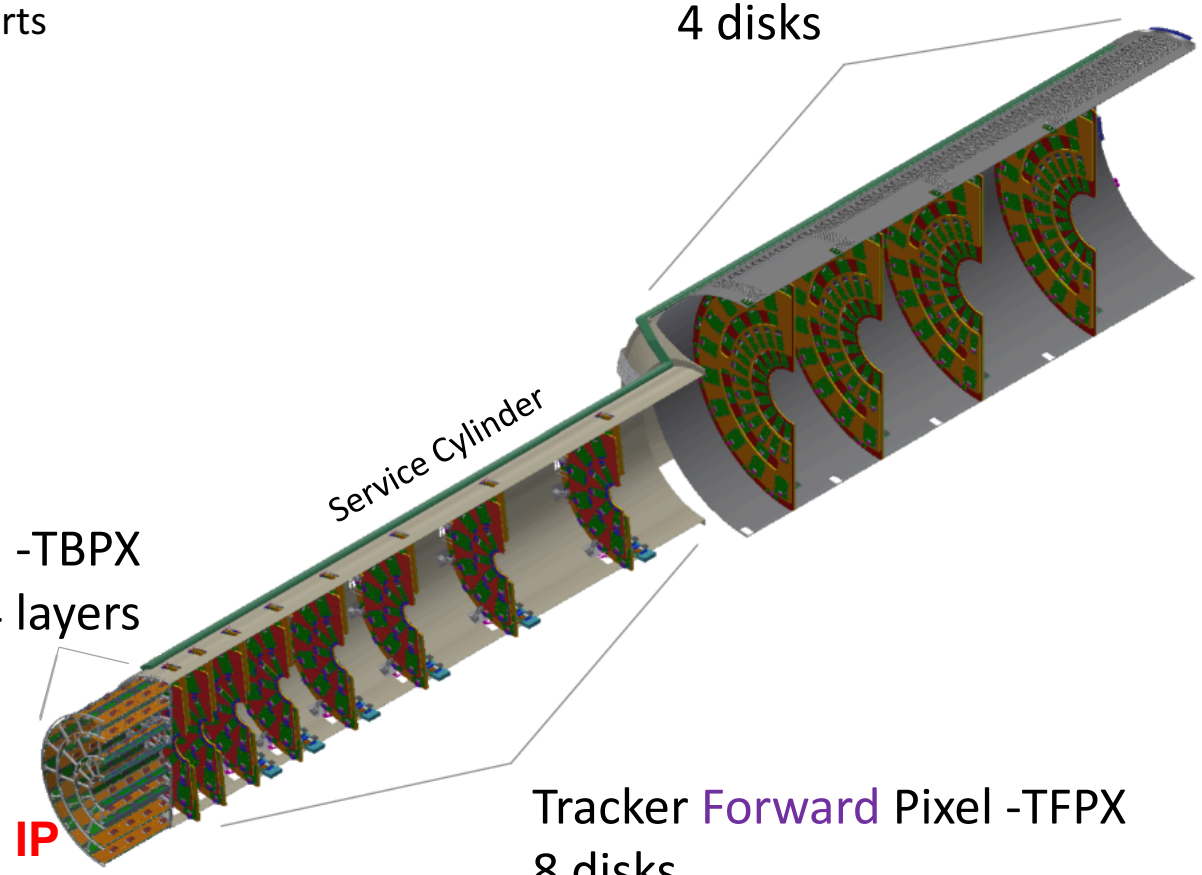
Optoelectronics & DAQ

¼ CMS Inner Tracker

Simple mechanics
no turbines-tilted modules

Simple installation/removal
for potential replacement/repair of parts

Tracker Extension Pixel -TEPX
4 disks



Tracker Barrel Pixel -TBPX
4 layers

Tracker Forward Pixel -TFPX
8 disks

Inner Tracker Layout: Extension to |η|= 4

Hybrid technology

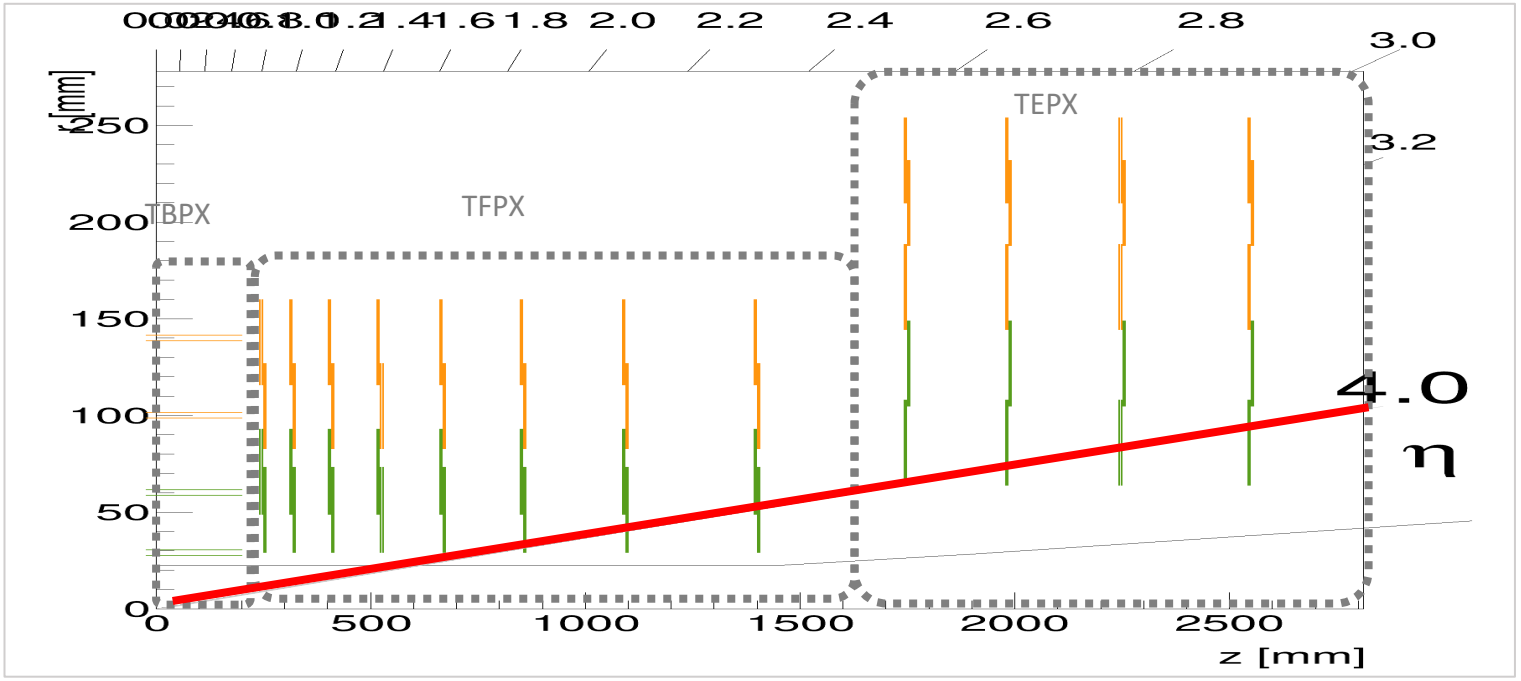
Total active surface of **~4.9 m²**

Optimization for production of **4k modules**

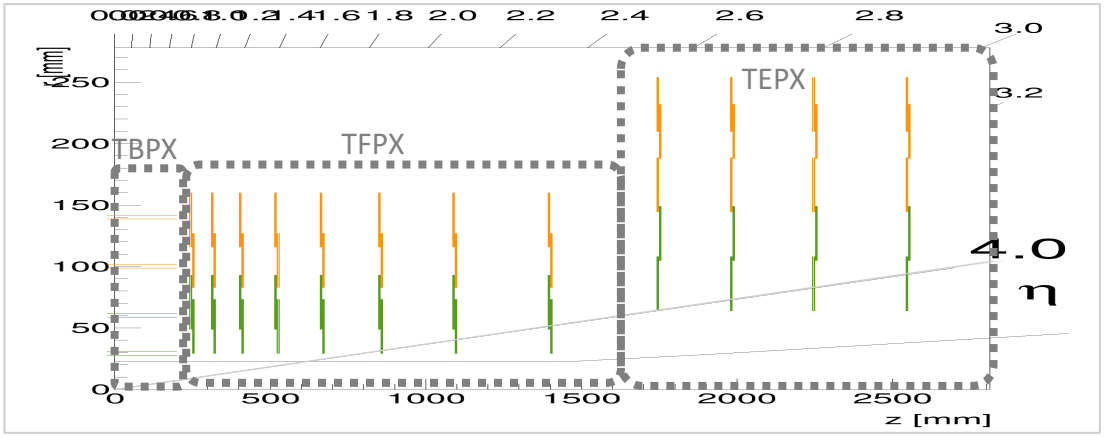
Minimal number of different module types:

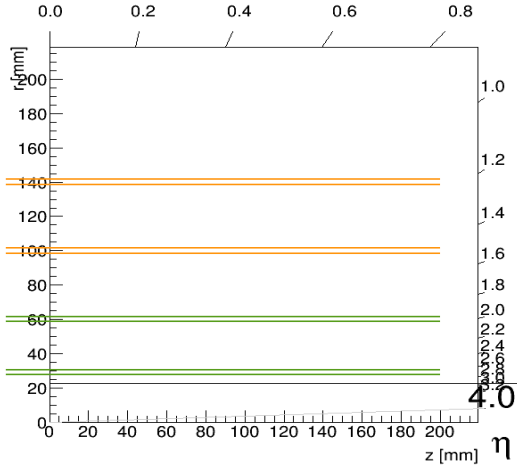
1x2 ROCs modules (inner parts)

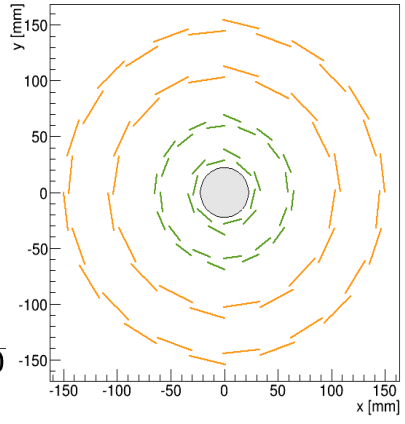
2x2 ROCs modules (outer parts)



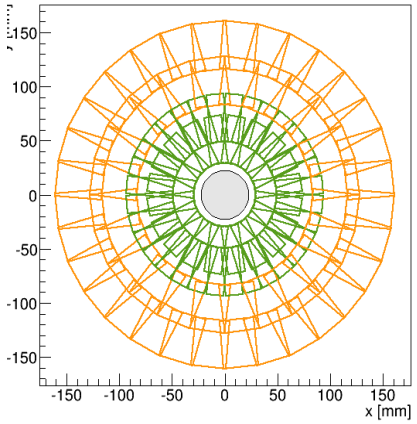
Inner Tracker Layout: Extension to |η|= 4



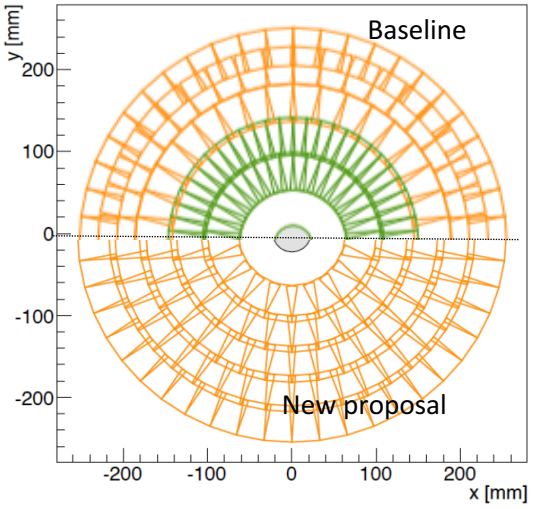




TBPX: 4 layers
4/5 modules per ladder



TFPX: 8 disks/end
4 rings/disk

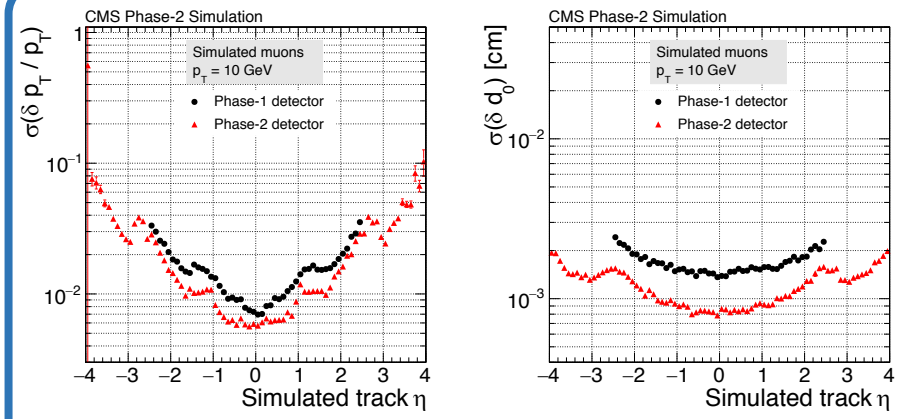


TEPX: 4 disks/end
5 rings/disk

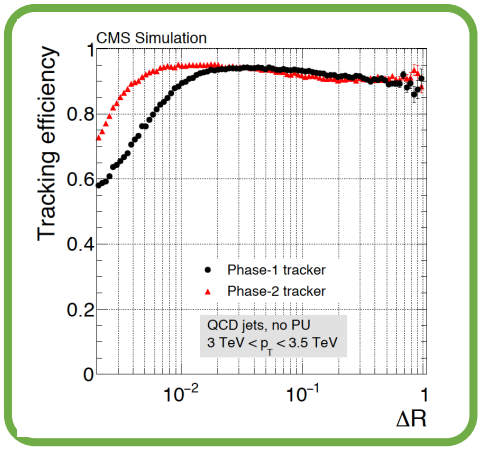
Overlaps both in r and r-ϕ
Hermetic coverage

Performance highlights

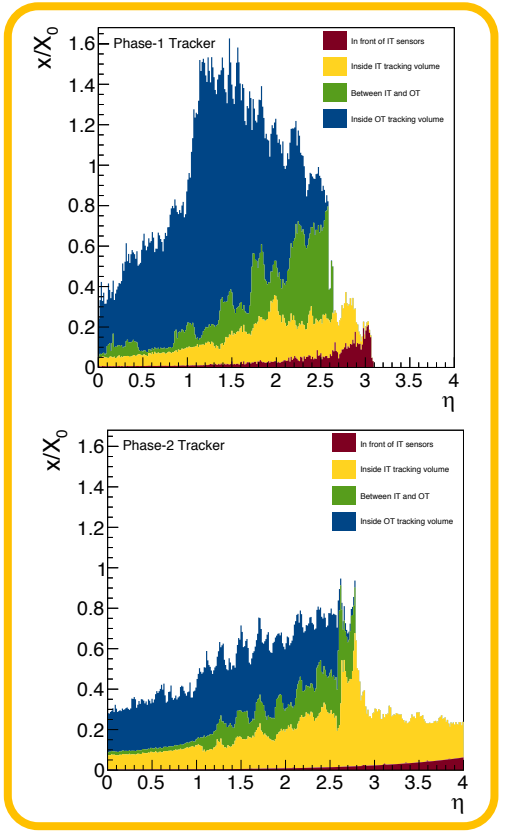
Improved resolution



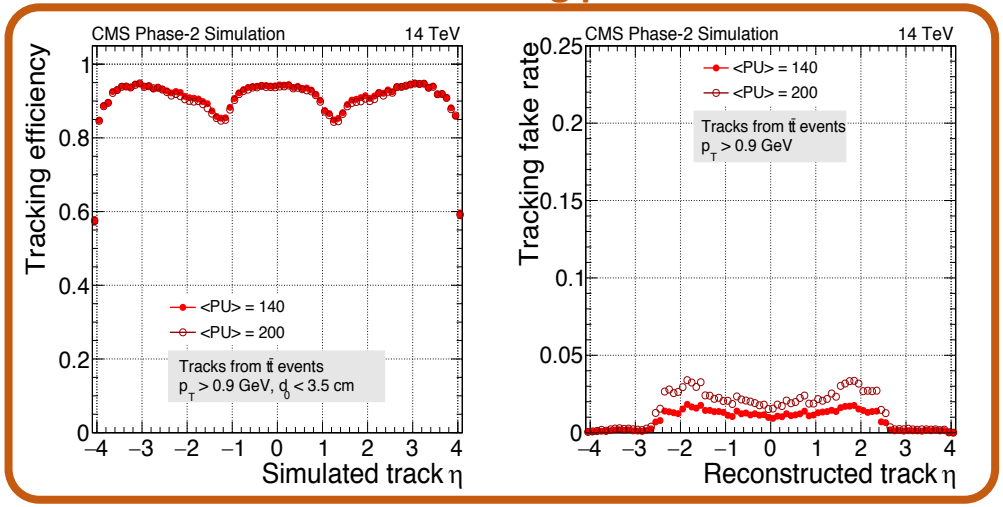
Improved efficiency in high pT jets



Reduced material budget

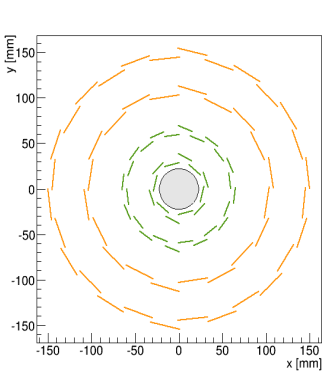


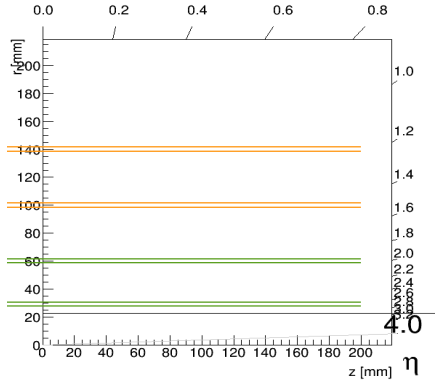
Robust track finding performance



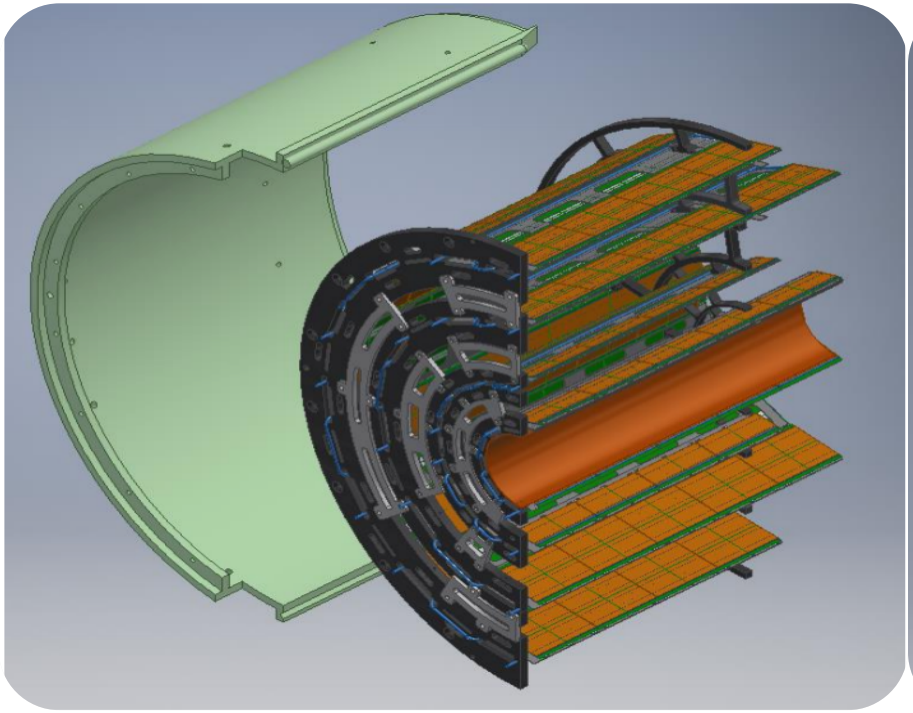
Closer look to TBPX, TFPX & TEPX

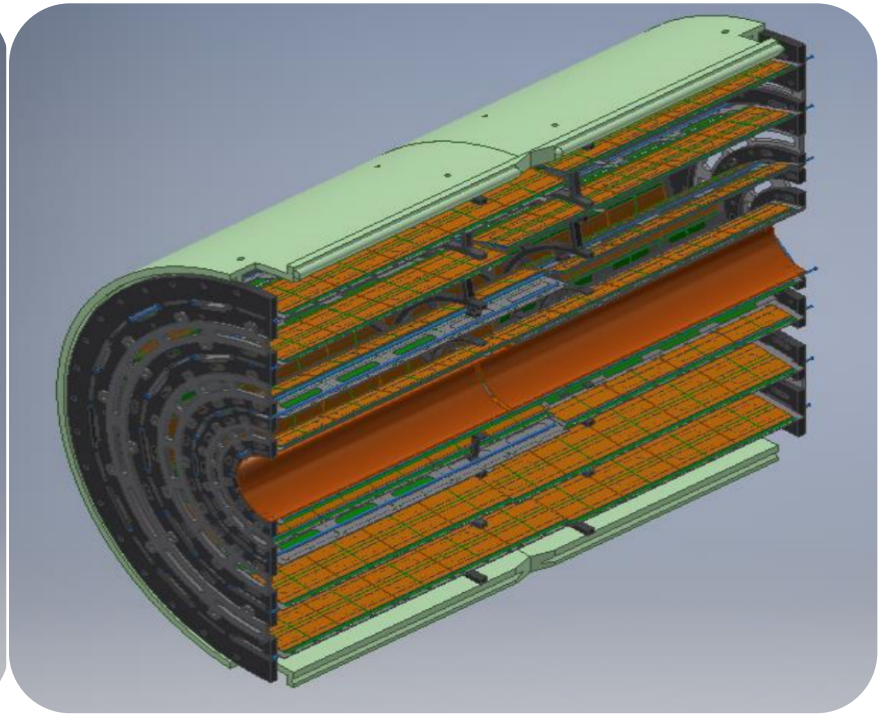
TBPX Mechanics





Layer 1@ 30 mm
Both faces of ladders loaded with modules
no |η|=0 projective gap





New way to split in 2 parts along z: 4 or 5 modules per layer (interleaved)

TBPX modules

High-Density Interconnect (HDI) to distribute signals and power to/from module

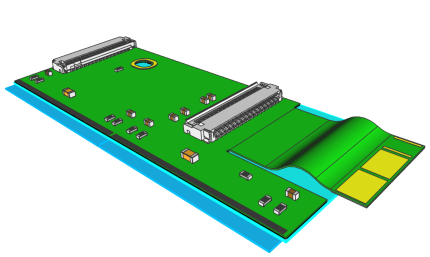
Simple module:

Pixel chip is the only active component

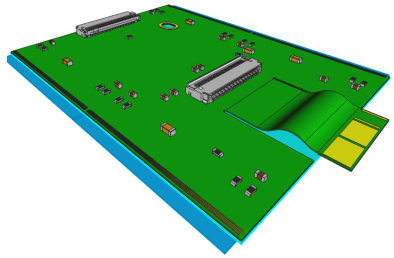
No auxiliary electronics

Passives: **decoupling caps** and **connectors**

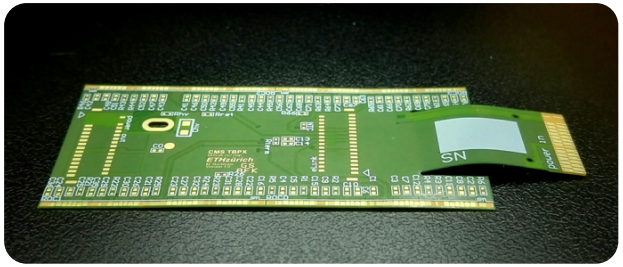
Wire bonding



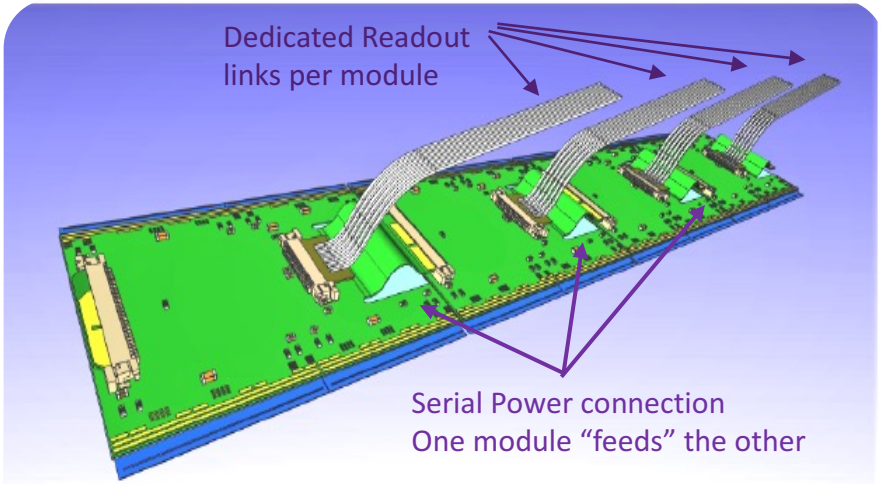
1x2 ROC module



2x2 ROC module



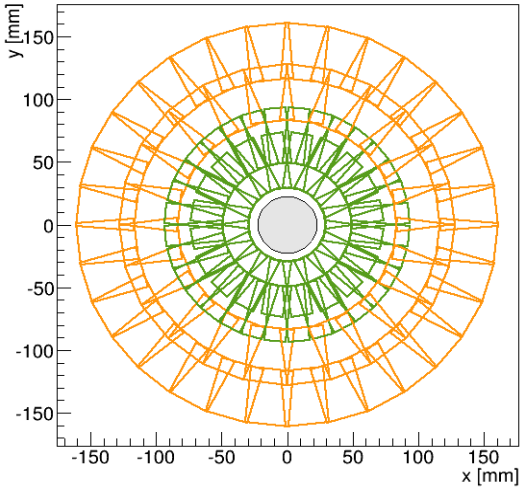
Prototype 2x2 HDI for RD53A chip (2018)

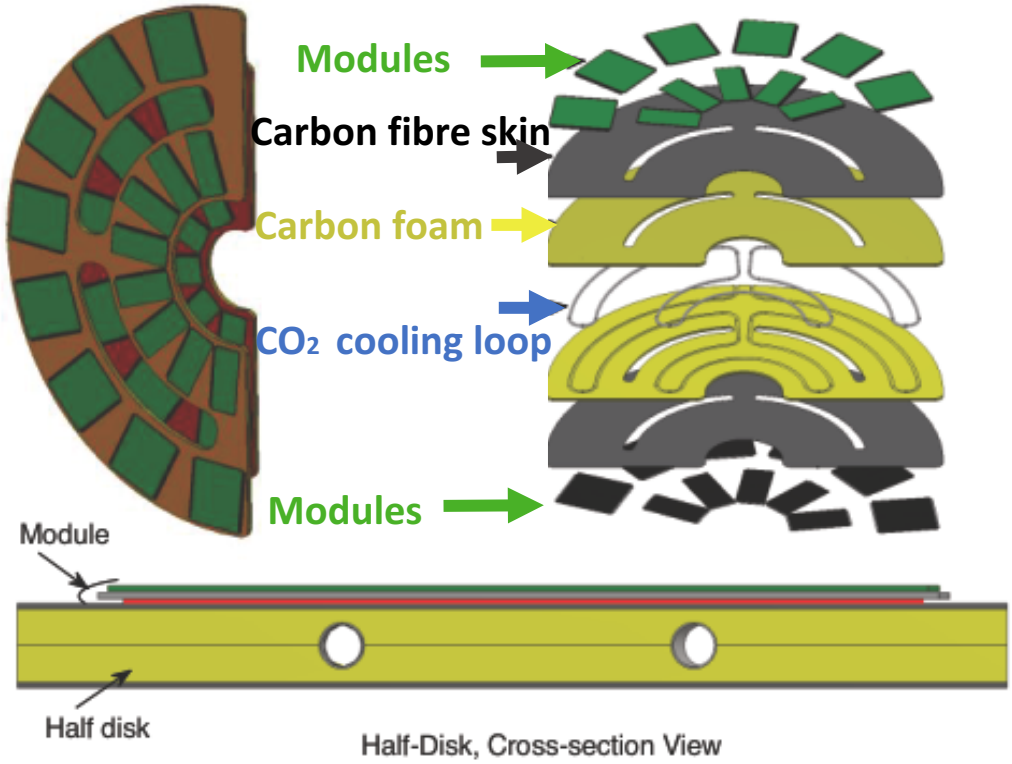


TFPX Dee

A ½ disk is composed of two Dees:
Odd dee: Ring 1+Ring 3
Even dee: Ring 2+Ring4

Modules of arranged on both sides of a dee- "sandwitch" structure





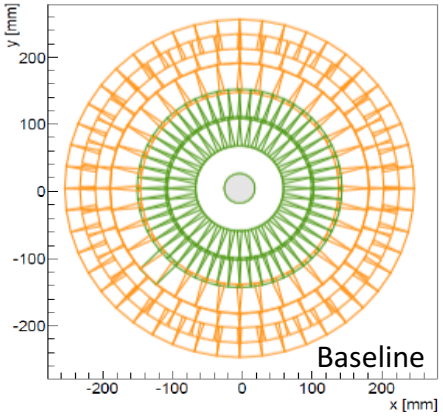
Half-Disk, Cross-section View

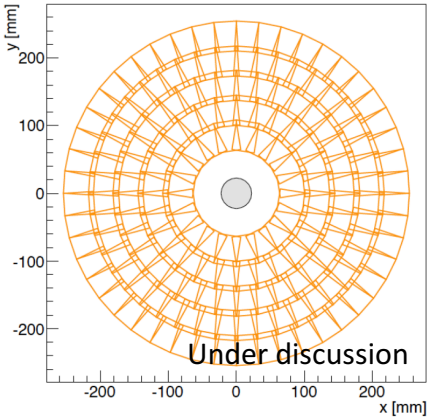
TEPX Dee & Luminosity measurement

Recently proposed layout wrt baseline uses one type of modules (2x2)

Alternative assembly wrt TFPX under study:

A ½ disk is composed of two identical Dees:
Each Dee:
Front side: Ring 1+Ring 3+Ring 5
Back side: Ring 2+Ring4

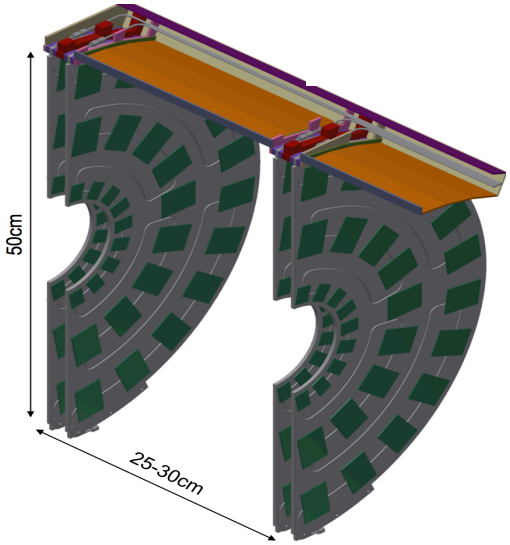




Luminosity measurement

10% extra triggers provided to TEPX to provide online BX-by-BX LUMI measurement

TEPX D4-R1 dedicated to LUMI/ BKGD – requires independent operation



1/8 of TEPX system:
2 ½ disks

Novel technologies and methods

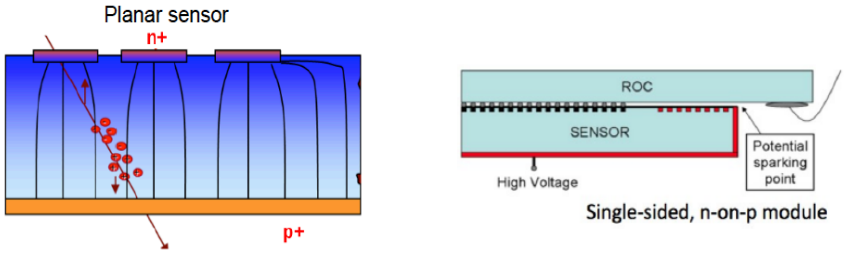
Pixel Sensors: R & D towards 1E16 range

Thin Planar n-in-p sensors:

Optimal d~100 - 150 µm- lower signal unirradiated

Main challenges:

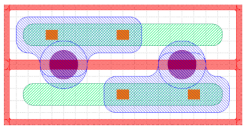
spark protection, limited space for structures, radiation



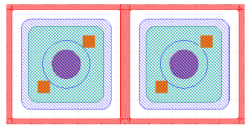
Small pitch pixel cells

Aspect ratio under study:

25x100 µm² (baseline)



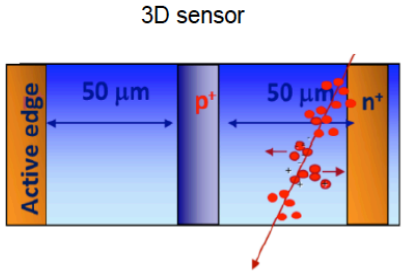
50x50 µm²



3D sensor:

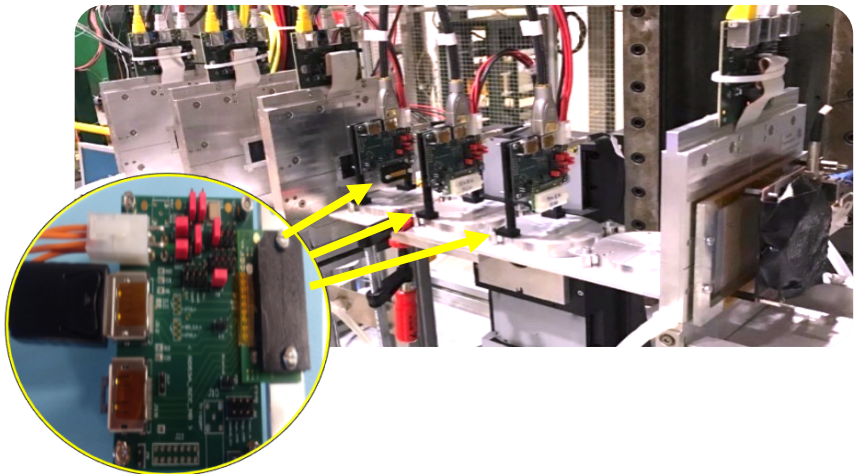
Option for TBPX L1/TFPX R1

Main challenge: complex fabrication



CMS sensors bump-bonded to RD53A chips allows to test to required radiation levels:

Light carrier board for irradiation campaigns (**88 sensors**) and tests beams in 2018-2019



Next generation pixel chip: RD53 chip

RD53A chip (½ size of final chip)

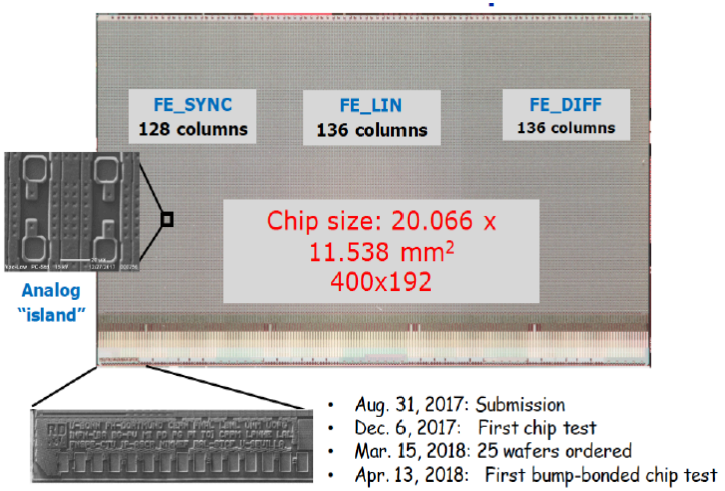
Design features:

50 x 50 µm^2 pixels

3 AFE, 2 digital architectures

Shunt-LDO for serial power

4***1.28 Gbps** output links – 1 ***160 Mbps** control link



Active test program:

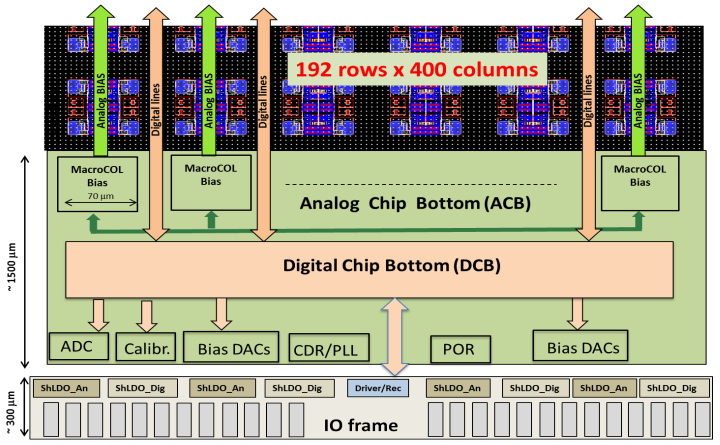
- **Chip is fully functional**
- **Meeting 500 Mrad tolerance specification**
  - Could reach 1 Grad (controlled conditions)?
- **All AFE show good performance with radiation**
  - Low Threshold < 1000e-

AFE review planned for Dec 2018

Working already on RD53B design

CMS final chip submission: Summer 2019

RD53A functional floorplan



Serial Powering of CMS pixel modules

Future pixel CMS detector requires ~50 kW on-detector power:
Increased number of channels and low voltage CMOS technology

Serial powering is the only viable solution for powering Phase 2 pixels:

- ✓ Low mass
- ✓ Integrated on-chip solution: Shunt-LDO regulators
- ✓ Radiation hard
- ✓ Not sensitive to voltage drops
- ✓ Smooth Operation with low noise

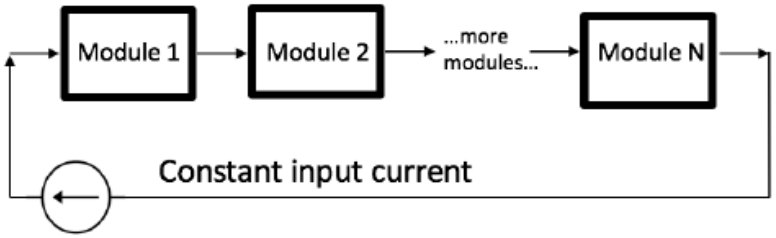
... never attempted before in a HEP experiment!

Across-module serial powering:

Iin "re-used" among loads in series
Total current constant- independent of actual I_{load}

Enough current injected to satisfy highest I_{load}
Any extra current, not used by load, gets burnt by shunts

Modules/ sensors grounds differ inside a chain



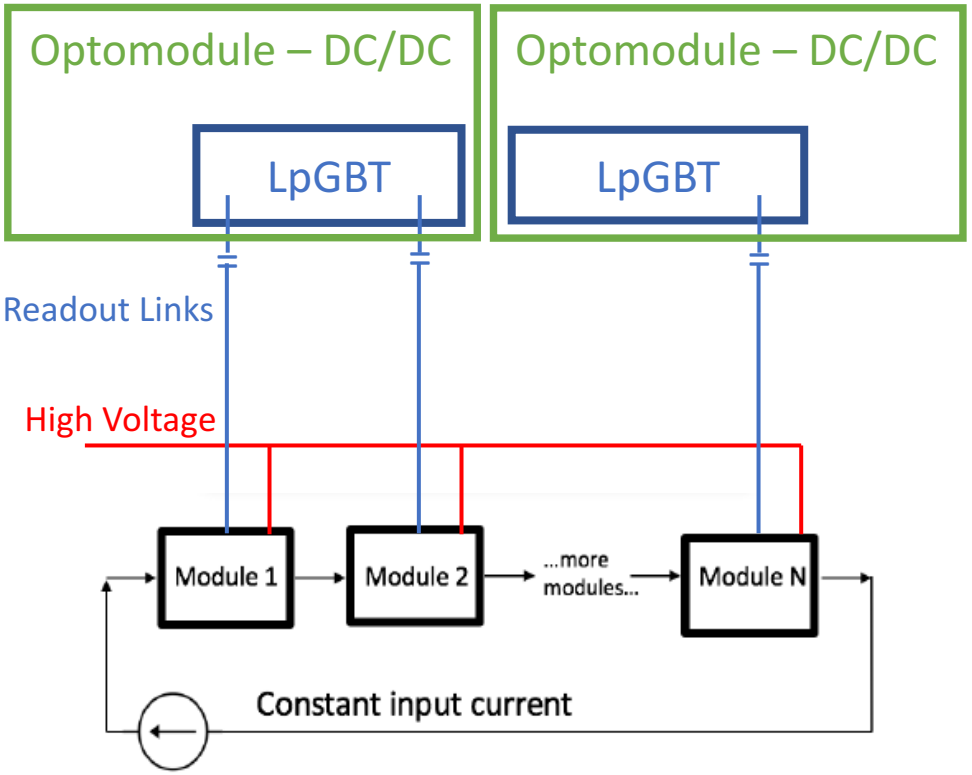
Serial Powering: challenging system issues

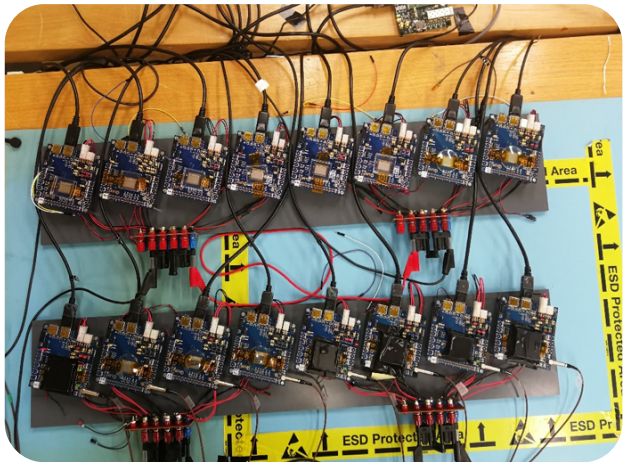
CMS serial powering system parameters:

Up to 11 pixel modules serially powered – 3D sensor chains will be shorter

Chips in a module (2 or 4) powered in parallel

~530 Serial power chains to power ~4k pixel modules





System test:
Successful operation of Serial power chain of 8 single RD53A modules and 8 RD53A chips for HV studies (8x2)

Shunt-LDO integration & hotspot

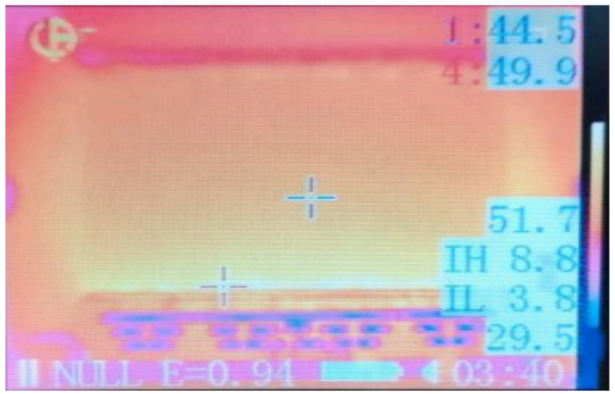
A full size pixel chip (440x328 pixels) would require 1.62 A @1.5V under normal operating conditions

Two specialised 2.0 A Shunt-LDO regulators integrated on-chip, one per power domain

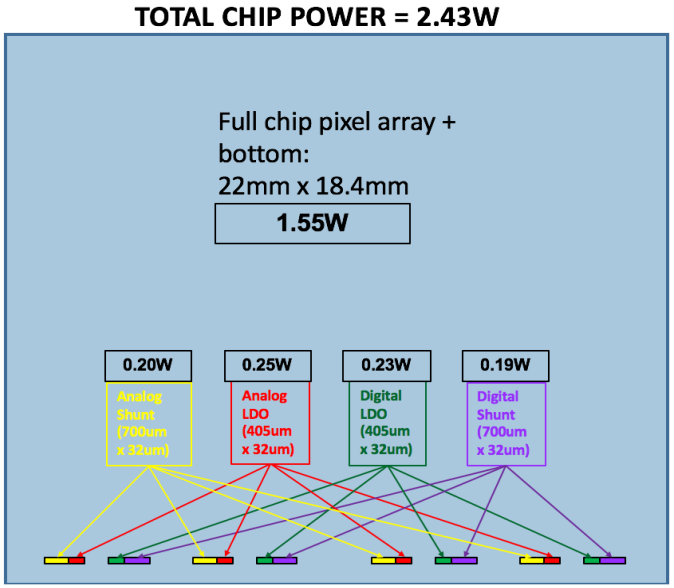
Each Shunt-LDO split in **4*0.5A blocks** for heat distribution and reliability

Nominal value: 25% current margin creates hotspot

NB! Cooling pipes below/close to Shunt-LDO hotspot



Picture of RD53A with thermal camera for Iin=2.0A, Vin =1.45V (2.9W)



CMS pixel chip nominal power dissipation

Light Mechanics & CO_2

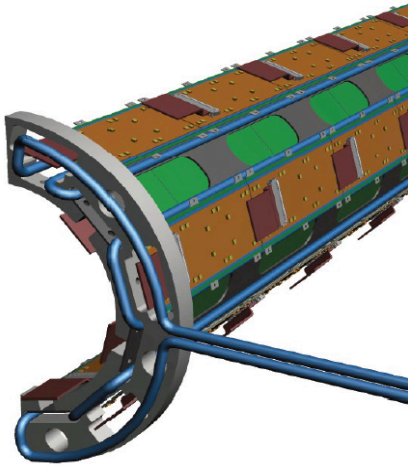
Light Carbon Fiber support structures

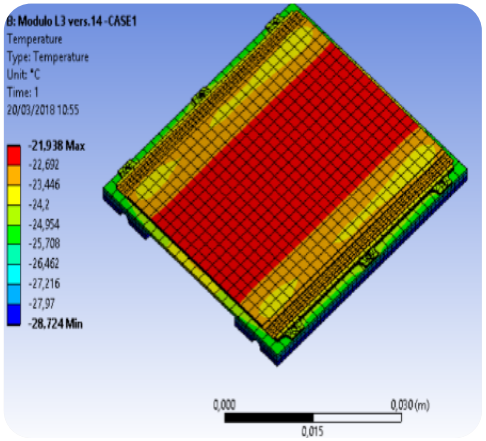
Low mass CO_2 evaporative cooling
removes heat generated on the module to operate sensors below -20°C

Cooling pipes below chip hotspots
Optimizing cooling parameters based on extensive thermal simulations

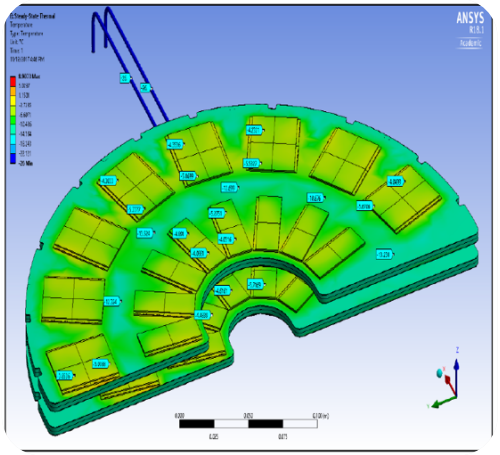

Prototype TFPX Dee


Prototype service cylinder piece


TBPX L1 cooling pipes driven below the chip hotspots



Example of TBPX L3 module thermal modelling

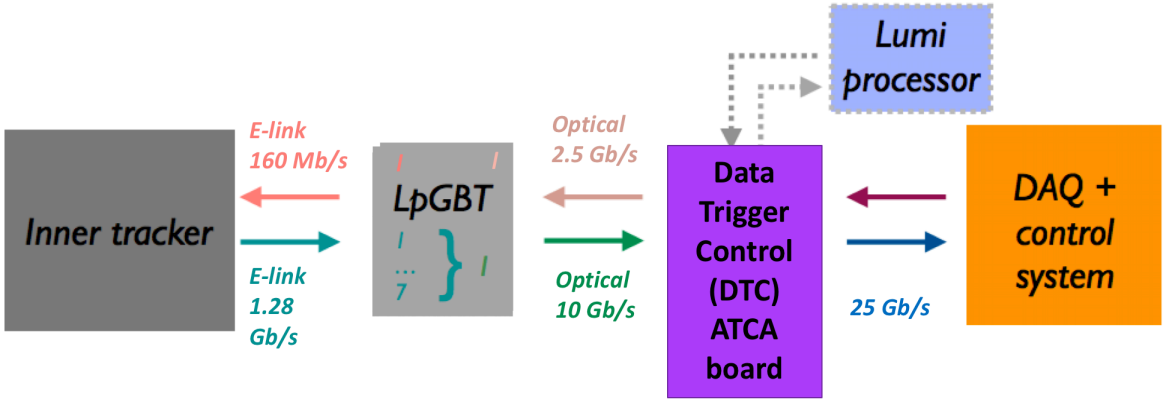


Sample TFPX Dee thermal simulation

High-B/W Readout chain

Up-links:
data from L1 accept, monitoring info to DAQ and control system

Down-links:
clock, trigger, commands, configuration data to modules



Up to 6 electrical up-links @1.28 Gb/s per module to LpGBT

Modularity depends on hit rate (location)
Efficient data formatting to reduce data rates (factor ~2)
25% bandwidth headroom on e-link occupancy

One electrical down-link @160 Mb/s per module from LpGBT

28 DTCs boards required for CMS IT:

Each DTC has two "half-DTC" FPGAs, each of which can receive up to 36 fibers.
Each "half-DTC" would be capable of sending 200 Gbps to DAQ.

Optomodules & integration

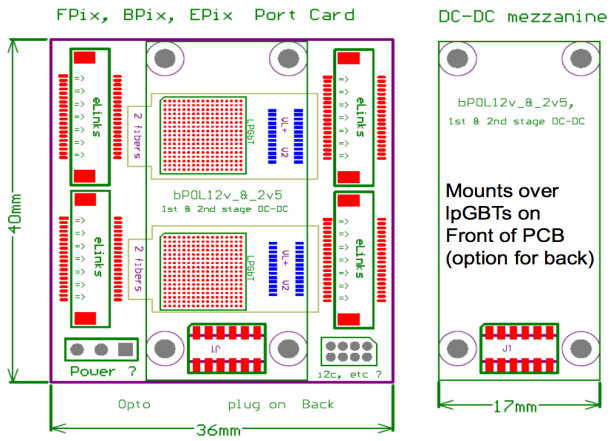
Optomodule (aka portcard) designed in 2018:

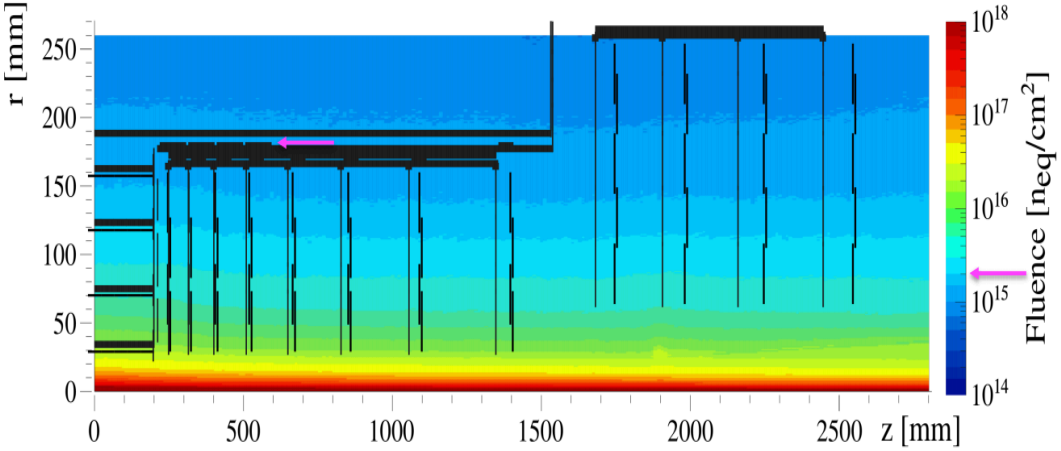
2 Low-power Gigabit Transceiver (LpGBT)

2 Versatile Link+ (VL+)

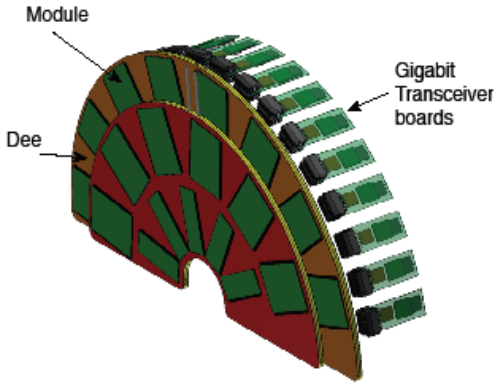
powered by a pair of DC-DC converters

~750 optomodules to readout/control CMS IT





Optoelectronics limits (1E15 n/cm^2 fluence, 100 Mrad) impose their integration at higher radii



TFPX Optomodules located @outer radii of a Dee

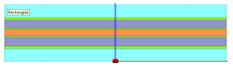
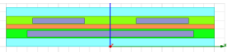
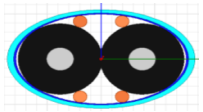
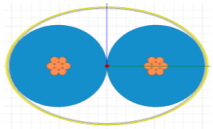
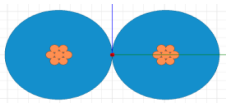
Low mass Electrical links

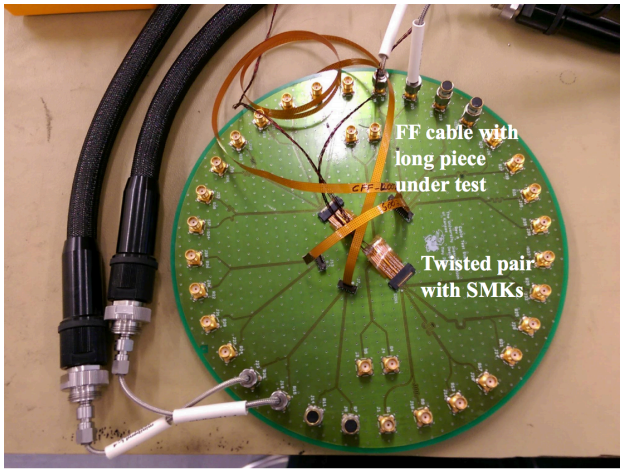
~7k readout + 4k control differential electrical links (e-links)

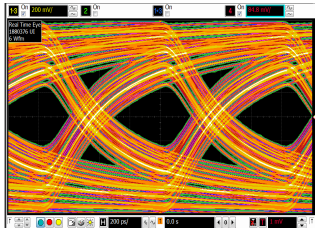
AC- coupled e-links due to serial powered modules

Various e-link options investigated with simulations and tests:

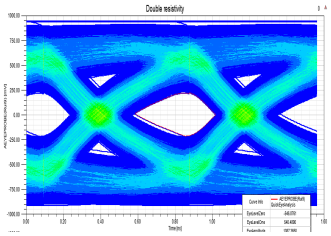
- Flex and twisted pair: 0.1 – 1m
- Objective: Minimize mass for acceptable cable losses
- Studying: Pre-emphasis, Cross coupling, Eye-diagrams

Image of the cable	Cross section for simulation in Q3D
A. 	
B. 	
C. 	
D. 	
E. 	





Alu flex measurement



Alu flex simulation

Summary

Many challenges for Phase 2 pixel detector & many **ongoing developments**:

❖ **New layout with extended forward coverage:**

- Ongoing **TEPX layout** under optimization incl. LUMI measurement

❖ **Electronics:**

- Radiation hard ROC
- Demonstrator RD53A chip working, used for sensor R & D
- Preparing for **final CMS pixel** chip submission

❖ **Sensor R & D**:

- **Ongoing campaigns**
- Investigating thin planar sensors structures, 3D for inner layer/ring, pixel aspect ratio

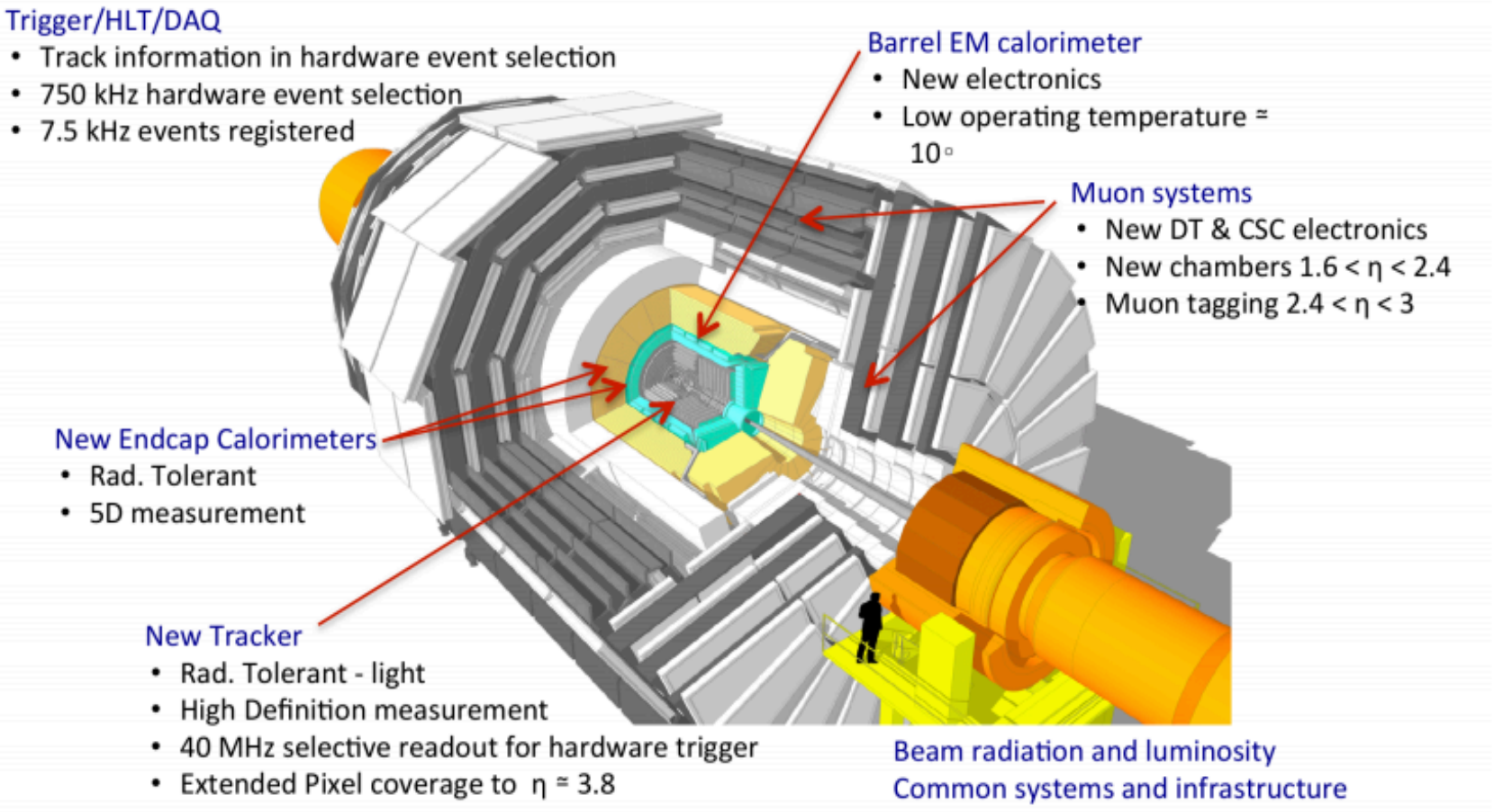
❖ **Novel methods: Serial powering, CO_2 cooling, light stuctures, easy installation**

- **Serial power chains** of RD53A modules**,** **thermal modelling** of modules, **first prototype structures**

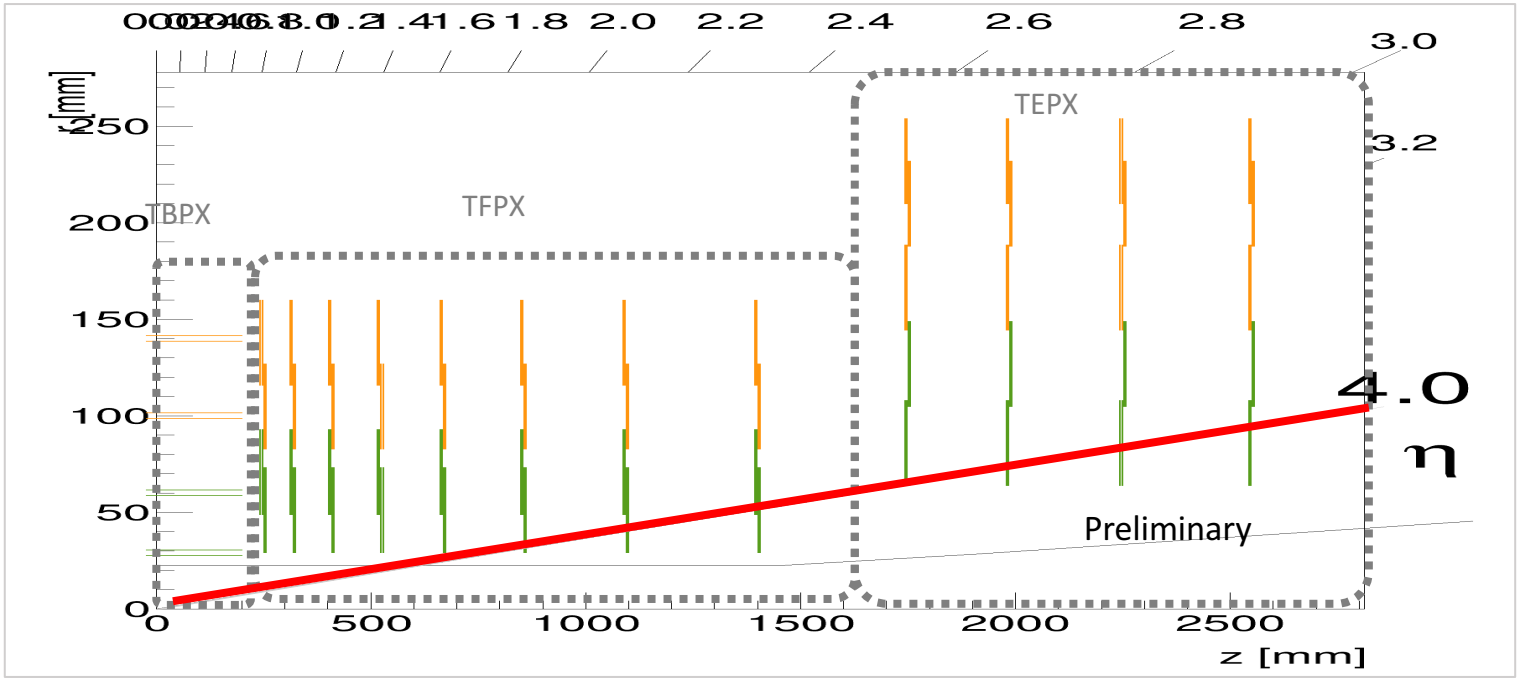
❖ **New DTC board, optoboards and e-links development**

Extra slides

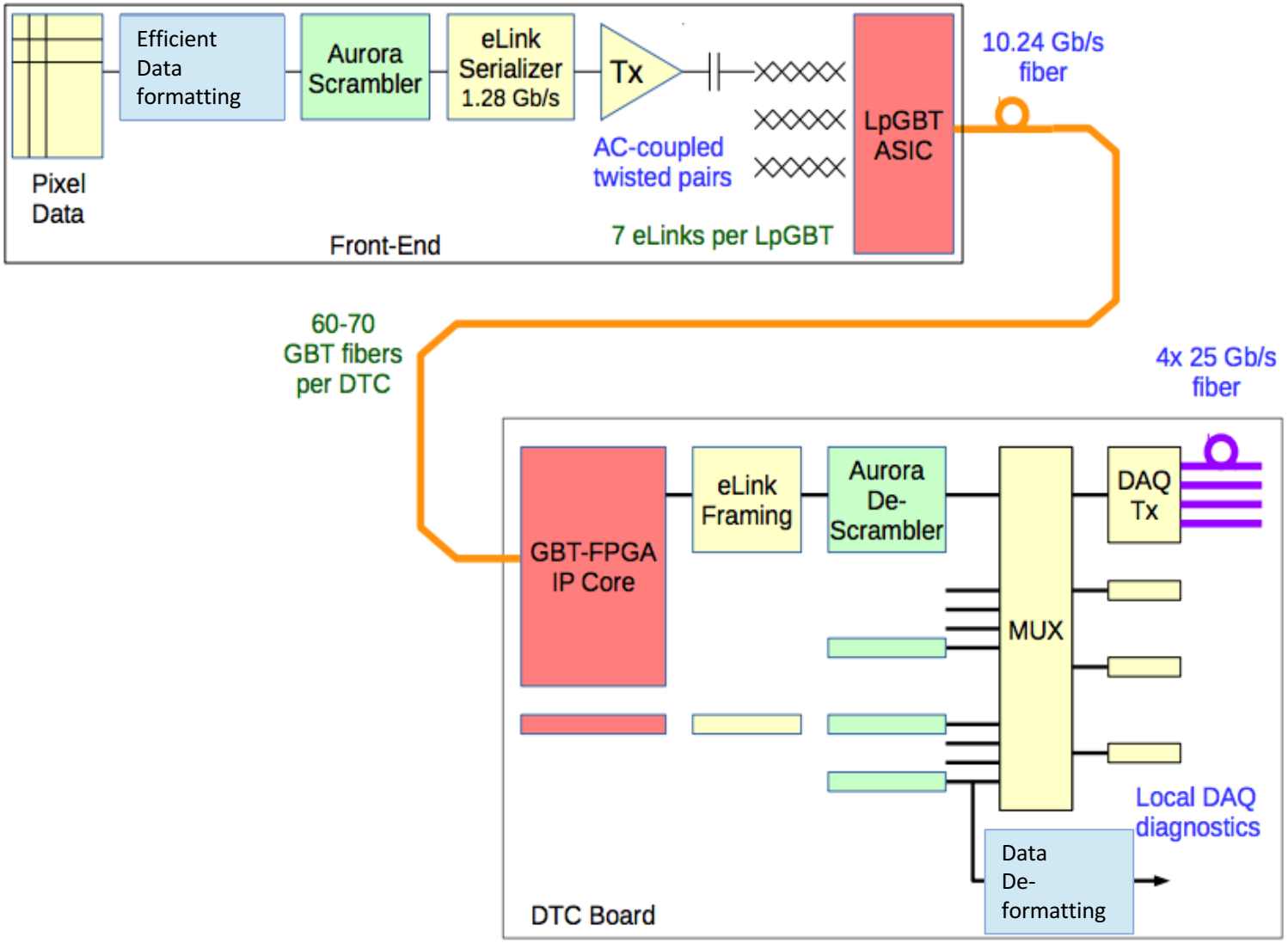
CMS Phase 2 upgrades



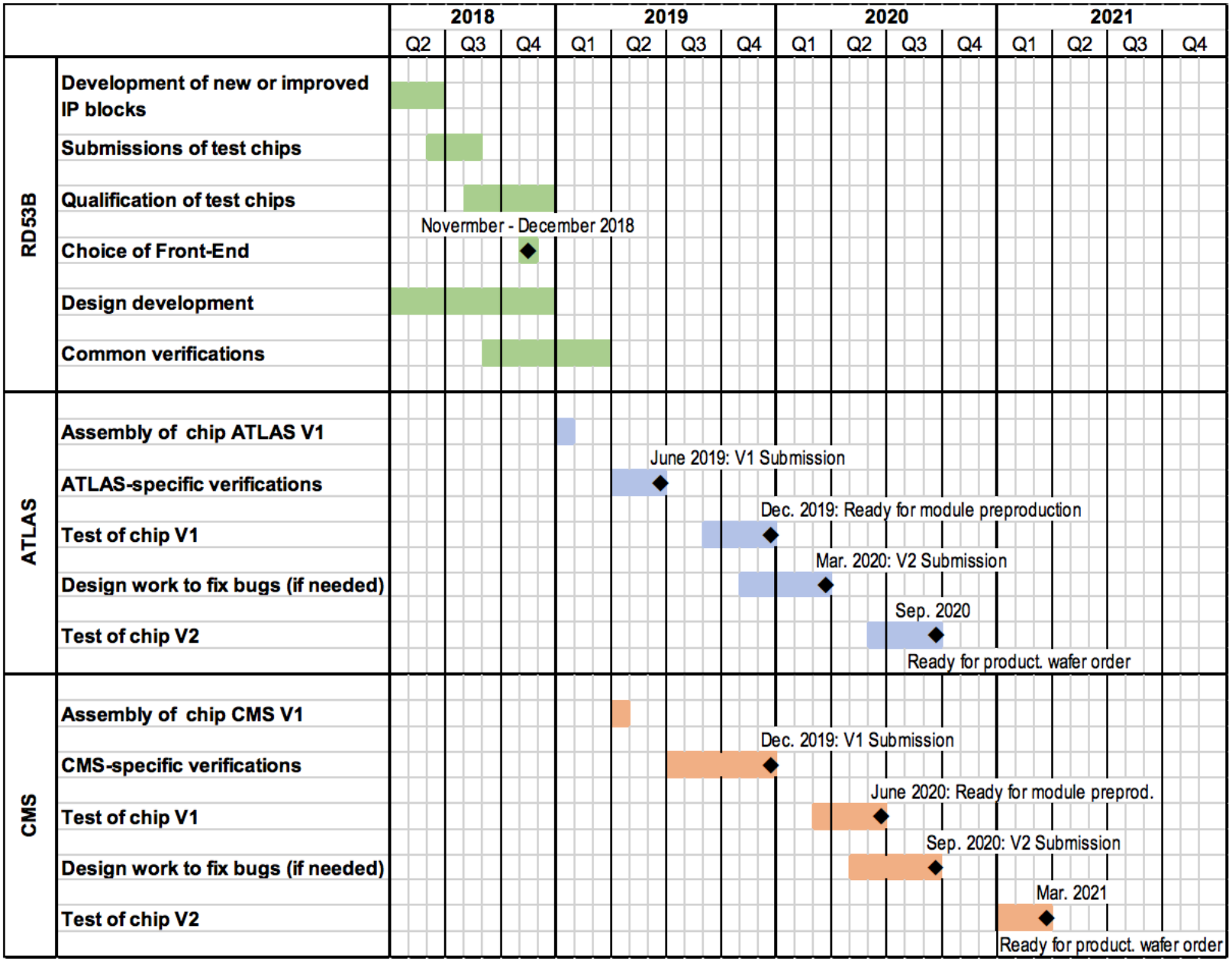
Inner Tracker Layout- Baseline



Readout chain- protocols



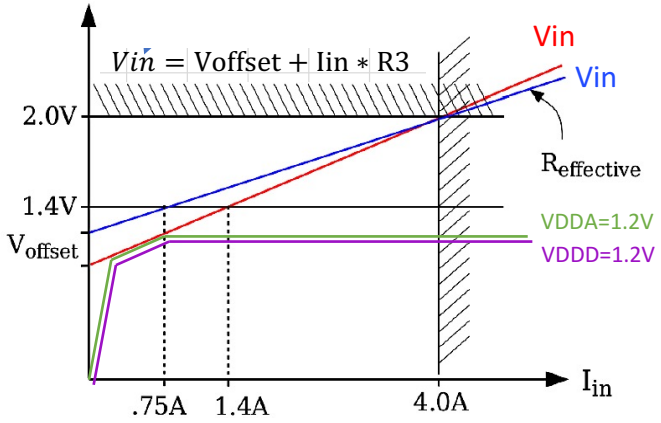
RD53B timeline



RD53A Shunt-LDO Resistive model

Shunt-LDO designed to make power load look like resistor with voltage offset.

- **Critical for appropriate current sharing between parallel chips and stable operation of serial powering.**
- Power consumption variations inside chip not “visible” from outside.
- Shunt current dynamically regulated to keep chip current constant.

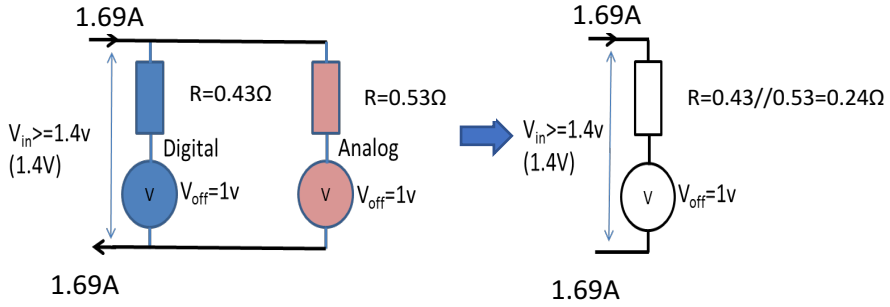


Shunt-LDO Parameters:

- Drop-out voltage (min 0.2V)
- Effective resistance
- Configurable offset
- Extra headroom is user’s choice (10%, 20%, etc.)

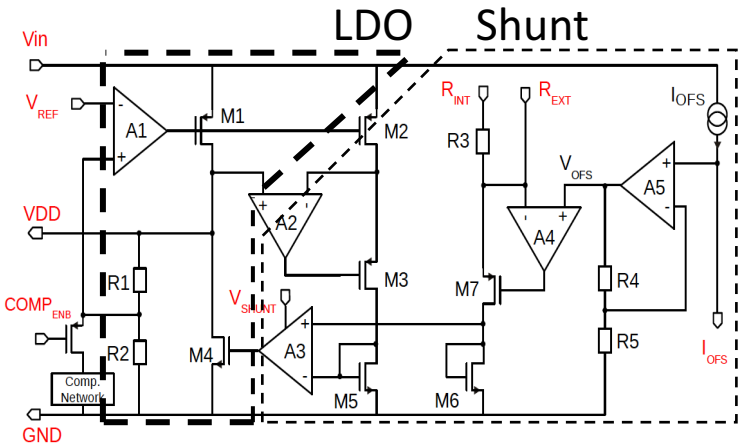
Nominal operation of full size chip (400x328 pixels):

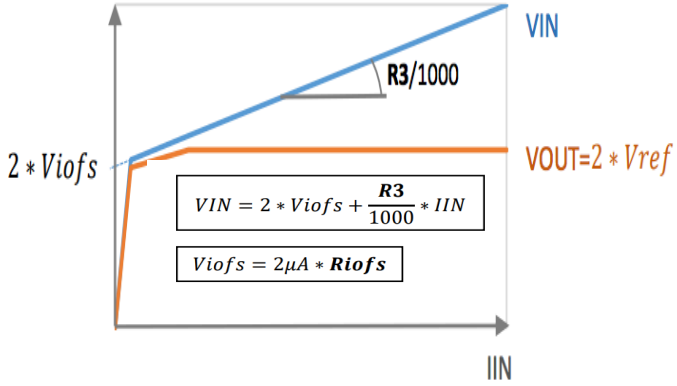
- Drop-out voltage of ~0.2V => **Vin=1.4V**
- **Voffset=1V**
- Current headroom **~25%** (will be less in the final)
- R3 adapted such that Vin(4A/chip)=2.0V
  - R_{digi} = (1.4V – 1.0V) / (0.75A *125%) = 0.43Ω
  - R_{ana} = (1.4V – 1.0V) / (0.6A *125%) = 0.53Ω
  - Total chip Req = 0.24Ω



RD53A Shunt-LDO regulator Designed by M. Karagounis

- **65 nm for Iin= 2 A** (FE-I4 version was 0.5 A).
- **Resistive behavior** allows for well-defined current sharing, determined by their effective resistance, which is configurable.
- **Configurable offset**, which allows an optimization of the power consumption in case of a failure of a chip in a module.
- Improved control loop to assure stability with **capacitive loads (from increased logic)**.
- **Off-chip decoupling capacitors** (uF) needed for LDO stability at the input and the output of the circuit:
  - C_{in} = 6 uF shared among chips in parallel
  - C_{out} = 2.2 uF per Shunt-LDO (2 per chip)
- The reference and offset voltages are provided by on-chip integrated BANDGAPs (two bandgaps per Shunt-LDO)
  - Vref value can be trimmed using four trimbits.





For an introduction to the Shunt-LDO circuitry see M.Karagounis paper:
https://indico.cern.ch/event/72160/attachments/1036621/1477145/Shunt-LDO_Regulator.pdf

Inner Tracker region