

#### Disclaimer – fine print:

- You have to live with my selection
- Impossible to represent everybody correctly apologies
- No posters talks only I try to be bit entertaining

# Summary or better, You tell me later if this is a summary!

Frank Hartmann

Institut für Experimentelle Teilchenphysik (ETP)

VGRTQ018

27<sup>th</sup> Vertex Conference — and we still love it

# The beginning 1992 – people told me about it

Basto Island, 1992



Kichard, 8057

Let us know by mail to BRENNER@YXCERN before <u>friday</u> 15.5.1992 if you are interested. Because of limited space a maximum of 30 persons can attend this workshop.

Everybody is welcome to suggest topics for the meeting and prepare a talk. A big paper screen and colour pens will be available for explanations.

We remind you of the primitive circumstances on the island and kindly ask you to bring your own sleepingbag.



Basto Island: cooked by the participants





Share your experience fully and freely

# The Intermediate Silicon Layers Detector





#### Frank Hartmann

Institut für Experimentelle Kernphysik - Karlsruhe

for the CDF ISL Group

VERTEX '98

28 September - 4 October 1998, Santorini Island, Greece



## The Laws of Vertex conferences

It must be at the water (lake, island or the sea) GREAT Job!!







Gulf of Bengal

- # It must be remote, that people are forced to have frank discussions no escape Check!
- # Plenary only! You must stay the whole length!
- **# Excursion must be AT LEAST 1/2 day long**







Good Job

A+ for location B for duration

- # My personal VERTEX law: Confess all problems that we all can learn
- **My personal 2<sup>nd</sup> VERTEX law: Food must be excellent!**



## Vertex conferences

#### 2018 Chennai, India

2017 Las Caldas, Asturias, Spain

2016 Isola d'Elba, Italy

2015 Santa Fe, New Mexico, USA

2014 Mácha Lake, Czech Republic

2013 Lake Starnberg, Germany

2012 Jeju, Korea

#### 2011 Rust, Austria

2010 Loch Lomond, Scotland, UK

2009 Mooi Veluwe, Putten, The Netherlands

2008 Uto Island, Sweden

2007 Lake Placid, New York, USA

2006 Perugia, Italy

#### 2005 Chuzenji Lake, Nikko, Japan

2004 Menaggio Como, Italy

#### **2003 Low Wood, Lake Windermere, Cambria, UK**

2002 Kailua-Kona Hawaii, USA

2001 Brunnen, Switzerland

2000 Sleeping Bear Dunes, Lake Michigan, USA

1999 Texel, The Netherlands

#### 1998 Santorini, Greece

1997 Mangaratiba, Rio de Janeiro, Brazil

1996 Chia, Sardignia, Italy

1995 Ein Gedi, Dead Sea, Israel

1994 Lake Monroe, Indiana, USA

1993 Lake Bohinj, Slovenia

1992 Basto Island, Finland

#### **Lessons Learned:**

- This is my 20<sup>th</sup> Vertex anniversary
- I should go more often

## Other vertex places and it's waters

Conference dinner in Nikko 2005 Legs are still hurting



Elba 2016
I am sure the water was **awesome** 



WOW - Ein Gedi swimming, muddy but warm



2003 Lake Windermere was freezing **cold** 



I was told, Loch Lomond was as cold

## I 'summarize'

- ★ Operational Experience 10
- # Application of Silicon Detectors in high/low backgrounds environment not sure what this means 2
- # Detector Design and Construction UPGRADE 9
- # Fast Timing 4
- # Future Collider experiments 3
- # Tracking and Vertexing 5
- # Electronics and System Integration 8
- **Social Activity**

Intro + social activity + 48 talks in 60 min You do the math how many seconds I spend on your contribution!

## First Silicon Strip Sensor (I found)

#### NUCLEAR INSTRUMENTS AND METHODS 97 (1971) 465-469;

Institut für Experimentelle Kernphysik der Universität and the Kernforschungszentrums Karlsruhe, Germany

The counters are large area ion-implanted detectors with a common aluminium contact and a front contact consisting of <u>five or twelve</u> gold strips separated by 0.2 mm.

Today, I simply try to continue the good old tradition.

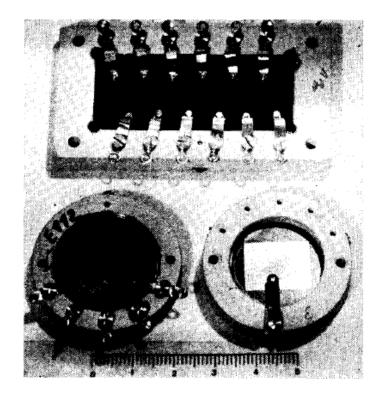


Fig. 1. Ion-implanted semiconductor detectors with subdivided front-contact and common back-contact.

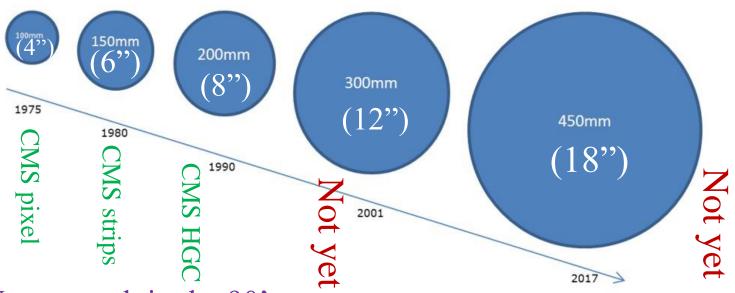
## Wafer sizes now and then

#### SILICON DÉTECTORS WITH 5 µm SPATIAL RESOLUTION FOR HIGH ENERGY PARTICLES

The detectors [2] are made of high-ohmic n-doped silicon single crystal wafers of 2" diameter and 280  $\mu$ m thickness (fig. 1). Using the planar process [1], p-doped strip diodes, covered by aluminium contacts, are implanted into one side of the wafer. On the other side a

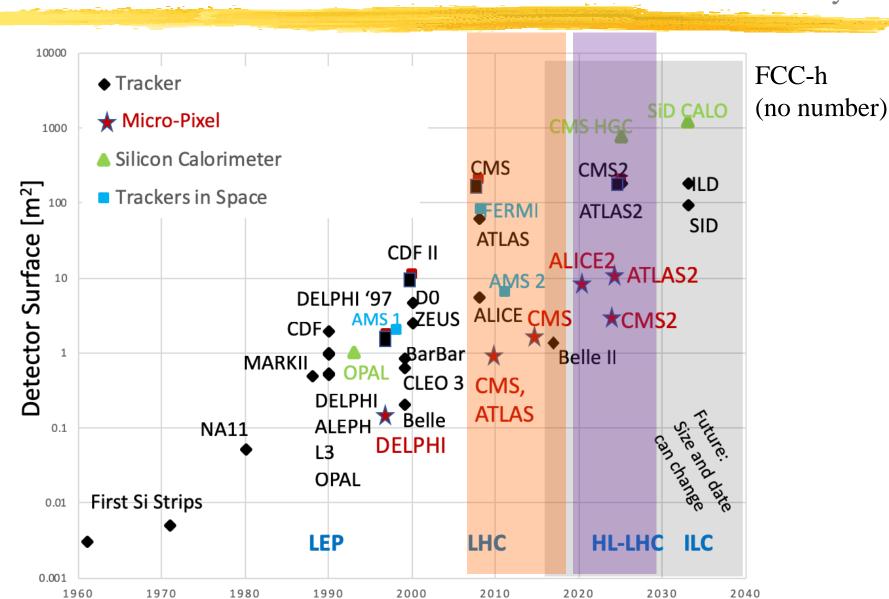
1983!

### Wafer Areas in Chip industries:



# Size matter! Does it?

Monday Tuesday Wednesday



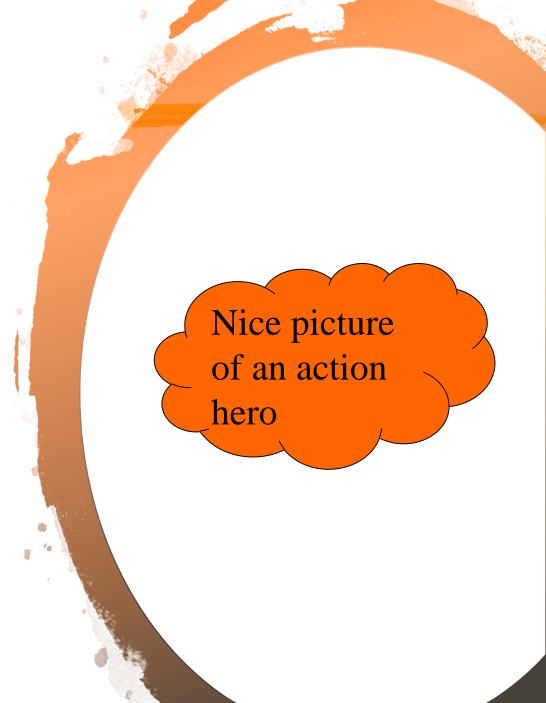
# You can never have enough acronyms, right? Anyhow, now they have been introduced ©

- TOT, TOA, MIP, HIP, TPC, PID, TOF, TRD, DEPFET, SNR, CCE, MAPS, PU, DCS, DSSD, DEPFET, QE, ENC, ESA, PCB, ASIC, FE, CMOS, ADC, DAQ, BX, TDR, LHC, IP, SMD, DAC, SEU, I/O, PLL, CLK, CSA, TID, IR, FADC, ECL, HCAL, RICH, FEA, PIN, DUT, RAM, QCD, CPU, HEP, NWELL, PWELL
- STAR, HFT, EEMC, BEMC, MTD, SST, PXL, DCA, IST, ATLAS, SCT, TRT, IBL MCC, TMT, MDT, TGC, FE4, S-Link, CMS, LS1, LS2, ROC, TBM, PROC, FPIX, BPIX, FEAST, TIB, TOB, TEC, TID, AOH, APV25, PP1, LHCb, VELO, EDV, R-CLUSTER, ALICE, ITS, SPD, SDD, SSD, HMPID, HS, HM, ECS, FEROM, BELLE2, HER, LER, PXD, SVD, DHP, SWD, DCDB, BEAST2, FANGS, PLUME, CLAWS, CDC, AFP, SiT, BSM, LQBars, MCP-PMT, PID (not the PID above), FE-I4, TCL, PPS, CT-PPS, CEP, RP, UFSD, VFAT2, FED, FEC, scCVD, pCVD, NINO, HPTDC, pnCCD, CCD, XMM, EPIC, eRosita, ATHENA, WFI, CAMP, FLASH, LCLS, FEL, SSJFET, RNDR, VERITAS, CoG, Mpix, HGCal, SM, VBF, SiPMs, CE-E, CE-H, OGP, QC, CALICE-AHCAL, GBT, L1, TV1, TV2, HGVROC, SKIROC, IpGBT, VU9P, EM, PF, PV, ONSEN, DHH, SOI, ŠW, LMU, RD53A, RD53B, ACB, DCB, FE65P2, CHIPIX, DRAD, VDDA, VDDD, LDO, IV, CV, TCT, EPI, CZ, MCZ, NIEL, DLTS, TSC, SIMS, SR, HVCMOS, DEMAPS, MAPS, DOFZ, PITS, FTIR, MW-PC, TPA, ILGAD, CCD (not the CCD above), MFP, BCM, BLM, Aurora, DBA, CBA, AFE, TMR, HiRadMat, ARIES, FLUKA, TCT(not the TCT above), TNC, SPS, SSDC, 1E, 2E, TCAD, PKA, CC, DCS (not the DCS above), b/w, EDR, TBPX, TFPX, TEPX, VL+, OT, IT, OPB, CTE, RF, HSLB, basf2, TT, UT, SciFi, TDR (not the TDR above), PRR, SALT, PEPI, GBT-SCA, CIS, ALPIDE, FCP, OL, CYSS, COSS, HIC, ABC, HCC, ABCstar, TTC, TA, FCC, FCChh, micron, JTE, DMAPS, HR-MAPS, HV-MAPS, ATLASpix, Monopix, CHESS, H35DEMO, CCPD, CACTUS, MALTA, TWCC, ADDR, ENGRUN1, CLIC, CLICpix, C3PD, ELAD, Allpix2, GEANT4, BRIL, MVA, LCFIPlus, ILD, SiD, ECAL, FPCCD, VTX, GFX, ID, ACTS, CTF, LSM, CA, GPU, EMCal, HMPID, ZDC, T0A, V0A, PHOS, MCH, MTR, FMD, PCA, DOF, FLP, EPN, TF, MWPC, GEM, TBA, ASD, ECD UBM, IMC, MET, TLPB, MEDIPIX, SLID, CMP, DBI, W2W, D2W, RDL, LTC, PACL, CMB STS, AMS, HGDT, HTC, VCR, STREAM, MSC ITN, TJ180nm, DPW, CMD, TSV, AIDA, SPAD, RDL, ISSCC, APSEL, VIPIC, HI-PVD, LCSL, ULITIMA, XIMOS, SOIPIX, SOFIST, BOX, PDD, INTPIX, FORCE, XRPIX, STREAM, UTIMATE, CBC, MPA, SSA, CIC, CKF, CDC

I almost overlooked PU - it is a word in the common dictionary, right?

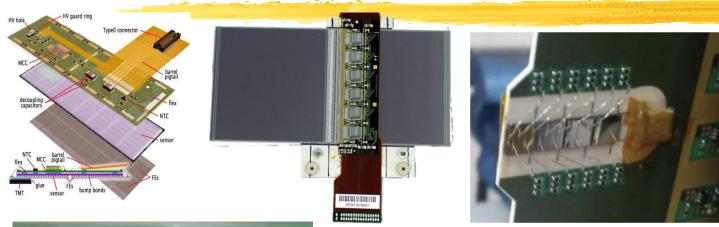
AKA some individuals working in hero mode whereas detectors live happily

# **Operations**



All modules are equal, aren't they?

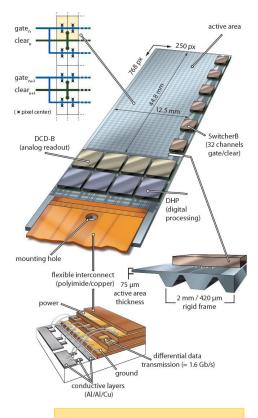
Can you identify yours?











Homework

– who is who?

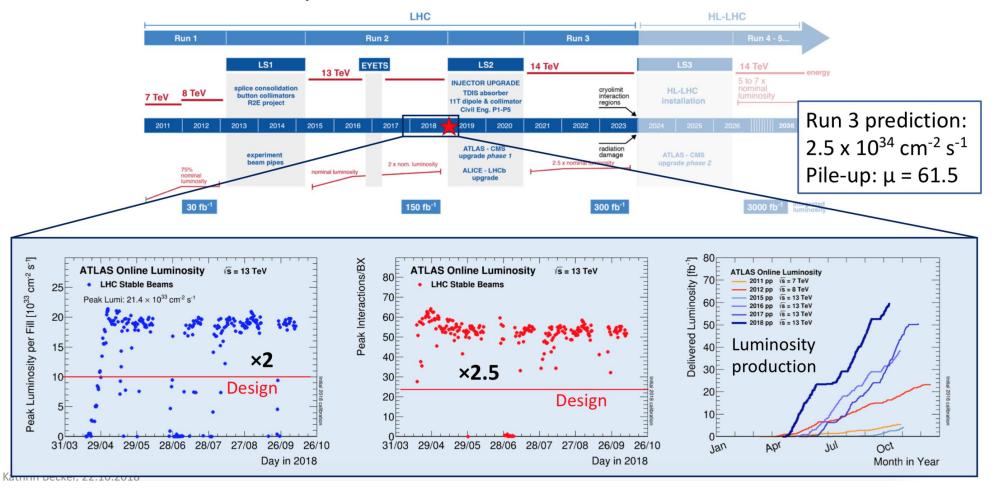




## The new normal

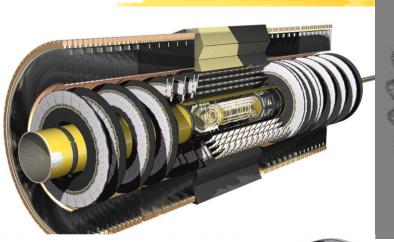


## LHC Roadmap and Performance in 2018

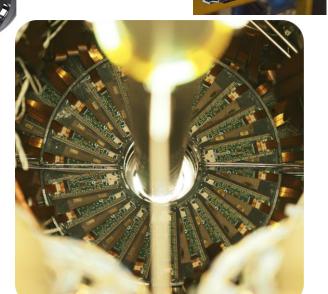


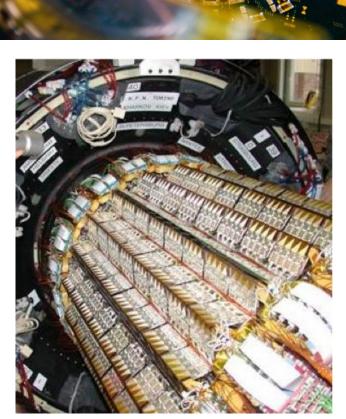
Presented by Kathrin Becker, Satoshi Hasegawa, Ivan Shvetsov, David Hutchcroft, Luca Bariogli, Benjamin Schwenker











# Problems are <u>not</u> authorized by the management!

## **#** They exist nevertheless! **Have you confessed all???** Hm??

- Basically Everybody: SEU − recovery automated Job
- ATLAS:
  - ☑ Pixel VCSELs on opto-boards die exchange during LS2
  - □ Upgrade and unification of readout system increase bandwidth
  - Mask pixel chips, where redundancy is neede due to bandwidth at high PU (small issue)

#### △ ALICE:

- □ Damage due Beam Loss the only one at LHC detectors AFAIK
- □ BELLE2 not a real problem, since according to plan
  - ≥ 1/10 equipped and good use of remaining volume by installing BEAST2 sensors (more later)
  - Lost optical connection to ~1/4 of one PXD module

BTW: despite all this — EVERYBODY took fantastic data
No. of working channels despite age good everywhere. Availability is awesome!

# Problems are <u>not</u> authorized by the management!

## They exist nevertheless! Have you confessed all???

**Hm??** 

- CMS interesting year:

- Modules with broken DC-DC broke due to HV=ON & LV=OFF
- ☑SEU in TBM only recoverable with power cycle (reset line missing)
- - new L1 with new ROC and TBM during LS2; damaged modules to be replaced
- **区MS** Strips fine (minus the well-known uncooled 3%)
  - HIP effect in the permille regime

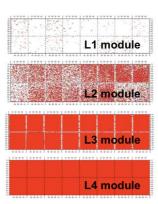


- **☑** Beware THE DOUBLE METAL
- ∠LHCb: "We are fine. Btw. We built a full spare VELO just in case"



☑ Missing cooling for LGADs as UFSD timing detector

Did I mention? — EVERYBODY took fantastic data



#### # ATLAS (RUN II):

- IBL inlet temperature instabilities, causing problems for the alignment:
  - too much flow! After flow reduction (orifices added to the pipework) problem solved

#### ALICE clogged filters (RUN I)

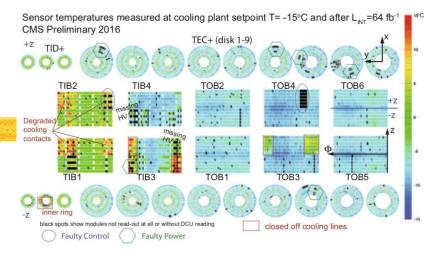
Filters 'inside' detector

**Before** 

After







https://indico.cern.ch/event/41288

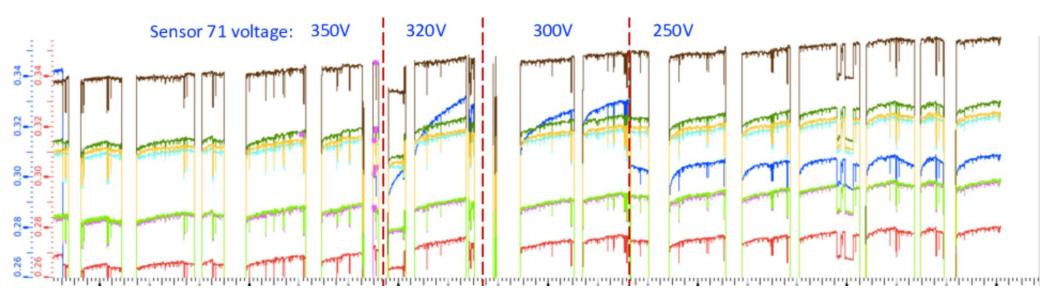
#### CMS TK— over-pressure incident (RUN I)

- close both sides of loops and warm upHV shorts, leaks, strongly degraded cooling contacts
- CMS (start of RUN II)
  - Ice clogged air pressure valve linesPipe not impervious to RH from outside air



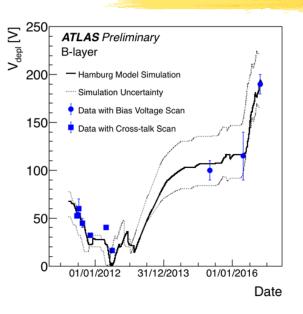
## Monitoring is crucial

### **#VELO**



# Radiation damage exists We are not inventing it to get new toys!

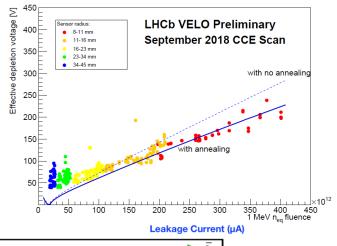


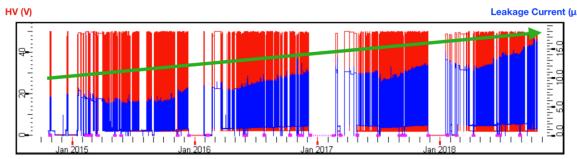


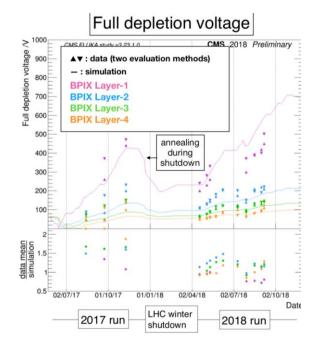
### **The Hamburg Model rocks**

### And even better, GianLuigi promised for PH2

Parametric description of operation parameters (signal, trapping, current) as a function of fluence and temperature.

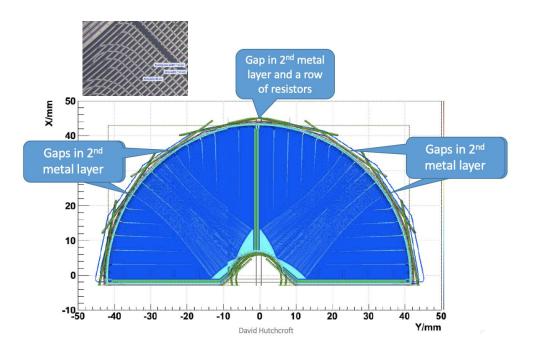


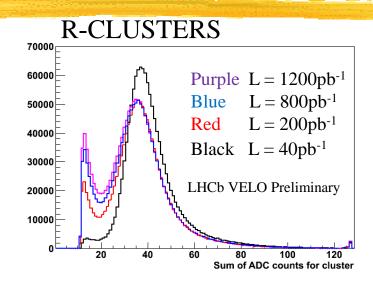


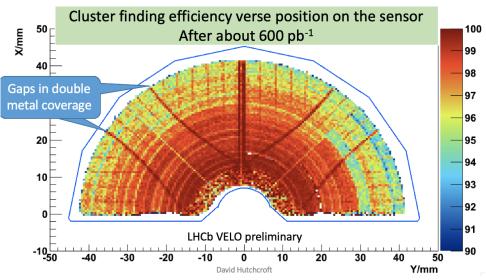


## LHCB - be wary about double metal

- # One day of David's life in the control room
  - David: "What is this?"
  - ☐ The collaboration: "Oh, we don't know."
    - -- Please investigate!"
    - ☑ And add the effect to the data simulation!
  - Use fake R-clusters to tune SIM.



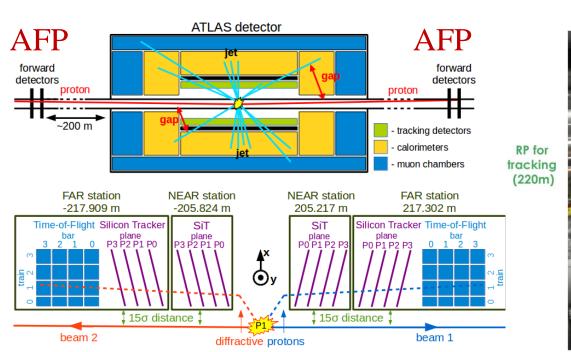




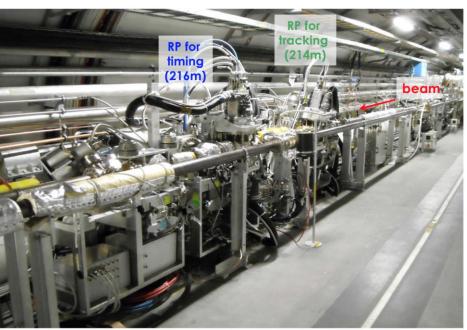
## AFP & CT-PPS do you remember what this stands for?

- **X** ATLAS Forward Proton Detectors
- **CMS-TOTEM Precision Proton Spectrometer**
- # Both in Roman pots ~ 200m away from main experiment
- # Both: timing & tracking stations

And both run stable and continuous



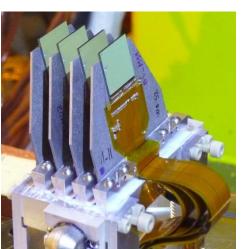
#### **CMS-TOTEM**

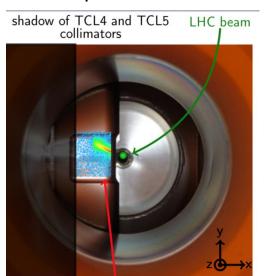


## AFP & CT-PPS

### Tracking station

- Highly non-uniform irradiation
- 3 D silicon sensor
- Edgeless
- Standard ATLAS or CMS pixel ROCs



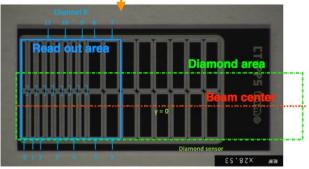


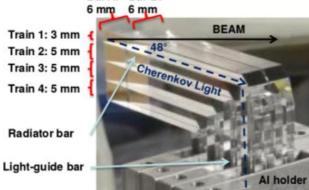
diffractive protons

#### **Timing Station TOF**

- To reduce background
- AFP: Quartz, Cherenkov, MCP-PM
- CMS: sc diamonds (double diamond same amplifier)
- CMS: LGADs (1ST in HEP) but not cooled 89









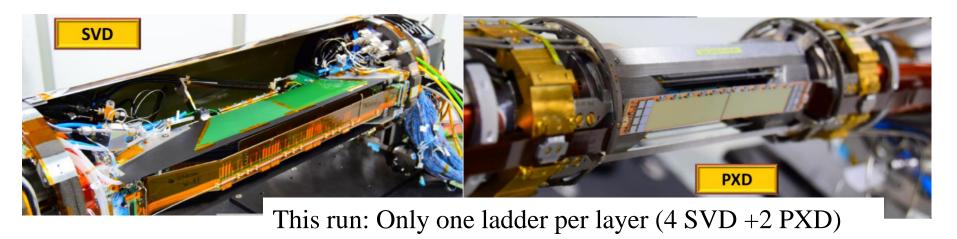


Vortex tube in AFP - NEW



## **BELLE 2 – pilot - First deployed DEPFET**

- # PXD and SVD fully integrated in Belle 2 DAQ, run control and HV control
- # SVD key operation features like S/N and cluster timing are within or exceeding TDR expectation
- ₩ PXD stable operation of 4 large, thinned sensors at low threshold (<1000e-), excellent S/N ratio



#### BEAST2 sensors to understand the environment:

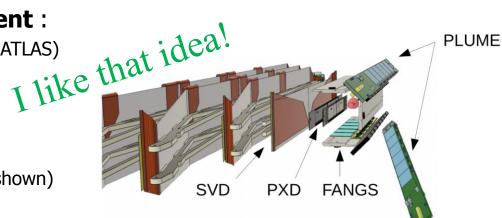
► FANGS: Hybrid silicon pixel detector with FE-I4 front end (ATLAS)

CLAWS: Plastic scintillators with SiPM readout (ILC)

PLUME: Double sided CMOS pixel detector (STAR)

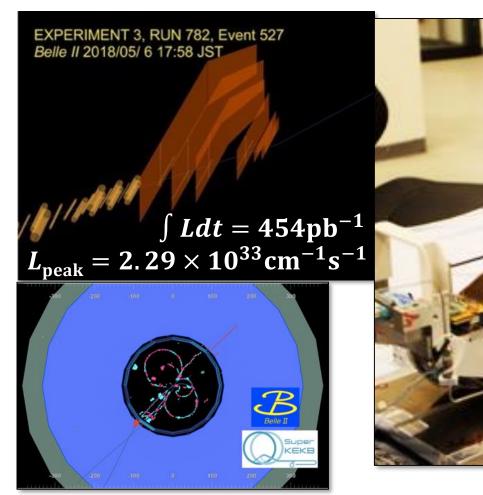
□ Diamond sensors for total ionizing dose measurement and for beam abort system (not shown)

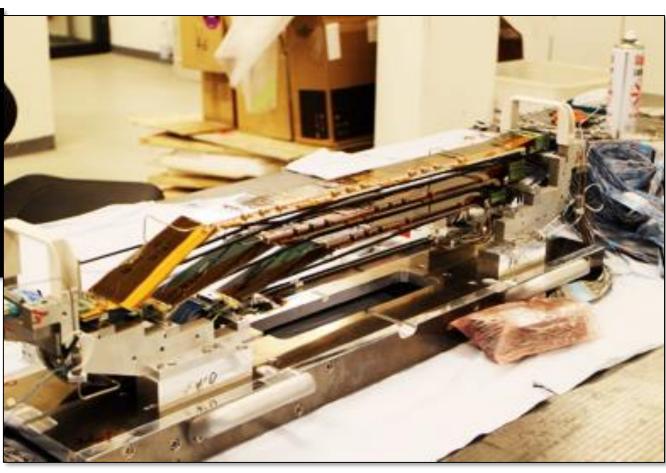
☑ 3He detector for thermal neutron flux measurement (not shown)

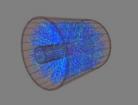


## One more on Belle2 pilot

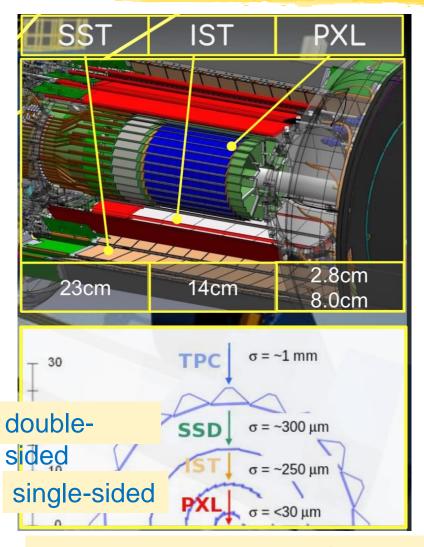
Insertion into Belle II in mid. Nov 2017





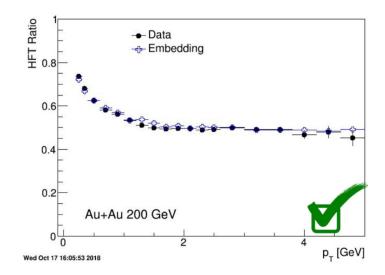


## **STAR – Heavy Flavor Tracker**



## **#Charm Physics**

- Wery lively walk-through to understand that tracking efficiencies requires
  - detailed simulations,
  - accounting for the sources of pileup background,
  - the misalignments of the detectors,
  - understanding of the uncertainties in our calibrations



PXL: Two layers of MAPS- ULTIMATE

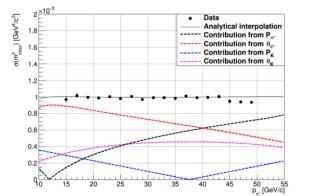
# Something special NA62-Gigatracker

By Matthieu Perrin-Terrin

- $\mathbb{H}$  B(K+ $\rightarrow \pi^+ \nu \overline{\nu}$ ) with 10% precision
- 😕 Beam Rate 0.8-1GHz **GIGA**
- Self-triggered
- ★ Time res <200ps
- # Peaking time 5ns
- # In beam pipe (vacuum)
- **#** On micro-channel cooling
- # Few noisy/dead pixels (< 100 per station)
- # Hit res 130 ps
- # Track res 75 ps

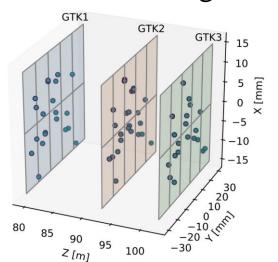


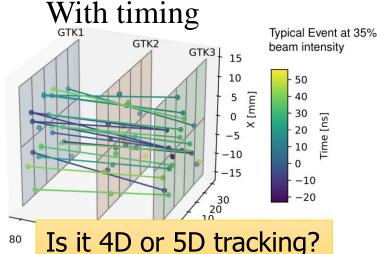
- Physics performance matches design performance
- ▶ Resolution of squared missing mass  $|p_{K^+} p_{\pi^0}|^2$  of  $K^+ \! \to \! \pi^+ \pi^0$

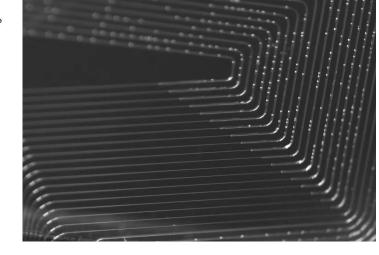


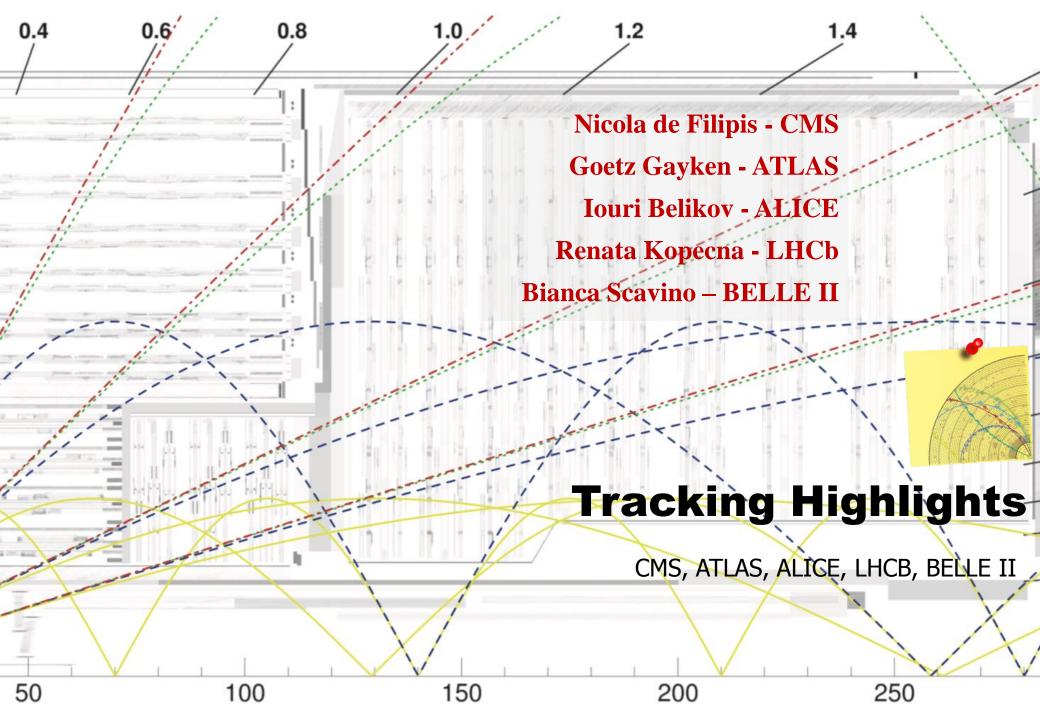


#### Without timing









#### Luminosity Run, 26th April 2018 First Hadronic Event

### Very simplified, therefore probably wrong and clearly incomplete

- **#** We align and calibrate
- # Hits, Cluster
- We do tracking in a sequence

  - Track Finding
    - ☑ Pattern recognition
    - **Kalman**

    - Legendre
    - **Use constraints:** 
      - Geometry, beam spot
      - Kinematic, Mass
  - Track Fitting
    - **Kalman**
    - ☑ Gaussian sum
    - Deterministic annealing
  - 3. Vertex and 2<sup>nd</sup> vertex identification

- **#** We can go
  - Inside → Out
  - Outside → In
  - Both
- **#** Seeding
- # We clean in between
- # Neural network can help
- # GPUs seem to help
  - ALICE GPU:
    - $\boxtimes$  2.5 5 times faster
    - 1 GPU replaces ~40 CPU cores
- Silicon only, +TPC+TRD, +Drift, +TRT
- **#** Different environment
- # b-tagging
- $\mathbb{H}$  Long lived particles (*Ks*,  $\Lambda$ )

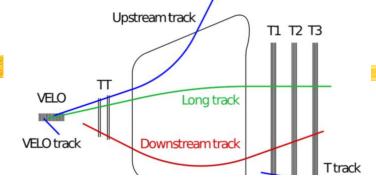








### LHCb actively finds everywhere



e.g. Downstream track for long lived particles (Ks,  $\Lambda$ )

#### Atlas ID track reconstruction:

**Build Clusters** 

Make track seeds

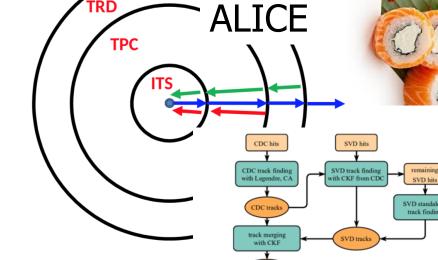
Find tracks

Handle merged Pixel cluster (NN)

Resolve ambiguities and fit track (GXF)

Extend to TRT

3



ATLAS, CMS

With the ALICE upgrade (**after LS2**) and continuous readout, z position of tracks in TPC not fixed anymore.

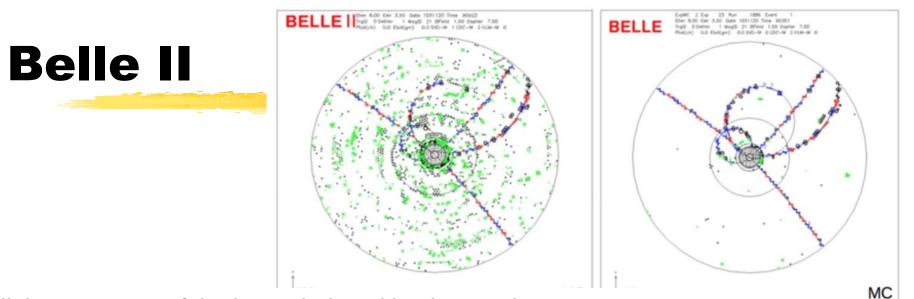
→ New ALICE ITS will then seed inside out

BELLE II

PXD hits

Fitting

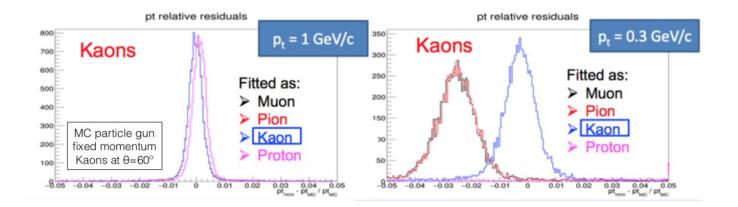
Track Finding



High occupancy of the beam-induced background:

11 tracks → few hundreds signal hits vs. 10<sup>4</sup> background hits

Deterministic Annealing Filter with 3 different mass hypotheses in parallel (π, K, p)
 Always uses all mass hypotheses



## **Alignment - ATLAS**

# Alignment

## Every 10 minutes

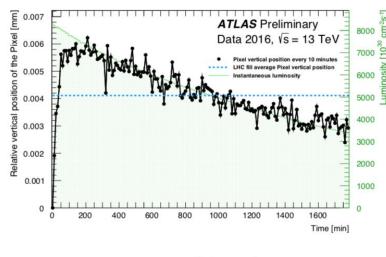
- based on global  $\chi^2$  minimisation of hit-to-track residuals,
- performed at different levels: sub-detector → layers → modules.
- Since run 2, alignment updates ( $\sim$  every 10 min):

#### IBL bowing correction

# 

 $O(100 \, \mu \text{m})$ 

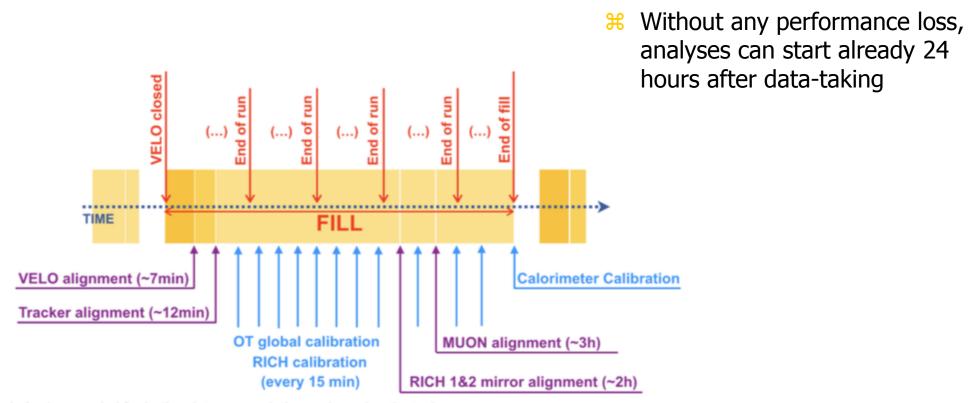
#### Pixel y-position



 $O(5 \,\mu\text{m})$ 

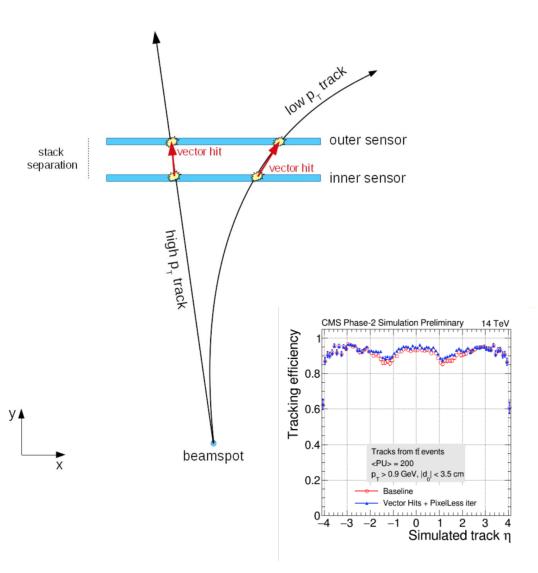
### Alignment and calibration – example LHCb

- Timely, iterative and automatic
- Real time alignment
- Same conditions online and offline ensured

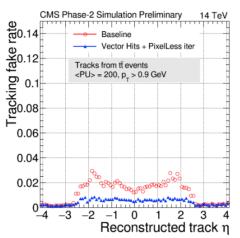


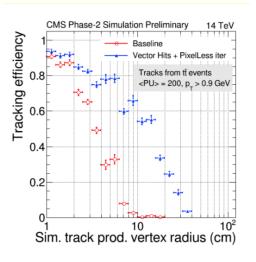
(...) - time needed for both a data accumulation and running the task

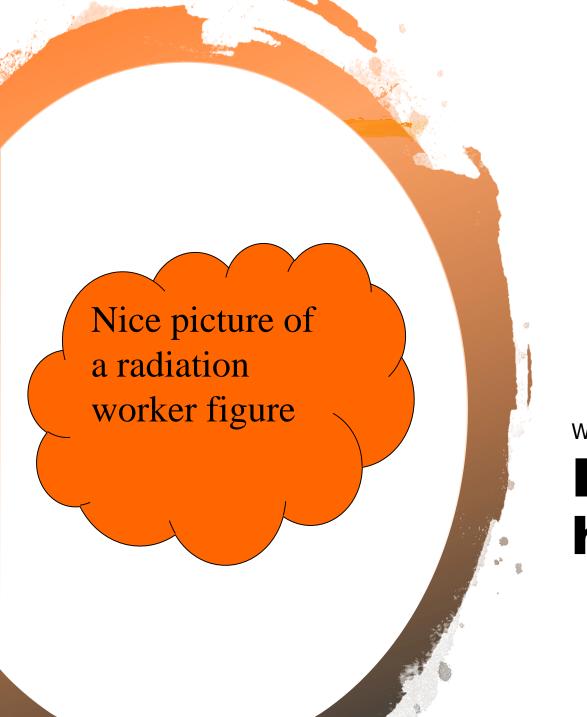
## **Example CMS – Phase II**



- # Closely spaced modules (~mm)
- vector hits in each layer
- **Reduces** combinatorics
  - DIRECTION
- # First very crude algo trial
  - Reduced fake rate significantly
  - Extends production radius







We withstand anything

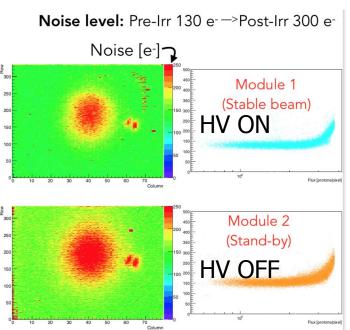
# Radiation hardness

## CMS, please learn from ATLAS

#### **Applause**, ATLAS started beam loss tests

- # At HiRadMat: High intensity pulsed 440GeV proton beam from SPS





Noise increase



# On Monday, I heard RD50 and RD42 are dividing the world



RD50 does silicon





RD50 does diamond



And where can I order sapphire detectors??

#### RD50 & RD42 – one simple slide

#### **#These RD collaborations are invaluable!**

THANK YOU

for providing unbiased results on many many fronts!

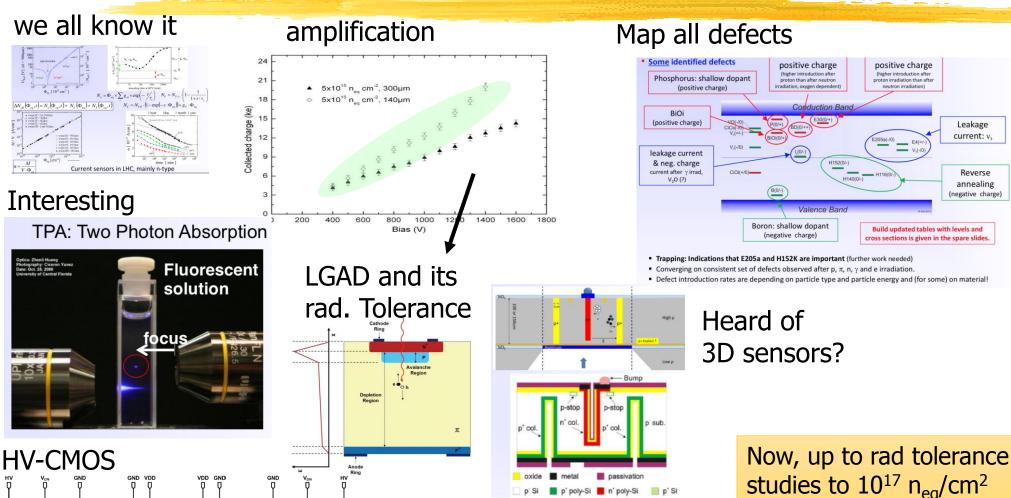
for providing test benches and facilities!

#### **X**Too many things - **I** give up to summarize!

#### **RD50** –

Summarizes and brought to you by Gianluigi Casse Obviously, large overlap with work inside experiment collab.

#### on a second thought, I do not like to give up ©



PW

NW

LFoundry 150 nm

**NWELL** 

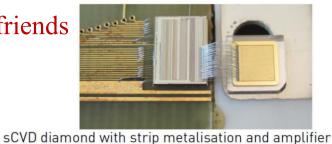
p-substrate

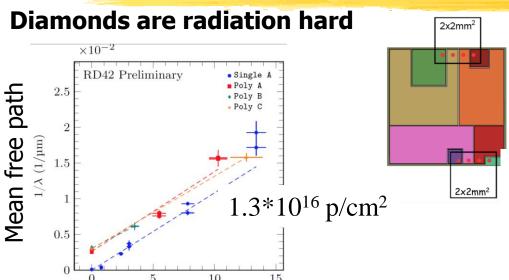
**PWELL** 

Interesting news/ideas about LGAD - later

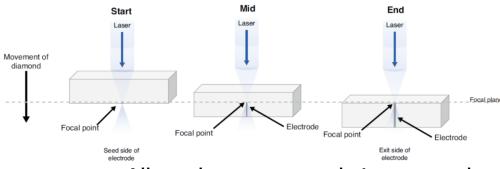
#### Diamonds are Harris Kagan's best friends

#### And ... RD42 in one slide



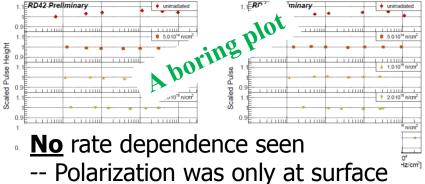


For BCM: some dynamic range into sensor design - pad sizes from 1mm<sup>2</sup> -32mm<sup>2</sup> work well



Last year rates up to 10MHz/cm² + doses to 4x10<sup>15</sup>n/cm²

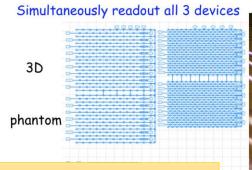
 $\times 10^{15}$ 

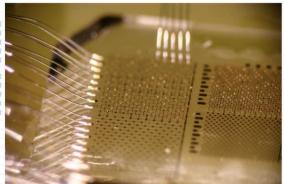


 $\phi$  (p/cm<sup>2</sup>)

Going 3D

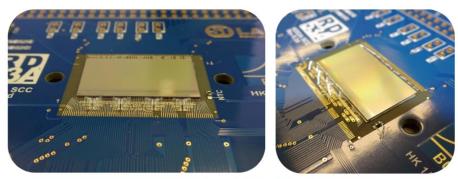
All work as expected; just tested after <u>irrad@3.5x10<sup>15</sup></u> p/cm<sup>2</sup>





Next - irradiation up to 10<sup>17</sup> p/cm<sup>2</sup>

# I'm from CMS and say, also in the name of ATLAS, THANK YOU RD53



The RD53A chip

- Size: 20 x 11.8mm<sup>2</sup> (half size of production chip)
- 400 columns x 192 rows (50x50 µm² pixels)



First 12" wafers at CERN with RD53A

- # 65nm pixel ROC for ATLAS and CMS Phase 2
- # RD53A test chip in hand
  - **△** WORKS
  - □ Unlocks sensor R&D



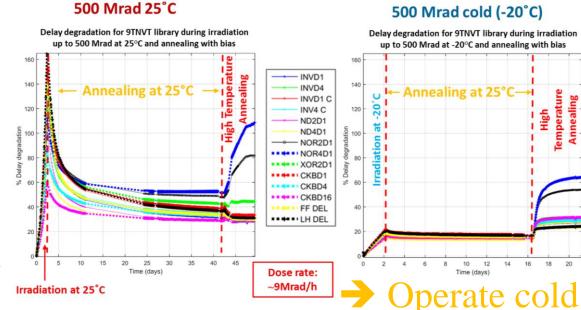
#### **RD53** – radiation tolerance

#### ★ Radiation damage above 100Mrad

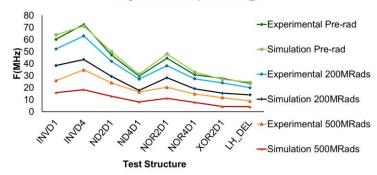
- Analog: transconductance, Vt shift:
  - Do not use the smallest possible transistors
- □ Digital: speed degradation.
- Radiate **cold** reduces damage
- # Anneal at RT helps
- # Simulation of rad damage works
- No significant change of serial power part after irrad.
- **#** Interesting
  - Trickle configuration might make Tripple Module Redundancy TMR obsolete

#### 500 Mrad cold vs room T

Room temperature and high temperature annealing with BIAS





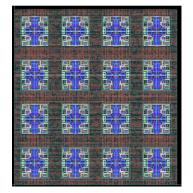


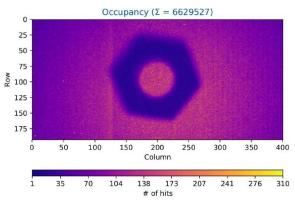
#### Since we are talking about RD53 already ...

#### 

- ~150 members of which ~40% ASIC designers, 24 Institutes from Europe and USA, both from CMS and ATLAS experiments
- **65nm technology** allows to design a smaller pixel capable to sustain extreme particle fluxes and long latencies
  - $\sim$  **2500** transistors/pix (50x50  $\mu$ m<sup>2</sup>)
    - $\boxtimes$  Same as in 50x250  $\mu$ m<sup>2</sup> in 130nm
  - ~2 trans/um2
  - RD53 chip 50% of area to digital
- - 'Unfortunately' all 3 work well; meaning the management has no easy choice
- Several test-beam DONE (AIDA-2020, ATLAS, CMS) by the sensor community to study planar and 3D silicon sensors. Currently also irradiated modules being studied.
  - Low thresholds (~800e- to 1200e-) are normally achieved

#### 8x8 pixel core





#### **#** Further reading – specs/features:

Pixel size 50x50um<sup>2</sup>; threshold 600e, intime threshold 1200 e, hit loss@ max rate <1%; trigger rate 1MHz, 12.5 us latency; >4 bits Time over Threshold; 1-4 links @ 1.28Gbits/s; 500 Mrad at -15C; Good SEU behaviour; <1W/cm2; T range -40C to +40C;Bias of edge and top "long" pixels; 6-to-4 bit dual slope ToT mapping; 80 MHz ToT counting; ATLAS 2-level trigger scheme TMR for SEU hardening; Power saving ~20%; Design for test scan chains; Optimal data formating and compression Date aggregation between pixel chips (CMS)

Sorry
– out of space

#### Can we have a better name?

#### RD53, on the path to the final chip RD53B

- **#** Common design team
- # CMS and ATLAS will get different chips

  - Both will have all functions choseable

	ATLAS	CMS	
Size	20x19.2 mm² (400 x 384)	22x16.4 mm² (440 x 328)	
Trigger	1 level: 1MHz, 10us 2 level: L0: 4MHz, 10us, L1: 600KHz, 25us	1 level: 750 kHz, 12 us	
Distance to the beam  → Hit rate	r = 4 cm	r =3 cm	
		CMS data aggregation between chips on pixel module	
Readout	ATLAS aggregator chip	LpGBT	
Serial powering protection	Passive protection PSPP (TBC)	Passive protection	

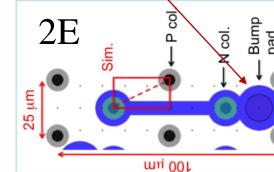
#### 3D - we all know how it works, right?

- No 3D zoo anymore. This is what we get:
- lpha Thin **Single Sided Double Column SSDC** on low  $\Omega$ cm wafer
- **#** Ratio 30:1!
- # Edgeless edge possible
- 35x100µm² 2E difficult to manufacture due to constraints on position of bump

P- high  $\Omega$ cm wafer

p++ low  $\Omega$ cm wafer

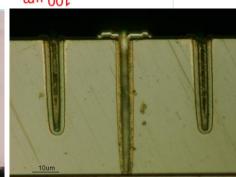
# Large sensors challenging

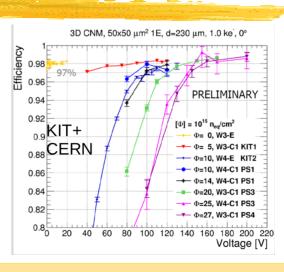


Metal to be deposited after thinning

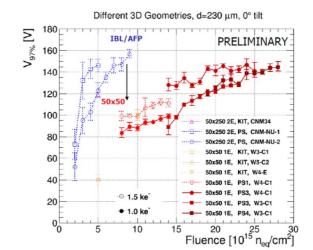
Handle wafer to be thinned down

5.3 μm!



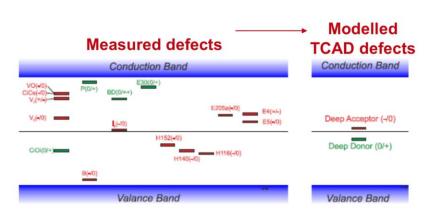


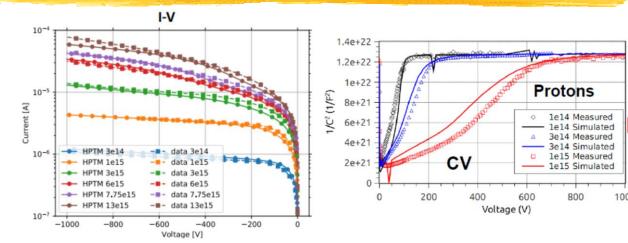
Unbelievable, They work after 3\*10<sup>16</sup> n<sub>ea</sub>/cm<sup>2</sup>

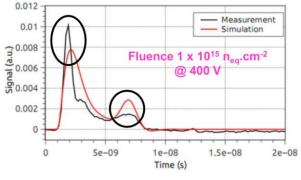


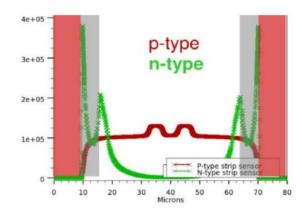
#### Radiation modelling gets better and better

- Iterate
  - Feed measurements into simulation
- - Allows good prediction to beyond 10<sup>15</sup> n<sub>eq</sub>/cm<sup>2</sup>
- **#** Also surface simulated
- Good to understand fields
- Works also for e.g. LGADs









- Predict the future
- Optimize your detector



Now, everything is radiation tolerant.

Let's build some detectors

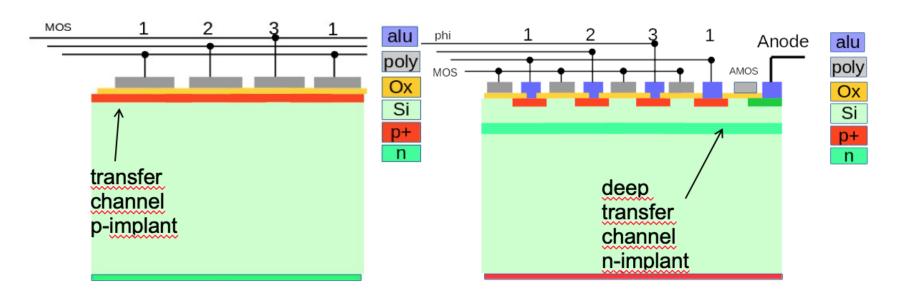
Radiation, please come in, we developed a tolerance

# Application of Silicon Detectors in high/low backgrounds environment

Still no idea what this means
BUT the talk pnCCD was very interesting

### Florian Schopper proudly presents

#### pnCCD



fully depleted MOS-CCD is derived from a Diode structure and collects holes. (LBNL, Dalsa)

fully depleted pn-CCD is derived from a <u>Driftsensor structure</u> and collects electrons. (HLL, pnSensor)

#### Improve speed:

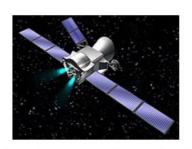
readout/line: 20µs → 4µs frame

transfer/line: 300ns → 60ns

Vbias up to 600V

### Florian Schopper proudly presents

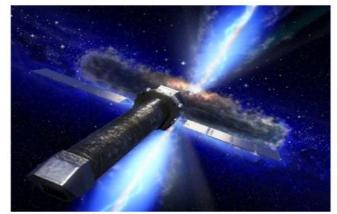
#### **Applications I: Astronomy**



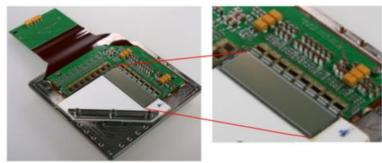
BepiColombo, ESA, launched only Adays ago, on its way to mercury



The MIXS instrument contains an array of SDDs (300 $\times$ 300  $\mu$ m<sup>2</sup>) with DEPFET readout nodes



ATHENA, launch 2028

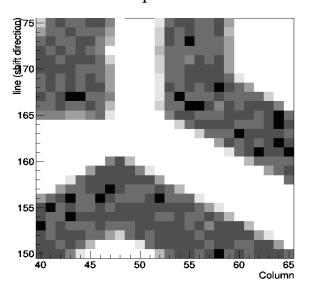


Wide Field Imager (WFI) DepFet array. 1 MPix with 120x120 µm² pixel

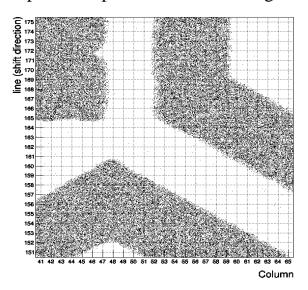
Florian: Launched! We test it when it arrives – in 5 years Frank to my fellow HEP friends: Don't do that!

# Applications Ib: high resolution spectroscopic imaging

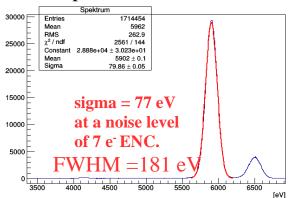
CCD pixels

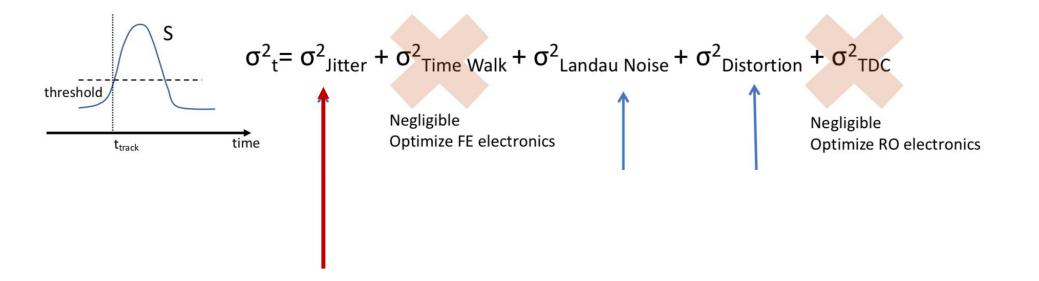


hit positions placed on 32x32 Subgrid



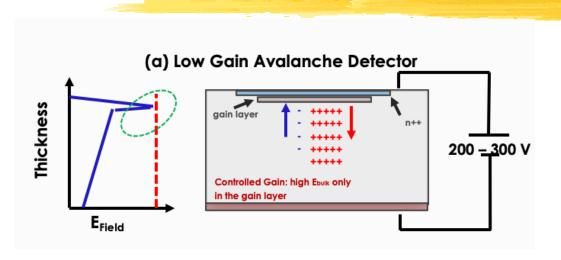
2x2 pixels are summed

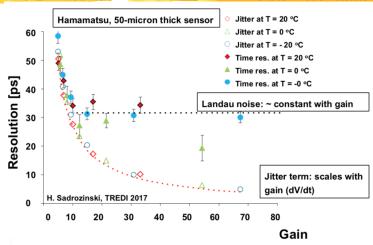




#### **THINGS with TIMING**

#### **UFSD** - the most intriguing news

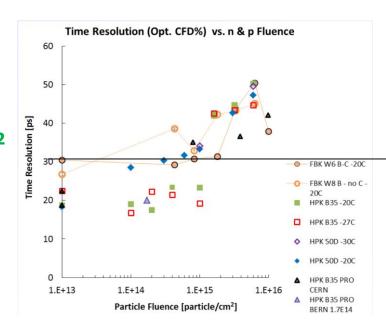




- # High gain low jitter good time resolution
- Gain layer in early LGADs lost with radiation due to donor removal (B displacement)

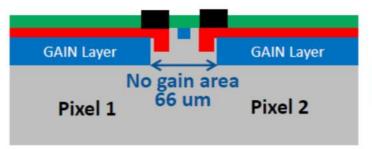
#### **∺** Boron+Carbon diffused helps up to 3\*10<sup>15</sup> n<sub>eq</sub>/cm<sup>2</sup>

- hurray, the goal was 1\*10¹⁵ n<sub>eq</sub>/cm²
- Carbon occupies interstitials Carbon is good
- Mind, 20 years ago, Carbon was evil
- Gallium instead of Boron didn't help



#### UFSD/LGAD – fill factor $66\mu m \rightarrow 1\mu m$

Standard JTE + p-stop isolation



Trench isolation could drastically reduce the inter-pixel border region down to few microns

#### Trench isolation technology

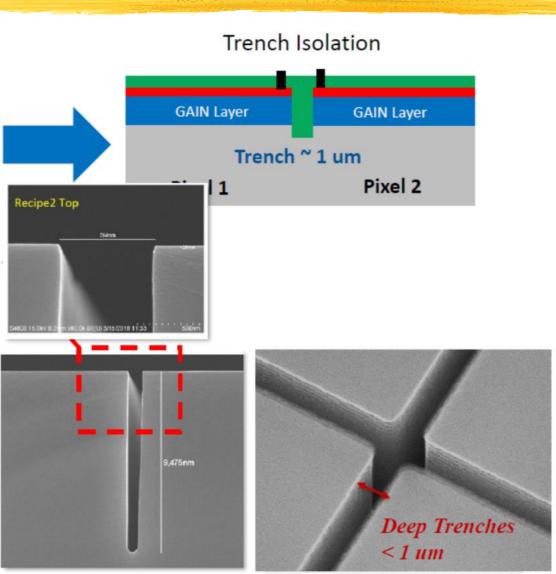
Typical trench width < 1 um

Max Aspect ratio: 1:20

Trench filling with: SiO<sub>2</sub>,

Si<sub>3</sub>N<sub>4</sub>, PolySi

CMM
CENTRE FOR MATERIALS AND MICROSYSTEMS

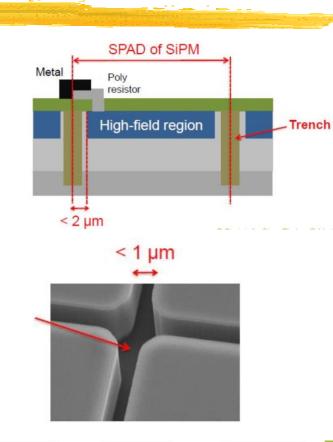


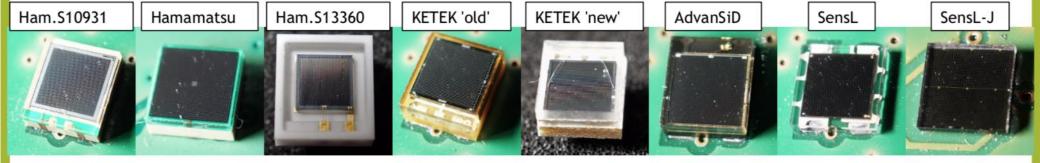
#### 150 ps timing brought to you by Rok Pestotnik

#### **UF-SIPMs**

- # SiPMs are attractive photosensors (also single photon)
- 150 300 ps FWHM are achieved in test samples with only one cell hits more cells hits full system (300 ps TOF.PET) timing is degraded by delayed contribution in multi-cell events

  - Further improvements
    - Separating the contributions by multi-threshold measurement/waveform sampling





### Ingredients for later talks

MAPS, depleted MAPS, HVCMOS

# Special mix of contributions from

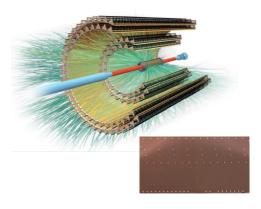
- Abishek Sharma,
- Eva Vilella Figueras,
- Thanushan Kugathasan,
- Heinz Pernegger

#### **MAPS** evolution





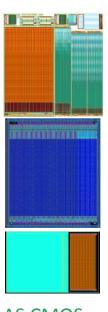
ULTIMATE in STAR
IPHC Strasbourg
First HEP MAPS system



ALPIDE in ALICE
First MAPS with sparse
readout similar to hybrid
sensors

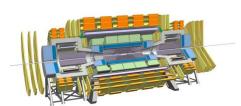
Chip-to-chip communication for data aggregation

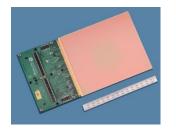
Important steps in every iteration



ATLAS CMOS
Depleted radiation hard
MAPS with:

Sparse readout Chip-to-chip communication Serial power



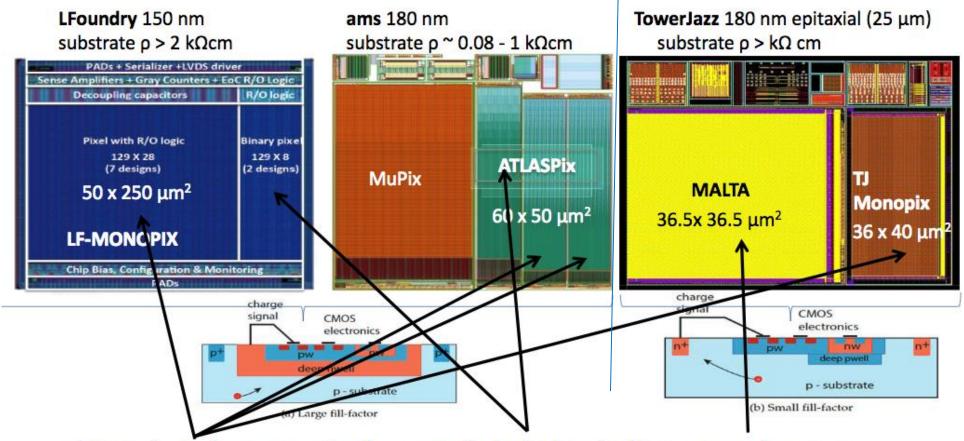


Serial power

FCC, CLIC, ...
Large stitched fast
radiation hard MAPS with:
Sparse readout
Chip-to-chip
communication

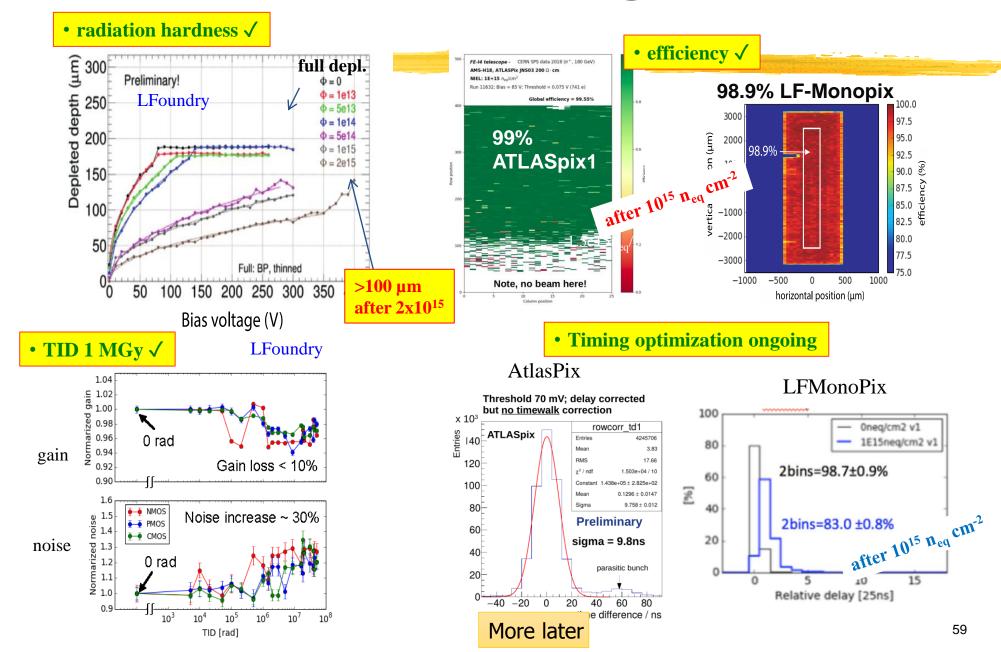
## Radiation hard CMOS sensor developments for ATLAS

- # Targeted towards outermost ITK pixel layer
- # Pursue designs with large and small electrodes

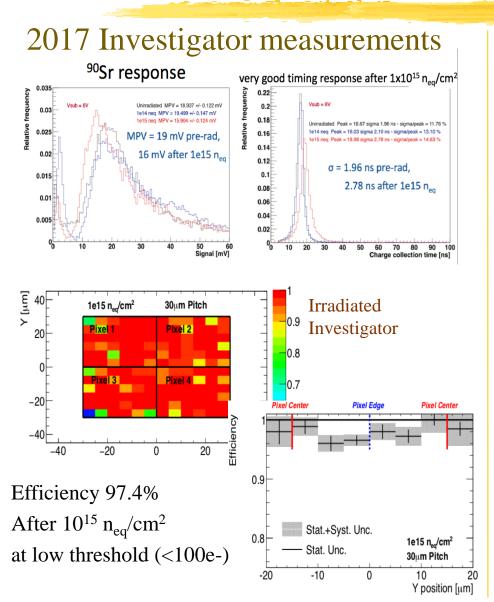


column drain (conservative) - parallel pixel to buffer - asynchronous

#### Preliminary results with large electrodes

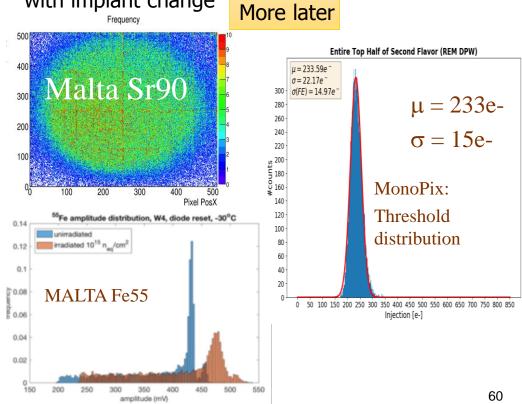


#### Preliminary results with small electrodes



#### 2018 MALTA & TJMonoPix work

- same FE design, different readout architecture
- Tests ongoing (lab, beam tests, irradiations) show excellent ENC ~ 10-20e-; good timing after irradiation
- Efficiency problem in corners after irradiation to fix with implant change



#### Life/work beyond the pixel cell



#### ATLAS CMOS-1 Periphery



Key focus now is the realization of an ATLAS-ready ASIC: include essential RD53 functionality in monolithic sensor

#### **Key topics : Hit data Memory and Trigger**

- Analysing memory design in order to efficiently use bandwidth, distribute power and use little space
- Memory: efficient storage concept : local EoC hit memory plus global memory for trigger latency

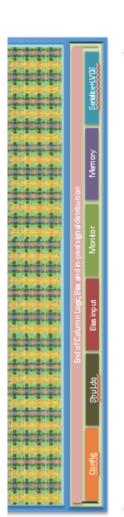
#### GREAT

#### **Key topics : Serializer and output**

- Data out after trigger is serialized with 1280 Mbps to go to aggregator with RD53 protocol
- Clock recovery from Clk/CMD 160MHz to receive from PP0

#### **Key topics: Power and bias, configuration**

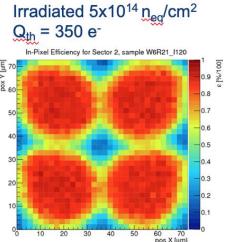
- Submitted designs of blocks for serial power: use on CMOS sensor shunt regulators for serial powering
- Implement configuration with RD53 protocol



#### CMOS, how to 'solve' the corners

#### Small collection electrode radiation tolerance

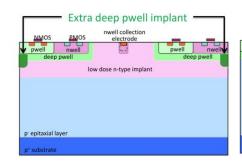
 $\begin{array}{c} \text{Unirradiated} \\ \text{Q}_{th} = 250 \text{ e}^{-} \\ \text{In-Pixel Efficiency for Sector 2, sample W6R6\_I138} \\ \text{2x2 pixels} \\ 36.4 \ \mu\text{m}^2 \\ \\ \begin{array}{c} \text{10} \\ \text{20} \\ \text{30} \\ \text{10} \\ \text{20} \\ \text{30} \\ \text{40} \\ \text{50} \\ \text{30} \\ \text{40} \\ \text{50} \\ \text{60} \\ \text{70} \\ \text{pos } \chi | \mu\text{m} \end{array}$ 

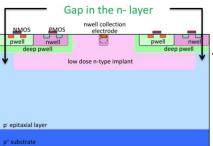


Issue: Detection efficiency loss in the pixel corners

#### Solution

Increase lateral electric field in critical sensor regions (corners)





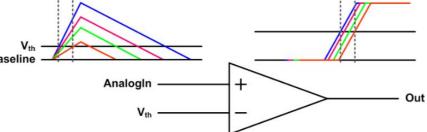


#### **State of the Art**

#### Time resolution of depleted CMOS sensors

## Sources of time uncertainty in depleted CMOS sensors Charge collection time Delay RO electronics

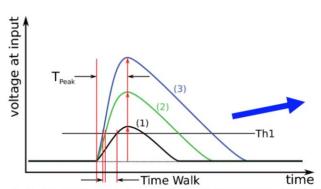
Time-walk



#### TW

- MuPix8 corrected − 7ns
- MALTA − 25 ns
- CACTUS − 100 ps (sim, very large pixels, large power)

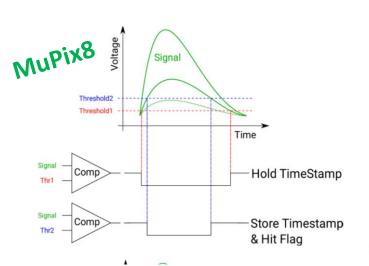
#### **#** Address TW



Ref.: R. Schimassek, IEEE NSS/MIC/RTSD, 2017

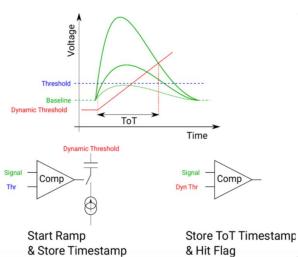
#### Time-walk compensated comparator

Threshold 1 triggers delay circuit Signal height controls delay



#### 2 threshold method

Th1 at noise level –min TW Th2 confirms signal



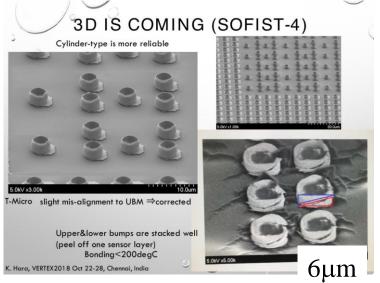
#### Ramp method

Constant Th & Linear dynamic Th

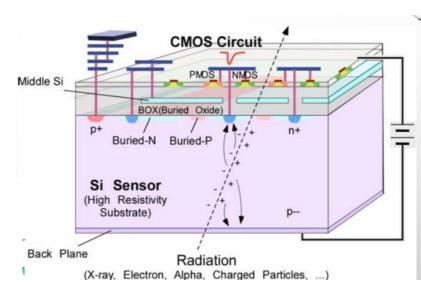
#### Very clearly presented by Kazuhiko Hara

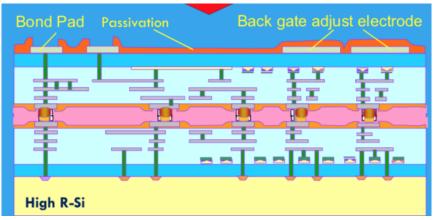
#### SOI

- Candidate for ILC
- Lots of interesting material here an excerpt:
  - Pixel 30x30 μm<sup>2</sup>
  - ightharpoonup Incredible space resolution ≤1.4μm
  - $\triangle$  Time resolution  $\sim 1 \mu s$
  - S/N 120 for 67μm thickness
- # And 3D is coming



#### LAPIS 0.2µm FD-SOI





BELLE II – PXD & SVD ALICE LHBC VELO & Tracker

ATLAS Pixel & ITK CMS IT & OT

These detectors will be awesome

### **Upgrades**

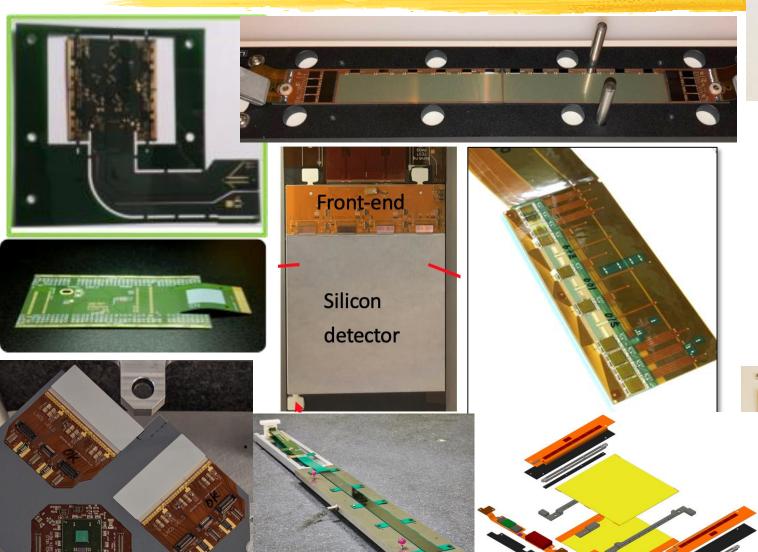
And, I have to say it:

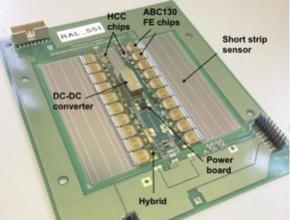
Share more problems!!

I want to learn from you!

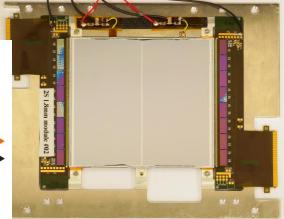
More homework – who is who?

#### **Modules** We use the same as today, right?

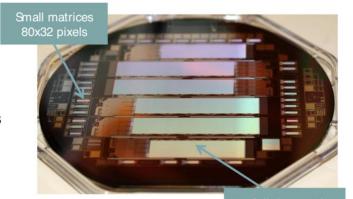








# Belle II – PXD – THANK YOU for doing the best possible





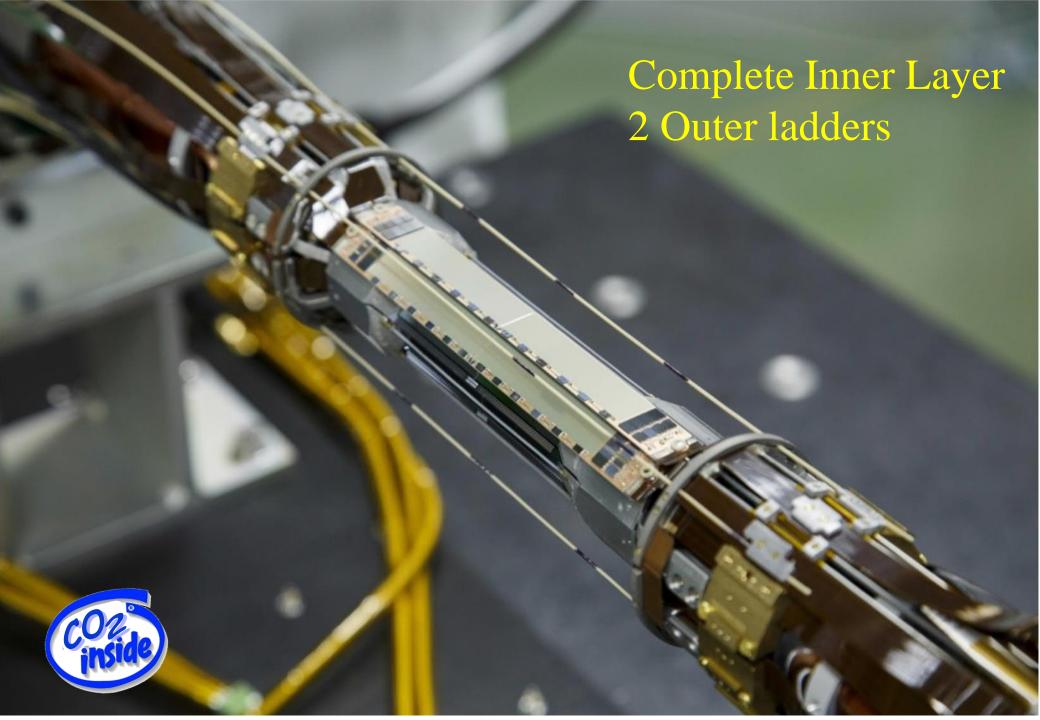
Module Type	FC+SMD	probe card test	kapton	characterization	ladders assembled	final test	
DATE A STORY		14 passed		13 passed		9 passed	
L1 BWD	14		14	1 rework ok		3 passed	
		45		44 1	13	1 b-grade	
		15 passed		11 passed			
L1 FWD	15		15	1 rework ok		3 lost	
				2 b- grade 1 lost			
		19 passed		17 passed		2 passed	
L2 BWD	20	1 rework ok	20	1 rework ok	\	2 passed	
				2 still to be tested	4	/	
L2 FWD	22	18 passed	20	13 passed	4		
		2 rework ok		2 rework ok, 1 lost			
		2 lost		4 still to be tested		2 lost	

6 x full size matrices 768 x 250 pixels

17 ladders glued (plus 10 dummy ladders during the qualification of the gluing

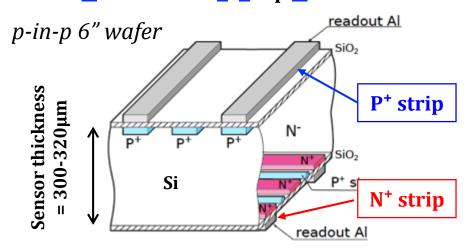
Ladders damaged during installation on cooling block due to particles Production stopped for further investigation – TEMP descope

→ in order to keep Belle II schedule a de-scoped PXD (complete inner layer + 2 outer ladders) is installed for the start of phase 3, installation of the full PXD scheduled for 2020

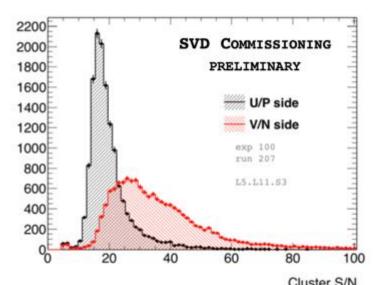


#### Belle II - SVD

#### **D**ouble-sided **S**i **S**trip **D**etector

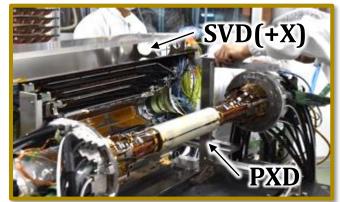






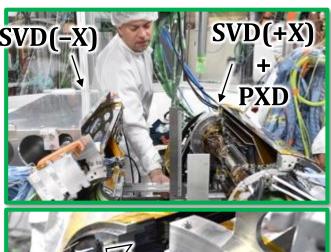
- SVD has run stably since July to mid
   Sept, collecting 30×10<sup>6</sup> cosmic events.
- # Efficiency >99% for most of the sensors

#### PXD + SVD "Marriage"













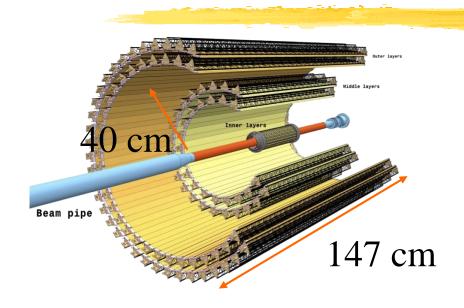


The combined VXD will be commissioned for one month before the installation to the Belle II detector by the end of 2018.

#### Serhiy Senyukov presents

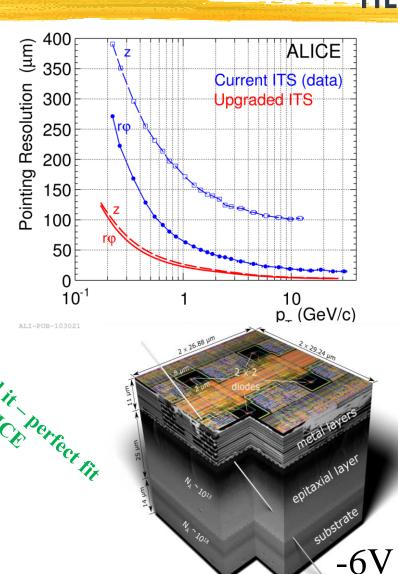
#### The ALICE Tracker Upgrade - Install LS2 (2020)





#### **3+4 layers of MAPS (CMOS) ~10m²**

- $\triangle$  27x29  $\mu$ m<sup>2</sup> pixels
- MAPS thinned to 50 μm  $\times$  ~0.3 % X<sub>0</sub> per layer
- **△ 12.5 G-pixels**
- Radial coverage **21 -** 400 mm
- Increase of readout speed  $1 \text{ kHz} \rightarrow 50 \text{ kHz} \text{ (pp)}$  and 400 kHz (PbPb)



#### The ALICE Tracker Upgrade - Install LS2 (2020)

#### **Manufacturing sites:**

Bari, Liverpool, Pusan, Strasbourg, Wuhan Daresbury, Frascati, LBNL, NIKHEF, Turin



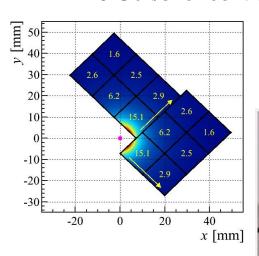


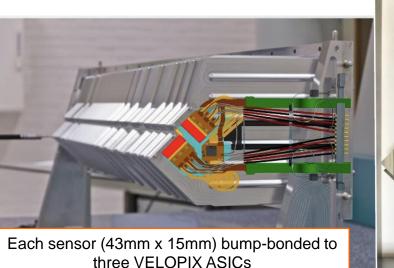
Assembly of the first inner half-barrel completed in June 2018

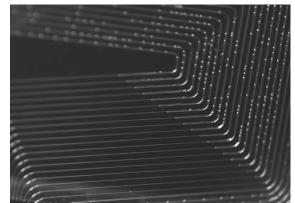
## LHCb VELO – LS2 – strips2pixel

- All-pixel detector 55x55  $\mu$ m<sup>2</sup> n-in-p 200  $\mu$ m thick pixels sensor, bias up to 1000V, readout with VELOPIX Very high rad (8x10<sup>15</sup> n<sub>eq</sub>/cm<sup>2</sup> for 50 fb<sup>-1</sup>until LS4) & non-uniform irradiation (~ r - 2.1)
- # Go closer: distance to beam 51 mm instead of 8.2 mm
- Sensors on CO<sub>2</sub> micro-channel cooling
- No hardware trigger

  - 20 Gbit/s for central ASICs



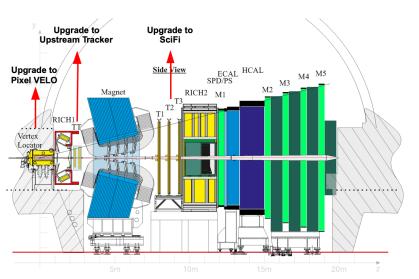






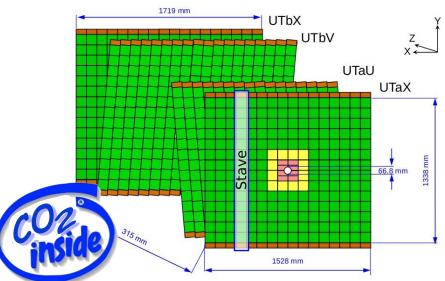


## **LHCb – Upstream Tracker**

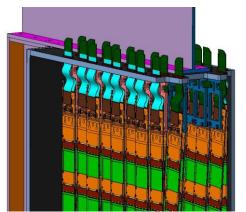


- **# ALL OK, but**
- **#** Problems with FE ASIC
  - Silicon ASIC for LHCb Tracking SALT

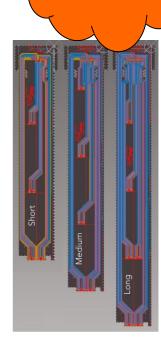
  - Obviously final design evaluation not yet done
- # 4th SALT iteration submitted







Long flex



Fingers

crossed

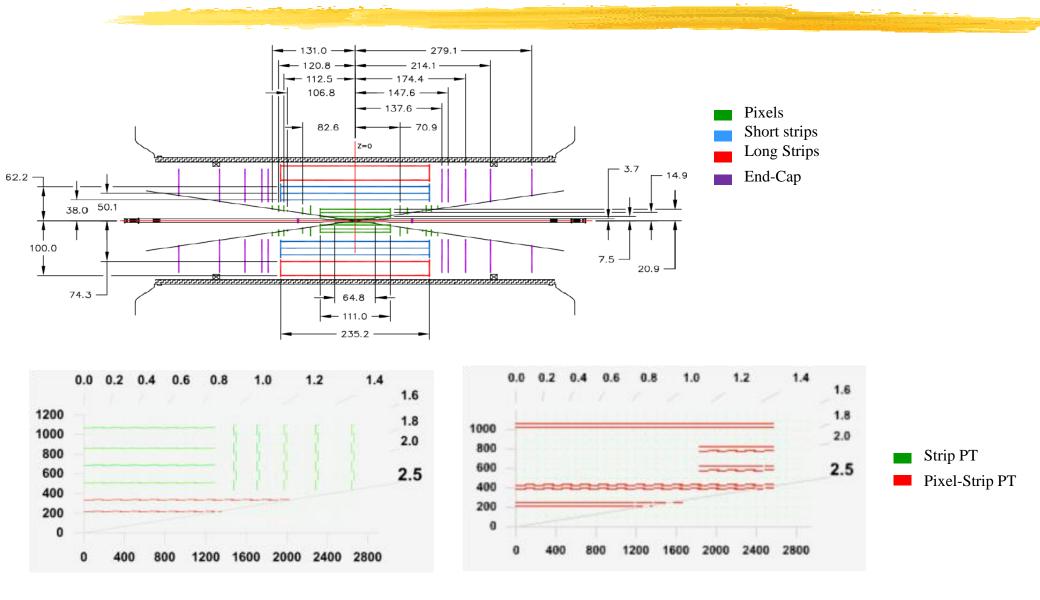
# ATLAS and CMS

Nicely presented by

Matthias Hammer, Stella Orfanelli, Serhiy Senyukov, Anirban Saha

Mixed by Frank Hartmann

# ATLAS & CMS Phase II -- ideas in 2010



## **Technologies**

#### **Pixels**

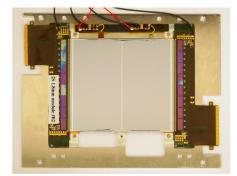
- **#** Light weight mech.
- **# Serial power**
- ₩ CO<sub>2</sub>
- # n-in-p sensors
- # RD53B (see earlier)

### **Outer Tracker**

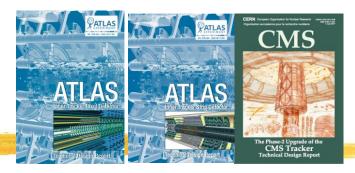
- # Light weight mech.
- # DCDC
- ₩ CO<sub>2</sub>
- # n-in-p sensors & 3D
- # ABC / CBC
- **# CMS Track Trigger**

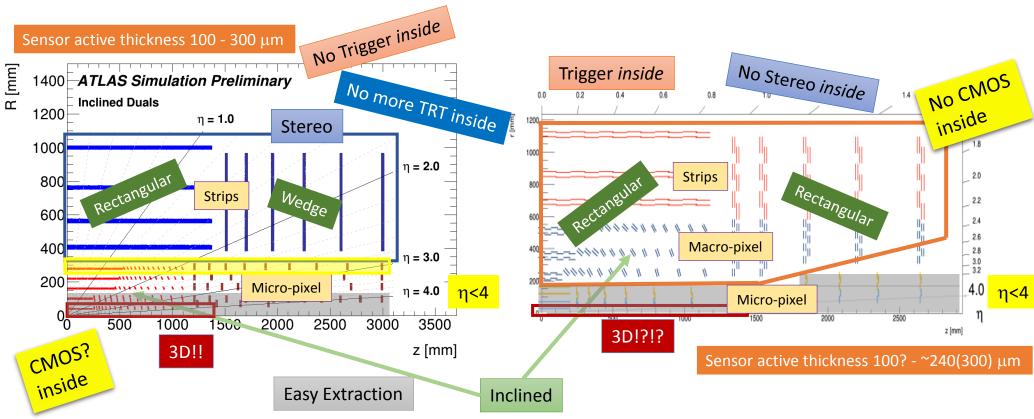
Good ingredients to be light





## The two beasts for LS3





All n-in-p inside with different thicknesses

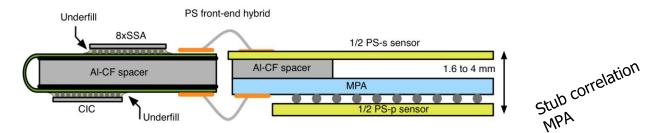
#### Homework:

Why does CMS has 2 more OT layers than ATLAS? Why has CMS one pixel layer less?

## Who triggered this triggering idea?

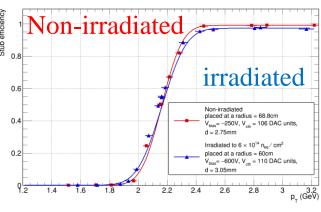
- @ full 40 MHz readout all hits/stubs compatible with p<sub>T</sub>>2 GeV
  - @L1 fully reconstructed tracks (p<sub>T</sub>>2 GeV) with ~ 1 mm vertex res.
- → The need to have Tracking in L1 defines largely the CMS Tracker design!

Thanks to CMS 3.8 T magnetic feld! Stub low pt track reads two sensors



Fun fact: ~80% of data rate is trigger data

Stub efficiency



→ Rate reduction - factor 10-100

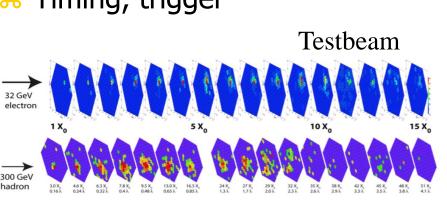
# **Welcome calorimetry**

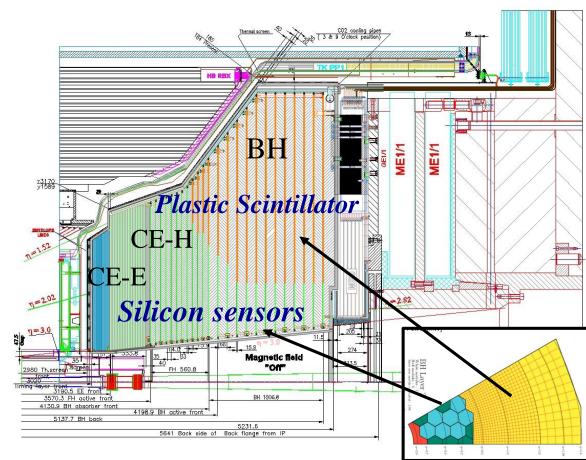
Proudly presented by Shashi Dugad

**5D Calorimeter (X, Y, Z, t, ΔE)** 

- # CMS endcap calorimeter **fka** High Granularity Calorimeter
   HGCAL will operate at T=-30°C
- # The silicon part
  - △ ~600 m<sup>2</sup> of silicon
  - $\triangle$  ~6M channels, 0.5 or 1 cm<sup>2</sup> cells
  - ~25000 modules (8" sensors)
- # + Plastic scintillators

  - △ 400k SiPMs on tile
- # Timing, trigger





Tungsten/Pb

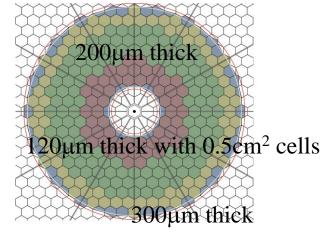
CE-E: 28 sampling layers  $-25 X_0 + \sim 1.3 \lambda$ 

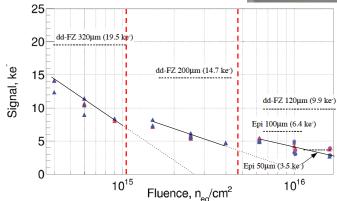
stainless steel

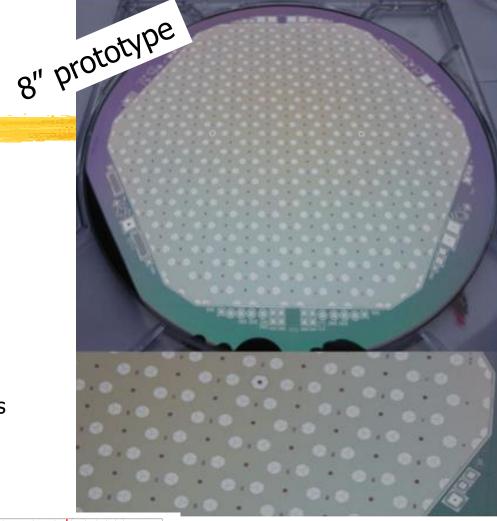
**24** sampling layers –  $9 \lambda$ 

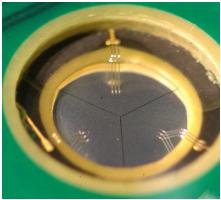
## **HGCAL** sensors

- # Hexagonal to maximize use of area
- $\sharp$  120, 200, 300  $\mu$ m thick n-in-p pad sensors
  - No biasing scheme
- # Cell size  $\sim 0.5$  or  $\sim 1$  cm<sup>2</sup>
  - Smaller cell size in central region
    - □ Due to occupancy and noise
- # Tested *OK* at 1.5x10<sup>16</sup> n<sub>eq</sub>/cm<sup>2</sup> neutron only
- # Cells are wire-bonded to a PCB on top with holes









# Potential Future

3D integration

FCC

ILC

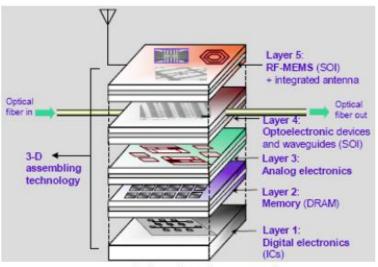
CLIC

Nice picture of a person looking in a crystal ball

## By Valerio Re

## 3D vertical integration

## - one dimension too much for me



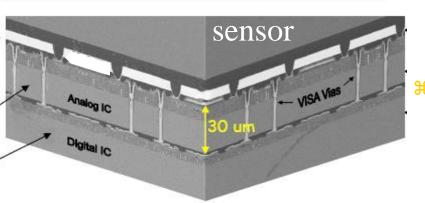
The industry dream

- Denser (smaller form factor)
- # Faster (reduced delay because of shorter interconnects)
- **#** Lower power (smaller interconnect capacitance)
- **K** Lower cost (sizably less expensive than aggressive CMOS scaling)
  - In CMOS electrode and digital must fit into cell
- **X** Integration of dissimilar technologies
  - sensor, analog, digital, optical
  - Monolithic



- Improve resolution
  - shrink pixel size and pitch, down to 20 μm or even less

#### Possible HEP dream (schematic)



#### Preserve or even increase pixel-level electronic functions

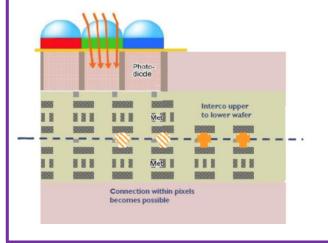
- handling of high data rates, large dynamic range, high resolution analog-to digital conversion and timing, sparsification, large memory capacity, intelligent data processing...: presently this also contributes to limiting the minimum size of pixel readout cells
- Decrease amount of material
  - Thin sensor and electronics (50 -100 µm total thickness)

For ILC??

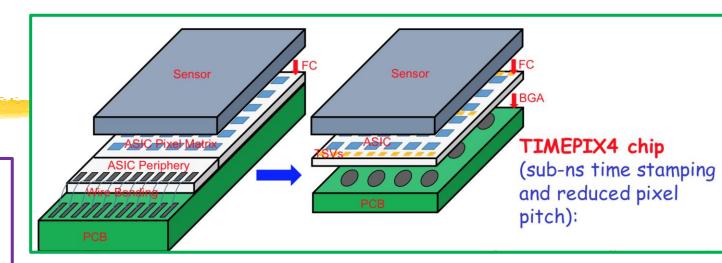
## **3D II**

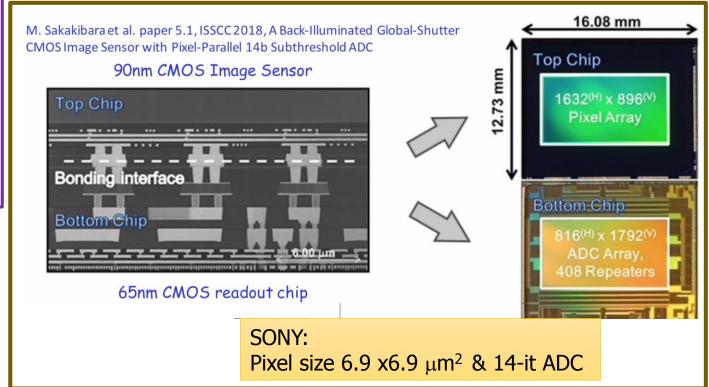
## LFoundry

 now Hybrid / Stacking is developed to improve fill factor, speed, low power, ...



Which is for us?
Which for industry?





# Ok, $10^{16}$ $n_{eq}/cm^2$ works. Let's go to $10^{17}$ $n_{eq}/cm^2$ .

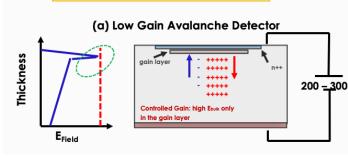
From the OFF: but we need  $10^{18} n_{eq}/cm^2$ 

- $\aleph$  Physicist: **Ok**, thin is good,  $\rightarrow$  let's go thinner 50 $\mu$ m
- # Engineer: Sorry, **NO**, signal is not enough and amplification via very high voltage does not work
- Physicist: **But** it will be amplified after several 10<sup>15</sup> n<sub>eq</sub>/cm<sup>2</sup> and then it stands the voltage change of doping by rad.!
- # Engineer: Sorry, NO, what do I do until then?
- # Physicist: **OK**, then we build an amplification layer a la LGAD
- Engineer: But LGAD works only until several 10¹⁵ n<sub>eq</sub>/cm²
   donor removal
- # Physicst: Haha, and then ...
- Engineer: **OK might work**.
  - Please solve the LAGD fill factor issue allowing small pixels otherwise the S/N is probably still too low.
- Use different amplification mechanism for different fluence levels
- → Control the gain (bias voltage)

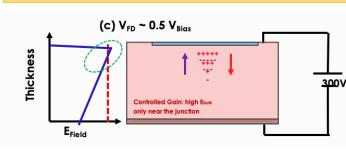
Physicist = Nicolo Cartiglia



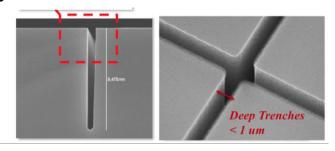
#### Gain via gain layer



### Gain via Vbias and bulk doping

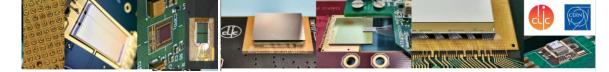


#### Physicst answer:



# **CLIC**

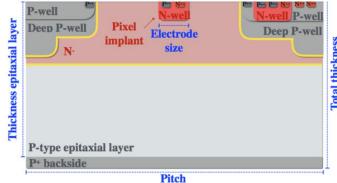
### A=140 m<sup>2</sup> silicon



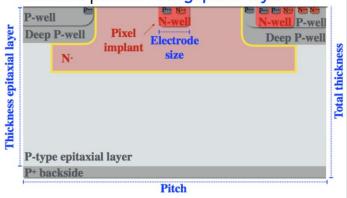
Studied by Ruth Magdalene Munker

- **K** Tracker
  - Spatial res. 7 μm
  - Material 1-2 % X₀/layer
  - □ Timing res O(ns)
- # Vertex
  - Spatial res. 3 μm
    - ≥ 25x25 μm pixels
  - Material 0.2 % X₀/layer
  - □ Timing res O(ns)
- **#** Technologies under investigation:
  - - ⋉ BB + passive sensor
    - □ Glued (capacitively coupled) 
       + active CMOS
  - Monolithic:
    - **⋉** SOI
    - **MINION** HR CMOS
    - Next generation of HR CMOS
- K Large number of studies shown

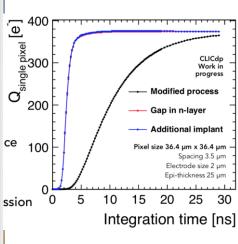




#### Modified process with gap in n-layer:



### Simulated



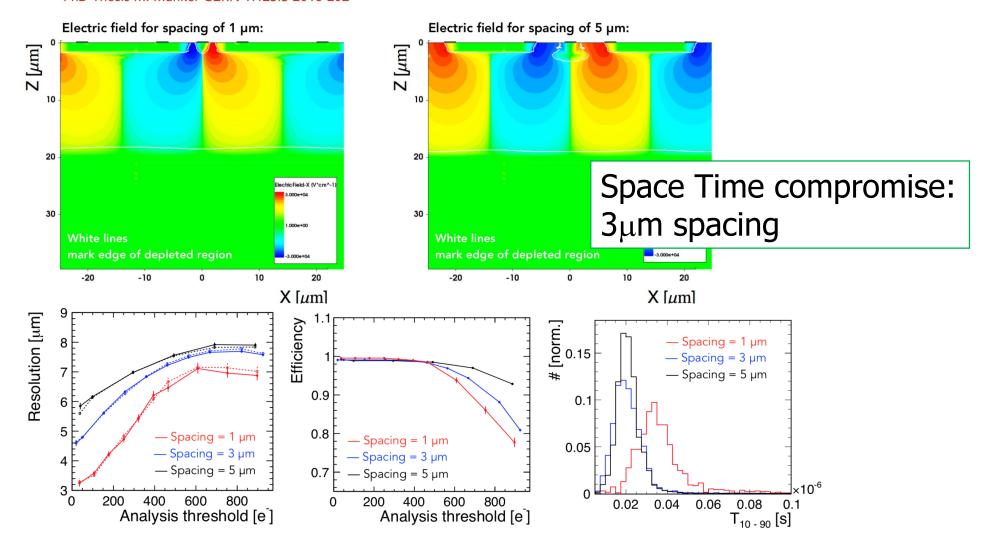
Submitted - MALTA

Shape field - helps with timing and corners

# **CLIC**, one representative study

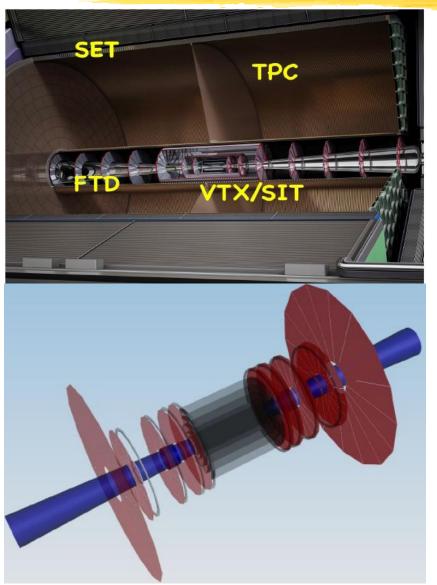
Results of 2D TCAD simulations for different spacings for the modified process:

PhD Thesis M. Munker CERN-THESIS-2018-202

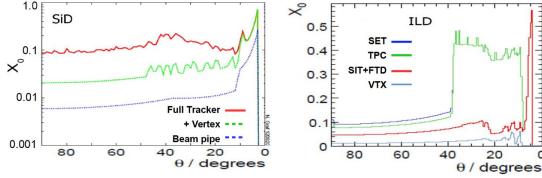


### By Gagan Mohanty for the SiD and ILS collaboration

## ILD and SiD @ ILC usual question: which is which



100MeV track reconstruction Super low material budget



#### Current sensor R&D:

- $20x20 (16x16) \mu m^2 pixel$
- DEPFET, FPCCD, SOI and CMOS and 3D vertical integration

What is the need of hour?

Political decision in Japan and rest-of-the world

### Explained to you by Estel Perez Codina

## FCChh aka I need another crystal ball

- # FCC-hh (pp-collider)
  - △ 100 km long tunnel (Geneva area)
  - ∼16T magnets
  - $\triangle$   $\sqrt{s}=100\text{TeV}$
- # How do we build a detector suitable for 100 TeV pp collisions?

Parameter	(HL) LHC	FC	FCC-hh	
Collision vs energy [TeV]	14	1	100	
Dipole field [T]	8.33	:	16	
Circumference [km]	26.7	97	97.75	
# IP	2 & 2	2	2 & 2	
Bunch spacing [ns]	25	25	25 (5)	
Luminosity/IP [10 <sup>34</sup> cm <sup>-2</sup> s <sup>-1</sup> ]	(5) 1	5	30	
# Events/bunch crossing	(135) <mark>27</mark>	170	<b>~1000</b> (200)	

- "Baseline" "Ultimate"
- 10 years 15 years

- # High precision **tracking up to |η|~4** (is 2.5 at LHC)
- **10-20% for 10 TeV tracks** (10% at 1TeV at LHC)
- **Reconstruct tracks in the dense environments** created by boosted jets.
- **#** Provide efficient **b**, **c**, **T-tagging**
- # Etc.

- # Sensor 10<sup>18</sup>n<sub>ea</sub>/cm<sup>2</sup>
- **¥** Spatial resolution 10μm everywhere

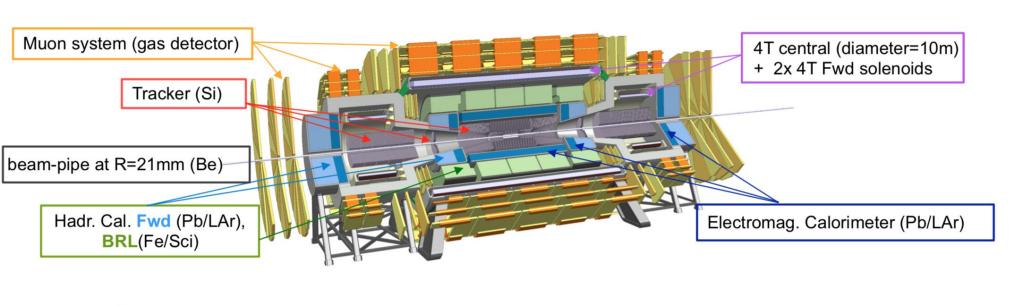
We have a new challenge!

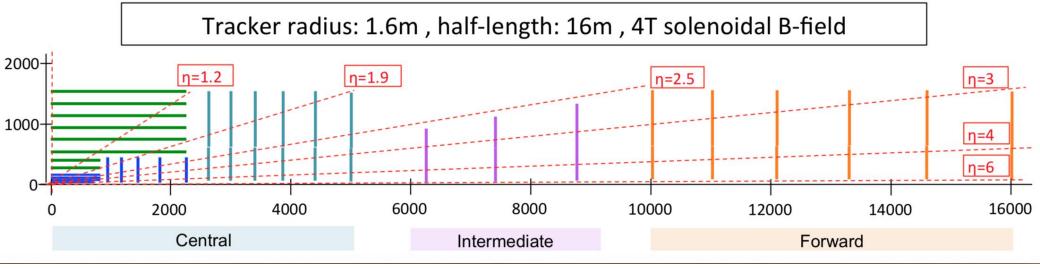
O(20) ab<sup>-1</sup> per experiment

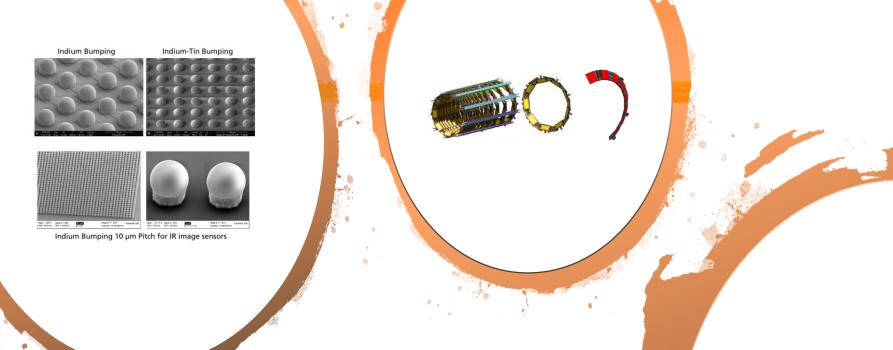
in **25 years** of operation

NEXT: FCC Conceptual Design Report by the end of 2018

# Reference detector layout



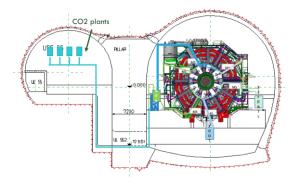




Cooling Mechanics

Interconnection

# This morning



#### WHERE?



LHCb Velo 1.6 kW @ -25 C





#### In the near future ...



Source: The LHCh Collaboration, LHCh VELO Upgrade Technical Design Report, CERN/LHCC 2013-021, Nov 2013



Source: H. Ye" Thermal Test and Monitoring of the Belle II Vertex Detector" Forum on Tracking Detector

Source: A. Lymanets et al, "The Silicon Tracking System of the CBM at FAIR: detector development and system integration" TIPP 2014



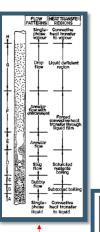
CO<sub>2</sub> probably also inside Paola Tropea



VERTEX 2018 - Chennai

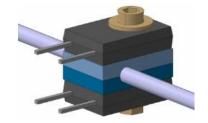
#### Then there are the details

CMS Pix Phase I upgrade 7 kW @ -25 C

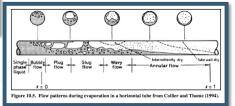


Vertical pipe

Horizontal pipe \_\_\_



Pre-heater concept tested (2x10W resistors clamped to pipe)



#### AND THEN? AT HL-LHC...

PAOLA.TROPEA@CERN.CH



Outer Tracker

nner Tracker

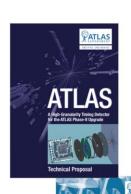
Barrel Timing Layer

ndcap Timing Laye

VERTEX 2018 - Chennai





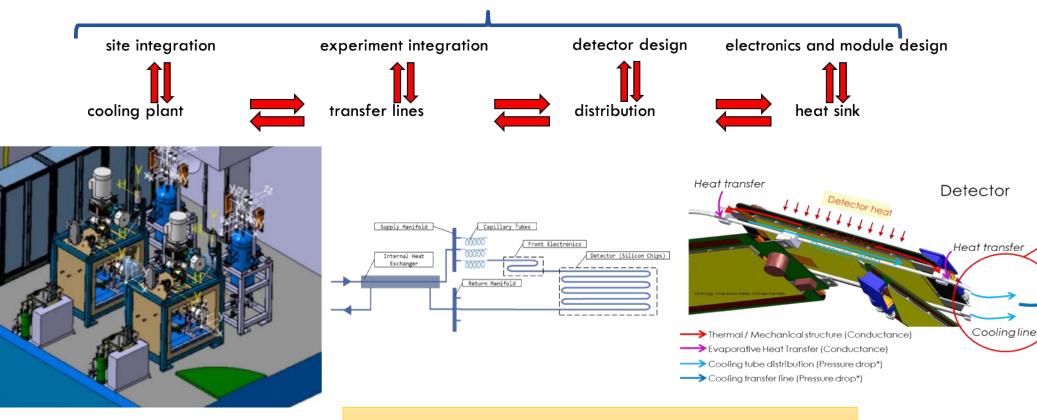




A good order of magnitude bigger & more complex than ever....

# CO<sub>2</sub> systems - The design chain

# The complexity of an <u>evaporative</u> system: each design modification on a components would influence the behaviour of the full system: how?



Need a lot of chats & coffee

## **Advanced mechanics for silicon tracker**

# Mechanical properties are driven by needs of Track Based Alignment (TBA)

# Thermal properties are driven by radiation damage issue

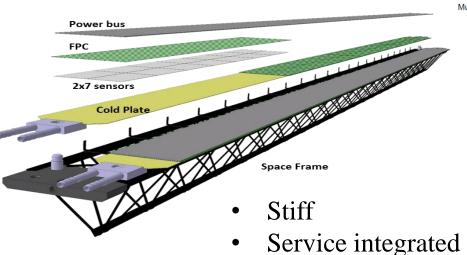
□ bring cooling as close to heat sources as possible

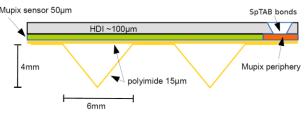
# Future experiments require  $0.1X_0/1X_0$  per layer

Material-optimized layouts do require tilted module geometries

Services must be tightly integrated into structures

Stiffness optimization and material optimization





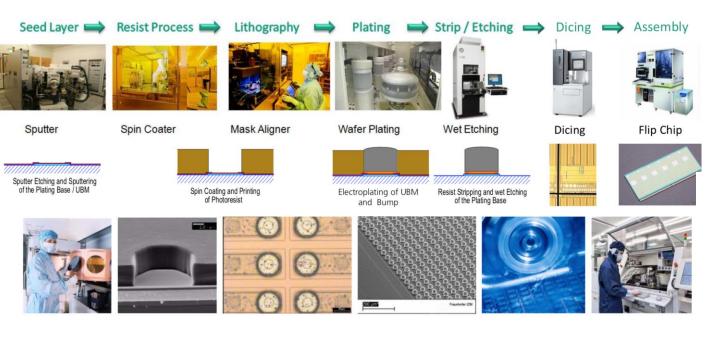
Ultra low mass

I do not like mechanics and services – <u>too heavy</u>

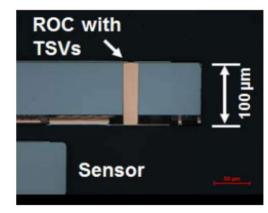
tilted

# Hybridization techniques

#### Wafer Level Packaging: Micro Bumping and Hybridization Process



- For the immediate future, we go with **BB** and **TSV**
- # Later (see 3D), we want **more**



Cross section of ROC-Sensor Module, with Cu filled TSV





Low cost Standard >500µm > 50µm

Advanced Challanging < 50µm < 20µm



@ IZM – thank you always being patient with us

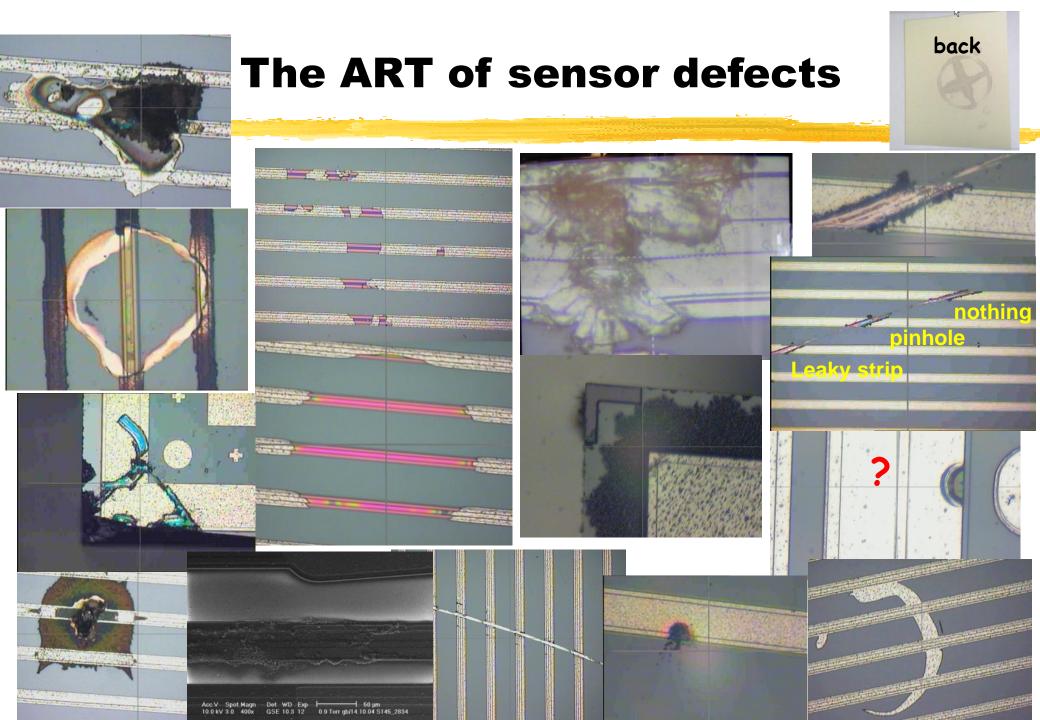
# Organisers Thank You

# GREAT Job!! A+++++



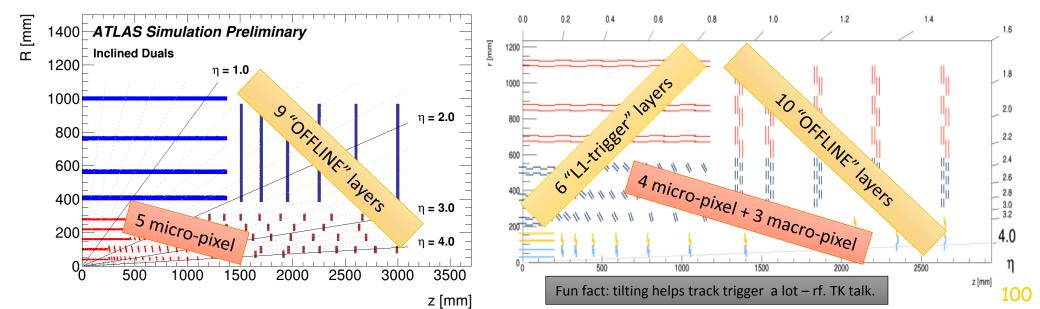


# Backup



## Please, explain the numbers of layers

- **38** Why has CMS 6 and ATLAS *only* 4 outer layers?
  - You need to count "OFFLINE" and "L1-trigger" layers separately!
  - With a fine granular pixel, only few outer layers are needed to measure p<sub>⊤</sub>
    - **区** Few = enough + redundancy
      - -- 4 seems a perfect number even for an inner 4-layer pixel detector
- Why ATLAS has 5 pixel layers and CMS only 4?
  - △ CMS has in fact 7 "pixel" layers, counting the 3 PS-layer with 1.5mm macro-pixels.



## Next to the beam pipe

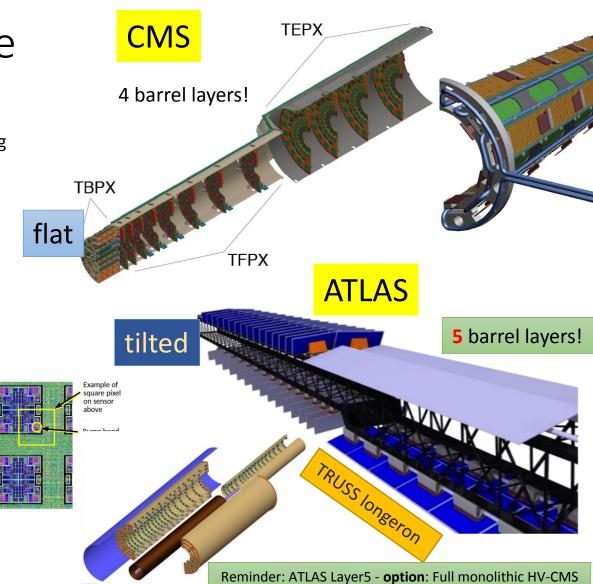
#### Many commonalities:

- "Classical" hybrid pixel detectors with bump-bonding
  - THIN Planar n-on-p or 3D detectors (inner layers)
    - Both need coating to prevent sparking
  - Common R&D on chip RD53A 65nm TSMC
  - Modules: Doublets, Quads chip of singlets (ATLAS only)

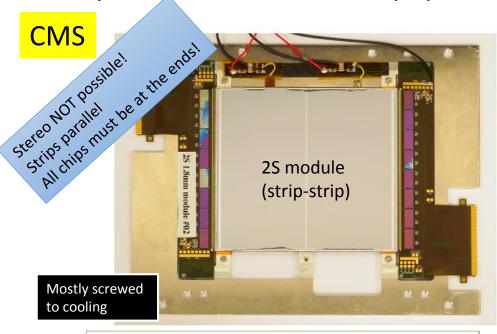
**RD53** 

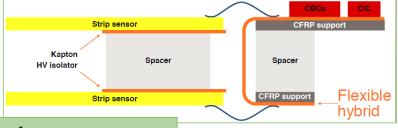
Digital "sea"

- Different pixel cell layouts being tested:
  - 50 x 50 μm preferred by ATLAS
  - 25x100 μm preferred by CMS
- Serial Powering (part of RD53)
- Both detectors up to  $\eta=4$
- Both easily extractable (half-shells)
- Surface: 2\*CMS < 1\*ATLAS</li>



## Away from the beam pipe





Interesting feature: The module is the system! No other electronics!

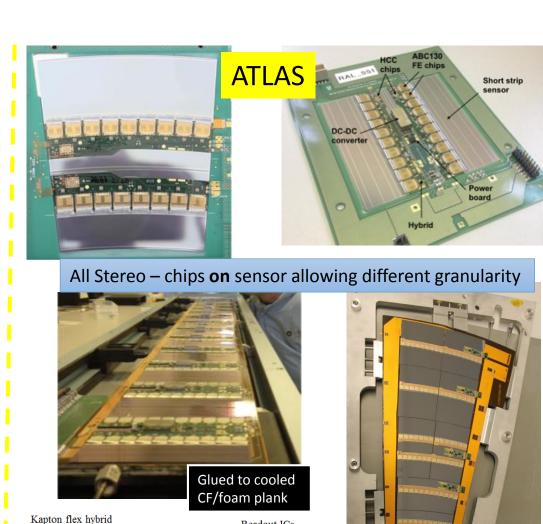
No full-size PS prototype yet

Si Strip

sensor

Carbon fiber

facing



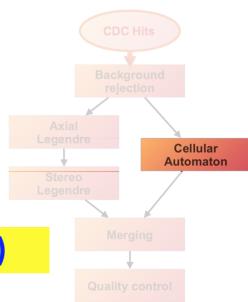
Readout ICs

Ti coolant tube

High T conductivity foam

#### Cellular Automaton

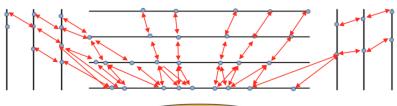




## What is Cellular automaton (CA)

#### The CA is a track seeding algorithm designed for parallel architectures:

- In a CA, a network of cells evolves in discrete time steps from an initial state according to predefined rules, depending only on the values of the cells in the local neighborhood.
- A graph of all the possible connections between layers is created
- Doublets are created for each pair of layers (compatible with a region hypothesis)
- A cell is defined as a segment linking three hits.
- Neighborhood rules : pair of hits in common and similar eta
- Evolution rules: At each time step a cell increases its state if on its left it has a neighbor with the same state.
- The neighbor fit triples are joint in a longer seed
- · Fast computation of the compatibility between two connected cells
- No knowledge of the world outside adjacent neighboring cells required, making it easy to parallelize



MVA filters or hand crafted features

• Hit connection through bridging

**Clusters** 

**Triplets** 

**Segments** 

- Build segments from individual hits in each super layer
- Build tracks from segments

## **CMS**

- **seed generation:** it provides initial trajectory candidates
  - internal to the tracking detector (inner tracker or muon system)
  - external by using input from other detectors (calorimeters).
- □ building trajectories starting from seeds: it is based on the Kalman filter formalism and consists of:
  - layer navigation provides a list of reachable layers from the current layer in a given direction.
  - propagator: each reachable layer provides measurements (rec hits)
     compatible with a trajectory candidate
  - updator: each compatible measurement is combined with the corresponding predicted trajectory state

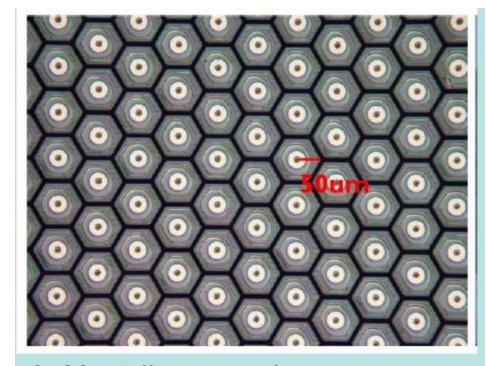
## And then we have 3D trenches for timing

#### Advantages:

- High average field
- Uniform weighting field
- Initial pulse (largely) independent of position
- Very Radiation Hard

#### • Drawbacks:

- Possible fabrication problems
- High electrode capacitance



A. Montalbano et. al. NIMA 765 (2014), 23

## CMS HGCAL

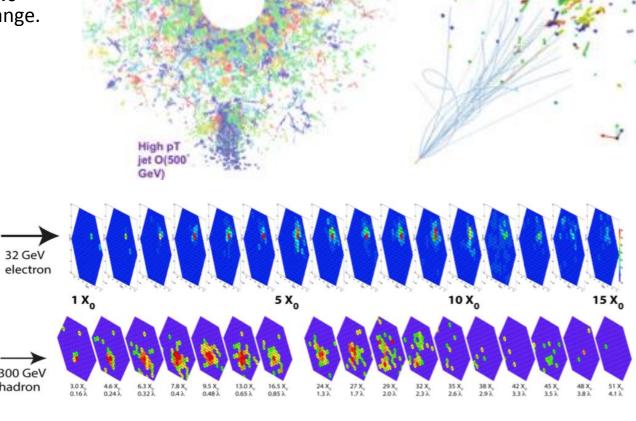
- Not a MIP detector
  - Some smaller calibration cells
  - Allows for MIP tagging 'following' a 'track'

Flat

300 GeV hadron

x,y viev

- Very high dynamic range 1-5000 MIPS
  - CSA Charge amplifier/shaper plus a TOT Time- over-Threshold circuit. This allows to span the necessary huge dynamic range.
- Intrinsic timing resolution of
  - <50 ps for S/N>10
  - ~20 ps for S>20 MIPS
  - For charged and neutral particles
- L1 Trigger



acks and clusters identifiable

Longitudinal (3D) shower view

Concept works, see test beam