Operational Experience of the ATLAS SCT and Pixel Detector

Kathrin Becker (Freiburg) on behalf of the ATLAS collaboration
Vertex 2018, October 22, 2018
The ATLAS Inner Detector

- **Transition Radiation Tracker (TRT):**
  - 350000 channels
  - 130 μm track resolution
  - 4 mm element size

- **Semi Conductor Tracker (SCT):**
  - 6.3 million channels
  - 17 x 570 μm \((r\phi \times z)\) resolution
  - 130 μm x 12 cm element size

- **Pixel detector/Insertable B-Layer (IBL):**
  - 92 million channels (80/12)
  - 10 x 115 μm / 8 x 40 μm \((r\phi \times z)\) resolution
  - 50 μm x 400 μm/250 μm element size

Focus on Silicon detectors
The Pixel Detector

- 3 hit system up to angular coverage of $|\eta| < 2.5$
- 3 barrels and 2 x 3 endcap disks
- $C_3F_8$ evaporative cooling
- 1.7 m$^2$ of silicon
- 1744 pixel modules

Each pixel module consists of:

- 1 planar n-on-n sensor 60.8 x 16.4 mm active area, 250 $\mu$m thick, 46080 pixels
- 16 FEI3 front-end chips plus one controller (0.25 $\mu$m CMOS)
  - Front-ends are bump-bonded to the sensor.
  - Charge measurement using 8-bit ToT information.
- 1 flex that provides electrical connections
- Data rate per module: 80-160 Mbps

Radiation-hard: $1 \times 10^{15}$ MeV $n_{eq}$ cm$^{-2}$
50 Mrad
IBL – Insertable B-Layer

- Innermost layer of the pixel detector, coverage of $|\eta| < 3$
- New in LHC Run 2, installed in 2014
- 14 staves, 0.2 m² of silicon
- CO₂ evaporative cooling
- 280 IBL modules
- Planar sensors (central) and 3D sensors (forward)

Each IBL module consists of:
- Sensor:
  - Planar slim edge n-on-n sensor, 200 μm thick
  - 3D n-on-p sensor with 2 electrodes per pixel, 230 μm thick
- 2 or 1 FEI4 front-end chips (0.13 μm CMOS)
  - Front-ends are bump-bonded to the sensor.
  - Charge measurement using 4-bit ToT information
- 1 flex that provides electrical connections
- Data rate: 160 Mbps

Radiation-hard
$5 \times 10^{15}$ MeV $n_{eq}$ cm$^{-2}$
250 Mrad
Each SCT module consists of:

- Two strip sensors crossing at 40 mrad
- Single-sided p-in-n sensor, 285 µm thick, 768 strips
- 2 x 6 ABCD front-end chips (0.8 µm biCMOS)
  - Binary readout: hit = signal > threshold
  - 3 consecutive time bins sampled per trigger
- Data rate: 40 Mbps
LHC Roadmap and Performance in 2018

- Run 3 prediction: $2.5 \times 10^{34} \text{ cm}^{-2} \text{s}^{-1}$
- Pile-up: $\mu = 61.5$

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**ATLAS Online Luminosity**

- Peak Lumi: $21.4 \times 10^{33} \text{ cm}^{-2} \text{s}^{-1}$
- Design: $\times 2$

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**ATLAS Online Luminosity**

- Peak Interactions/BX
- Design: $\times 2.5$

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**ATLAS Online Luminosity**

- Delivered Luminosity (fb$^{-1}$)
- Month in Year

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LHC Roadmap and Performance in 2018

→ LHC performs superbly well above design specs

Operational challenges:
• Bandwidth: Tackled mainly in 2017
• Radiation dose:
  • Radiation damage
  • Impact of Single-event upsets (SEU)

Run 3 prediction: $2.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$
Pile-up: $\mu = 61.5$
ATLAS Silicon Trackers in 2018

- Detectors in great shape, even after 10 years!
- Operational fraction:
  - IBL: 99.3%
  - Pixel: 94.9%
  - SCT: 98.6%

- 2018 has been the most intense luminosity production year yet...
  ... Pixel/IBL and SCT have become even better!!
- Deadtime is at 0.15% for Pixel/IBL and 0.09% for SCT
  → Improved with respect to previous years due to continuous improvements in firmware and DAQ
- High quality data (99.7%)

Data quality fraction per sub-detector:

<table>
<thead>
<tr>
<th>Inner Tracker</th>
<th>Calorimeters</th>
<th>Muon Spectrometer</th>
<th>Magnets</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel</td>
<td>SCT</td>
<td>TRT</td>
<td>LAr</td>
</tr>
<tr>
<td>99.7</td>
<td>99.7</td>
<td>100</td>
<td>99.5</td>
</tr>
</tbody>
</table>

Made possible by diligent efforts by the respective operation teams
Upgrade of Pixel Readout to IBL Readout system

<table>
<thead>
<tr>
<th>Layer</th>
<th>Old rate</th>
<th>New rate</th>
<th>Intervention</th>
</tr>
</thead>
<tbody>
<tr>
<td>Layer 2</td>
<td>40 Mbps</td>
<td>80 Mbps</td>
<td>WS 2015/2016</td>
</tr>
<tr>
<td>Layer 1</td>
<td>80 Mbps</td>
<td>160 Mbps</td>
<td>WS 2016/2017</td>
</tr>
<tr>
<td>Layer 0</td>
<td>160 Mbps</td>
<td>160 Mbps</td>
<td>WS 2017/2018</td>
</tr>
<tr>
<td>Disks 1,3</td>
<td>80 Mbps</td>
<td>80 Mbps</td>
<td>WS 2017/2018</td>
</tr>
<tr>
<td>Disks 2</td>
<td>160 Mbps</td>
<td>160 Mbps</td>
<td>WS 2017/2018</td>
</tr>
</tbody>
</table>

In 2018 unification of the Readout system brings operational advantages regarding maintenance and developments.

All layers expected to have < 70% bandwidth usage at 100 kHz trigger rate for $\mu = 61.5$! → Good for Run 3!
Bandwidth strategy - SCT

1. Front-end links limit
   - If no redundancy in readout → safe for Run 2 and Run 3
   - In case of redundancy apply chip masking to avoid module-wide error → avoid “double hole” impacting efficiency

2. S-Link
   - Remapping fibres in 2017 to optimize bandwidth usage
   - Running per default in supercondensed mode → safe for Run 2 and Run 3
   - Pile-up of 70 is a hard limit. → Fine, if LHC does not over-perform in Run 3
Radiation Damage – Impact on Operations

• Leakage currents
• Depletion voltage
• Charge collection
• Noise & gain

• Single Event Upsets (SEU)
  • Rate is function of instantaneous luminosity

Addressed via static configurations, e.g. determined by calibration or by collision data → changeable only between LHC runs

Addressed on-the-fly during an LHC run
Modelling of radiation damage

- Assess radiation damage of Pixel/IBL and SCT to project long-term health
- Increase in $V_{\text{depl}}$ and $I_{\text{leak}}$
- Good agreement with the “Hamburg” model and “Sheffield-Harper” model

<table>
<thead>
<tr>
<th></th>
<th>End of Run 2 [MeV n_{eq} cm^{-2}]</th>
<th>Limit [MeV n_{eq} cm^{-2}]</th>
</tr>
</thead>
<tbody>
<tr>
<td>IBL</td>
<td>$\sim 9 \times 10^{14}$</td>
<td>$5 \times 10^{15}$</td>
</tr>
<tr>
<td>B-Layer</td>
<td>$\sim 4.5 \times 10^{14}$</td>
<td>$1 \times 10^{15}$</td>
</tr>
</tbody>
</table>

- IBL has room until limit
- B-Layer possibly already at >40% of its dose
Radiation effects on charge collection

Pixel hit occupancy per unit of \( \mu \)
- Observe decrease as function of integrated luminosity
- Caused by drop in charge collection efficiency and decrease of time over threshold (ToT)
- Cause is charge trapping in pixel sensor

Operational measures
- Increase the HV
- Decrease the thresholds → Interplay with bandwidth
- Set per production year

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Run 2 Bias Voltage Evolution:

- **Ensure detectors are fully depleted**
- Regular increase in IBL and B-layer
- 2018: First increases for Layer-2, Disks, and SCT Barrel 3

### Threshold evolution

- **Recover charge efficiency degradation**
- Threshold lowered for IBL, B-layer, and disks
- 2018 config as efficient as 2015 config

<table>
<thead>
<tr>
<th>Layer</th>
<th>2017</th>
<th>2018</th>
</tr>
</thead>
<tbody>
<tr>
<td>IBL</td>
<td>2500e, ToT&gt;0</td>
<td><strong>2000e, ToT&gt;0</strong></td>
</tr>
<tr>
<td>B-layer</td>
<td>5000e, ToT&gt;5</td>
<td><em><em>4300e</em>, ToT&gt;3</em>*</td>
</tr>
<tr>
<td>Layer-1</td>
<td>3500e, ToT&gt;5</td>
<td>3500e, ToT&gt;5</td>
</tr>
<tr>
<td>Layer-2</td>
<td>3500e, ToT&gt;5</td>
<td>3500e, ToT&gt;5</td>
</tr>
<tr>
<td>Pixel disks</td>
<td>4500e, ToT&gt;5</td>
<td>3500e, ToT&gt;5</td>
</tr>
<tr>
<td>SCT Barrel 3</td>
<td>150 V</td>
<td>150 V</td>
</tr>
</tbody>
</table>

* central |η|: 43000e, forward |η|: 5000e
Noise – Example SCT detector

• Noise in SCT stable over the years
• Stability ensured by regular calibrations shifting the threshold

Frequent steps in noisy channel counts due to calibration results applied
Single Event Upsets in front-end chips

- Registers in Pixel/IBL have triple redundancy and majority logic to protect against SEU. SCT has no protection.
- SEU in front-end chip observed for IBL and SCT
  - SEU → change in configuration
  - Decrease or increase in occupancy
- Mitigation: Chip reconfiguration
  - SCT: every 90 lumiblocks (1 per hour)
  - IBL: every 5s at reset of L1 ID → no increase of busy time
Single Event Upsets in single pixels

- SEUs can corrupt single pixel registers in IBL
- Produces quiet and noisy pixels → increases during data taking
- Method now developed that reconfigures pixel configurations together with frontend (every 5s)
- Not yet deployed but ready for Run 3

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SEUs and Desynchronization – Example SCT

- Energy deposition in p-i-n diode causes bit flip of trigger → trigger lost, desynchronization of module
- Error flag assigned to module → watchdog then reconfigures the individual module and includes it back into data taking
- Module recovery restricts count of link errors to < 5 at any time
- Remark: desynchronization is not just caused by SEUs
- Similar measures in place for Pixel/IBL

Power supply crate trip → no power to 48 modules
Read-Out Driver reconfigure → no data from 36 modules

ATLAS SCT Preliminary
$\sqrt{s} = 13$ TeV, data 2017
Pixel reverse annealing

• Reverse annealing is a serious issue for the Pixel detector

• Already end-of-year shutdowns have effects → WS 2017/2018 only 10 warm days

• If Pixel Detector is warm during Long-Shutdown 2 → depletion voltage will increase far beyond the operational limit of 600 V

• It is crucial to keep the detector cold as long as possible in Long-Shutdown 2

Predictions for b-layer
SCT depletion voltage projection

- Assuming 60 fb$^{-1}$ per year in Run 3 (on the low side)
- $V_{\text{depl}}$ larger for warm scenario and $I_{\text{leak}}$ slightly smaller
- Cooler operation temperature would decrease $I_{\text{leak}}$
- Sufficient headroom for Run 3
- But: would like to keep detector cold during Long-Shutdown 2 to minimize HV in Run 3
Planes for Long-Shutdown 2

• Pixel VCSELs on opto-boards have been dying since 2016, possibly due to humidity, 14 dark channels this year
  → All opto-boards will be exchanged to be safe for Run 3
  → Requires access to the detector

• SCT has seen faults in power supplies during Run 2 from the 48V power packs and the 48V/5V DC/DC converters
  → DC/DC converters could be reproduced and will be exchanged for the full system
  → Power packs (commercial) do not exist anymore, replacement system in development to be installed during 2020 for half of the detector

• Improve calibrations to deal with increase of radiation damage in Run 3
Conclusion

• Data taking of Run 2 is almost concluded. Pixel and SCT are more than 2/3 through their journey!

• Pixel and SCT: still in great shape after 10 years

• Radiation damage more and more visible
  • Increase of bias voltage to ensure full depletion
  • Changes in pixel threshold to ensure good charge collection efficiency
  • SEU effects well under control

• Run 2 operations have been a success
  • Improvement in deadtime and data quality via upgrades on hardware and firmware of the readout and the DAQ system
Thank you for your attention!
BACK-UP
• Desynchronisation under control (< ~1% level) despite higher luminosity in 2017
Calibration - IBL

• High luminosity impacts significantly Pixel and IBL response over time.

• Regular monitoring and tuning of pixel detector allows to maintain running conditions and optimise performance.

• It involves pixel team as a whole to monitor and control evolution throughout Run 2.

• Run-3 conditions will be even more challenging. Experience and feedback from Run-2 will be useful.

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• The occupancy is the number of hits per pixel per event, and mu is the number of interactions per bunch-crossing for events collected by a zero-bias trigger in 2018.
Pixel connection scheme

30 modules (dark channels) were recovered over YETS