RADIATION HARDNESS FOR RD53

Luis Miguel Jara Casas on behalf of the RD53 collaboration

OUTLINE

1. Introduction
2. RD53A chip
3. Radiation tolerance
4. TID Radiation test results with RD53A
    1. Power measurements
    2. Analog front end measurements
    3. Ring oscillator measurements
5. Single Event Upsets
6. Conclusions and next plans

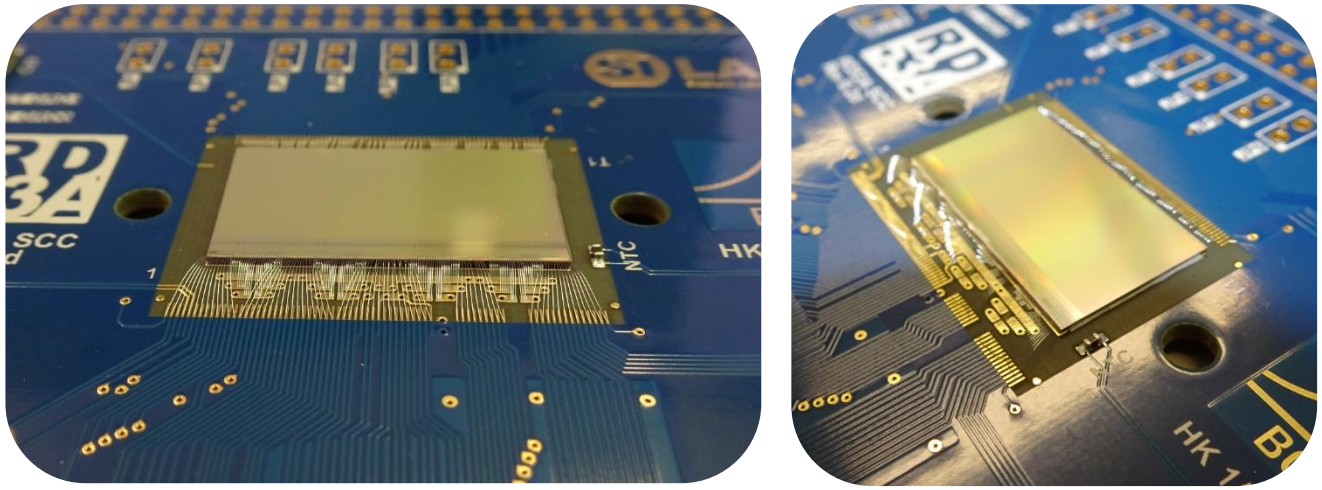
1. INTRODUCTION

- The RD53 collaboration [1] is a joint effort between ATLAS and CMS communities.
- For the design of the pixel readout chips for the innermost layers of particle trackers at future HL-LHC for high energy physics experiments.
- RD53A goals:
  - Comprehensive understanding of radiation effects in the 65 nm technology chosen [2].
  - The development of tools and methodology to efficiently design large complex mixed signal chips
  - Development and characterization of a full size readout chip featuring a 400×400 pixel array with 50 µm pitch
- Conformed by 24 institutions from Europe and USA

(Bari, Milano, Padova, Bergamo-Pavia, Pisa, Perugia, Torino)

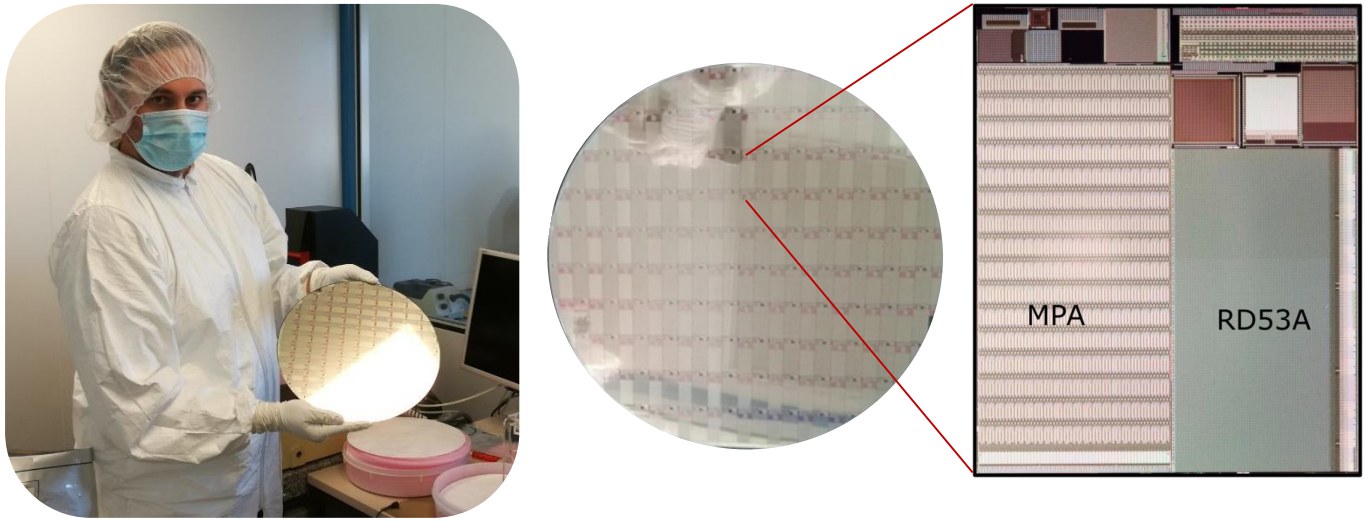
2. RD53A CHIP

- The RD53A is intended to demonstrate, in large format IC, the suitability of the chosen 65nm CMOS technology for the innermost layers of particle trackers for the HL-LHC upgrades of ATLAS and CMS
- RD53A is not intended to be a final production chip.
- It will form the basis for production chips of ATLAS and CMS.
- It contains design variations for testing purposes
  - Three analog front-end flavours
  - Two digital readout architectures
- Submitted at the end of August 2017 in a shared engineering run with CMS MPA and other test chips for cost sharing (12")



The RD53A chip

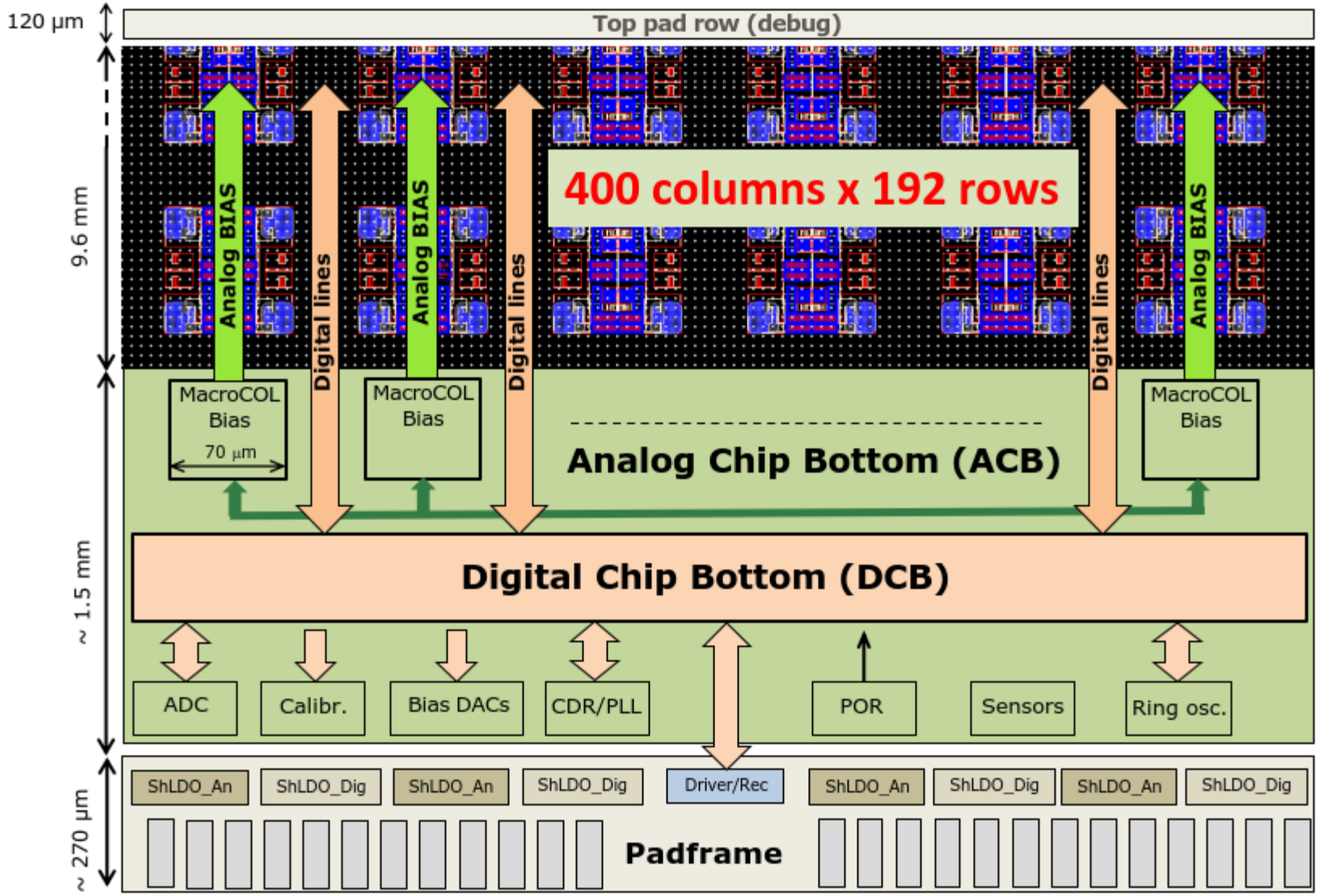
- Size: 20 x 11.8mm^2 (half size of production chip)
- 400 columns x 192 rows (50x50 µm^2 pixels)



First 12" wafers at CERN with RD53A

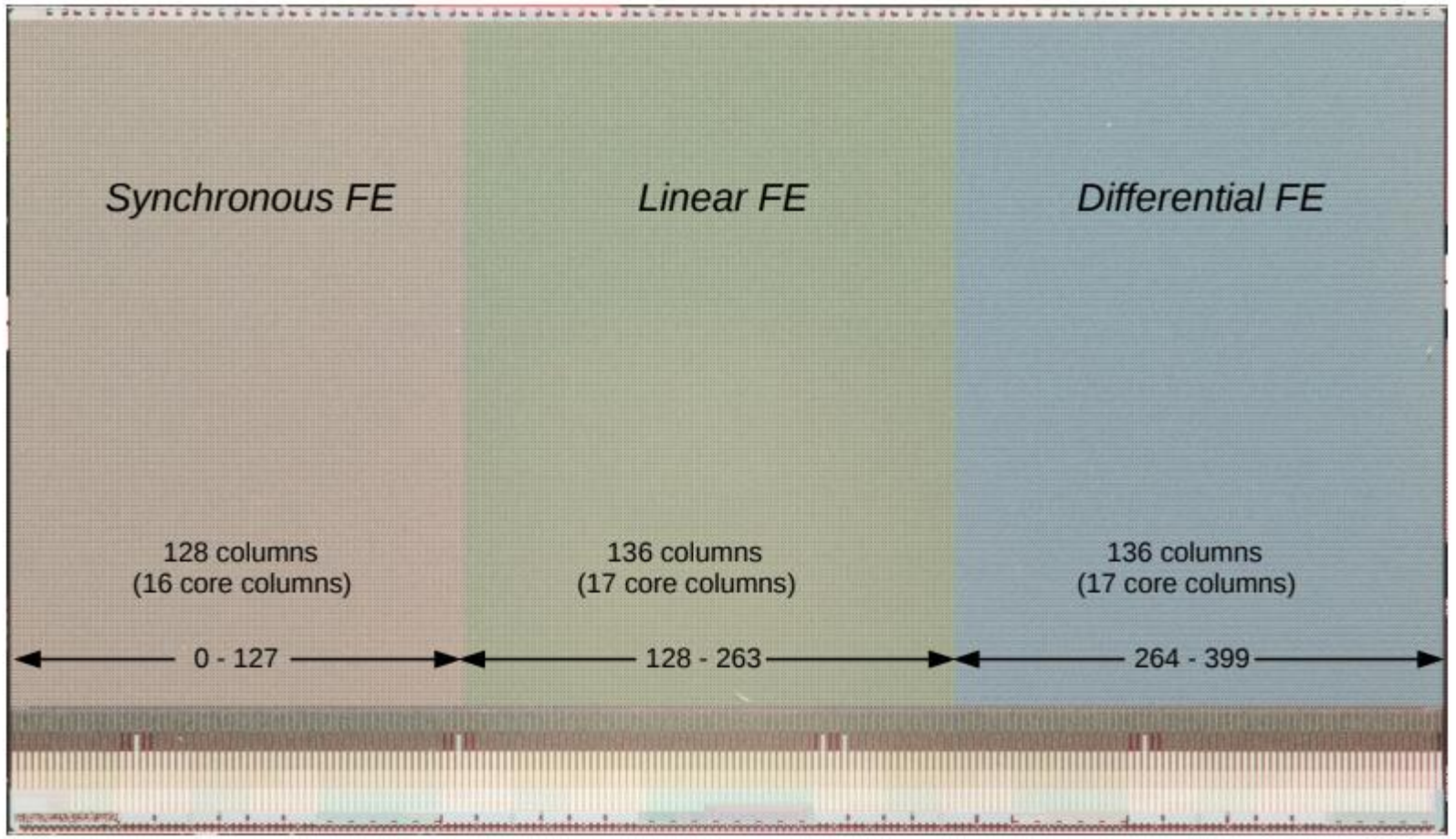
2. RD53A CHIP

RD53A functional floorplan



2. RD53A CHIP

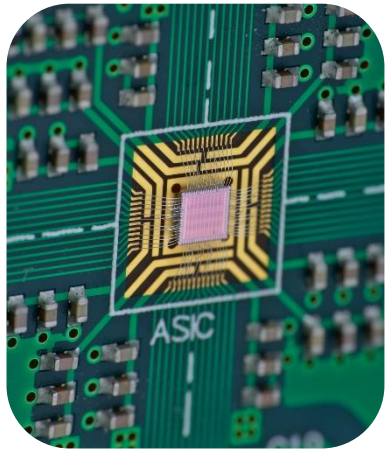
Front-end flavours in RD53A



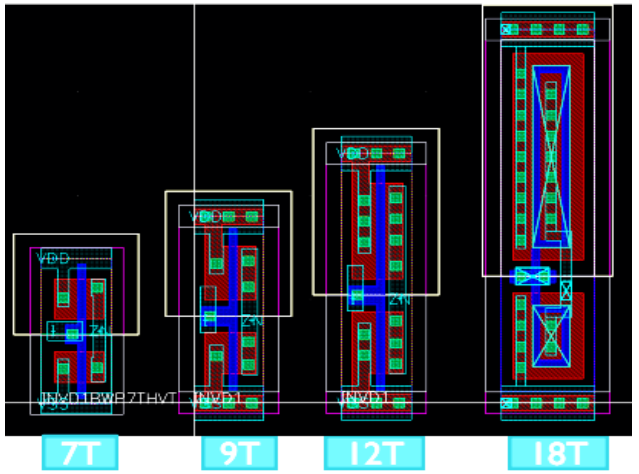
- 3 Analog Front-end flavours: Synchronous, Linear and Differential.
- Each analog front-end flavour takes almost one third of the matrix.
- More details in Lino Demaria's talk: https://indico.cern.ch/event/710050/contributions/3161658/ (Thursday 25th)

3. RADIATION TOLERANCE

- RD53A was designed with a guarantee of meeting specs at 500 Mrad by making and using simulation models and treating radiation damage as an additional corner in the design.
- 200Mrad and 500Mrad simulation models were developed to 'predict' the circuit behaviour during design phase.
- Significant radiation damage above 100Mrad:
  - Analog: transconductance, Vt shift:
    - Analog design guidelines:
      - Wp≥300nm
      - Lp ≥120nm
      - Ln ≥ 120nm
  - Digital: speed degradation.
- Extensive radiation campaigns have been carried out to qualify the technology:
  - Prototypes of all IPs and Front-ends, small scale demonstrators: FE65_P2, Chipix 65.
  - DRAD chip [3]: test to study the effects on standard cells.



The DRAD chip



Layout of the same gate for different libraries in DRAD chip. The height of the libraries are 1.4µm in 7T, 1.8µm in 9T, 2.4µm in 12T and 3.6µm in 18T.

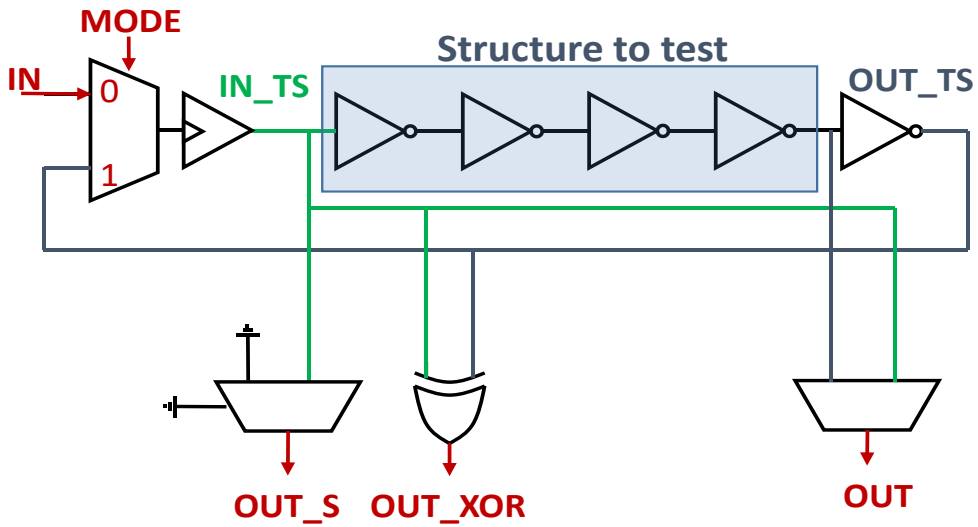
DESCRIPTION OF THE LIBRARIES OF THE DRAD CHIP		
Library	**Description**	
7T_HVT	7-tracks, High V_t, foundry library W_p ≥150nm, W_n ≥ 150 nm, L = 60nm	FOUNDRY LIBRARY
9T_HVT	9-tracks, High V_t, foundry library, W_p ≥210nm, W_n ≥ 190 nm, L = 60nm	
9T_NVT	9-tracks, Normal V_t, foundry library , W_p ≥210nm, W_n ≥ 190 nm, L = 60nm	
9T_NVT_2W	9-tracks, Normal V_t, modified width: W_p ≥300nm, W_n ≥ 190 nm, L = 60nm	MODIFIED FROM FOUNDRY LIBRARY
12T_HVT	12-tracks, High V_t, custom: W_p ≥ 700nm, W_n ≥ 390 nm, L = 60nm	
12T_NVT	12-tracks, Normal V_t, custom: W_p ≥ 700nm, W_n ≥ 390 nm, L = 60nm	
12T_LVT	12-tracks, Low V_t, custom: W_p ≥ 700nm, W_n ≥ 390 nm, L = 60nm	
12T_NVT_2L	12-tracks, Normal V_t, custom: W_p ≥ 920nm, W_n ≥ 410 nm, L = 130nm	
18T_LVT	18-tracks, Low V_t, ELT transistors W_p ≥ 3740nm, W_n≥1420nm, L = 60nm	CUSTOM MADE

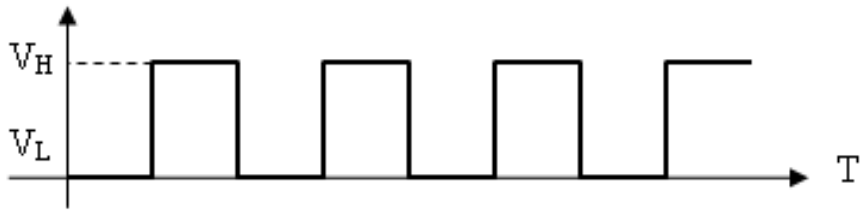
Libraries studied in DRAD chip

3. RADIATION TOLERANCE

DESCRIPTION OF THE STANDARD CELLS INCLUDED IN EACH LIBRARY	
Standard Cell	**Description**
INVD1	Inverter with driving strength = 1
INVD4	Inverter with driving strength = 4
ND2D1	2-input NAND gate with driving strength = 1
ND4D1	4-input NAND gate with driving strength = 1
NOR2D1	2-input NOR gate with driving strength = 1
NOR4D1	4-input NOR gate with driving strength = 1
XOR2D1	2-input XOR gate with driving strength = 1
CKBD1	Clock buffer with driving strength = 1
CKBD4	Clock buffer with driving strength = 4
CKBD16	Clock buffer with driving strength = 16
DFCNQD1	Flip-Flop, asynchronous clear and driving strength = 1
LHCNQD1	Latch, asynchronous clear and driving strength = 1

Standard cells for each library in DRAD chip





$$Td \propto \frac{N}{f}$$

$N = number\ of\ gates$

$Td = Time\ delay\ of\ the\ gate$

Schematic of ring oscillator/delay chain test structure and input/output signals used to measure the time delay of the standard cell.

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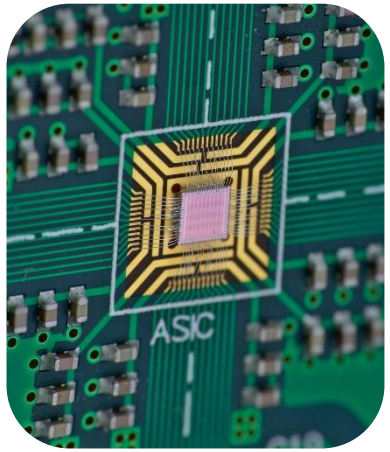

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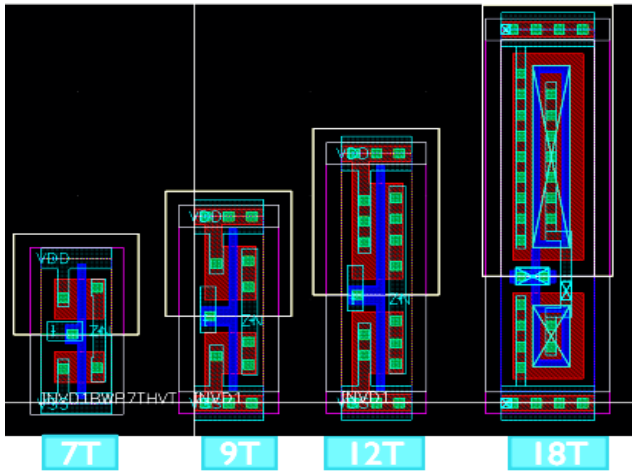

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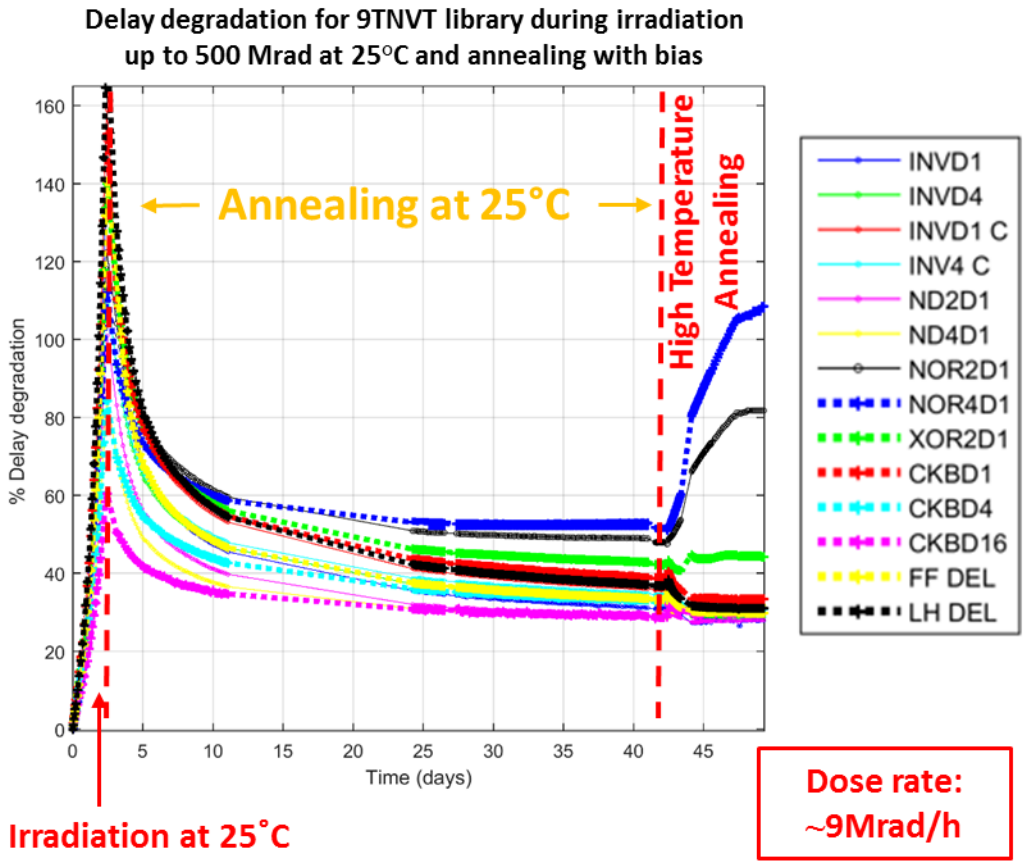
Libraries studied in DRAD chip

3. RADIATION TOLERANCE

500 Mrad cold vs room T

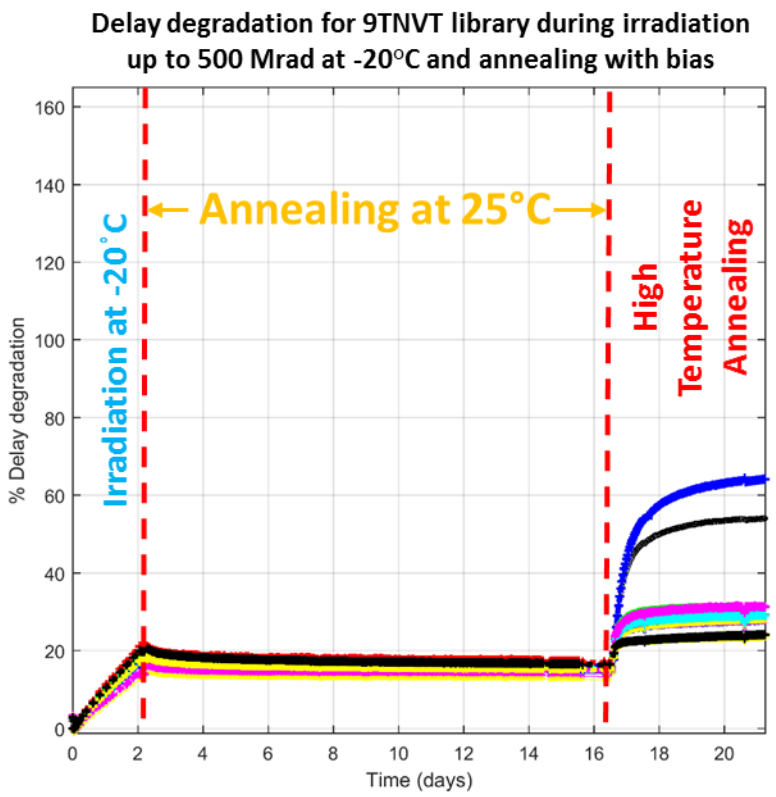
Room temperature and high temperature annealing with BIAS

500 Mrad 25˚C



Dose rate: ~9Mrad/h

500 Mrad cold (-20˚C)

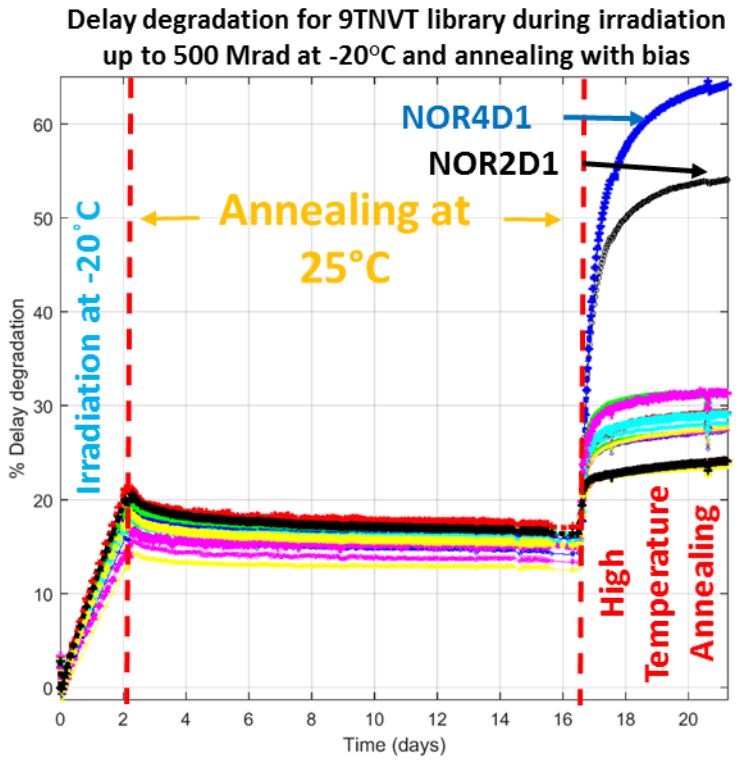


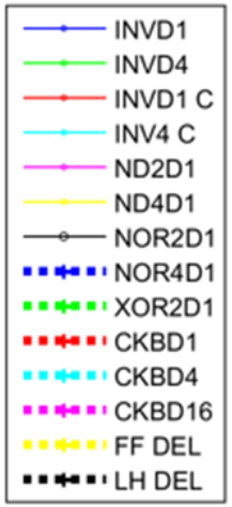
- Delay degradation of standard cells is much smaller when irradiation is done cold.
- Annealing at room temperature and with bias 'heals' part of the damage caused by irradiation, but high temperature annealing (~100°C) with bias degrades the speed of the standard gates.

3. RADIATION TOLERANCE

500 Mrad cold + annealing with bias vs without bias

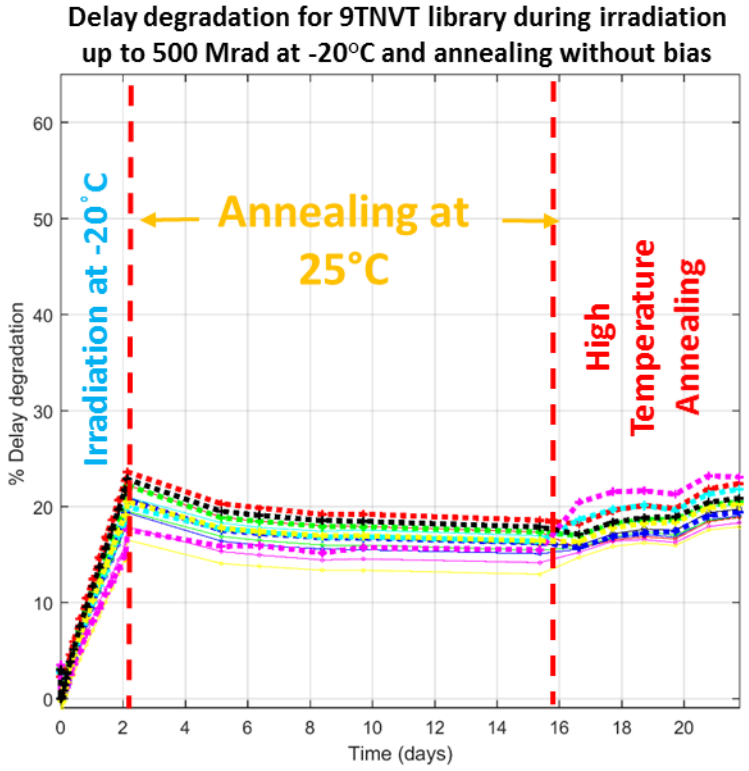
500Mrad cold (-20˚C)
Annealing WITH bias





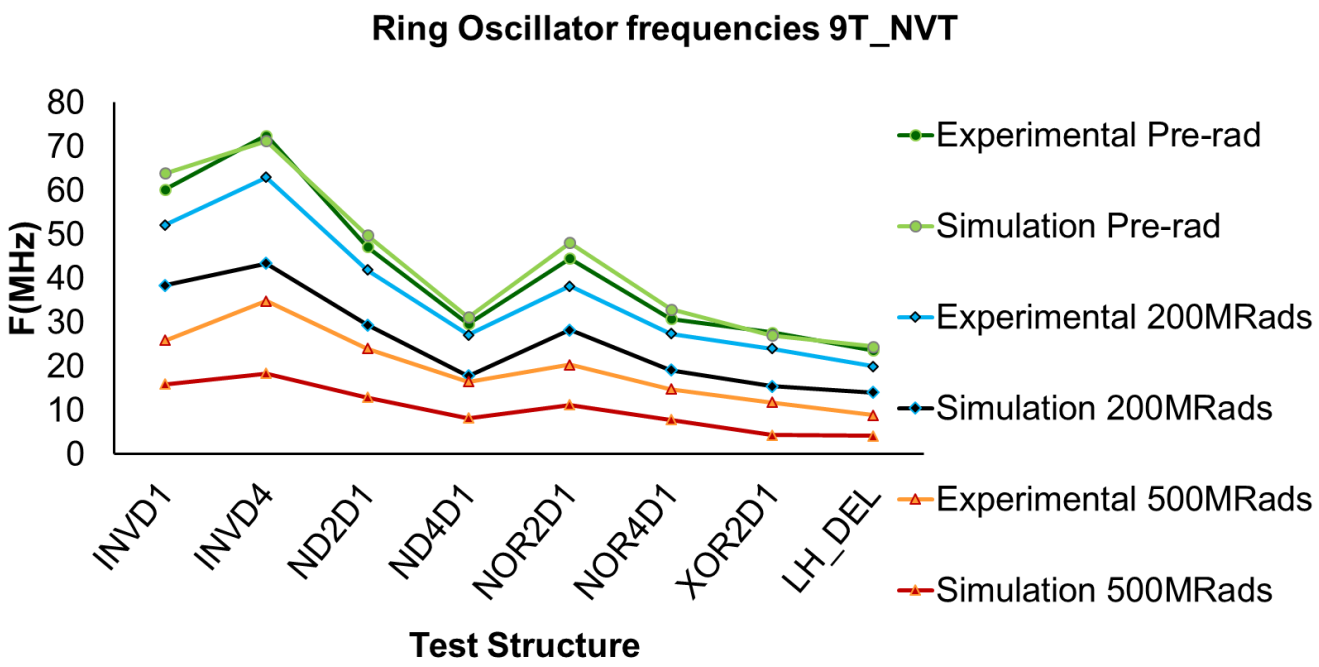
Dose rate: ~9Mrad/h

500Mrad cold (-20˚C)
Annealing WITHOUT bias



- When annealing is carried out without powering the chip, no significant gate delay degradation increase is seen.
- In conclusion, **control of environmental conditions** in the real experiment is crucial, and **annealing history** becomes very significant.

3. RADIATION TOLERANCE



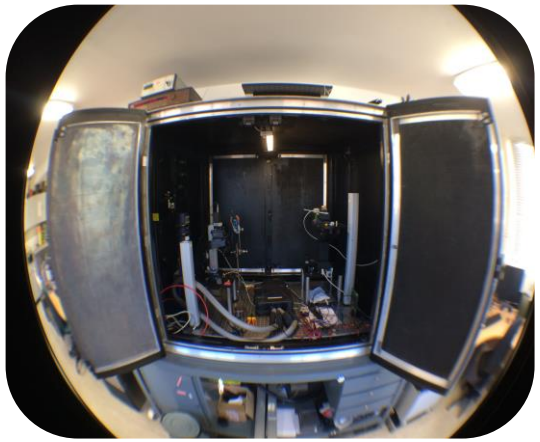
- 200Mrad and 500Mrad simulation models were developed by the radiation working group of the RD53 collaboration to 'predict' the circuit behaviour during design phase, based on fits to single transistor data.
- Models use worst case bias conditions but not high temperature annealing.
- The ring oscillators in DRAD chip were simulated with these models: the models are more pessimistic than measurements.
- The models were also used to simulate and assess the radiation hardness of RD53A.
- Conclusion: 9-Track Normal Vt library is adequate for both pixel array and chip bottom

4. RADIATION FACILITIES IN OUR COMMUNITY

- Irradiation needs to be wide enough to cover the whole chip with a uniform dose.
- The size of the chip makes this task difficult and slow (500Mrad tests are long).
- Most of the tests up to now have been done at high dose rate (order of Mrads/h)
- All the measurements shown in this presentation are done with chips without sensors.
- **Results** shown in this presentation were obtained at **high dose rate** (about 4Mrad/h) and **low temperatures** (-20°C) in radiation facilities among our community. **No annealing is included** in the results, which should bring some improvements if not done at high temperature and with bias.

CERN xray, ATLAS pixel group

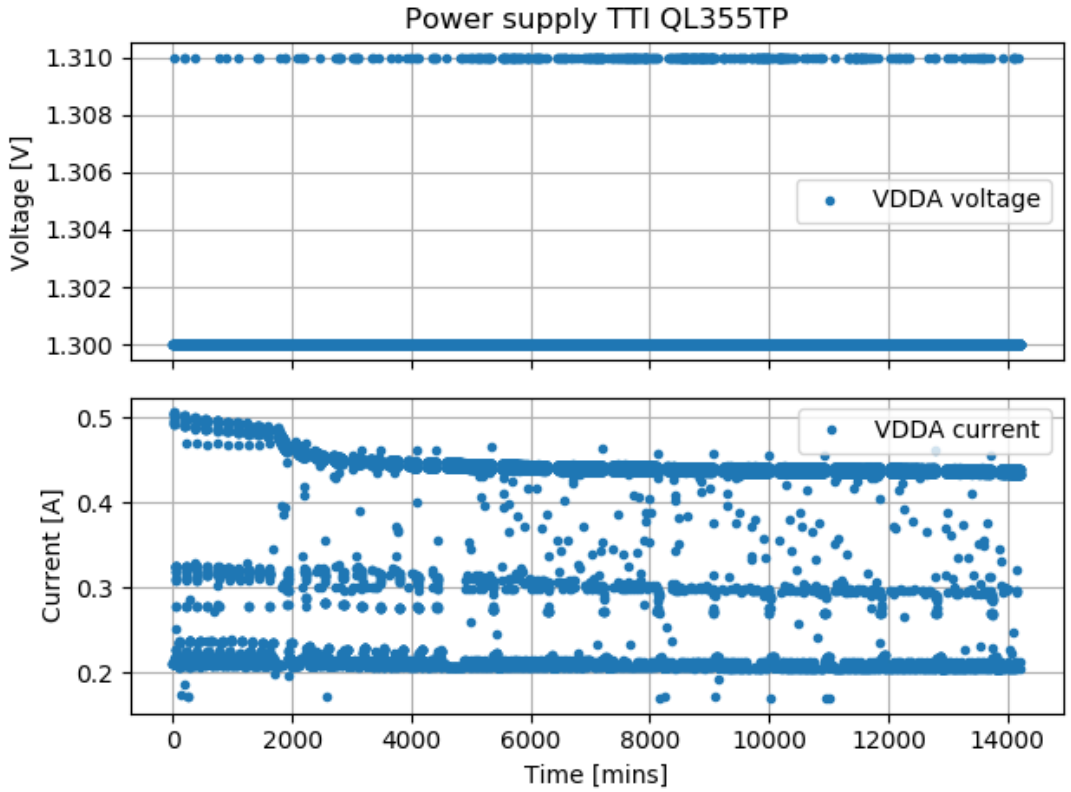
University of Glasgow

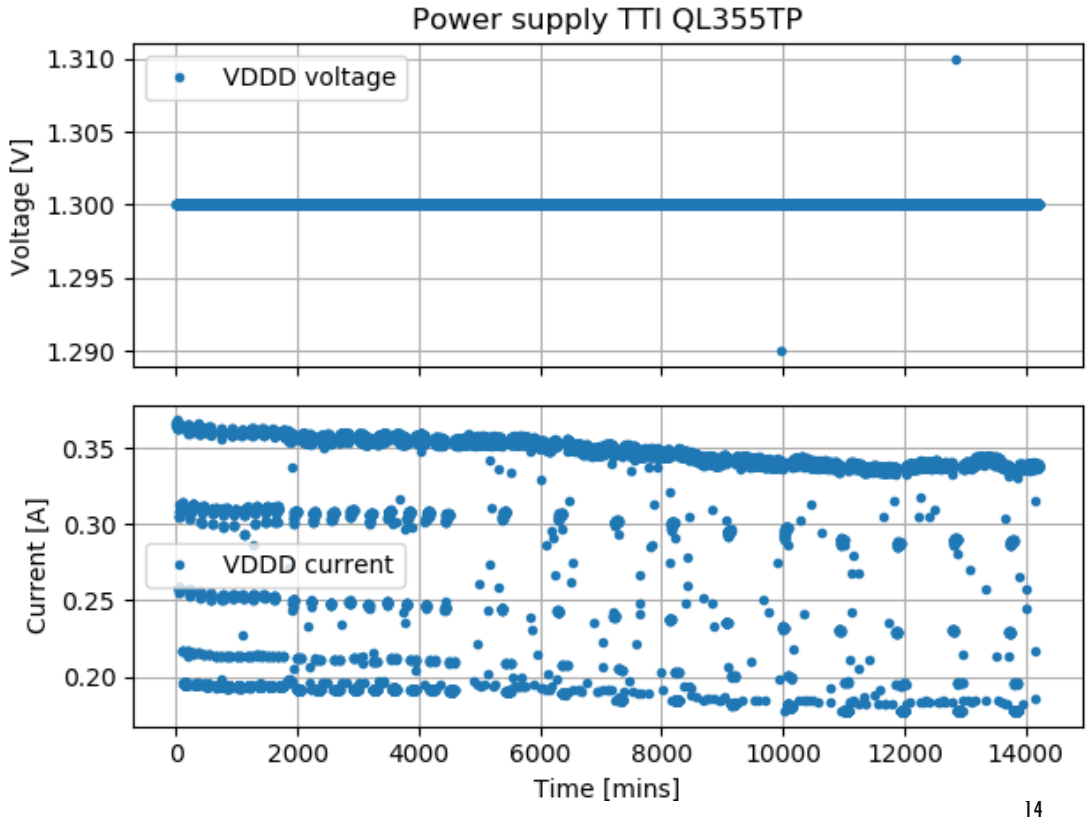


University of Bonn

4.1. POWER MEASUREMENTS

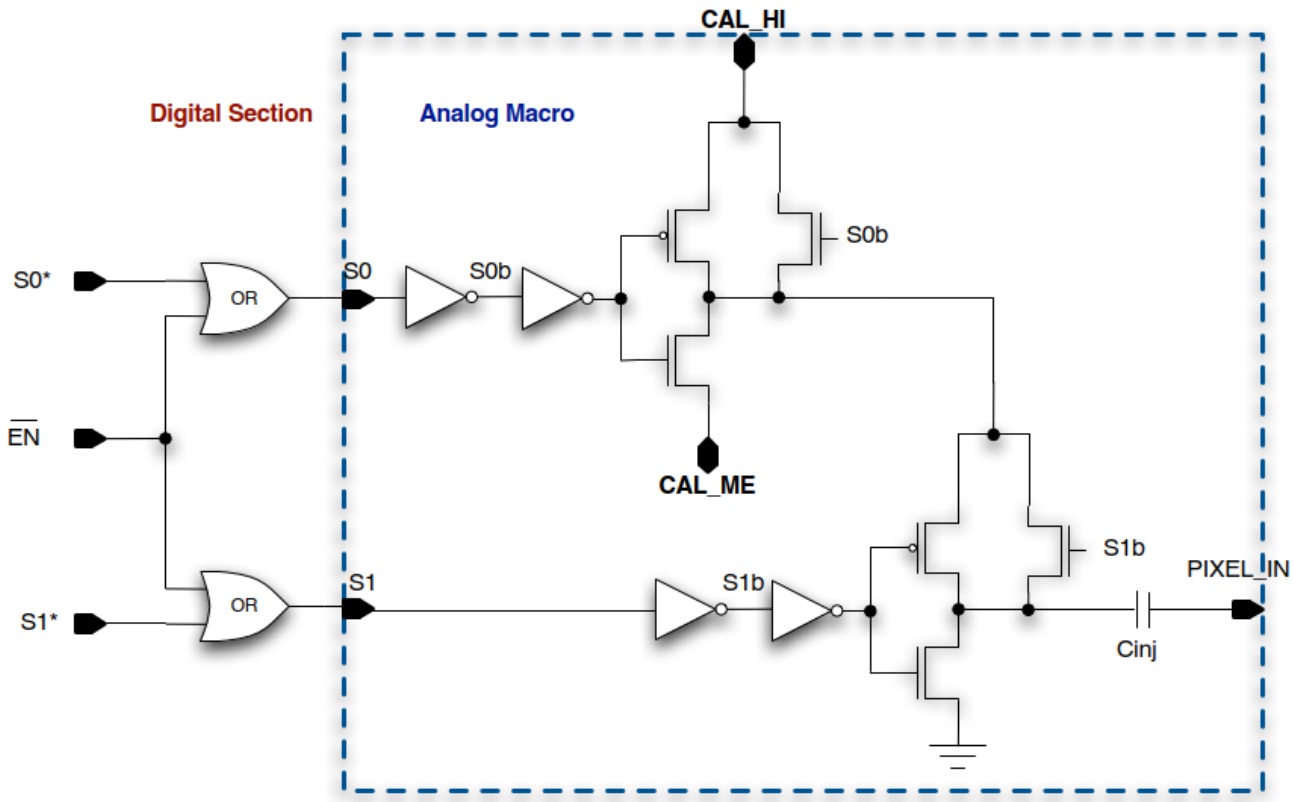
- Serial powering is the baseline choice for powering the ATLAS and CMS HL-LHC pixel detectors (see implications of this choice in tomorrow's talks on pixel detector for ATLAS and CMS upgrades)
- RD53A has two power domains (digital and analog), two ShuntLDOs providing VDDA and VDDD
- RD53A can also be configured to be powered in direct powering mode or LDO mode.
- No significant changes in power consumption were seen during irradiation up to 600Mrad in direct powering mode (only changes related to the different configuration of the chip):





4.2. ANALOG FE MEASUREMENTS

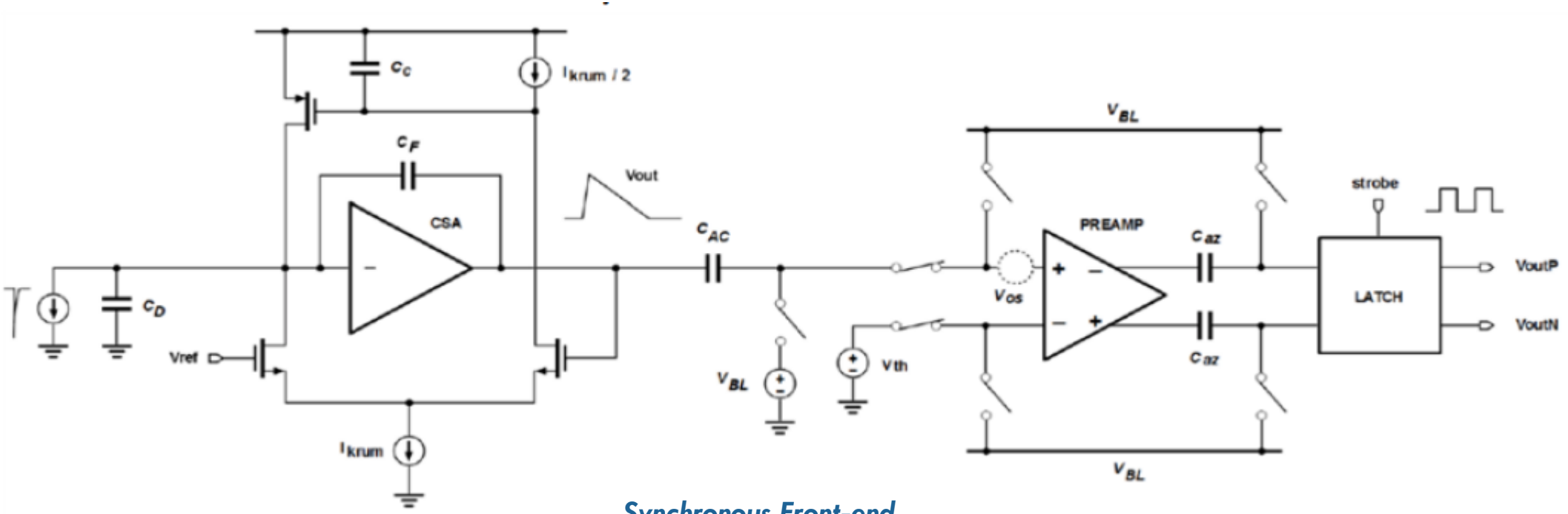
- Three different analog FE in RD53A for testing purposes.
- Results shown concern chip without sensor, generating the analog test pulse via the calibration injection circuit.
- This analog test pulse is derived from 2 defined DC voltages (CAL_HI and CAL_MED) distributed to all pixels, and a third level (local GND)
- Same injection circuit adopted for the three analog FEs.



Calibration injection circuit in RD53A chip

NOTE! All values in electrons reported in the presentation have a 15-20% uncertainty due to injection capacitance and calibration level variations between chips

4.2. ANALOG FE MEASUREMENTS: SYNCHRONOUS FE



Synchronous Front-end

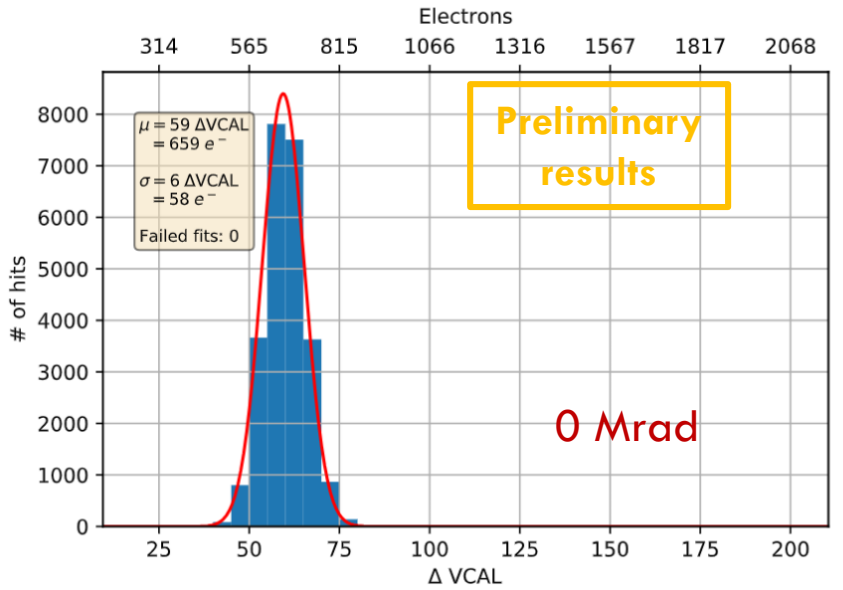
- Channel-to-channel threshold dispersion compensation is performed using the capacitors-based autozeroing technique, no trimming procedure is required, threshold tuning is very fast.
- Auto-zeroing could be performed during the Abort Gaps, every 80µs, tuning is re-optimized very frequently.
- No local trimming DAC needed, less prone to SEU misconfiguration, pixels don't risk to become too noisy.
- Optional Fast ToT feature: selectable frequency (in the 40-400 MHz range) 4-bit ToT counting. It decreases analog dead-time
- Fully functional after irradiation.

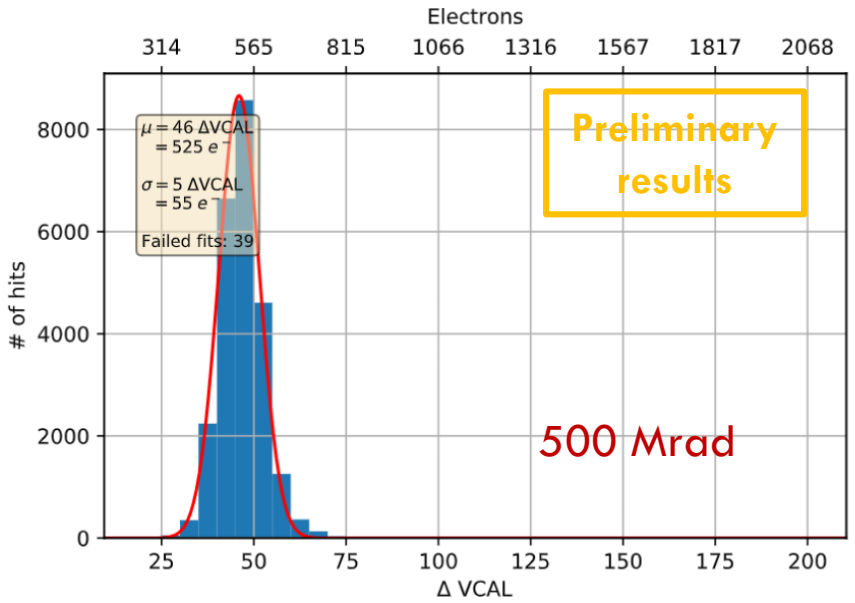
4.3. ANALOG FE MEASUREMENTS: SYNCHRONOUS FE

Chip SN 0x0595

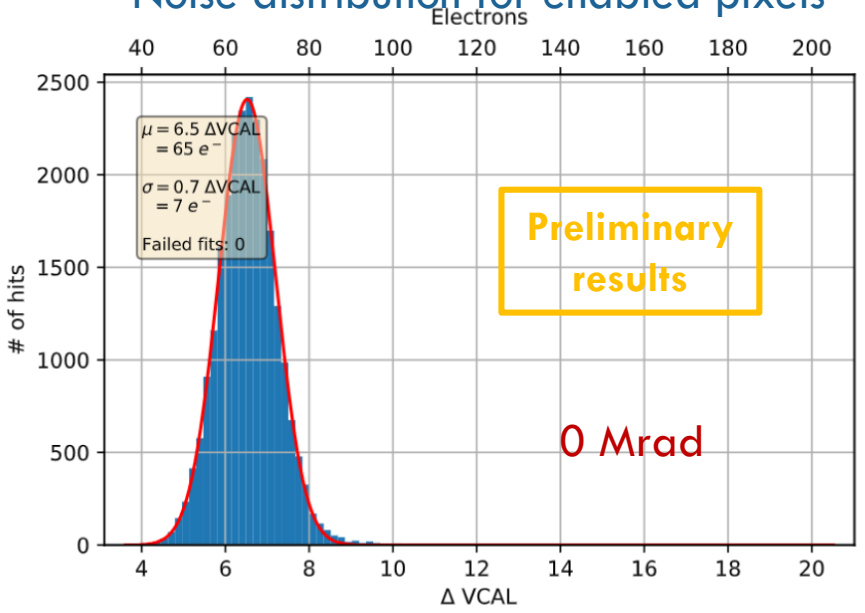
AZ pulse duration: 400ns

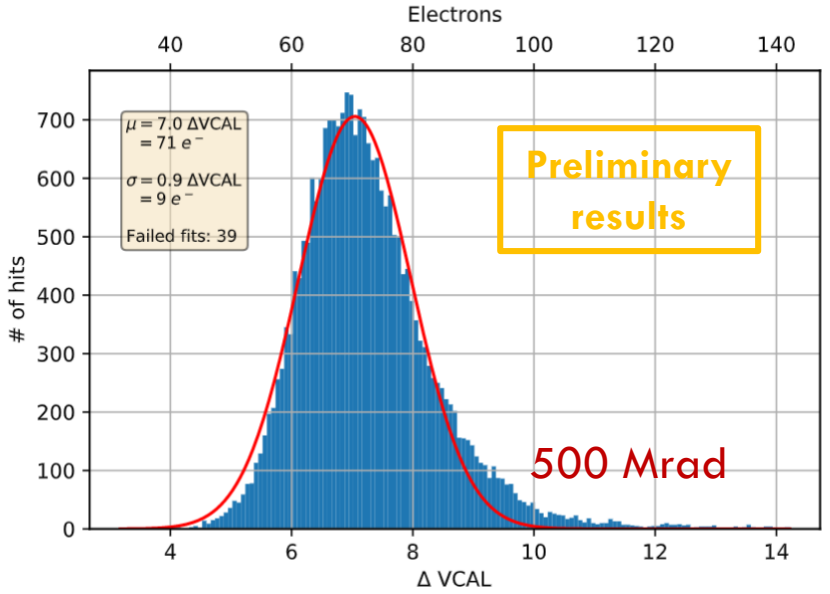
Threshold distribution for enabled pixels



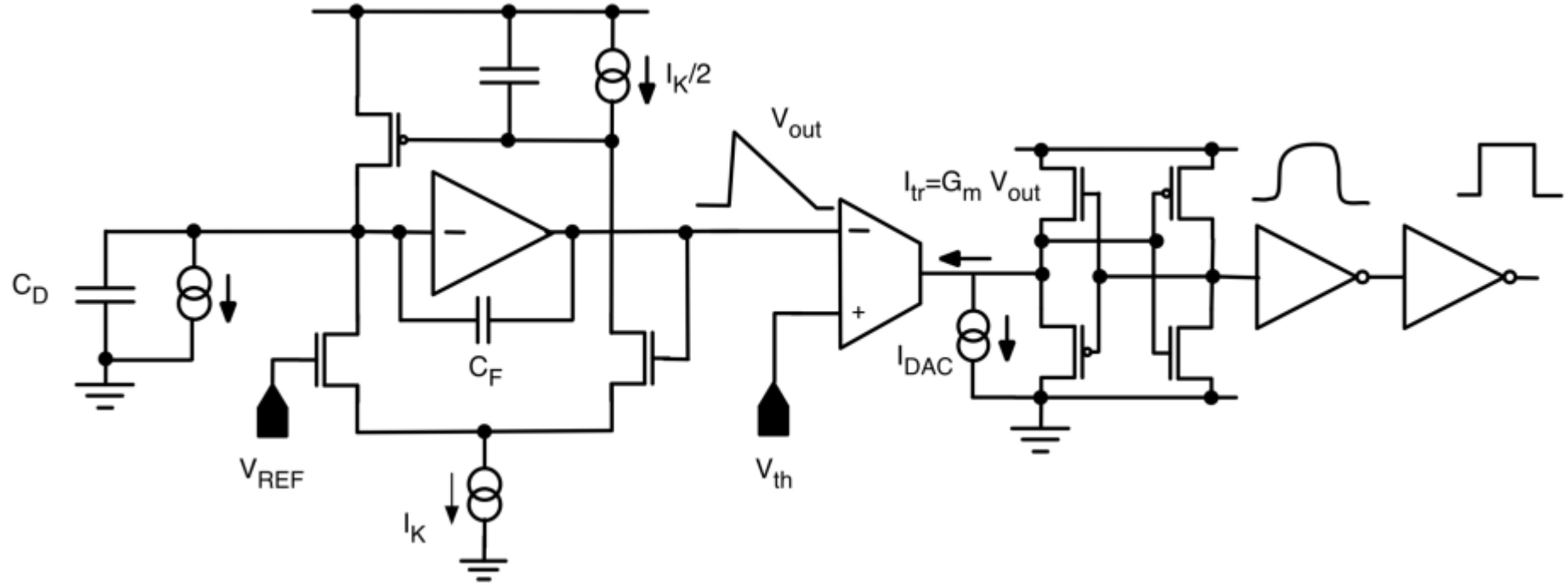


Noise distribution for enabled pixels





4.2. ANALOG FE MEASUREMENTS: LINEAR FE

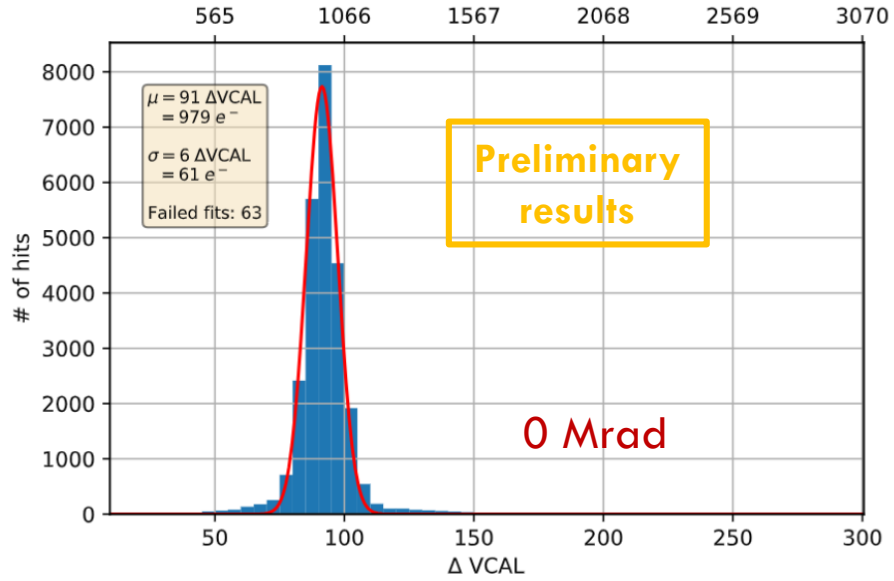


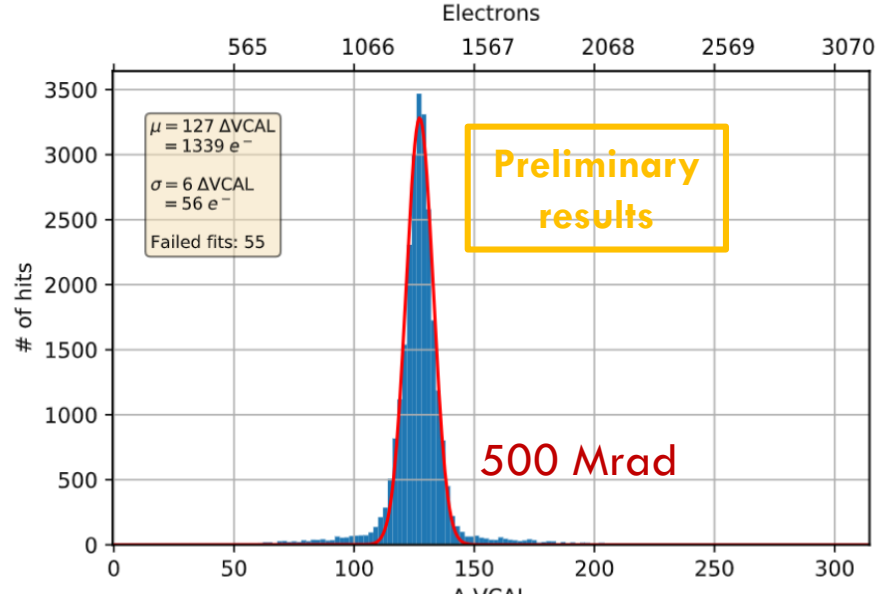
- Asynchronous FE
- In-pixel 4-bit threshold trimming DAC
- Tuning algorithms: injection based (used for results in this presentation) and noise based, results shown are obtained during the irradiation campaign, better tuning can be achieved.
- Fully functional after irradiation. Some outlier pixels in the threshold distribution, TDAC range will be increased and TDAC architecture improved.

4.2. ANALOG FE MEASUREMENTS: LINEAR FE

Chip SN 0x0595

Threshold distribution for enabled pixels after tuning





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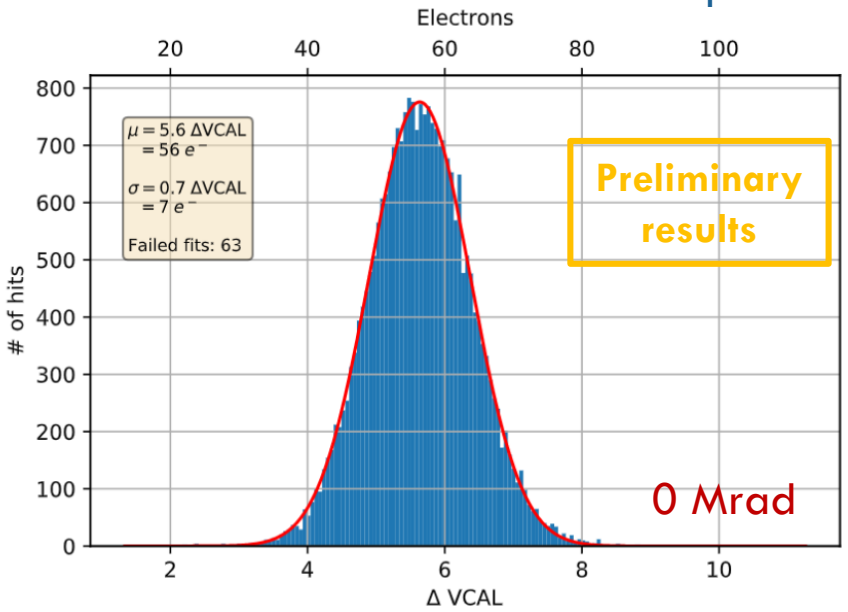

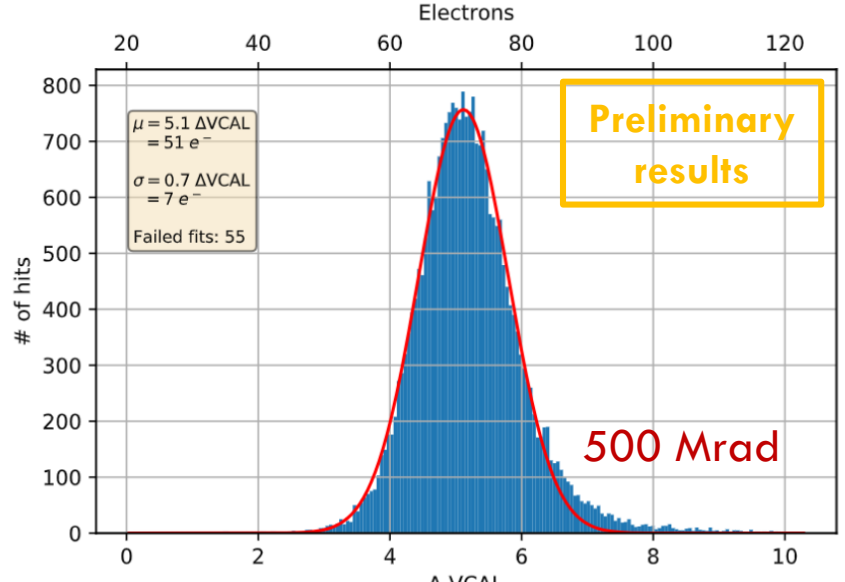

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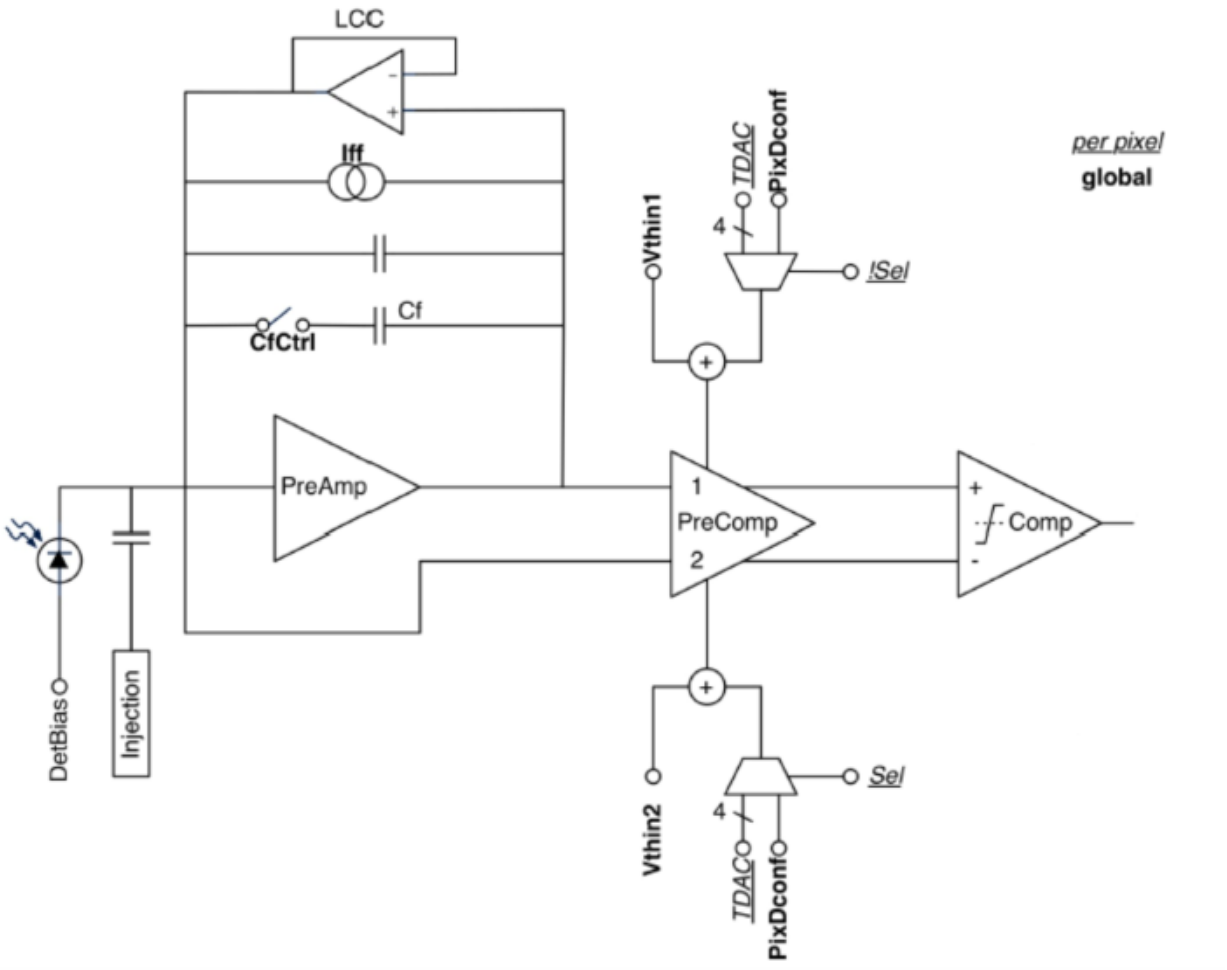

- Asynchronous FE
- In-pixel 5-bit threshold trimming DAC
- Fully differential architecture
- Tuning algorithms: injection based (used for results in this presentation) and noise based, results shown are obtained during the irradiation campaign, better tuning can be achieved.
- Fully functional after irradiation.

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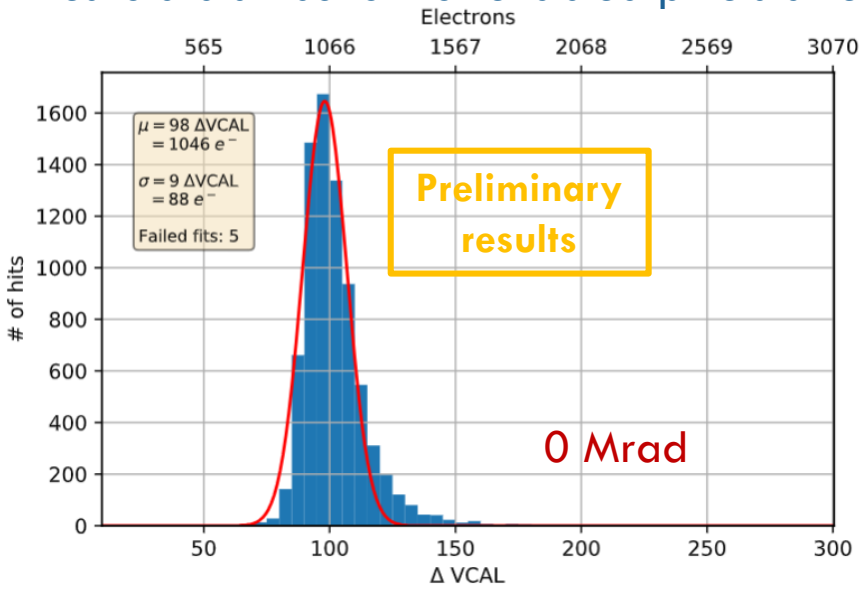
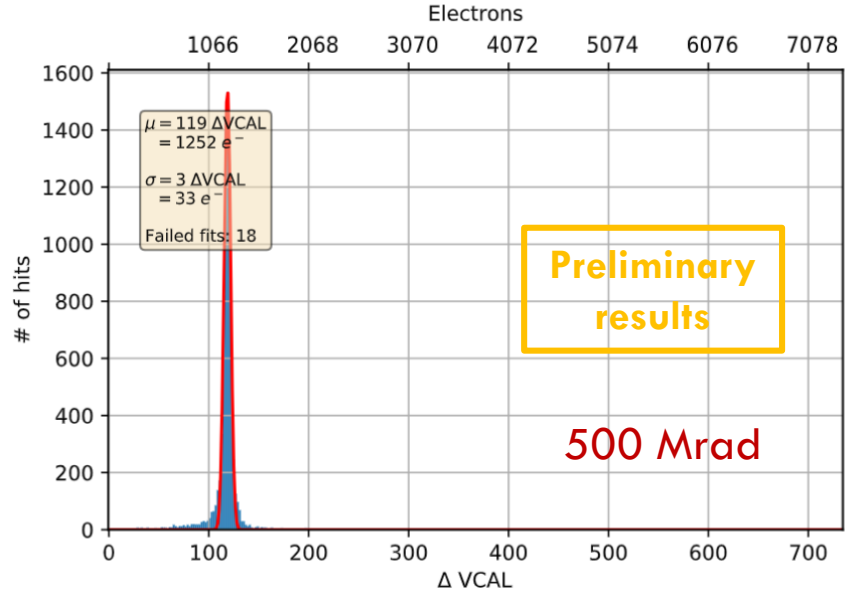
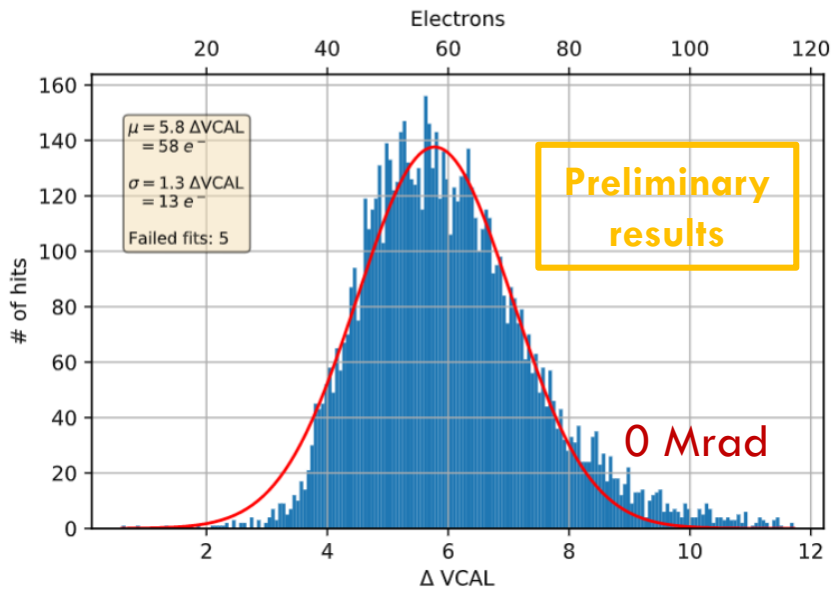
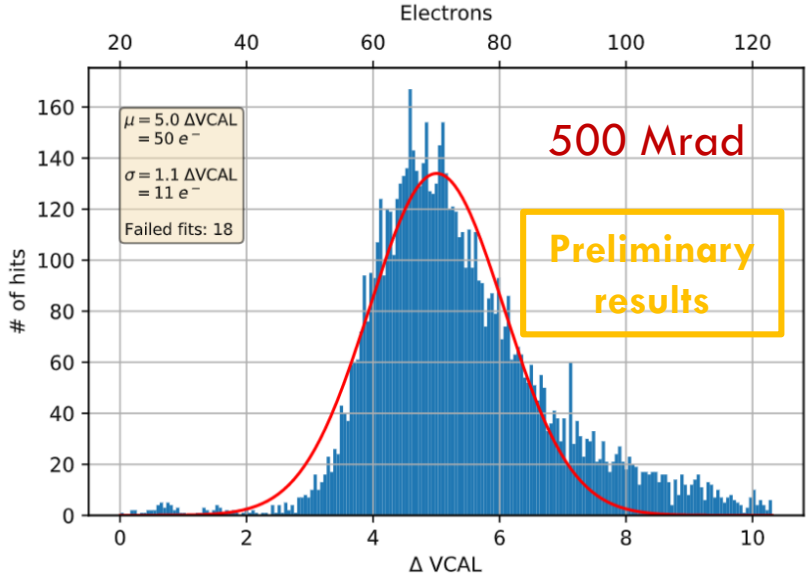
Threshold distribution for enabled pixels after tuning



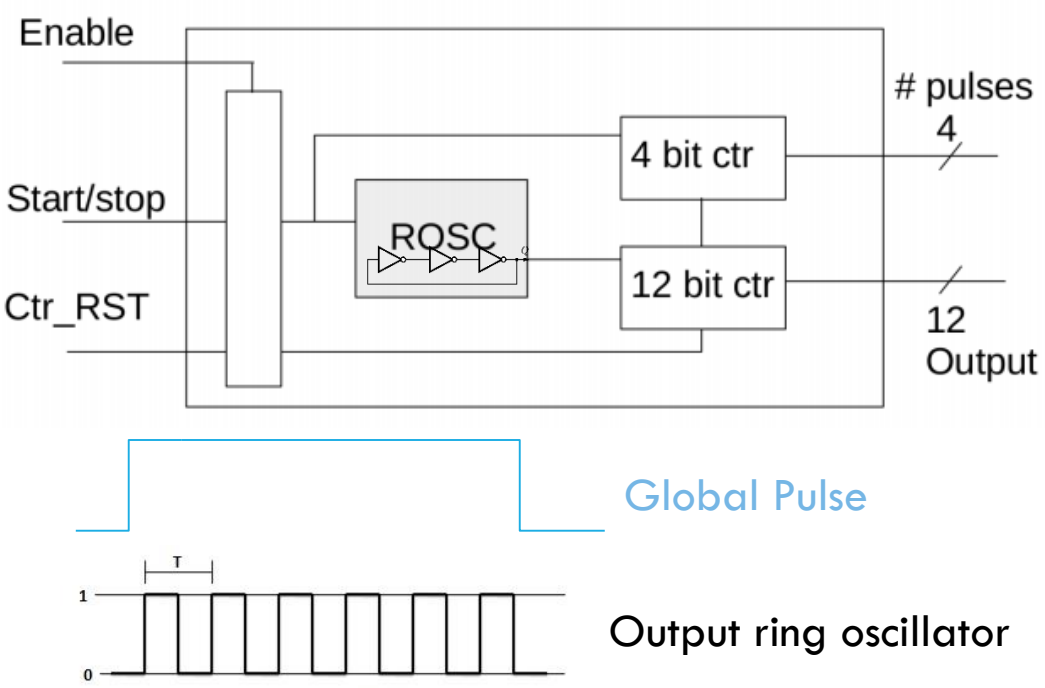


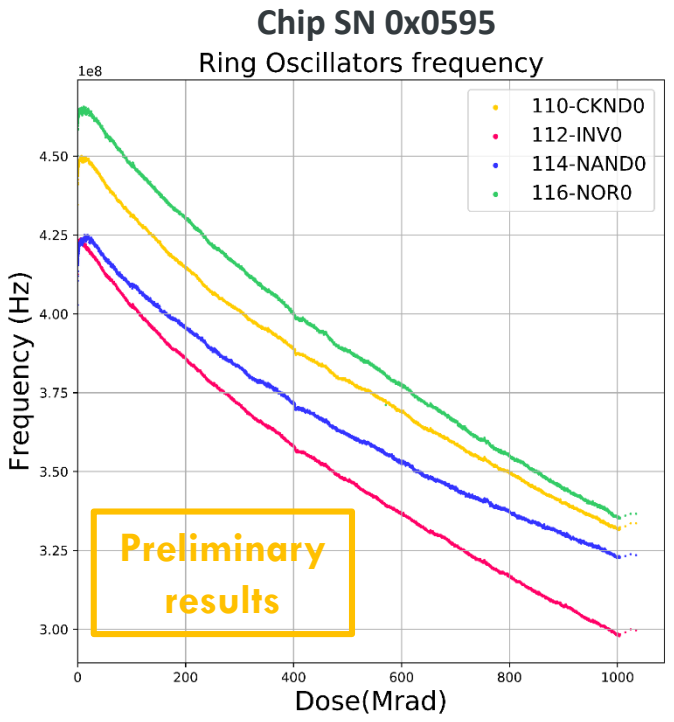
Noise distribution for enabled pixels

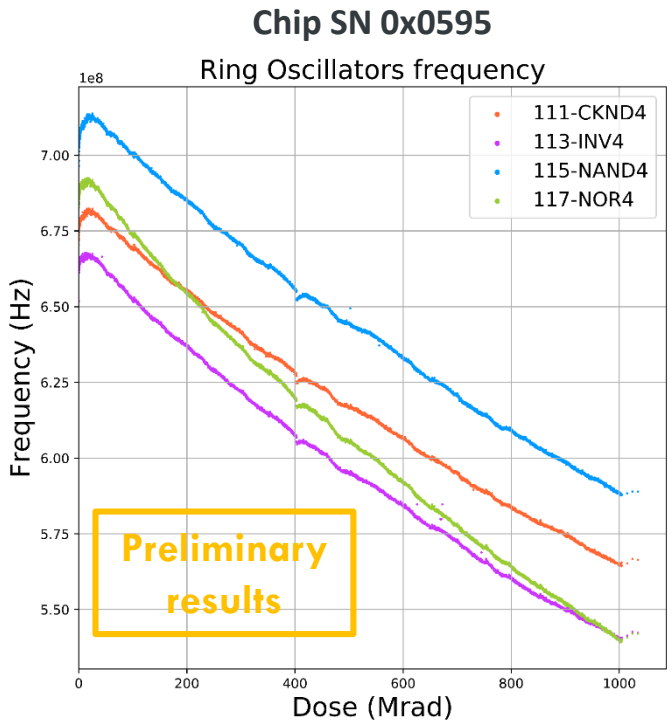




4.3. RING OSCILLATOR MEASUREMENTS

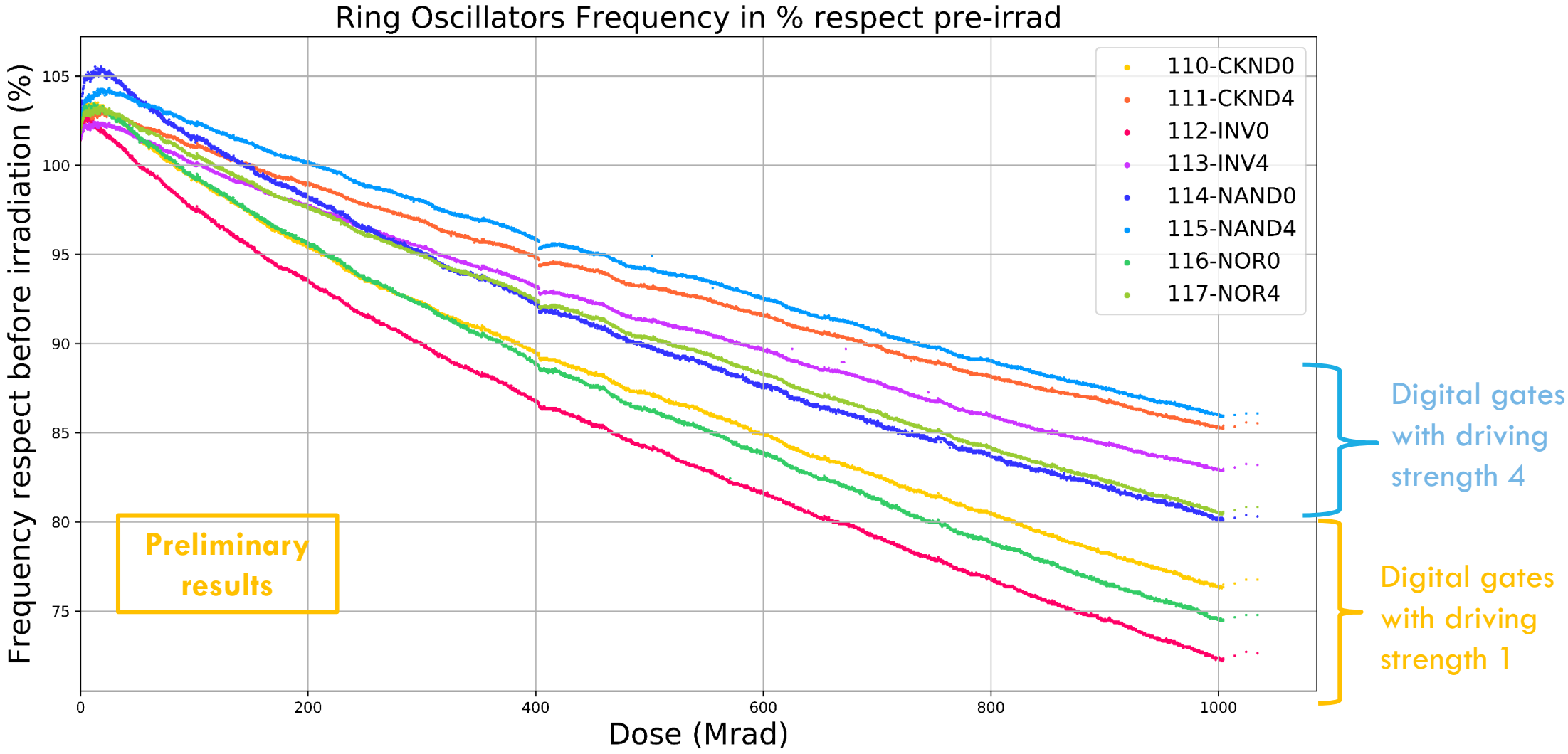




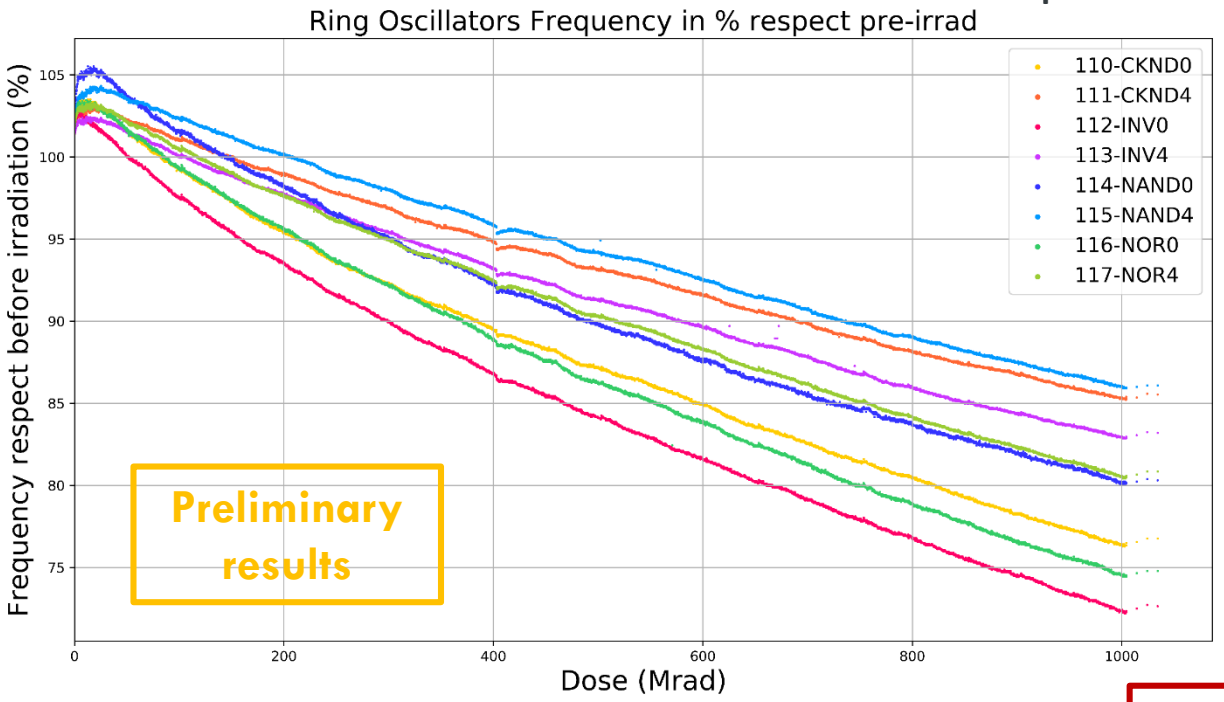


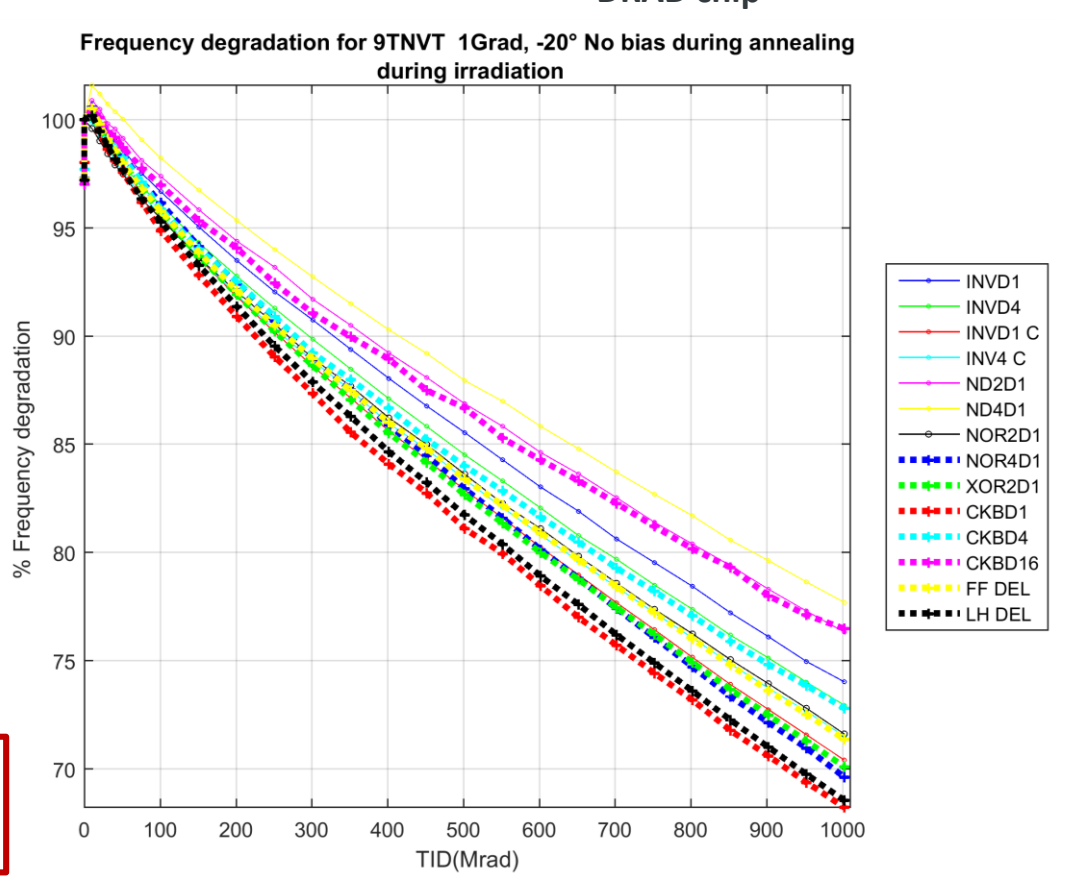
- Eight ring oscillators included in RD53A for radiation testing, built with different logic cells similar to DRAD chip with the chosen 9TNVT library.
- They are placed in the bottom right corner of the chip bottom
- Each oscillator drives a 12bit counter, that is enabled for a known amount of time set by configuration.
- Frequency of the rings can be easily obtained knowing the length of the enabling pulse and the number of counts obtained in the counter.

4.3. RING OSCILLATOR MEASUREMENTS



4.3. RING OSCILLATOR MEASUREMENTS





- **CHIP: 0x0595**
  Irradiated in Glasgow University, 3.9Mrad/h at -20°C

Annealing not included!!

- **DRAD chip**
  Irradiated at CERN, 9Mrad/h at - 20°C

Results of performance of the ring oscillators in RD53A with respect to DRAD in a similar range: RD53A degradation in the range of 72% to 87%, DRAD in the range 68% to 78%

5. SINGLE EVENT UPSETS

- SEU: RD53A supports 'trickle configuration': all the configuration (global and pixel configuration) can be gradually updated during operation by continually sending write commands in between triggers. This avoids the need for SEU hard configuration storage.

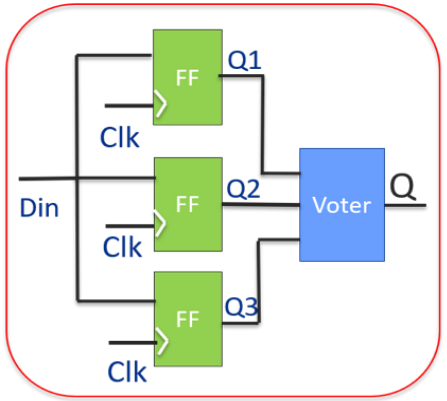
- Tests in different memory elements were done, potential use of DICE latches in the pixels would provide only an order of magnitude smaller upset cross section than standard latches

- Triple Modular Redundancy (TMR) is a common technique to mitigate soft error rates, but spacing between memory elements in a TMR in 65nm process has not been addressed so far.

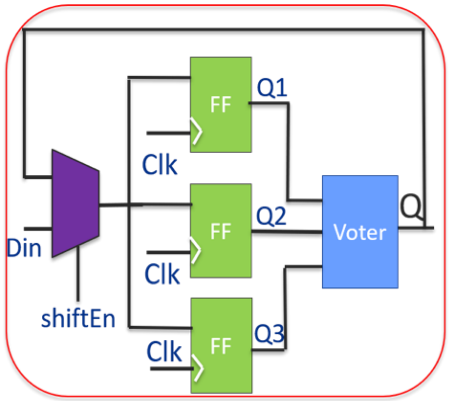
- A dedicated SEU chip, RD53SEU [4], has been designed to determine the best/affordable scheme for final chips:
  - Goal: characterize the soft error rates against the separation spacing and clock skew between memory elements in a TMR.

- Also SEU simulations will be carried out for the final chip.

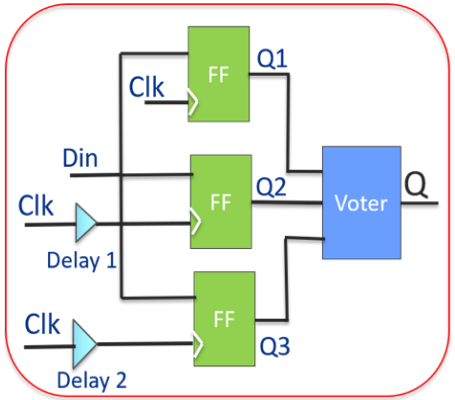
Different TMR versions studied in RD53SEU chip



Triple Modular Redundancy without correction



Triple Modular Redundancy with correction



Triple Modular Redundancy with clock skew insertion

6. CONCLUSIONS AND NEXT PLANS

- The RD53 collaboration has made an effort to study the radiation effects in electronics for the design and production of the pixel readout chips of ATLAS and CMS experiments at HL-LHC.
- Radiation test results with the RD53A prototype chip are very promising, showing good performance after high radiation doses. New radiation campaigns are foreseen in the early future, more specific measurements will be taken.
- Low dose rate test ongoing in our collaboration with Kripton source and preparations for a low dose rate test with Cobalt 60 are ongoing. Possibly a factor 2 worse with respect high dose rate [5].
- Also campaigns at room temperature are foreseen to compare effects with respect to low temperature.
- Tests with proton irradiated chip and sensors are on-going.
- SEU effects will be studied in RD53A.
- Full chip submission planned for 2019.

THANKS FOR YOUR ATTENTION!

REFERENCES

[1] J. Christiansen and M. Garcia-Sciveres, ***RD Collaboration proposal: development of pixel readout integrated circuits for extreme rate and radiation***, LHCC-P-006 (2013)

[2] F.Faccio et al., ***Radiation-Induced Short Channel (RISCE) and Narrow Channel (RINCE) Effects in 65 and 130 nm MOSFETs***, 2015, IEEE Transactions on Nuclear Science, Vol. 62, No. 6.

[3] L.M. Jara Casas, D.Ceresa, S.Kulis, S.Miryala, J. Christiansen, R.Francisco, D.Gnani, ***Characterization of radiation effects in 65nm digital circuits with the DRAD digital radiation test chip***, Journal of Instrumentation, Volume 12, February 2017

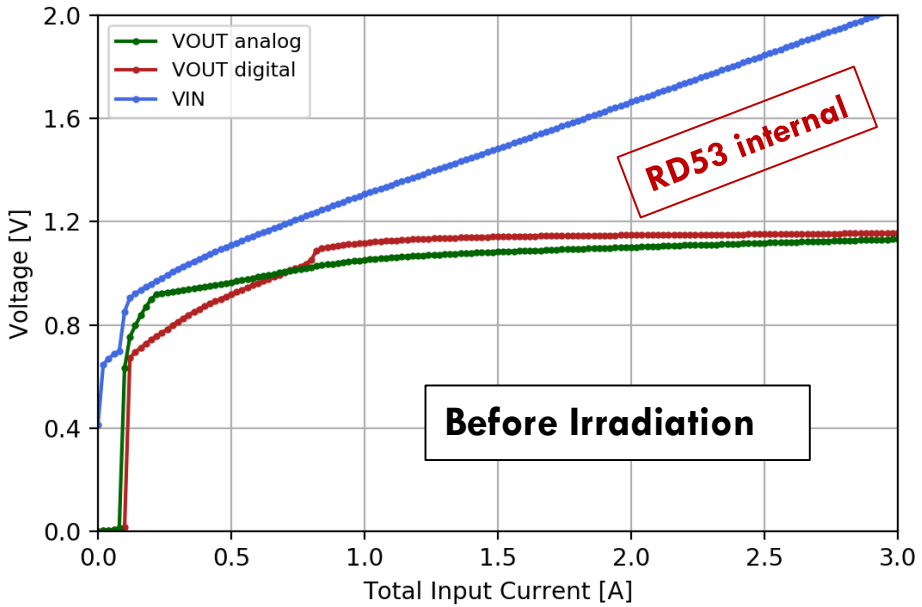
[4] S, Miryala, T. Hemperek, M.Menouni, ***Characterization of Soft Error Rate Against Memory Elements Spacing and Clock Skew in a Logic with Triple Modular Redundancy in a 65nm Process***, Proceedings of science, to be pusblished

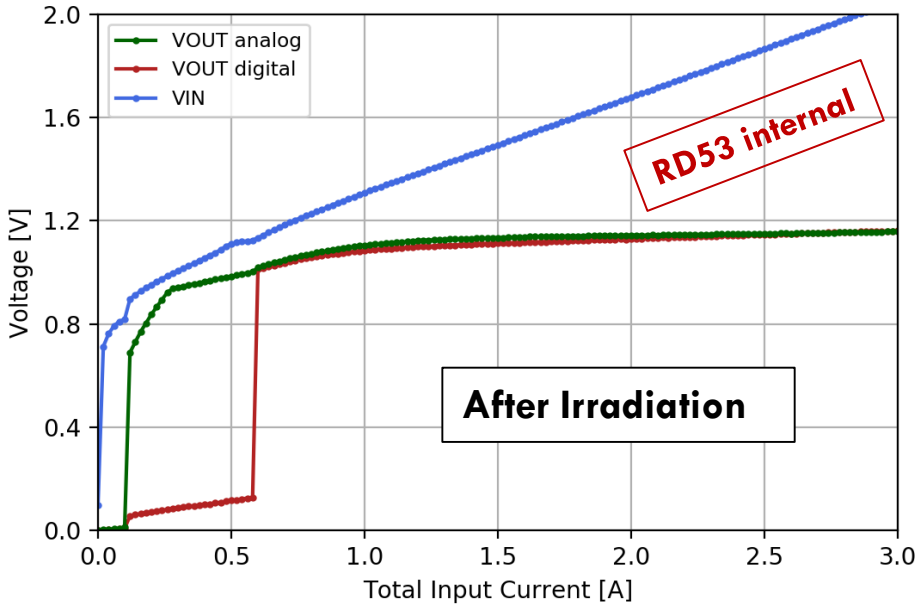
[5] G. Borghello et al., **Dose rate sensitivity of 65 nm MOSFETs exposed to ultra-high doses**, IEEE Transactions on Nuclear Science, PP(99), 1-1, 2018

BACK-UP SLIDES

SHUNT-LDO REGULATION AFTER 500MRAD IRRADIATION, -10°C

- IV-curve measurement with both regulators in parallel, Rint and external Vofs=0.5V

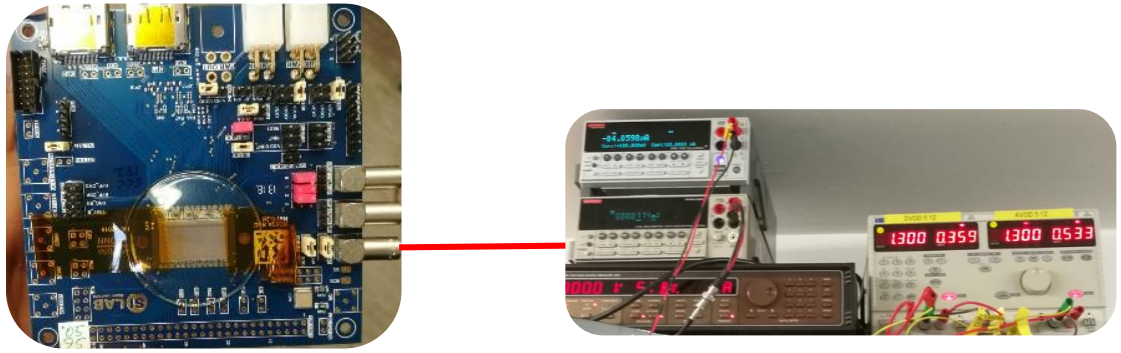


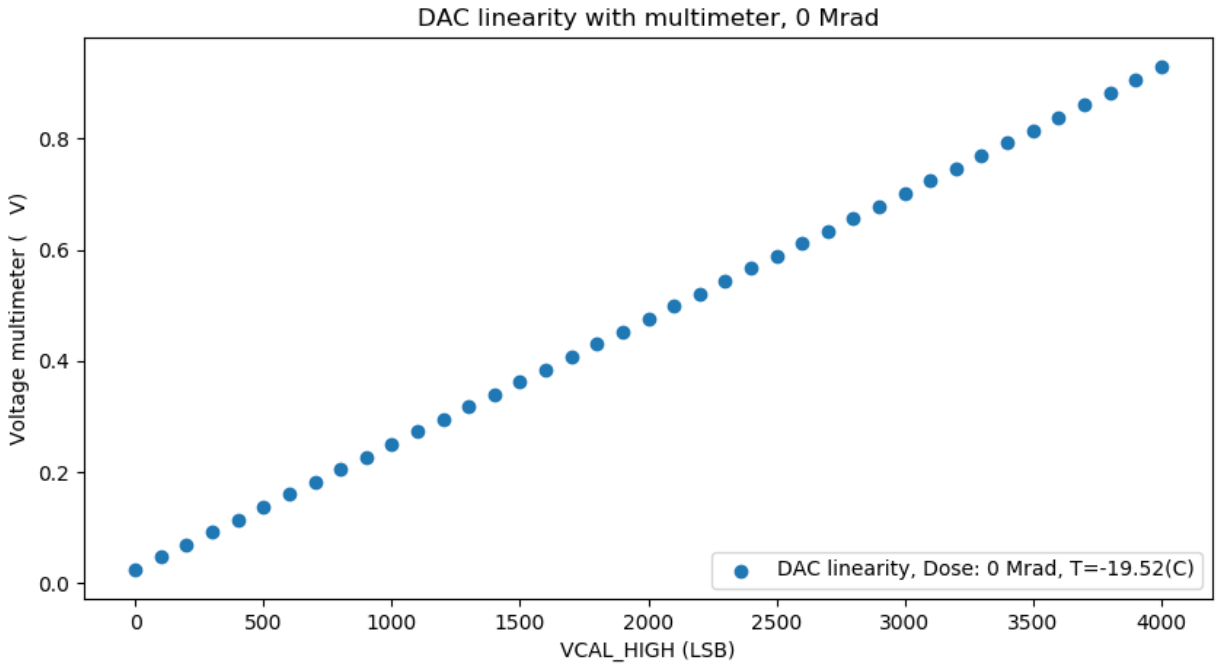


=> SLDO regulator meets specs after irradiation to 500MRad

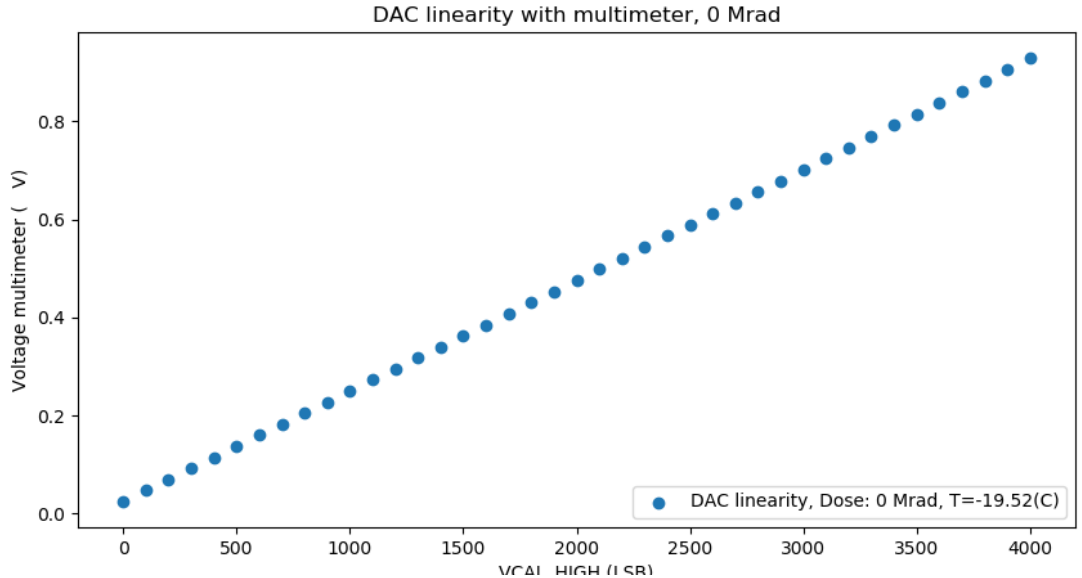
DAC LINEARITY

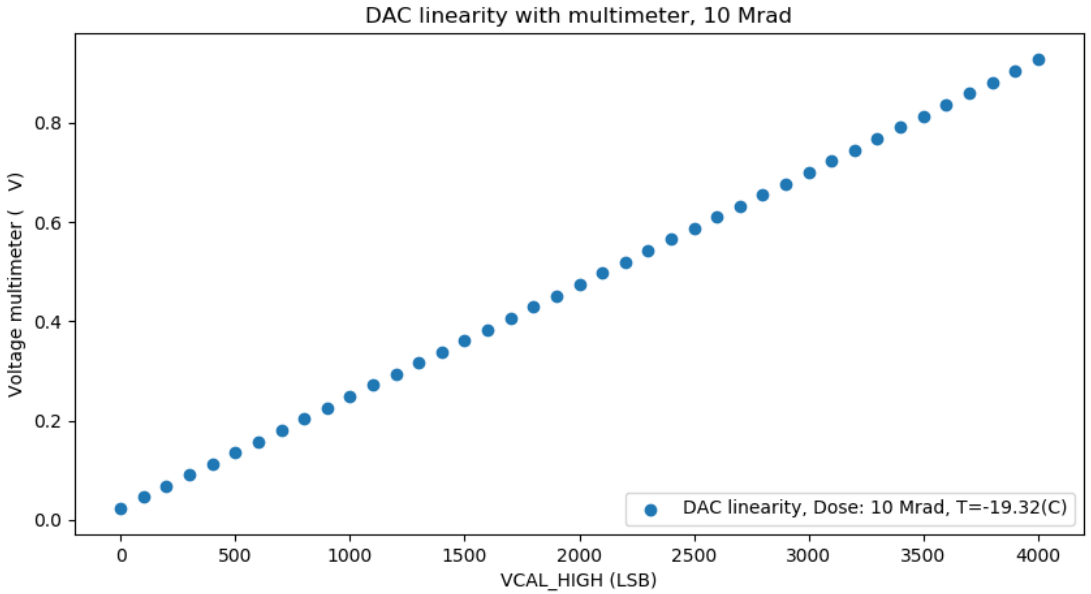
- Scans over the values of the VCAL_HIGH DAC and measures the resulting value with an external DVM.
- Steps of 100LSBs.
- This scan is also implemented in BDAQ using the internal ADC, results to be analysed.

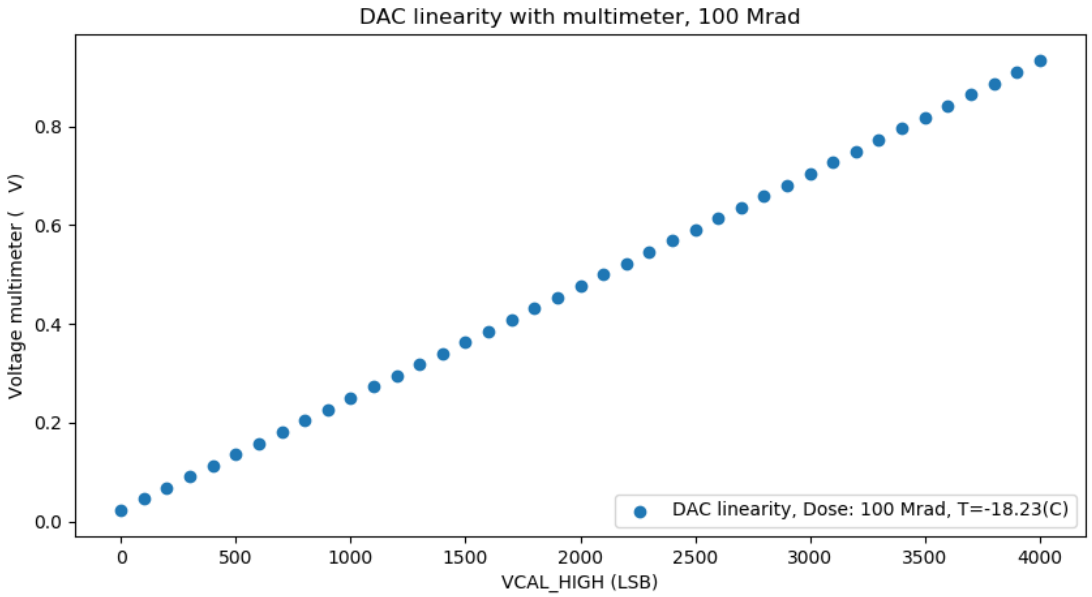


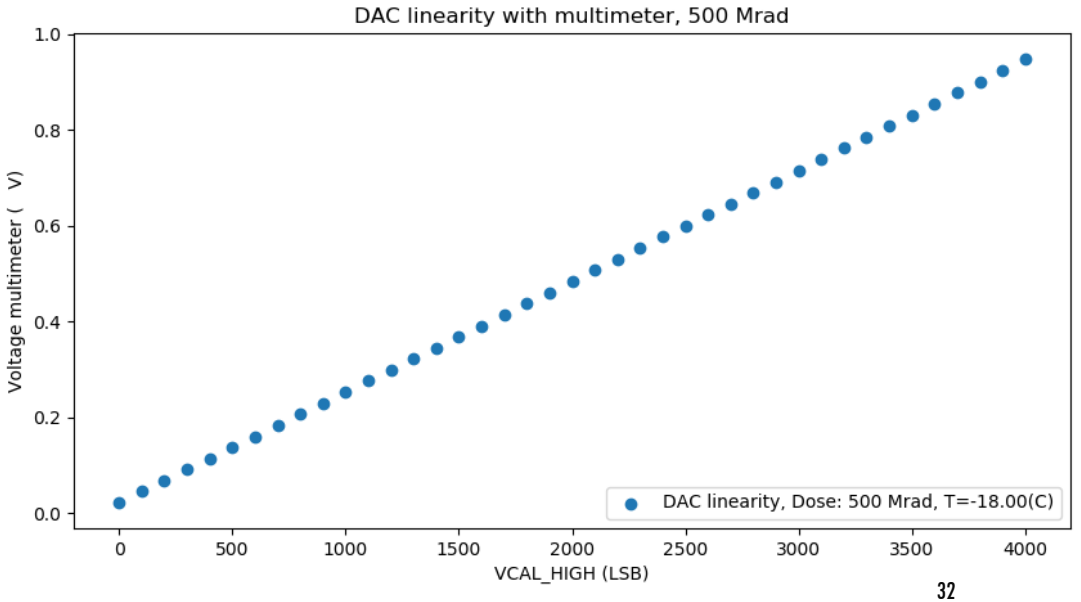


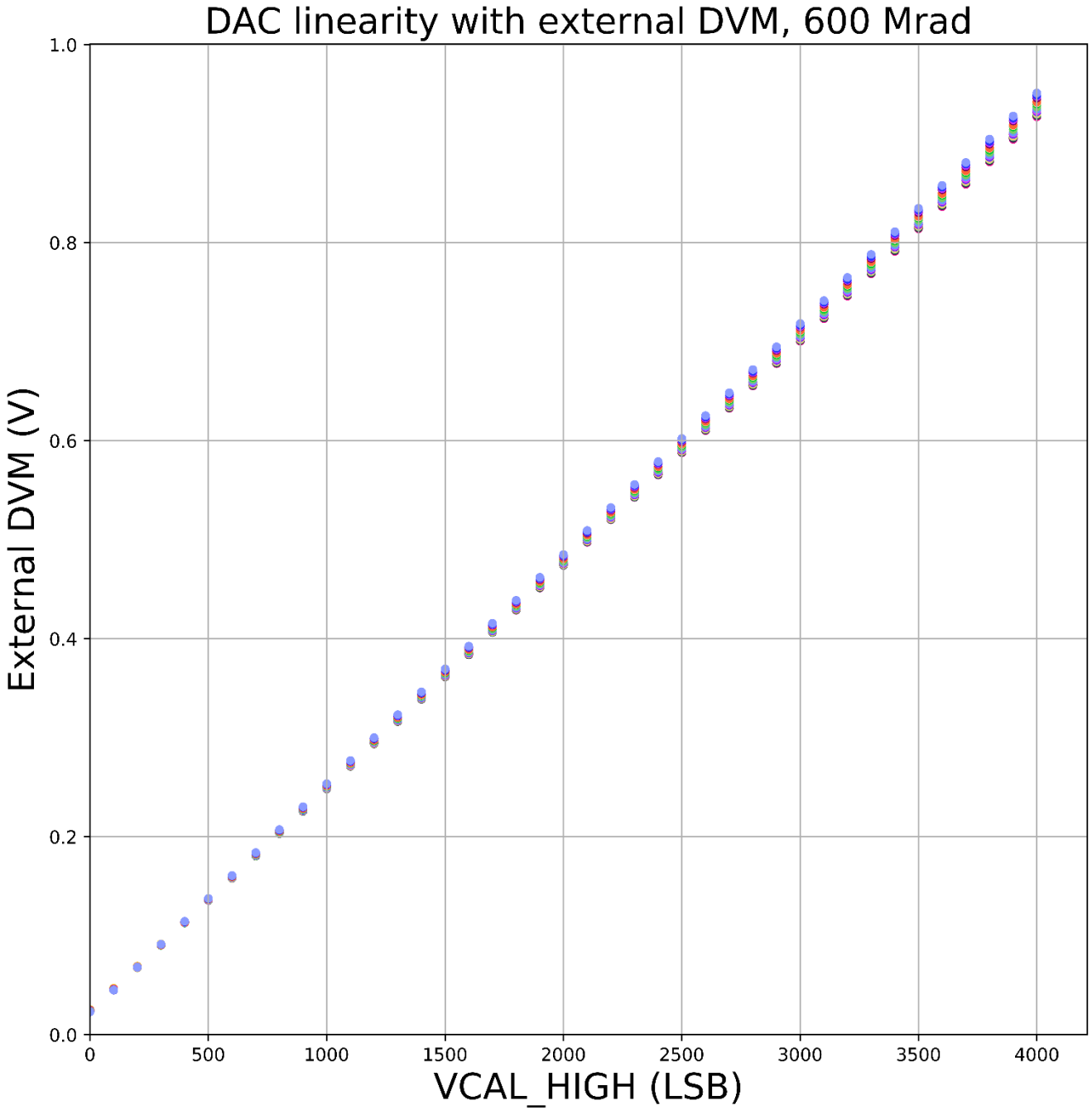
DAC LINEARITY



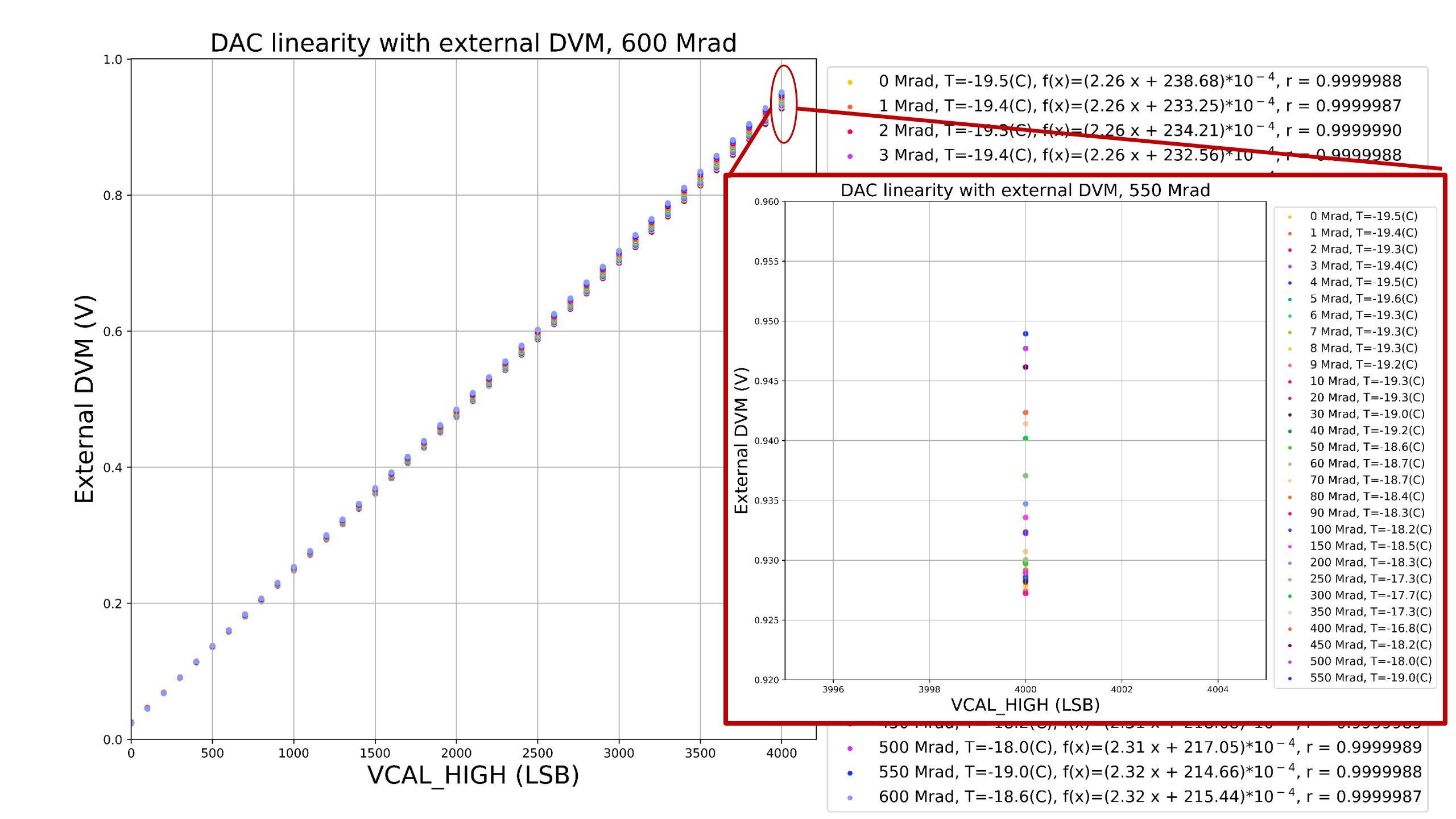


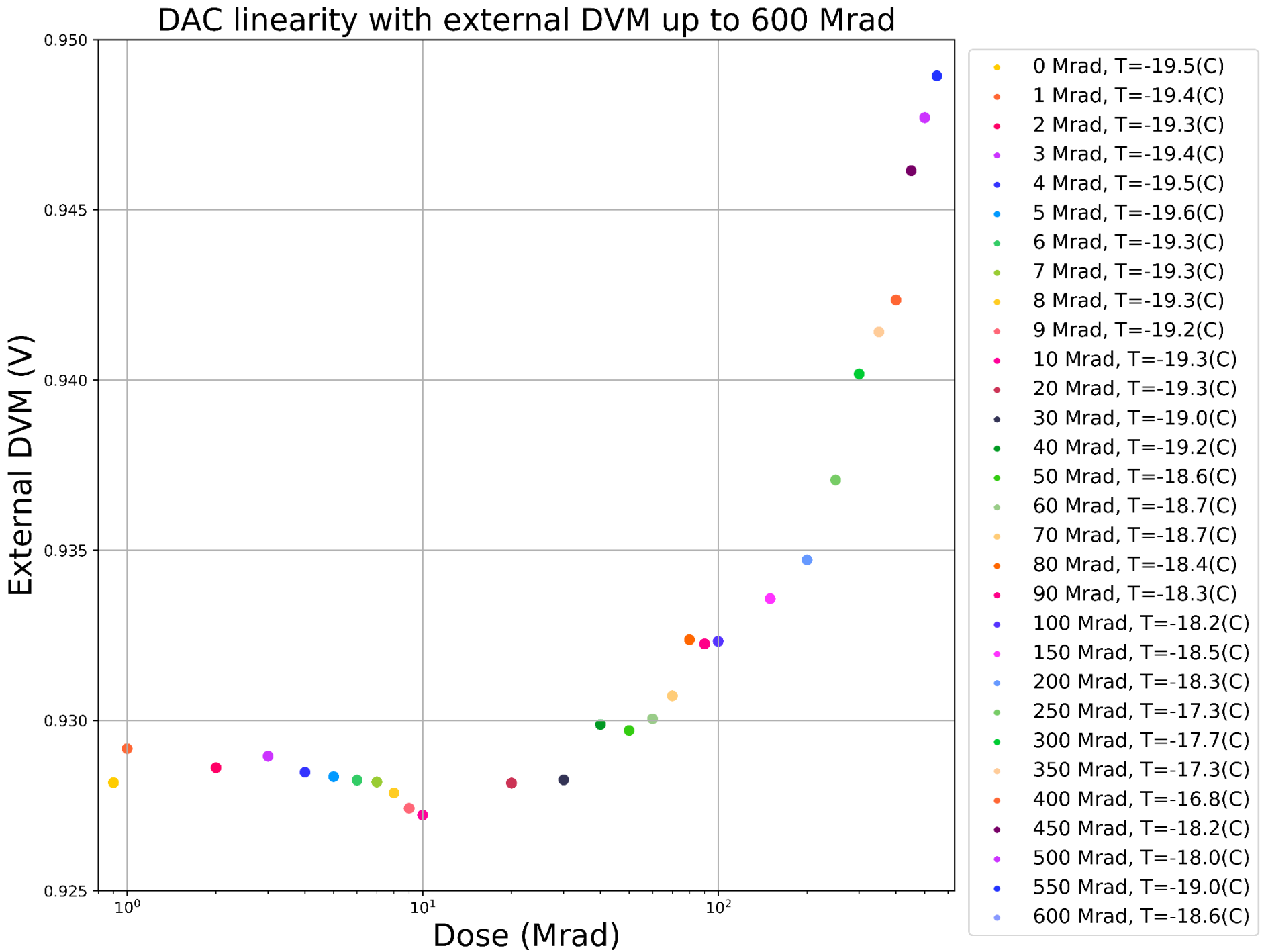


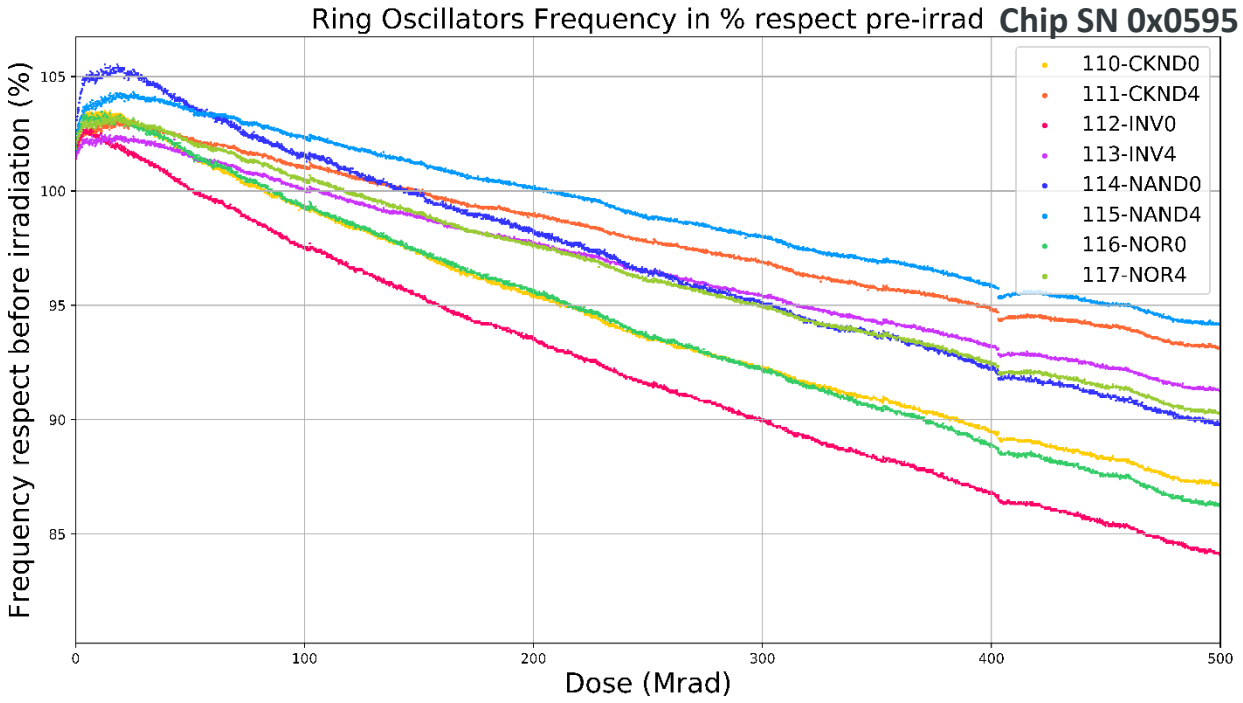


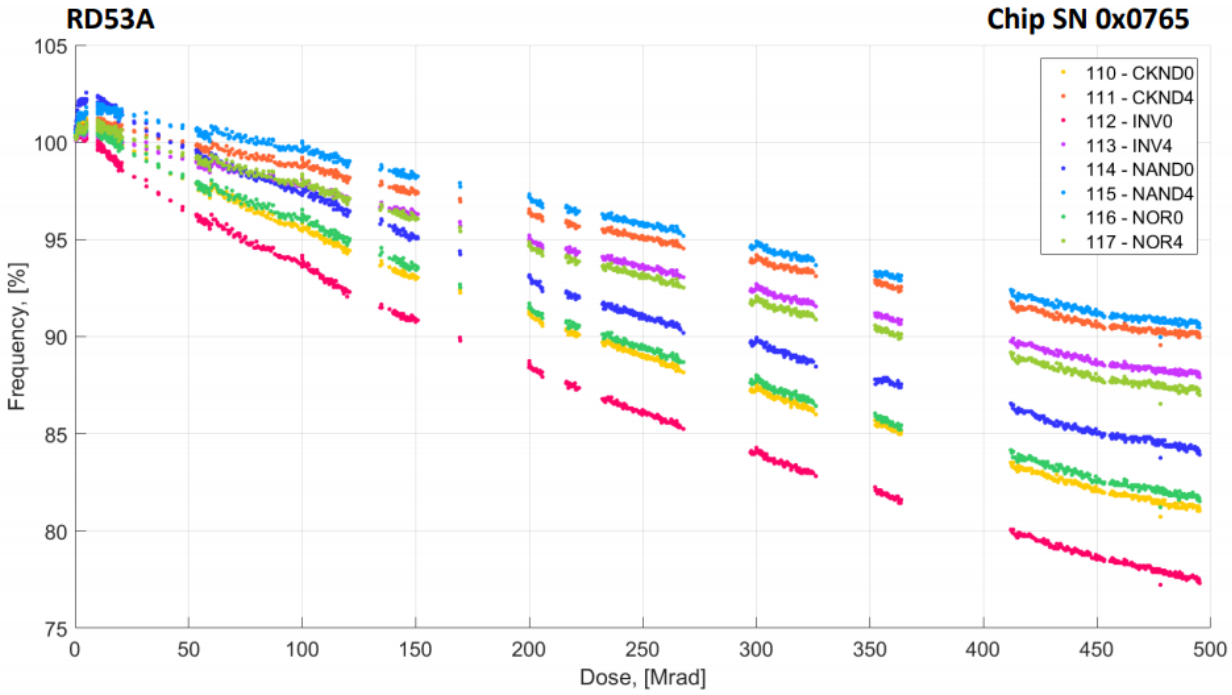


- 0 Mrad, T=-19.5(C), f(x)=(2.26 x + 238.68)*10^{-4}, r = 0.9999988
- 1 Mrad, T=-19.4(C), f(x)=(2.26 x + 233.25)*10^{-4}, r = 0.9999987
- 2 Mrad, T=-19.3(C), f(x)=(2.26 x + 234.21)*10^{-4}, r = 0.9999990
- 3 Mrad, T=-19.4(C), f(x)=(2.26 x + 232.56)*10^{-4}, r = 0.9999988
- 4 Mrad, T=-19.5(C), f(x)=(2.26 x + 231.26)*10^{-4}, r = 0.9999989
- 5 Mrad, T=-19.6(C), f(x)=(2.26 x + 230.23)*10^{-4}, r = 0.9999987
- 6 Mrad, T=-19.3(C), f(x)=(2.26 x + 230.27)*10^{-4}, r = 0.9999987
- 7 Mrad, T=-19.3(C), f(x)=(2.26 x + 231.06)*10^{-4}, r = 0.9999987
- 8 Mrad, T=-19.3(C), f(x)=(2.26 x + 230.97)*10^{-4}, r = 0.9999988
- 9 Mrad, T=-19.2(C), f(x)=(2.26 x + 229.72)*10^{-4}, r = 0.9999988
- 10 Mrad, T=-19.3(C), f(x)=(2.26 x + 229.26)*10^{-4}, r = 0.9999988
- 20 Mrad, T=-19.3(C), f(x)=(2.26 x + 224.34)*10^{-4}, r = 0.9999988
- 30 Mrad, T=-19.0(C), f(x)=(2.26 x + 222.10)*10^{-4}, r = 0.9999987
- 40 Mrad, T=-19.2(C), f(x)=(2.27 x + 221.03)*10^{-4}, r = 0.9999987
- 50 Mrad, T=-18.6(C), f(x)=(2.27 x + 222.17)*10^{-4}, r = 0.9999988
- 60 Mrad, T=-18.7(C), f(x)=(2.27 x + 221.76)*10^{-4}, r = 0.9999988
- 70 Mrad, T=-18.7(C), f(x)=(2.27 x + 221.28)*10^{-4}, r = 0.9999987
- 80 Mrad, T=-18.4(C), f(x)=(2.27 x + 222.43)*10^{-4}, r = 0.9999987
- 90 Mrad, T=-18.3(C), f(x)=(2.27 x + 223.08)*10^{-4}, r = 0.9999986
- 100 Mrad, T=-18.2(C), f(x)=(2.27 x + 223.25)*10^{-4}, r = 0.9999988
- 150 Mrad, T=-18.5(C), f(x)=(2.28 x + 221.98)*10^{-4}, r = 0.9999988
- 200 Mrad, T=-18.3(C), f(x)=(2.28 x + 221.65)*10^{-4}, r = 0.9999987
- 250 Mrad, T=-17.3(C), f(x)=(2.29 x + 221.50)*10^{-4}, r = 0.9999986
- 300 Mrad, T=-17.7(C), f(x)=(2.29 x + 219.69)*10^{-4}, r = 0.9999987
- 350 Mrad, T=-17.3(C), f(x)=(2.30 x + 218.71)*10^{-4}, r = 0.9999989
- 400 Mrad, T=-16.8(C), f(x)=(2.30 x + 216.99)*10^{-4}, r = 0.9999988
- 450 Mrad, T=-18.2(C), f(x)=(2.31 x + 218.08)*10^{-4}, r = 0.9999989
- 500 Mrad, T=-18.0(C), f(x)=(2.31 x + 217.05)*10^{-4}, r = 0.9999989
- 550 Mrad, T=-19.0(C), f(x)=(2.32 x + 214.66)*10^{-4}, r = 0.9999988
- 600 Mrad, T=-18.6(C), f(x)=(2.32 x + 215.44)*10^{-4}, r = 0.9999987


DAC linearity with external DVM, 600 Mrad
External DVM (V)
VCAL_HIGH (LSB)
0 Mrad, T=-19.5(C), f(x)=(2.26 x + 238.68)*10^-4, r = 0.9999988
1 Mrad, T=-19.4(C), f(x)=(2.26 x + 233.25)*10^-4, r = 0.9999987
2 Mrad, T=-19.3(C), f(x)=(2.26 x + 234.21)*10^-4, r = 0.9999990
3 Mrad, T=-19.4(C), f(x)=(2.26 x + 232.56)*10^-4, r = 0.9999988
DAC linearity with external DVM, 550 Mrad
External DVM (V)
VCAL_HIGH (LSB)
0 Mrad, T=-19.5(C)
1 Mrad, T=-19.4(C)
2 Mrad, T=-19.3(C)
3 Mrad, T=-19.4(C)
4 Mrad, T=-19.5(C)
5 Mrad, T=-19.6(C)
6 Mrad, T=-19.3(C)
7 Mrad, T=-19.3(C)
8 Mrad, T=-19.3(C)
9 Mrad, T=-19.2(C)
10 Mrad, T=-19.3(C)
20 Mrad, T=-19.3(C)
30 Mrad, T=-19.0(C)
40 Mrad, T=-19.2(C)
50 Mrad, T=-18.6(C)
60 Mrad, T=-18.7(C)
70 Mrad, T=-18.7(C)
80 Mrad, T=-18.4(C)
90 Mrad, T=-18.3(C)
100 Mrad, T=-18.2(C)
150 Mrad, T=-18.5(C)
200 Mrad, T=-18.3(C)
250 Mrad, T=-17.3(C)
300 Mrad, T=-17.7(C)
350 Mrad, T=-17.3(C)
400 Mrad, T=-16.8(C)
450 Mrad, T=-18.2(C)
500 Mrad, T=-18.0(C)
550 Mrad, T=-19.0(C)
500 Mrad, T=-18.0(C), f(x)=(2.31 x + 217.05)*10^-4, r = 0.9999989
550 Mrad, T=-19.0(C), f(x)=(2.32 x + 214.66)*10^-4, r = 0.9999988
600 Mrad, T=-18.6(C), f(x)=(2.32 x + 215.44)*10^-4, r = 0.9999987


DAC linearity with external DVM up to 600 Mrad
External DVM (V)
Dose (Mrad)
0.950
0.945
0.940
0.935
0.930
0.925
10^0
10^1
10^2
0 Mrad, T=-19.5(C)
1 Mrad, T=-19.4(C)
2 Mrad, T=-19.3(C)
3 Mrad, T=-19.4(C)
4 Mrad, T=-19.5(C)
5 Mrad, T=-19.6(C)
6 Mrad, T=-19.3(C)
7 Mrad, T=-19.3(C)
8 Mrad, T=-19.3(C)
9 Mrad, T=-19.2(C)
10 Mrad, T=-19.3(C)
20 Mrad, T=-19.3(C)
30 Mrad, T=-19.0(C)
40 Mrad, T=-19.2(C)
50 Mrad, T=-18.6(C)
60 Mrad, T=-18.7(C)
70 Mrad, T=-18.7(C)
80 Mrad, T=-18.4(C)
90 Mrad, T=-18.3(C)
100 Mrad, T=-18.2(C)
150 Mrad, T=-18.5(C)
200 Mrad, T=-18.3(C)
250 Mrad, T=-17.3(C)
300 Mrad, T=-17.7(C)
350 Mrad, T=-17.3(C)
400 Mrad, T=-16.8(C)
450 Mrad, T=-18.2(C)
500 Mrad, T=-18.0(C)
550 Mrad, T=-19.0(C)
600 Mrad, T=-18.6(C)





Comparison with previous tests:

- **CHIP: 0x0595**

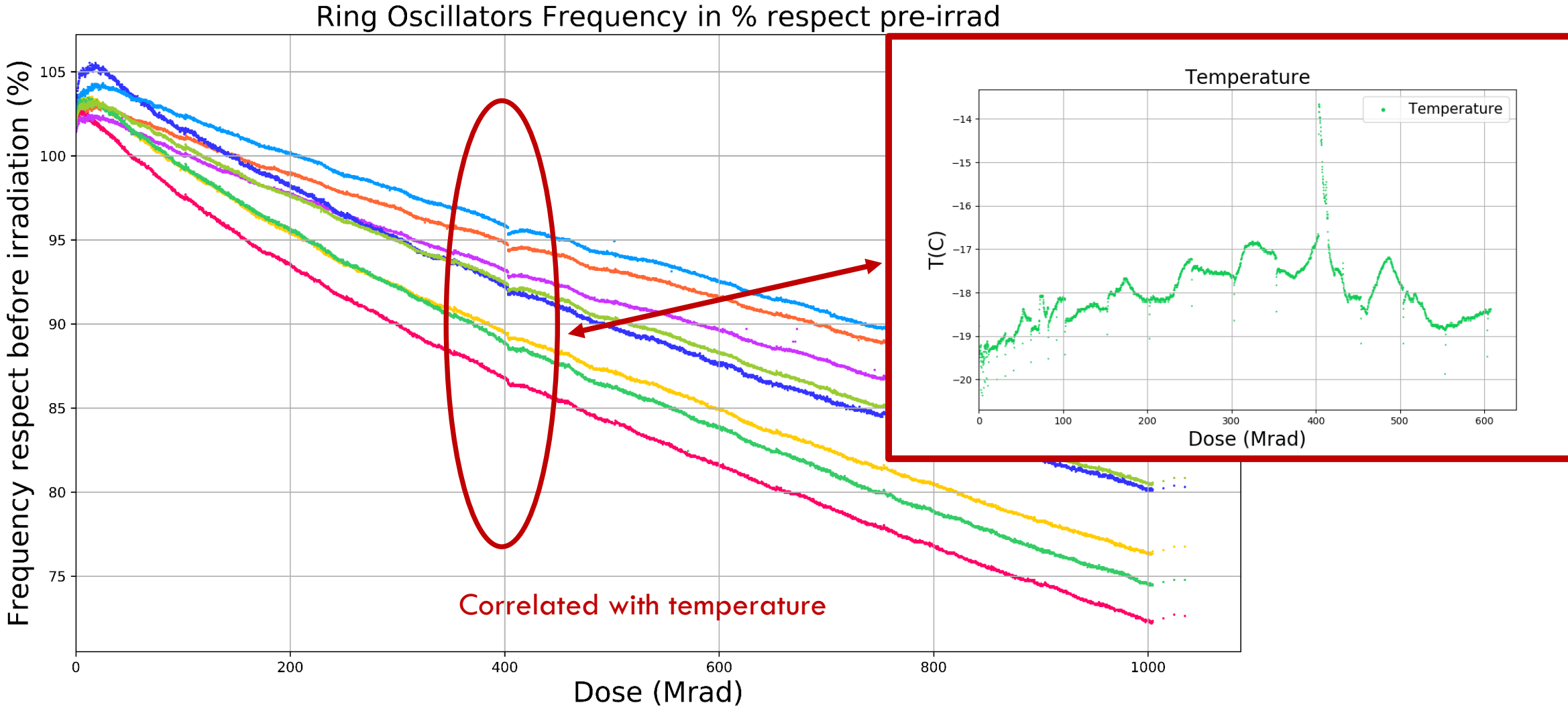
  Irradiated in Glasgow, 3.9Mrad/h campaign described in this presentation (here only plotting up to 500Mrad for comparison).

Difference between the two chips after 500Mrad is not big, about 3%difference after 500Mrad

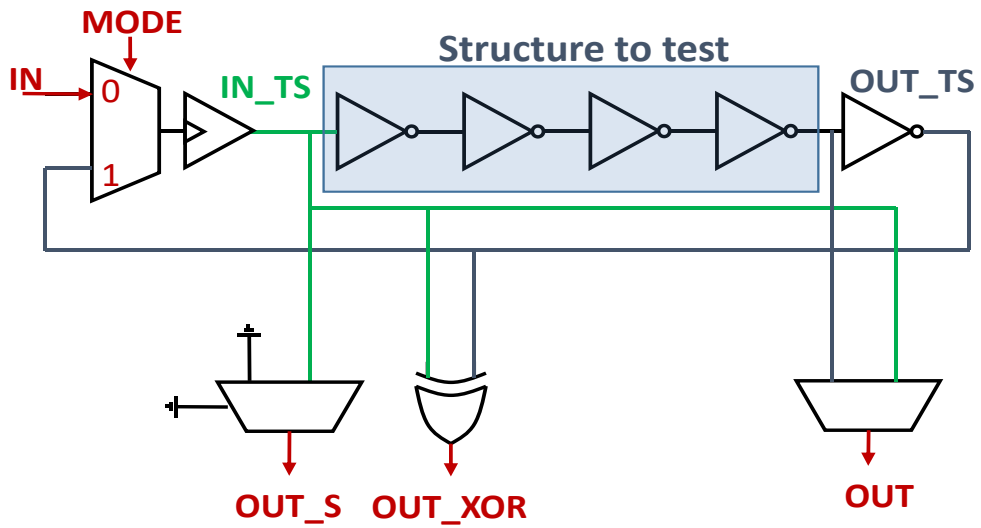
- **CHIP: 0x0765**

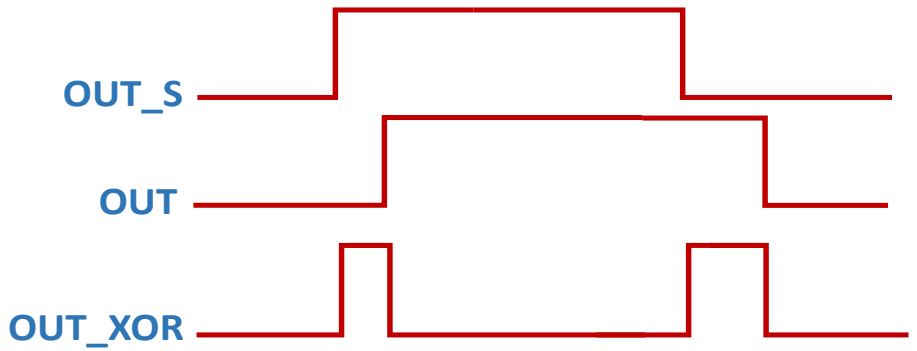
  Irradiated at CERN, 3.9Mrad/h, results explained by Vasyl Drozd in https://indico.cern.ch/event/743169/contributions/3085369/attachments/1698462/2734424/RingOsc_Drozd_07_08_2018.pdf

RING OSCILLATOR MEASUREMENTS



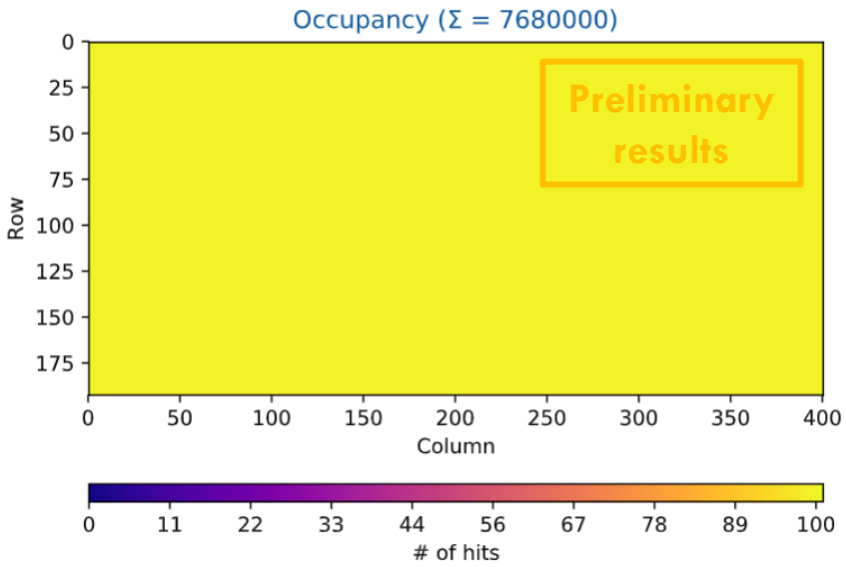
RING OSCILLATOR MEASUREMENTS IN DRAD CHIP

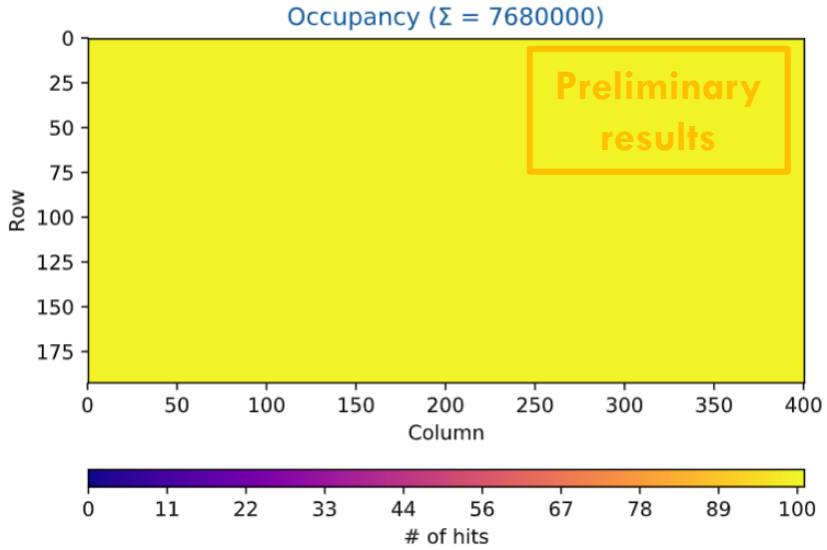




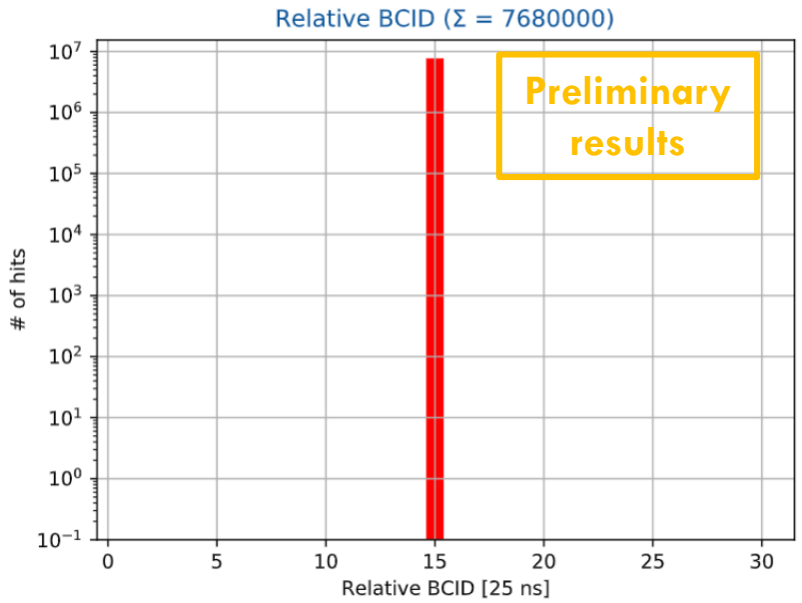
DIGITAL TESTS

- Chip is operating after 500Mrad.
- Command decoder responds, the chip is configurable.
- In order to test the digital buffering, signals can be sent to the digital domain simulating the output of the analog front-ends.
- No difference in Bunch Crossing ID and number of hits detected were seen after 1Grad.





Pre-irradiation



After 1Grad