Fast Timing and 4D Tracking with UFSD Detectors

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Outline

• 4D Tracking in HEP
• Timing in Silicon Detectors
• The UFSD Project
  • Front End Electronics
  • Detectors
  • Timing Performance
  • Radiation Hardness
• The CMS Endcap Timing Layer in HL-LHC
• Conclusions
The coming challenge:
High Luminosity = High Pile Up

CMS 78 vertices reconstructed

RMS 4.5 cm

Line density (mm$^{-1}$)

Vertex position (cm)
How to make use the timing information

1. Improve reconstruction by adding time information to each track point

2. Determine the correct vertex track assignment

Correct event reconstruction  Correct trigger assignment

associate single hit timing to track reconstruction

3-Jet event?  2-Jet and Missing Et event
IN HL-LHC ($2 \times 10^{35} \text{cm}^{-2}\text{s}^{-1}$)

- 150-200 vertices / beam crossing
- line density up to 1.8-2mm$^{-1}$
- $<t_{\text{vertex}}>_\text{RMS} \approx 200\text{ps}$
- a vertex separation resolution of 250-300μm → 10-15% overlapping 2 events

Event loss = Luminosity loss

With 30ps time resolution, instances of vertex merging are reduced from 15% in space to 1% in space-time

**Mip Timing Layer** proposal at CMS to consolidate particle flow performance at 140PU events, and extend it to 200PU (and similar proposal in ATLAS)
4D Tracking in HEP requires:

- High spatial resolution $\rightarrow$ Silicon Detectors
- High time resolution (~10ps)
- Fast FE electronics
- High radiation tolerance
- High fill factor (~1)
- High density $\rightarrow$ low power
Silicon Detector Time Resolution

\[ \sigma^2_t = \sigma^2_{\text{Jitter}} + \sigma^2_{\text{Time Walk}} + \sigma^2_{\text{Landau Noise}} + \sigma^2_{\text{Distortion}} + \sigma^2_{\text{TDC}} \]

Negligible
Optimize FE electronics

Negligible
Optimize RO electronics

\[ \sigma_{\text{Jitter}} \approx N/(dV/dt) \approx t_{\text{rise}}/(S/N) \]

- needs Gain to increase S/N
- needs thin detector to decrease \( t_{\text{rise}} \)

\[ i_{\text{Max}} \propto \text{Gain} \]

NB: signal amplitude DOES NOT depend on detector thickness

Decreases with detector thickness
Intrinsic Limit \( \sigma_{\text{Landau Noise}} \approx 20\text{ps} \)

\[ I_{\text{Ramo}} \approx q \cdot v_{\text{drift}} \cdot E_w \]

Requires uniform \( v_{\text{drift}} \) and \( E_w \)

parallel plate geometry
strip implant \( \sim \) pitch
Ultra Fast Silicon Detectors

use **Low Gain Avalanche Detectors layout** (Gain ~5-20 in p⁺/n++ junction with E~300kV/cm) and optimize design in order to

- optimize geometry for uniform E and $v_{\text{drift}}$
- optimize radiation hardness
- optimize doping profile for optimal gain
- optimize thickness, go to thin detectors (~50μm) to have small signal $t_{\text{rise}}$

NB: Gain **very sensitive** to doping concentration (few %)

Excellent agreement with TCAD simulation (best fit van Overstraeten model)
Characteristics of FE Electronics

**Current Amplifier**
- Fast slew rate
- Higher noise
- Sensitive to Landau bumps
- More power

**Integrating Amplifier**
- Slower slew rate
- Lower noise
- Signal smoothing
- Less power

**Time measuring circuit**

<table>
<thead>
<tr>
<th>Technology</th>
<th>CMOS 110 nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channels</td>
<td>8</td>
</tr>
<tr>
<td>Sensor capacitance</td>
<td>2-10 pF</td>
</tr>
<tr>
<td>Input dynamic range</td>
<td>3 fC - 60 fC</td>
</tr>
<tr>
<td>Analog gain</td>
<td>7 mV/fC</td>
</tr>
<tr>
<td>GBW</td>
<td>14 GHz</td>
</tr>
<tr>
<td>RMS noise (C=6pF)</td>
<td>800 μV</td>
</tr>
<tr>
<td>Discriminator output</td>
<td>2 – 14 ns</td>
</tr>
<tr>
<td>Power consumption</td>
<td>18 mW/ch</td>
</tr>
<tr>
<td>AVDD/DVDD</td>
<td>1.2 V/2.5 V</td>
</tr>
</tbody>
</table>

50ps time resolution achieved on test beam.
Close collaboration with FBK:

- **UFSD 1** FBK (300μm) various test structures to validate gain doping profiles, layout design, first irradiation tests 2015

- **UFSD 2** FBK(55μm) focused to doping profiles validation, doping element validation for radiation hardness (B or Ga, and Carbon concentration splits) 2017

- **UFSD 3** FBK (55μm), wafers for optimization of Carbon concentration fine splitting, layout design for fill factor optimization, pixel design and uniformity check for CMS ETL prototype 2018

UFSD 2 and UFSD 3 parallel productions with **CNM** and **HPK**
UFSD Time resolution

UFSD best resolution achieved so far **30ps**
UFSD3 splits (stepper production)

20 wafers with combinations of

- **Low** and **High** gain layer diffusion profiles
- 5 splits of Carbon doses (A,B,C,D, no Carbon)
- 5 splits of gain layer doses
- Epi vs FZ

Wafers delivered in summer 2018
UFSD3 I-V and C-V curves, uniformity check

56 CMS ROC

10 bad channels out of 5600 in 7 gain splits <0.2%

Same results
On ALTIROC and MoveIT structures
76 detectors tested from 16 Wafers (836 strips), 7 bad Channels

Breakdown voltages and CV curves as expected
UFSD3 fill factor test structures

Dedicated test structures to study and minimize interstrip dead region

Currently no gain area

CNM 70μm
HPK 100μm
FBK 70μm

30μm gap corresponds to 96% fill factor, target!
p-stop could be replaced by tranches, 1μm wide

How to further increase fill factor

Trench isolation technology
- Typical trench width < 1 μm
- Max Aspect ratio: 1:20
- Trench filling with: SiO₂, Si₃N₄, PolySi

Safe design
UFSD2 - UFSD3 test structures fill factor studies

UFSD3 test structures: moving from «safe» to «aggressive» design, the $V_{BD}$ decreases strongly. «aggressive» design $V_{BD}$ is so low that the structure is not fully depleted and the interpixel dead region increases wrt «intermediate» ts.

A long uniform p-stop might be causing early breakdown by shifting its potential away from the n++ pixel via punch-through.
TCT laser scan on a 2x2 test structures and strips. Results indicate that $V_{BD}$ decreases when large p stop areas are present, and that charge amplification occurs mostly in the corners.

The effect is not present for UFSD3 structures for the experiments (CMS, ATLAS, MoveIT) where each pad is surrounded by a single p-stop.
Fill factor: a possible alternative under study

- 100% fill factor
- Segmentation is achieved via AC coupling

The AC read-out sees only a small part of the sensor:
small capacitance and small leakage current.

N.Cartiglia TREDI 2015, M.Mandurrino (INFN grant Resistive AC coupled Silicon Detectors, 2018)
LGAD radiation tolerance studied within the CERN RD50 collaboration
Radiation fluences requested to operate at HL-LHC ~5 \(10^{15}\) particles/cm\(^2\), radiation doses of 150Mrad (primarily due to Non-Ionizing Energy Loss)

\[ N(\Phi) = N(0) \times e^{-c\Phi} \]

gain layer radiation depletion

Effects:
1. same effects of standard n-p Si detectors: increase of Leakage Current (decrease T), increase of \(V_{BD}\) and \(V_{FD}\), due to increase of doping concentration. Creation of trapping centers (minimize the effect going to thin sensors (!))
2. peculiar on LGAD:
   1. Further increase of leakage current (and power) due to gain layer: go thin, keep gain low
   2. UFSD2: Gain loss due to gain layer acceptor removal. Boron atoms are displaced and become interstitial, thus not contributing to the doping profile: increase \(V_{bias}\), change acceptor (add Carbon to decrease interstitial phase space, and test replacing Boron with Gallium)
Results from UFSD irradiation test campaign: Gallium doped gain layer is the most radiation sensitive. Carbon is very effective, both with Gallium and Boron. Boron+Carbon wins!
24 GeV/c protons produce the same amount of initial acceptor removal as a function of the fluence (particles/cm²) as neutrons.

Gain recovery is well described by simulation (WF2). At higher doses high $V_{\text{bias}}$ gain layer disappear but gain starts occurring in the bulk.
UFSD2 irradiation tests, time resolution

30-35ps resolution @ 1.5e15 $n_{eq}/cm^2$, which corresponds to HL-LHC ETL CMS lifetime of 4000fb$^{-1}$
The Endcap Timing Layer for CMS at HL-LHC

CMS Endcap Timing Layer

1.6 < |\eta| < 2.9

~1800 sensors = ~15m²

Single pad 1x3mm²
In the current TP, recently proposed to move to ALTIROC geometry (1.3x1.3mm²)
ETL detector power consumption

Large fluctuations at small radii, requires specific R&D (increase $V_{bias}$ fragmentation by reducing sensor dimensions requires better fill factor performances).
Outlook and conclusions

• irradiation campaign on UFSD3, detectors irradiated and ready for testing (currently being done in Torino)

• fill factor: probably needed a new dedicated UFSD3.x run on interstrip geometry optimization. Improve TCAD simulation

• 2 postdocs studying and designing optimized FE electronics for UFSD fast timing applications in Torino

• collaboration ongoing on side projects
  • MoveIT (development of fast beam monitor for Hadrontherapy treatments)
  • PSI R&D plan for enhancement of soft (1-5keV) x-ray detection
  • Resistive AC coupled Silicon Detectors (TCAD simulation and first run in preparation)

• growing involvement in ETL activities (deadline for ETL TDR march 2019)

• more UFSDn to come....

• LGAD is a fast developing but mature technology (4 manufacturers on the market)

• 4D tracking is an HEP experimental need. UFSD are being proposed for large area detectors in HL-LHC (~30m² in CMS and ATLAS)
Acknowledgments

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16 sensors tested → 400 pads
- @ 250V the 0.25% of the pads deviate from the optimal behavior
- @ 300V the 0.5% of the pads deviate from the optimal behavior
  - the 0.25% of the pads is in BD
- @ 350V
  - 12.5% of the sensors in BD before 350V
  - 2.6% of the pad in BD (on sensors not in BD)
Carbon depletes the gain layer

\[ d = \left[ \frac{2 \varepsilon V_{\text{bias}}}{qN} \right]^{1/2} \]