



Contribution ID: 101

Type: not specified

Radiation hardness studies and irradiation test results of RD53A chip, a large scale chip demonstrator for pixel readout at the HL-LHC

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ABSTRACT: The RD53A prototype chip is a 400x192 pixel readout integrated circuit (IC) designed to qualify the chosen 65nm CMOS technology for the development of the final production IC of the Phase-2 upgrade of ATLAS and CMS experiments at the High-Luminosity (HL) Large Hadron Collider (LHC). This 20.0mm by 11.8mm chip has been designed in the framework of the RD53 collaboration [1], a joint effort between ATLAS and CMS communities, and it contains design variations for testing purposes, different analog front-end and digital architectures.

The harsh environment of HL-LHC including a peak luminosity of $5 \times 10^{34} \text{cm}^{-2}\text{s}^{-1}$, an estimated ionizing dose (TID) of 1Grad and 1MeV neutron equivalent fluence of $2 \times 10^{16} \text{cm}^{-2}$ accumulated during their lifetime and very high rates of the order of 3GHz/cm², sets challenging requirements for the detectors of these experiments. The RD53A collaboration has made an effort to characterize the radiation effects in the 65nm CMOS technology, whose radiation tolerance properties have been investigated for analog and digital circuits with specific test chips.

The RD53A chip includes ring oscillators to characterize the radiation damage on digital circuits, and also a radiation sensor. Design techniques to overcome the radiation effects and TID test results up to 500Mrad will be reported.

KEYWORDS: Radiation damage to electronic components; Radiation-hard electronics, pixel readout chip.

References

[1] J. Christiansen and M. Garcia-Sciveres, RD Collaboration proposal: development of pixel readout integrated circuits for extreme rate and radiation, LHCC-P-006 (2013)

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