Monolithic CMOS sensors at HL-LHC (pp)

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With many thanks to my colleagues who kindly provided material

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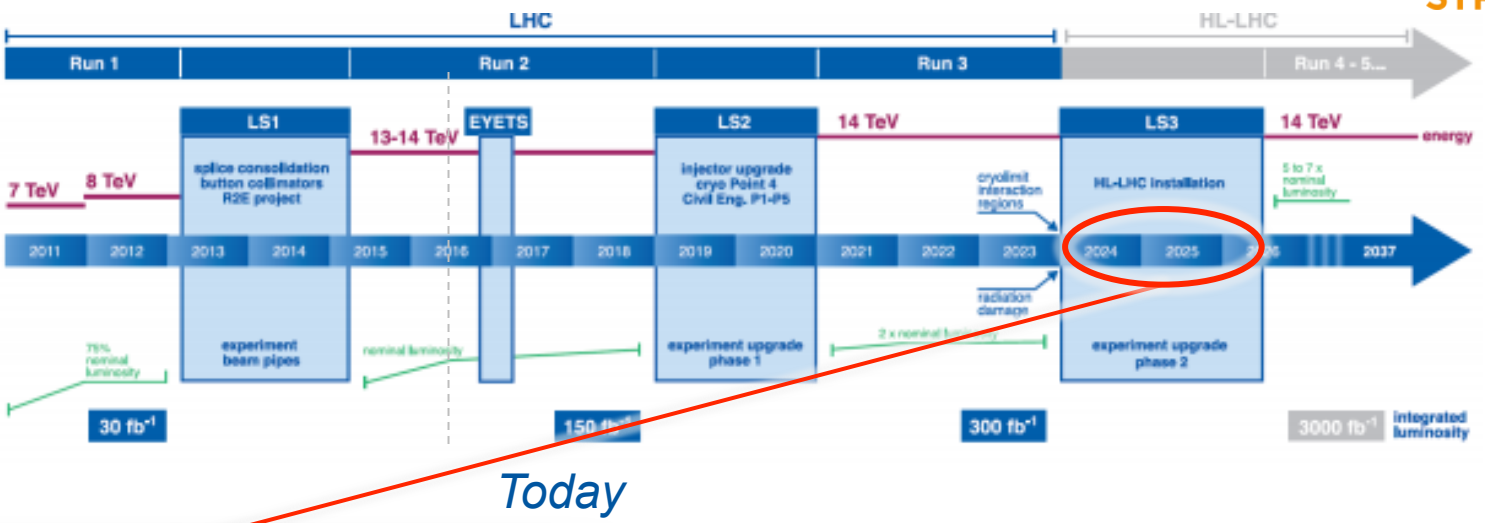
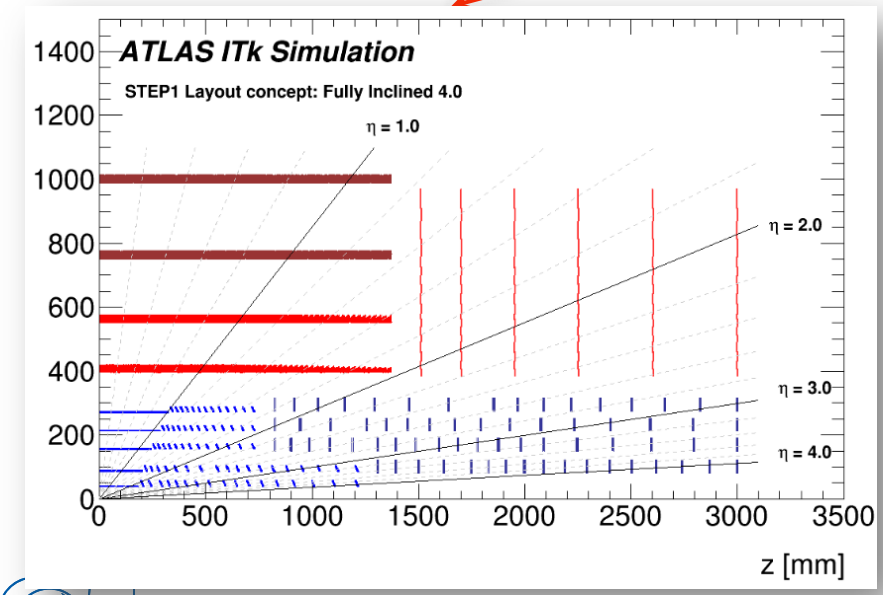
Tracker Upgrade @ LHC



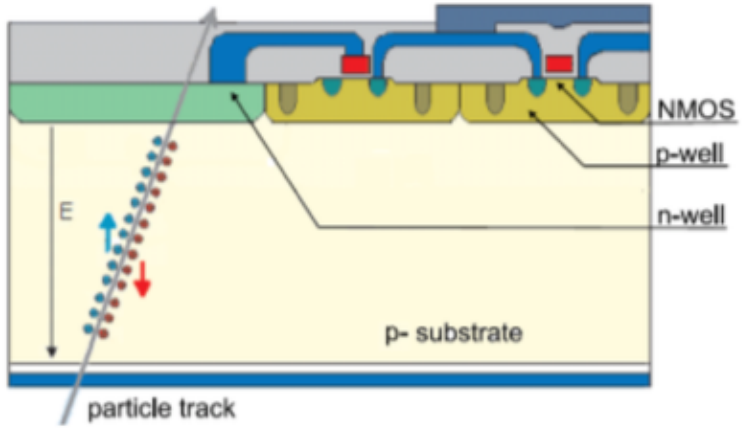
Today



- **2024/25: Phase 2 ATLAS** ATLAS completely replace its trackers
- ~ 160 m^2 silicon strips
- ~10 m^2 silicon pixel

Monolithic Silicon Pixel Detectors

Depleted Monolithic Active Pixel Sensors



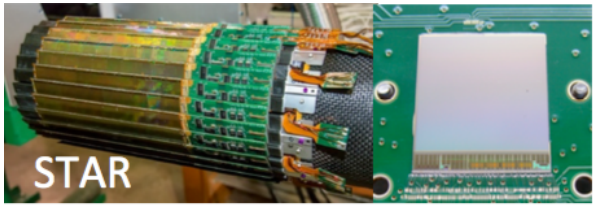
- Depletion is key for fast signal response and radiation hardness
- Thin detector with high granularity

- FE electronics is integrated in sensor and produced on commercial CMOS processes
- **Allows very thin sensors to achieve ultimate low mass trackers (0.3% X/X_0 in Heavy-Ions or <1% for pp)**
- **High volume and large wafers (200mm) reduces detector costs and allows large area pixel detectors**
- **Saves costs of bump-bonding (cost driver for hybrid silicon detector systems**

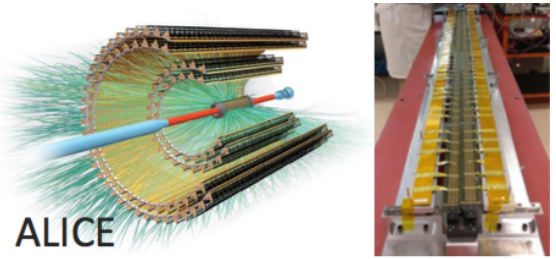
DMAPS/CMOS for Trackers

See talks Monday/Tuesday — today

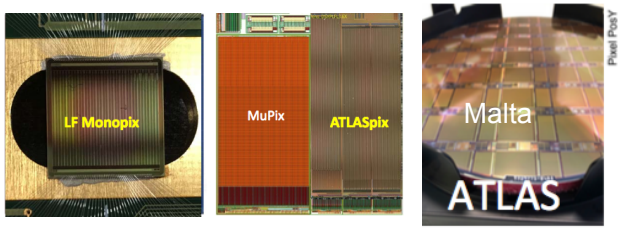
	RHIC STAR	LHC - ALICE ITS	CLIC	HL-LHC Outer Pixel	HL-LHC Inner Pixel	FCC pp
NIEL [n_{eq}/cm^2]	10^{12}	10^{13}	$<10^{12}$	10^{15}	10^{16}	10^{15}-10^{17}
TID	0.2Mrad	<3Mrad	<1Mrad	80 Mrad	2x500Mrad	>1Grad
Hit rate [MHz/cm^2]	0.4	10	<0.3	100-200	2000	200-20000



Ultimate Sensor



Alpide Sensor

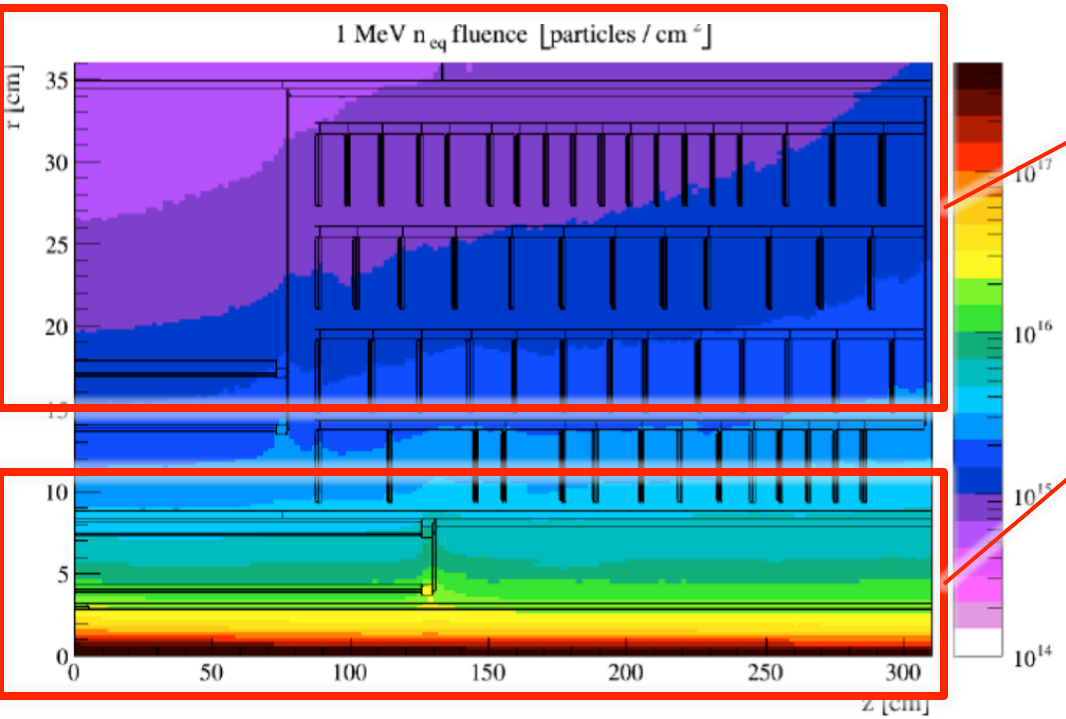


Monopix & AtlasPix & Malta Sensor

- Advances in commercial CMOS technologies combined with dedicated designs allowed significant progress from STAR to ALICE to ATLAS in areas like radiation hardness, response time, hit rates
- **Strong interest to fully exploit potential of MAPS in future Trackers**
  - **High granularity, Low material budget and power, Large area at reduced cost (cf hybrid)**
  - **CMOS foundries offer substantial processing power to enable significant performance gains**

Environment at HL-LHC (pp)

- Radiation level, hit rates and bunch structure for silicon detector dominate the development of sensors and Front-end electronics
  - 25ns BC
  - L1 trigger rate (e.g. ATLAS 4MHz)



- Strip layers
  - NIEL ~ 10^{14} neq/cm^2
  - TID ~ 10Mrad
  - Larger area O(100m^2)
- Outer pixel layers
  - NIEL ~ 10^{15} neq/cm^2
  - TID ~ 50Mrad
  - Larger area O(10m^2)
- Inner layers
  - NIEL ~ 5x10^{15} to 10^{16} neq/cm^2
  - TID ~ 1Grad
  - Smaller area O(1m^2)

ATLAS CMOS Pixel Collaboration

- Collaboration of ~25 ATLAS ITK institutions

The STREAM MSC ITN

- The STREAM Project is the Marie Skłodowska Curie **Innovative Training Network for CMOS Sensor Development** in the context of LHC experiments and for selected industrial applications

- The STREAM research and training program focuses on the development of **radiation hard CMOS sensor technologies** for innovative scientific and industrial instruments.

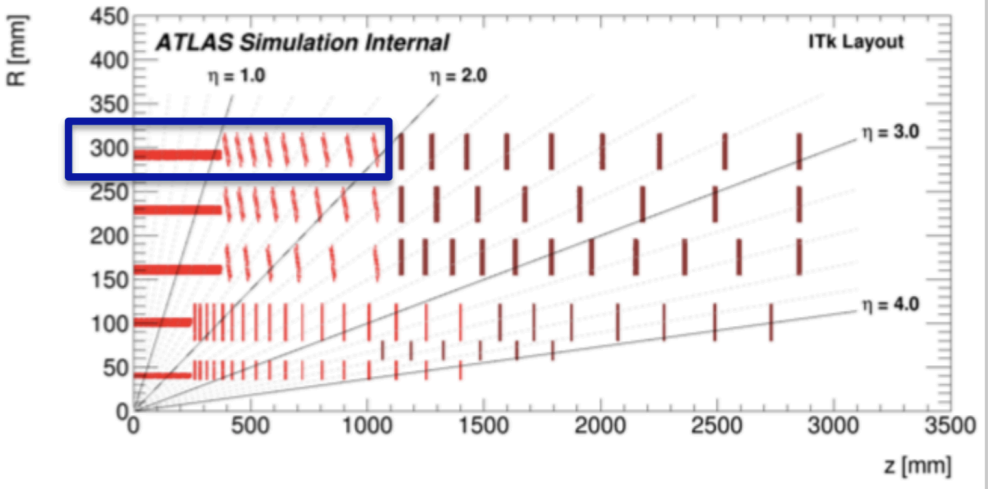
- STREAM offers **17 fellowships for the Early-stage researchers** to participate in the design and test of novel radiation hard CMOS sensors

- Parts of the ATLAS CMOS RD on CMOS sensors are supported through the STREAM MC fellows

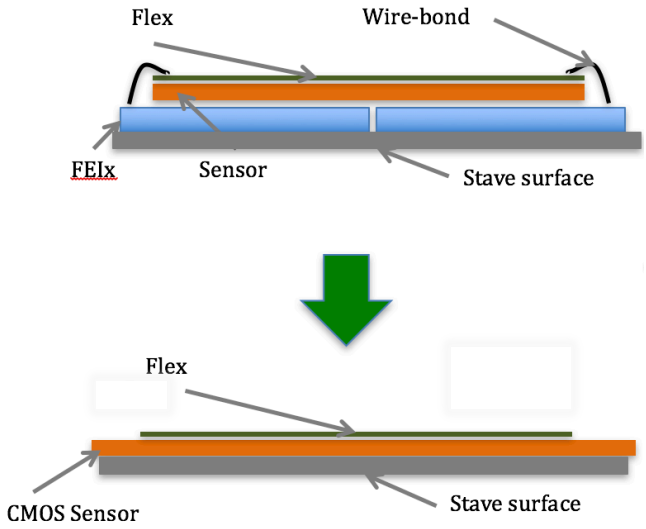
- **STREAM Website:** http://stream.web.cern.ch/

CMOS considered for ATLAS ITk

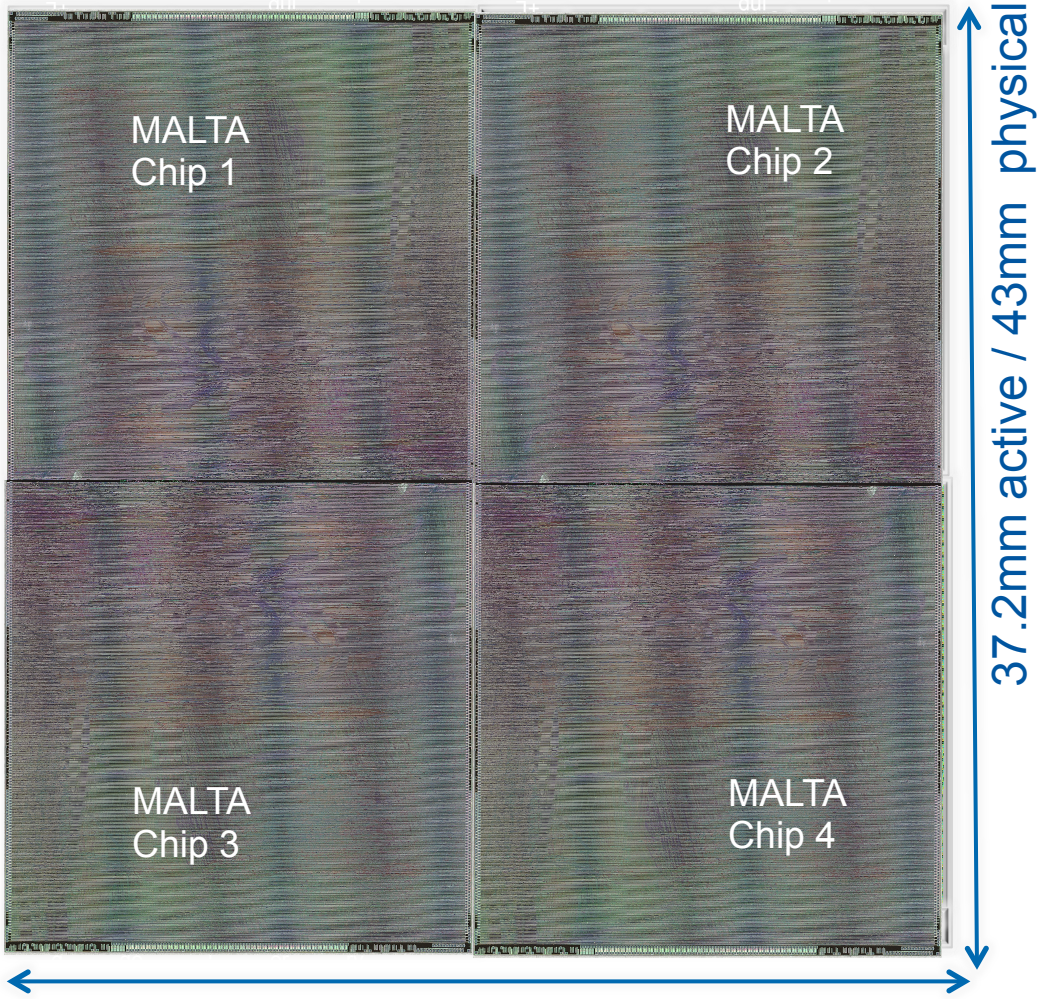
- Outermost layer of ITk Pixel Barrel
  - 2016 quad modules
  - 3m^2 (~45% of outer barrel layers)
- For 4000 fb-1 integrated luminosity
  - TID = 80Mrad
  - NIEL 1.5 x 10^{15} n_{eq}/cm^2



- Monolithic CMOS sensors are considered as option for the outermost layer
  - Saves bump bonding for ~45% of outer barrel system
  - Substantial cost reduction and reduced module assembly time
  - Requires “Drop-In” module compatibility to hybrid module



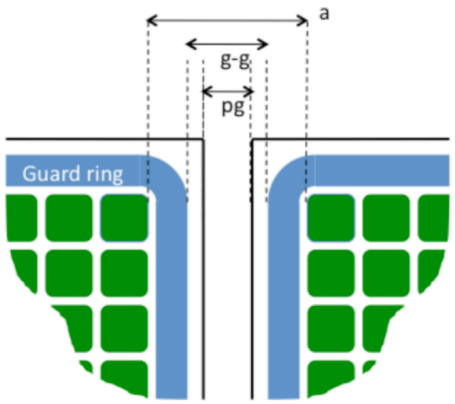
ATLAS CMOS "Quad" Module



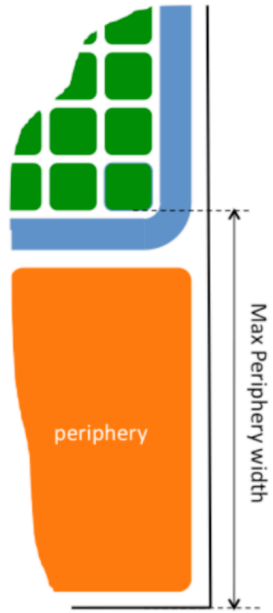
- Require electrical and mechanical compatibility with baseline hybrid modules
  - Close links to RD53 developments
- CMOS Module is assembly of 4 sensor dies in 2x2 chip matrix "CMOS Quad Module"
- Do not consider stitching for CMOS modules
- Aim at minimal gap region
- Goals prototype ITK CMOS Quad Module:
  - Demonstrate mechanical assembly of CMOS based Quad module
  - Electrical readout within constraints of existing chips

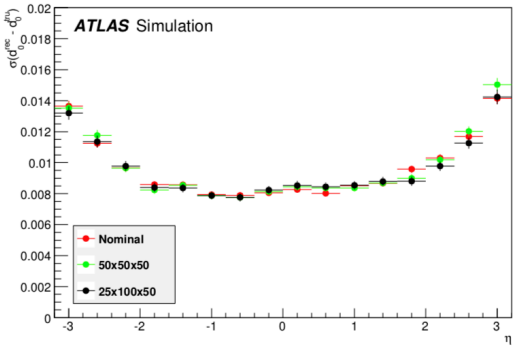
Specs for ITk CMOS modules

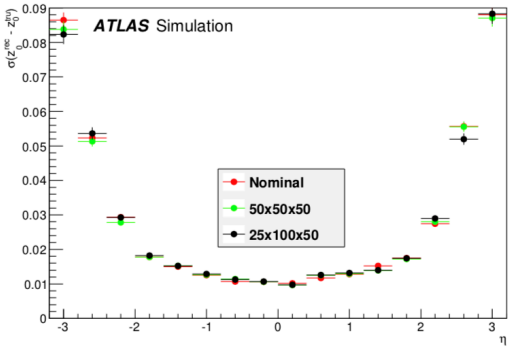
- Mechanical module envelope:
  - 41.1 (η) x 42.1 (RΦ) mm^2
- Chip size:
  - 20.5 x 21 mm^2
- Pixel pitch:
  - technology dependent, not critical for performance
- Active area:
  - hybrid is 20 x 19.2 mm^2
  - due to large module overlap, considering trading off some area for additional periphery space
  - greater than 18mm in RΦ
- Positioning:
  - 100 μm between seal lines (pg)



a ... active area gap
G-g ... guard ring – guard ring gap
Pg ... physical gap

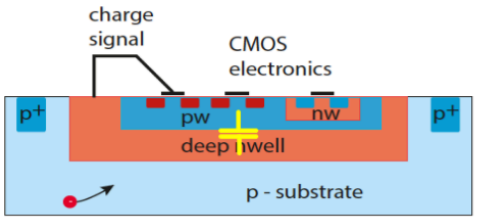






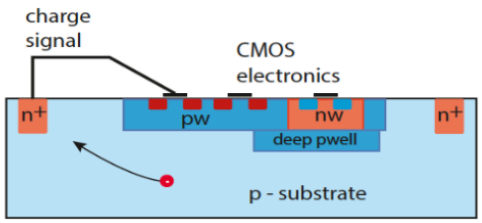
Different CMOS sensor designs

- Large electrodes



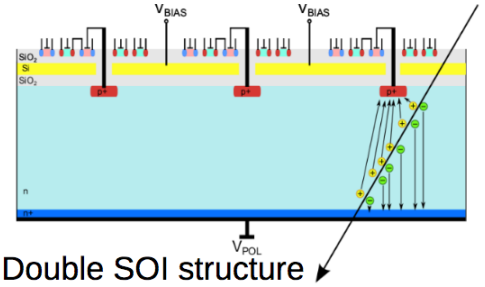
- Electronics in collection well
- No or little low field regions
- Short drift path for high radiation hardness
- Large(r) sensor capacitance (dpw/dnw) ->higher noise and slower @ given pwr
- Potential cross talk between digital and analog section

- Small electrodes



- Electronics outside collection well
- Small capacitance for high SNR and fast signals
- Separate analog and digital electronics
- Large drift path -> need process modification to usual CMOS processes for radiation hardness

- "Burried" electrodes (SOI)



Double SOI structure

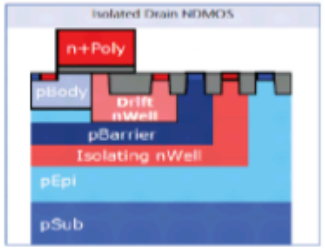
- Electronics and sensor in separate layer
- Can use thick or thin high resistivity material and HV (>200V)
- Special design/ processing to overcome radiation induced charge up of oxides

Radiation hard CMOS sensor

$$d \sim \sqrt{\rho \cdot V}$$

1 **"High" Voltage add-ons to apply 50 – 200 V bias**

2 **"High" Resistivity Substrate Wafers (100 Ωcm – kΩ cm)**

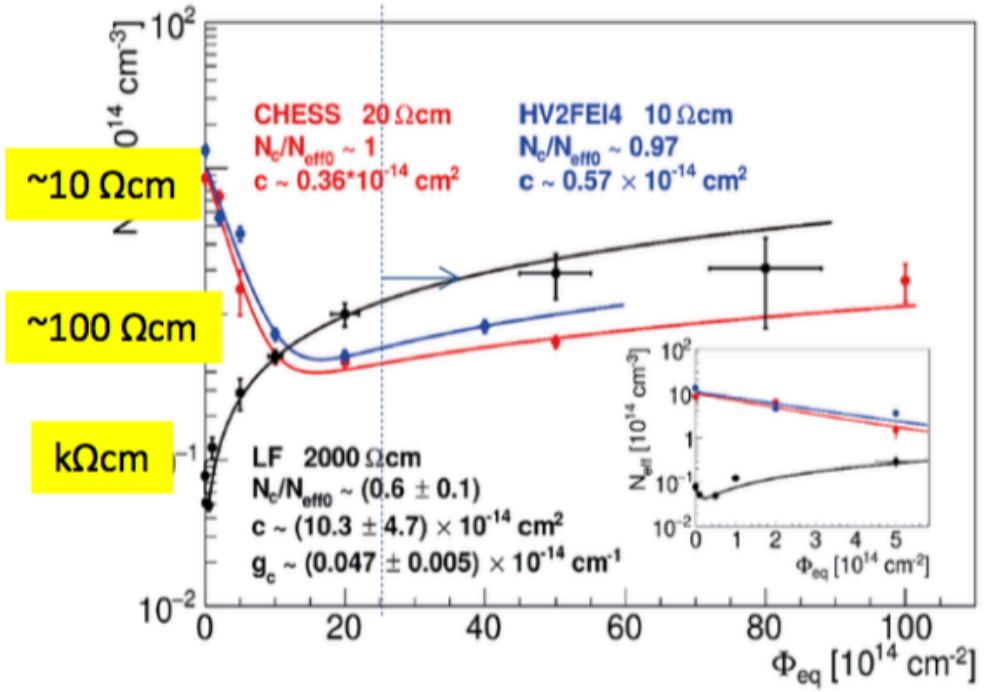


from: www.xfab.com

3 **Multiple (3-4) nested wells (for shielding and full CMOS)**

4 **Backside Processing (for thinning and back bias contact)**

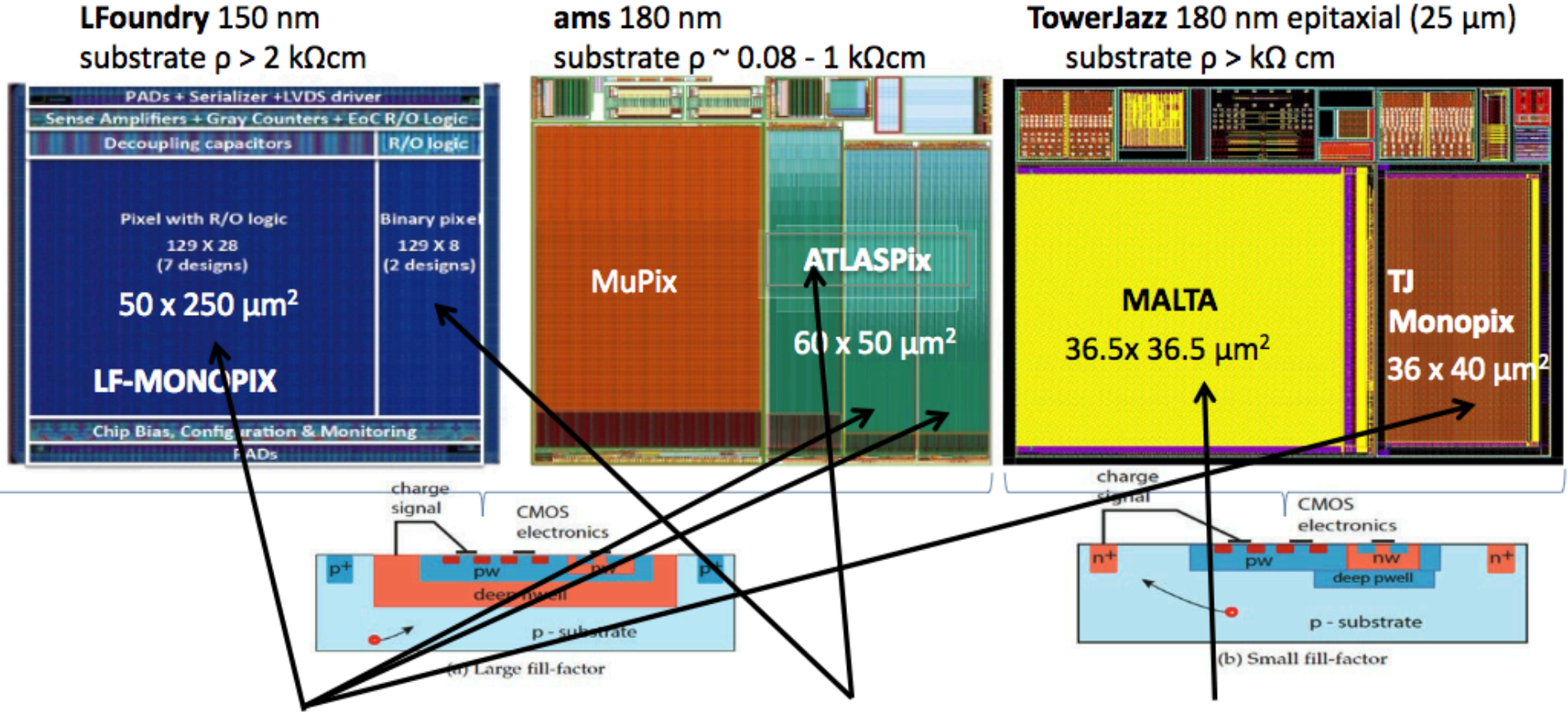
Effective resistivity after HL-LHC irradiation ~ O(100Ωcm)



I. Mandic et al., JINST 12 (2017) no.02, P02021

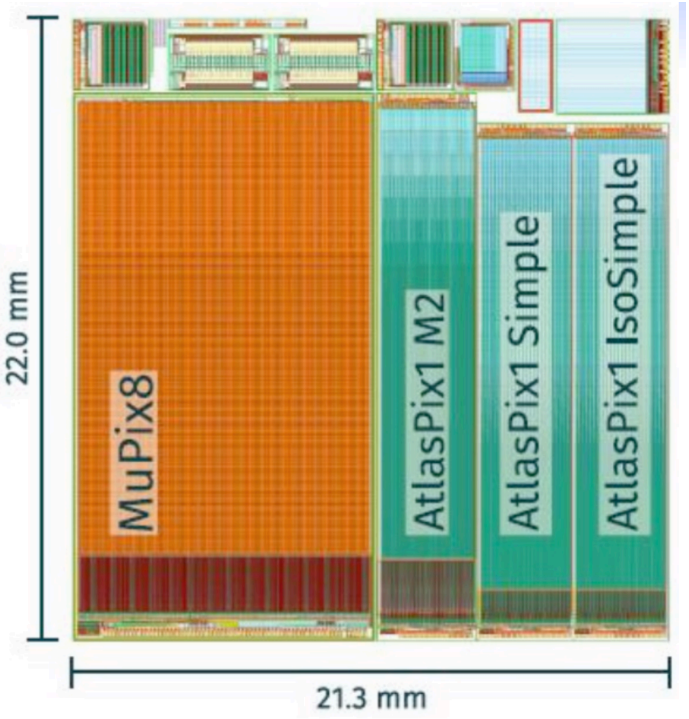
CMOS sensor developments for ATLAS

- Use “medium” feature size processes 150nm to 180nm which allow for combination of HV-tolerant design and choice of HR substrates/epi-layers



HVCMOS sensors (AMS 180nm)

Developments in context of ATLAS and μ3e experiment using large n-electrodes in different HR substrates

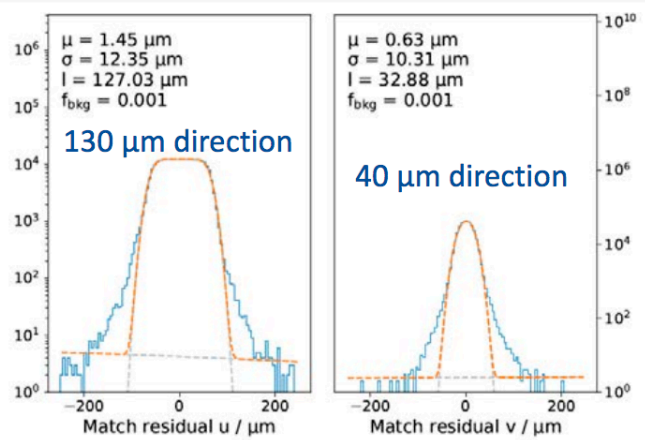


ATLASPix1 M2
- 320×56 pixel matrix
- 50×60 μm2 pixel size
- triggered readout

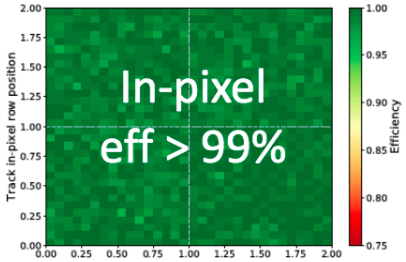
ATLASPix1 Simple
- 400×25 pixel matrix
- 40×130 μm2 pixel size
- asynchronous Readout of signal to periphery with "column drain"-type buffer/ToT in periphery

Karlsruher Institut für Technologie

Resistivity 80 Ωcm & 200 Ωcm



65V HV bias
Threshold 840 mV

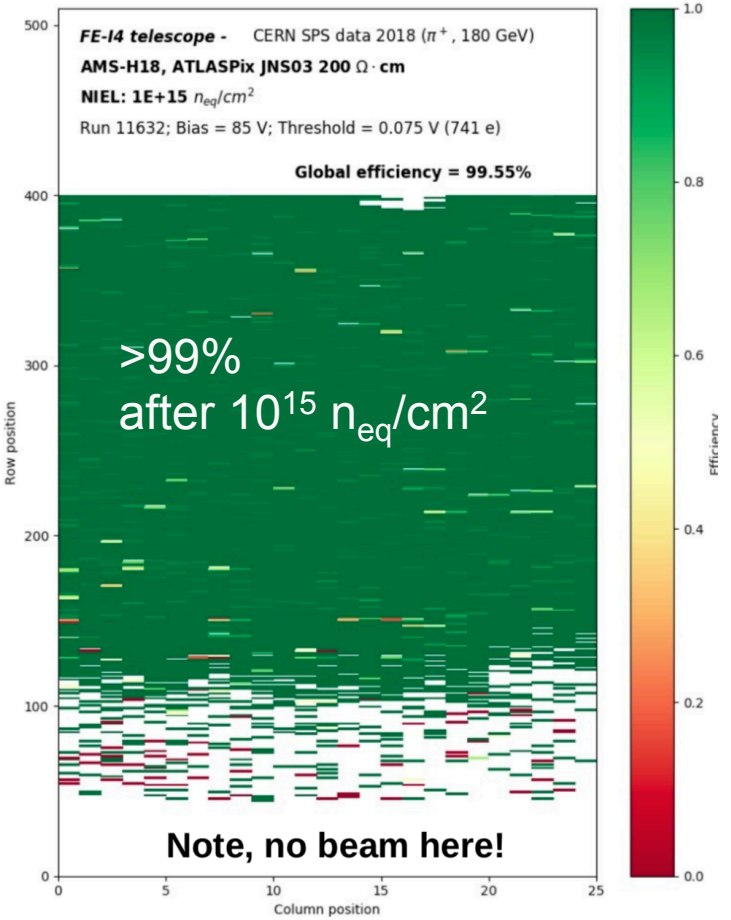


ATLASPixSimple1 irradiation

- Neutron irradiated samples of different substrate resistivities 80/200Ωcm) to Atlas ITk outermost layer specs

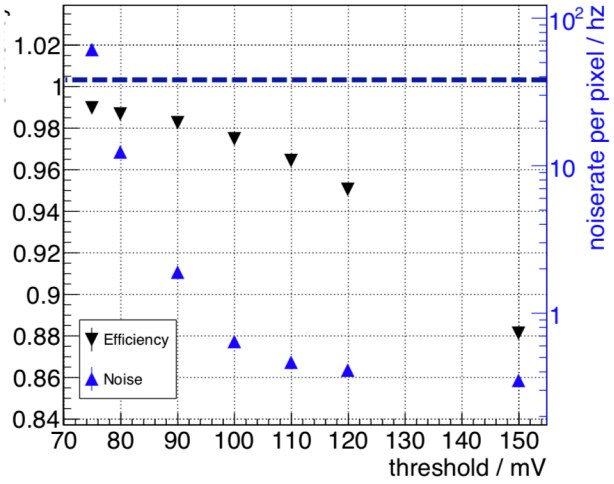
ATLASPix1 Simple
• 40×130 µm2 pixel Size

full efficiency after irradiation with neutrons



$2 \cdot 10^{15}$ n_{eq}/cm^2
200 Ω cm
final (100mu)
T ~ 10°C

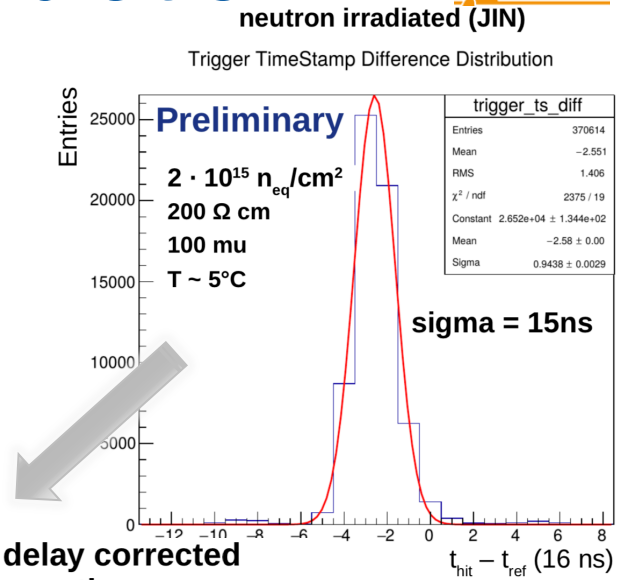
bias = 95 V



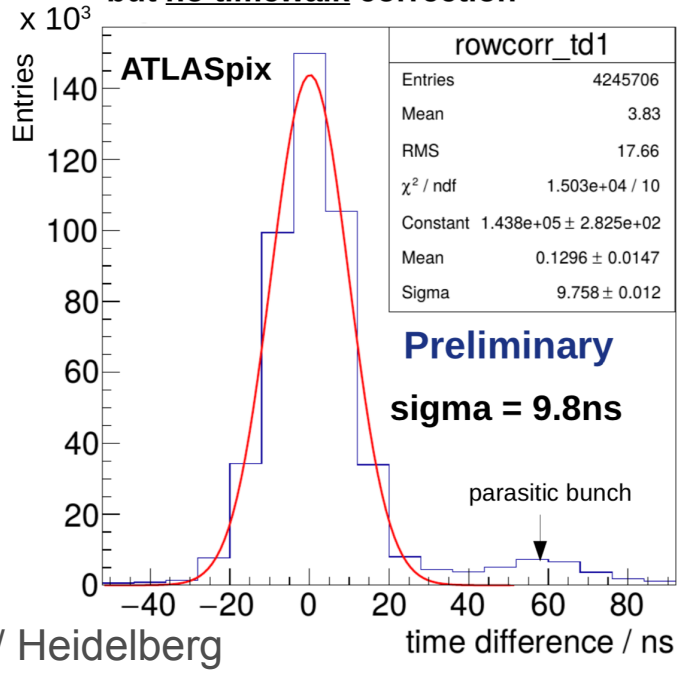
ATLASPixSimple1 irradiation

- **25ns time requirements on response time**
  - Sum of **analog time-walk** and **signal latency in column**
  - Translates to time resolution σ ~6ns required
- In-time efficiency ~84% after irradiation
  - Low threshold and off-line delay correction
- Further effort in improvement of analog time walk on-going
  - e.g. through TW compensated comparator or 2-threshold like Mu3e MuPix sensor
- Optimize signal transmission along column to periphery

Correct for column signal delay and lower threshold



Threshold 70 mV; delay corrected but no timewalk correction

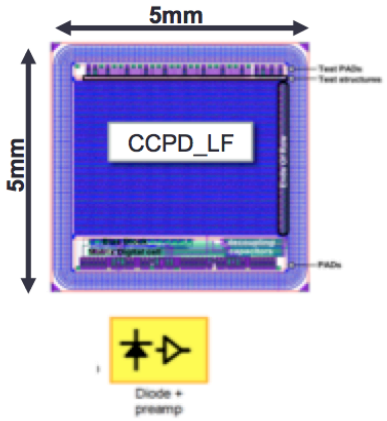


LFoundry ATLAS prototypes

- Developed sensors in 150nm process on 2kΩcm substrates

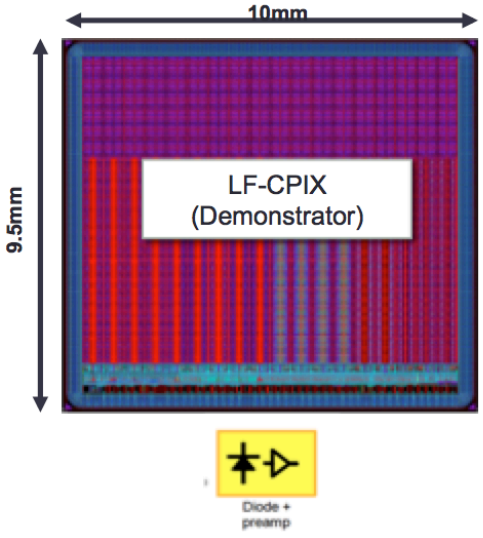
2014~2015
Small size demonstrator

CCPD_LF:
33×125µm² pix ; 6pix → 2 FEI4 pix
5×5 mm² IC, **bondable to FE-I4**
Bonn / CPPM / KIT



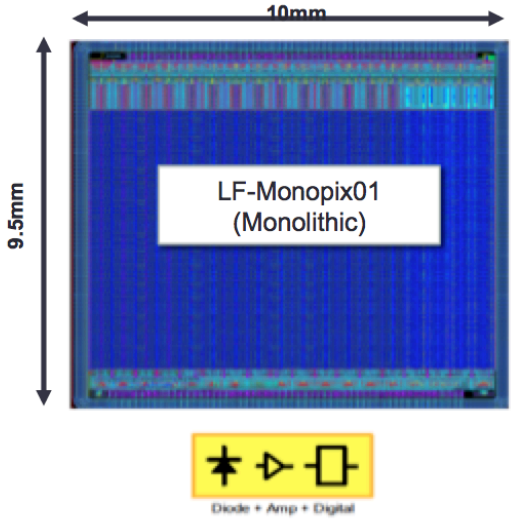
2016~2017
Large size demonstrator

LF-CPIX:
50×250µm² pix ; diff. pix flavors
10×10 mm²; 2 versions -Guard-Ring-
Bonn / CPPM / IRFU



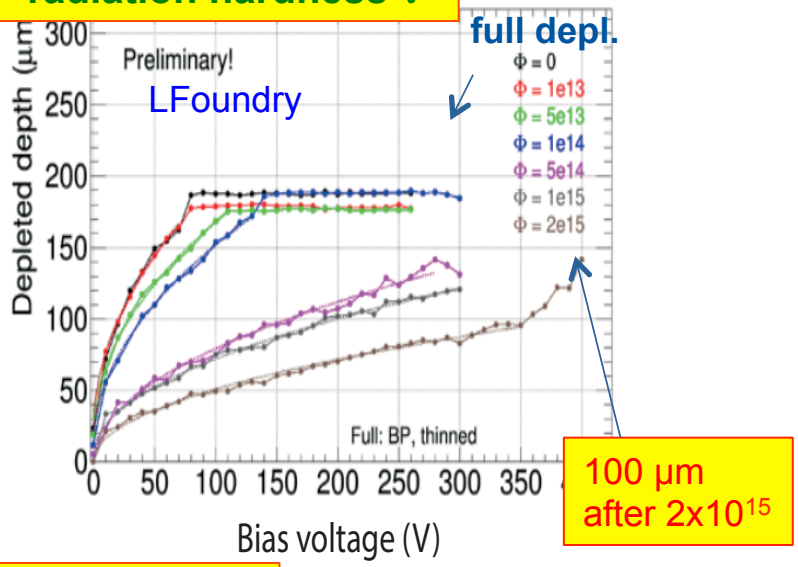
2017~Present
Large Monolithic demonstrator

LF-Monopix:
50×250µm² pix.
Analog pixel part from LF-CPIX
10×10 mm².
1st full monolithic demonstrator
Bonn / CPPM / IRFU

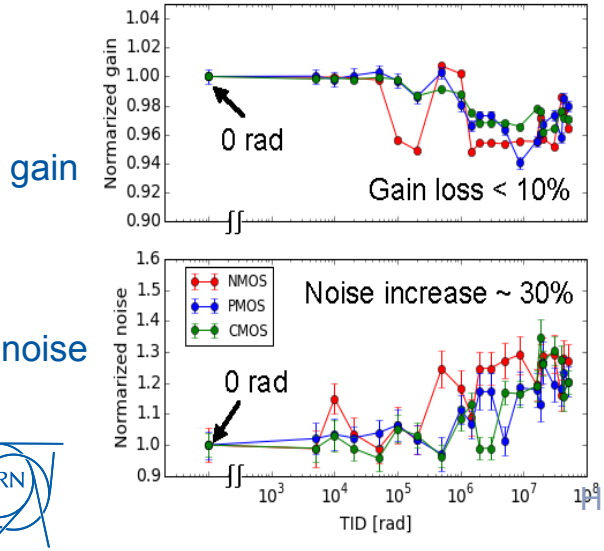


LF-CPix and MonoPix Sensor

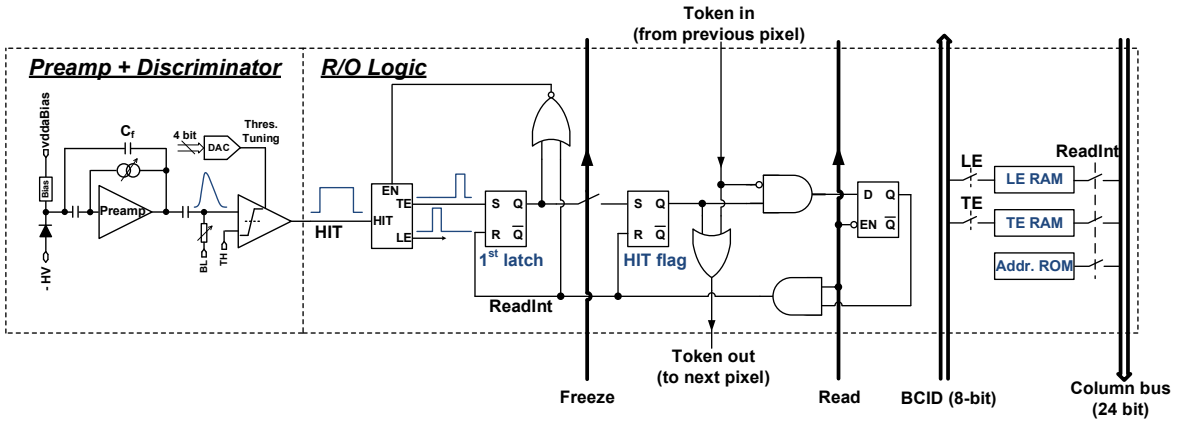
• **radiation hardness ✓**



• **TID 1 MGy ✓** LFoundry



- Implements Column drain architecture in large-electrode pixel, similar to what is used in current hybrid pixel detector
- Full depletion of 200um thick substrates before irradiation
- After irradiation ~100um depletion



LFMonoPix before/after irradiation

- Non-irradiated

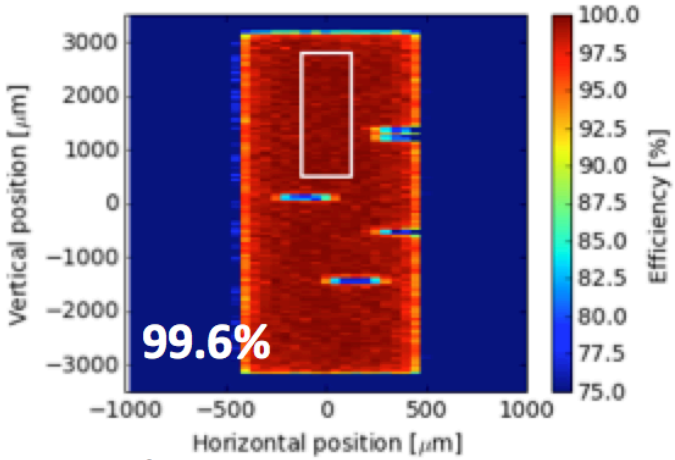
  Columns: 16-20

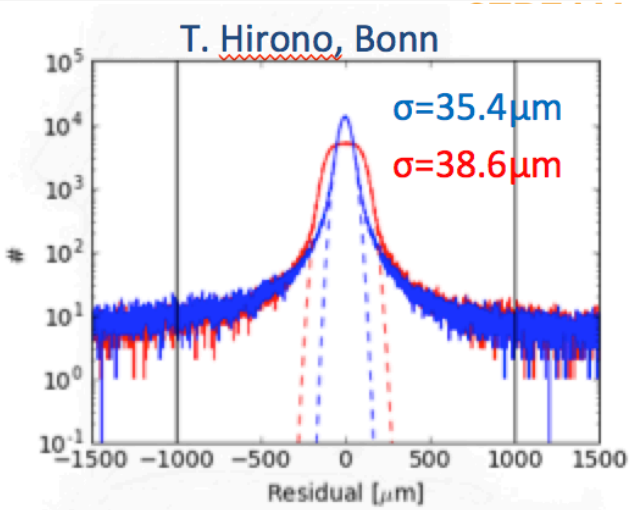
  TH ~ 1600 e^-

  HV: -200V

  Temp: dry ice

  Masked pixel: 5/516





- $1 \times 10^{15} n_{eq}/cm^2$ (neutron @ JSI)

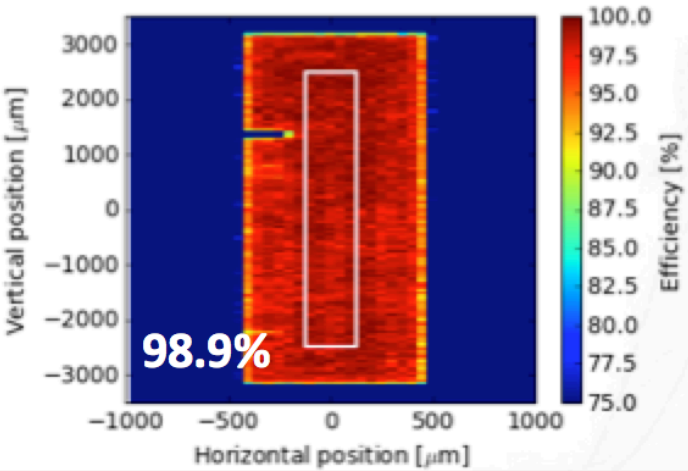
  Columns: 16-20

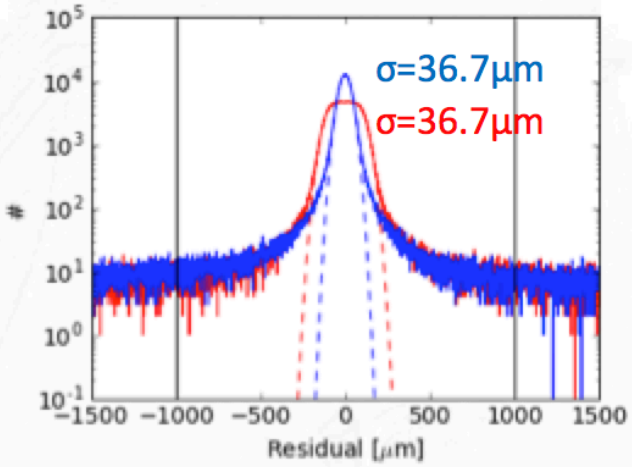
  TH ~ 1800 e^-

  HV: -130V

  Temp: dry ice

  Masked pixel: 1/516

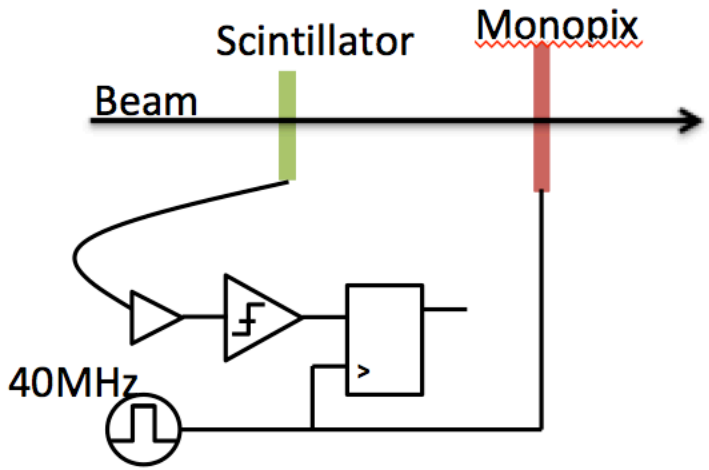




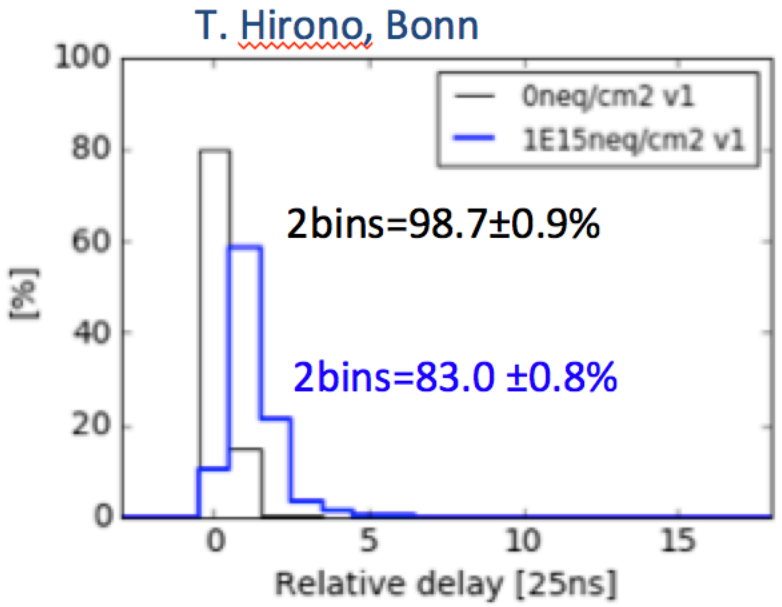
Noise occupancy < 10^{-7}/25ns, more than an order of magnitude lower than requirement

Tianyang Wang/Bonn

LFMonoPix before/after irradiation



Delay = (Monopix LE) - (Scintillator LE)

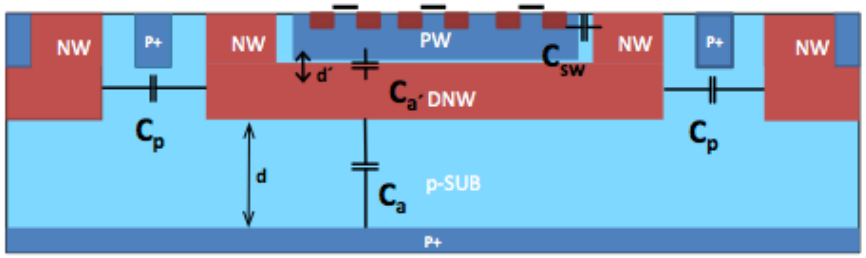


- Measurement limited by the timing resolution given by the 40 MHz clock
  - *Promising, but more precise measurement needed*
- Higher time walk for irradiated chip @ default settings, can be improved by
  - *Optimization of DAC settings, e.g. CSA/discriminator bias*
  - *Higher bias voltage + thinning and back side bias => larger signal*

Input capacitance is critical

- On sensors described sofar, the **analog & digitial circuit is placed inside collection well**
- Input capacitance is dominated by additional capacitance between n-well and p-well

Hybrid planar pixels (e.g. ATLAS IBL): **Cin = 109 fF**
(Havranek et al, NIMA 714 (2013) 83-89
CMOS pixel extrapolation: **Cin ≈ 200 fF**



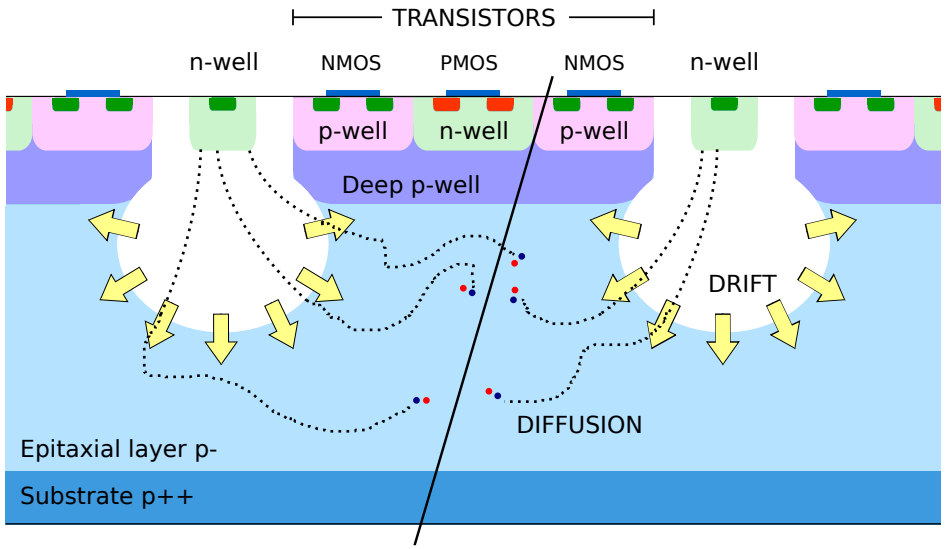
- Response time: $\tau_{CSA} \propto \frac{1}{g_m} \frac{\mathbf{C_d}}{C_f}$
- Noise: $ENC^2_{thermal} \propto \frac{4}{3} \frac{kT}{g_m} \frac{\mathbf{C_d^2}}{\tau}$

Total input capacitance drives peaking time and ENC
Counteract by increasing transconductance – but this increases power consumption significantly

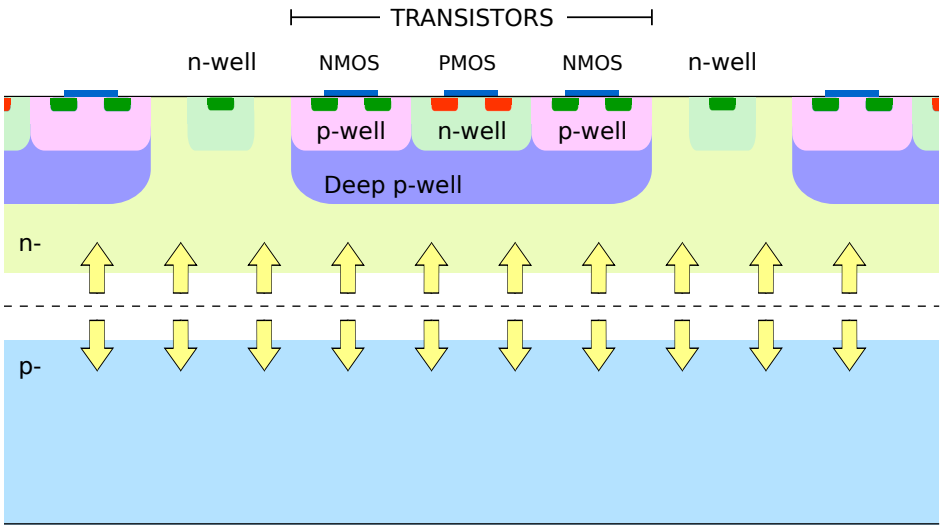
- Additionally digital signals are contained in collection well – hence risk of severe cross-talk of digital signals to collection well
  - Can be minimzed by special source follower (P. Rymaszewski / Bonn)

TowerJazz 180nm MALTA sensor

- Small collection electrode (few um²)
- **Small input capacitance (<3fF) allows for fast & low-power FE**
- High S/N for a depletion depth of ~20um
- To ensure full lateral depletion, uniform n-implant in the epi layer (modified process)



Standard Process



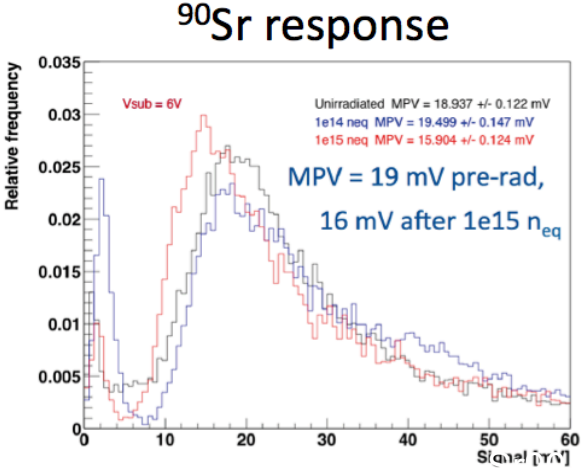
Modified Process

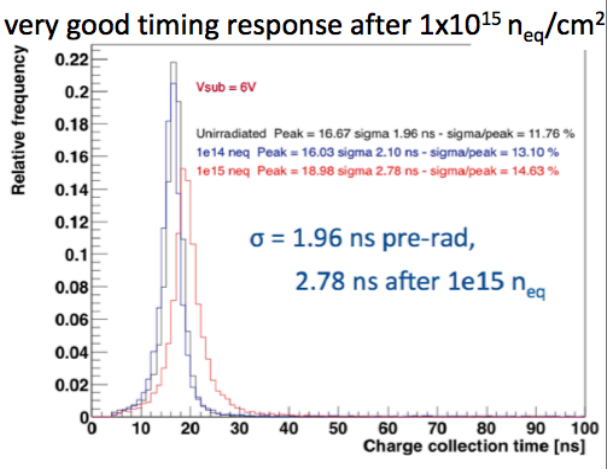
W. Snoeys et al. DOI 10.1016/j.nima.2017.07.046

Initial results with small electrodes

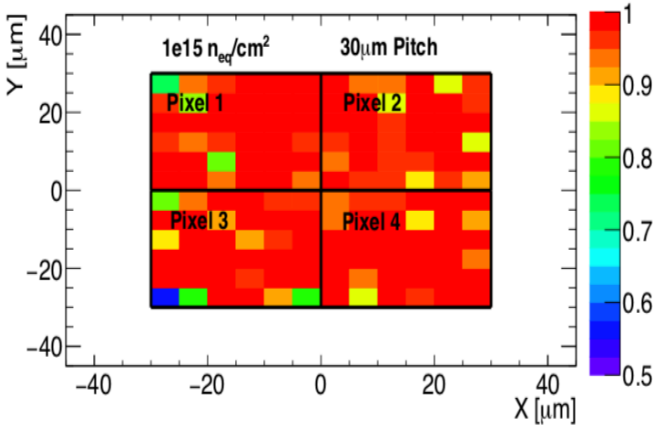
- **TJ180nm Investigator Sensor**
  - Developed in context of ALICE ITS
  - Studies of influence of pixel pitch, electrode size & spacing
- Irradiated and measured for studies in ATLAS

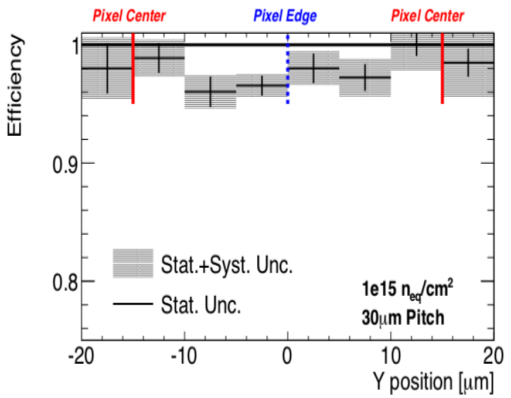
2017 Investigator measurements





Irradiated Investigator





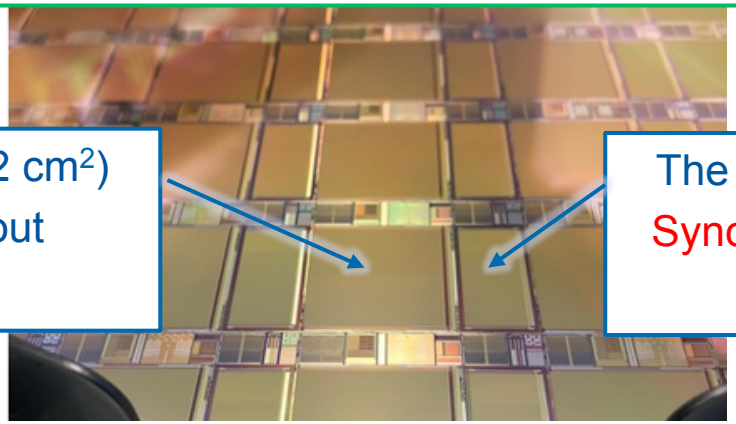
H. Pernegger et al 2017 JINST 12 P06008

Efficiency 97.4%
After 10^{15} n_{eq}/cm^2
at low threshold (<100e)

MALTA & MonoPix – Novel depleted CMOS sensors with small electrodes

Design of two large scale demonstrators to match ATLAS specifications for outer pixel layers

The "MALTA" chip (2 x 2 cm^2)
Asynchronous readout architecture

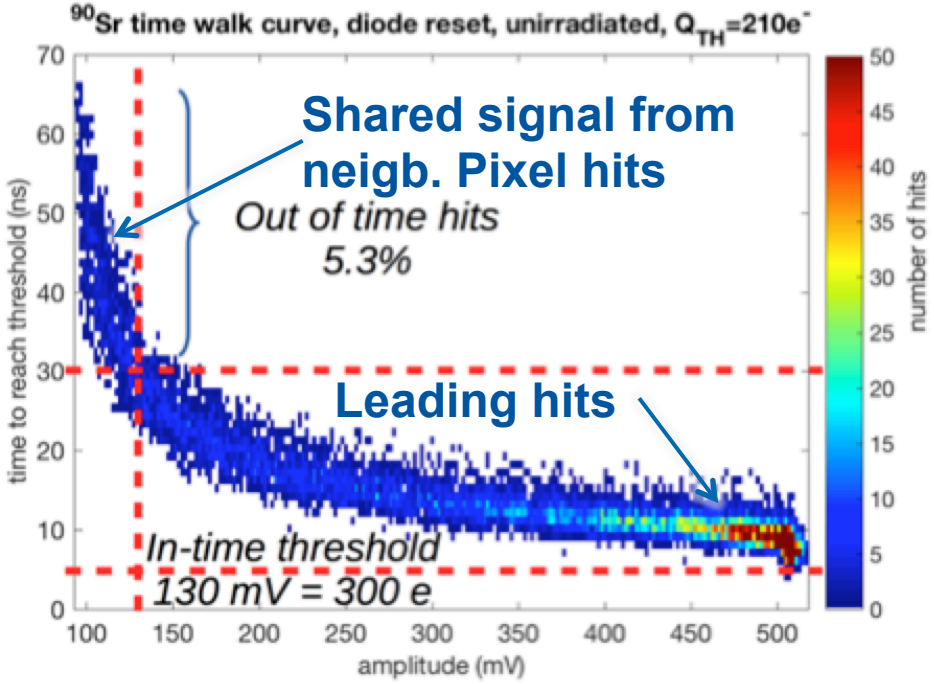


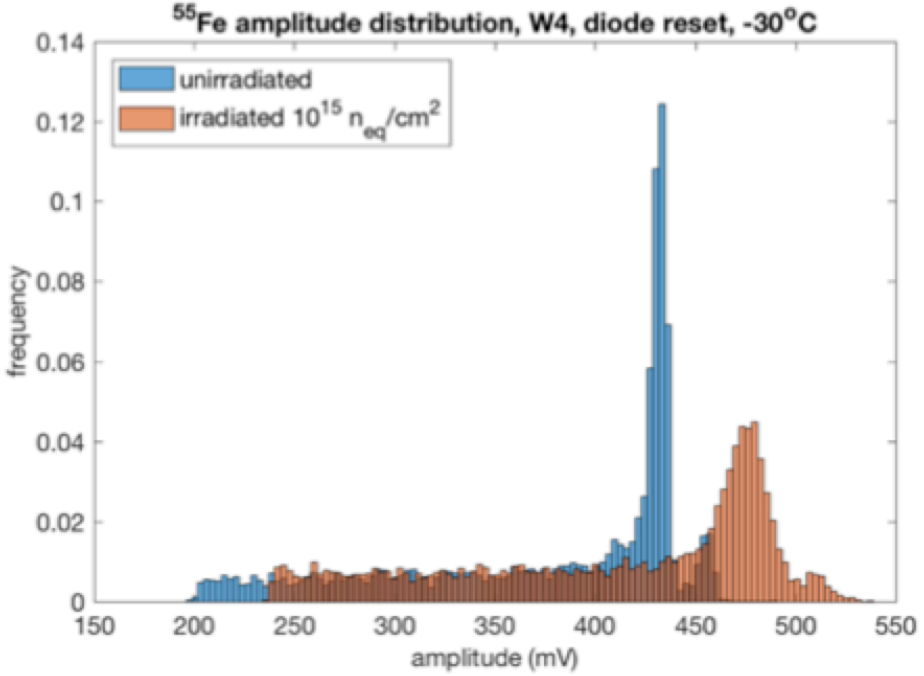
The "TJ-Monopix" chip (2 x 1 cm^2)
Synchronous readout architecture.

- **The ATLAS "MALTA" and "MonoPix" chips** for **high hit rate suitable for HL-LHC pp-collisions**
  - **Radiation hard to >10^{15} n/cm^2 & Shaping time 25ns** (BC = 25ns)
  - **MALTA: Asynchronous readout** architecture for high hit rates and fast signal response
  - **MonoPix: Synchronous Column drain** readout architecture

MALTA analog after irradiation

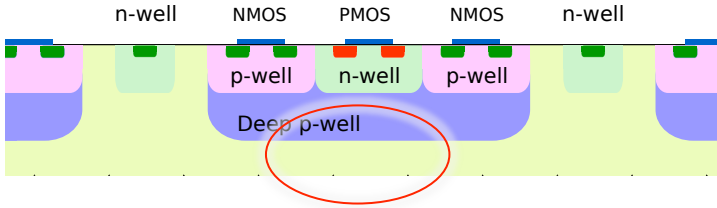
- Neutron irradiated 10^{15}neq/cm^2
- Good analog performance for ENC and timing
- Need improvement on threshold dispersion



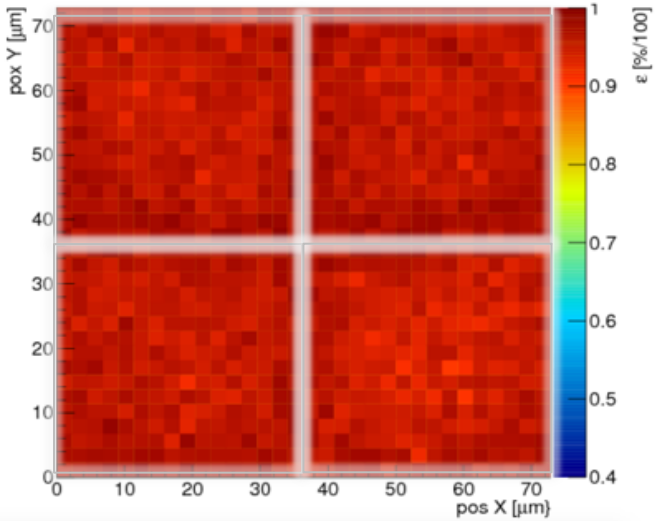


Efficiency with small electrodes

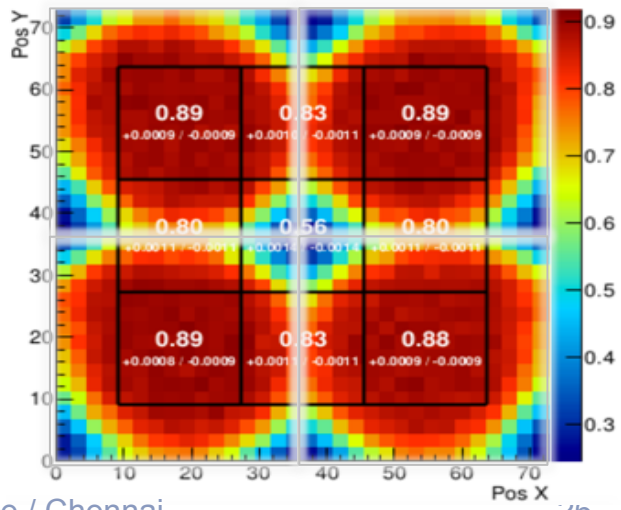
- Corner efficiency one of the essential questions
- Due to small collection electrode, the field configuration and charge collection under DPW in pixel corner is critical
  - Require full depletion under the DPW
  - Operating at low threshold is essential
  - Transversal field components in corner is needed for radiation hardness



Unirradiated @ 250e- threshold
2x2 pixel at 36um pitch

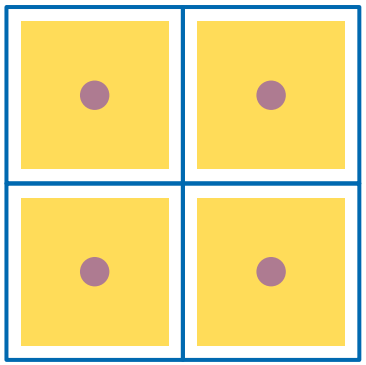


Irradiated 10^{15}n/cm^2 @ 350e- threshold
2x2 pixel at 36um pitch

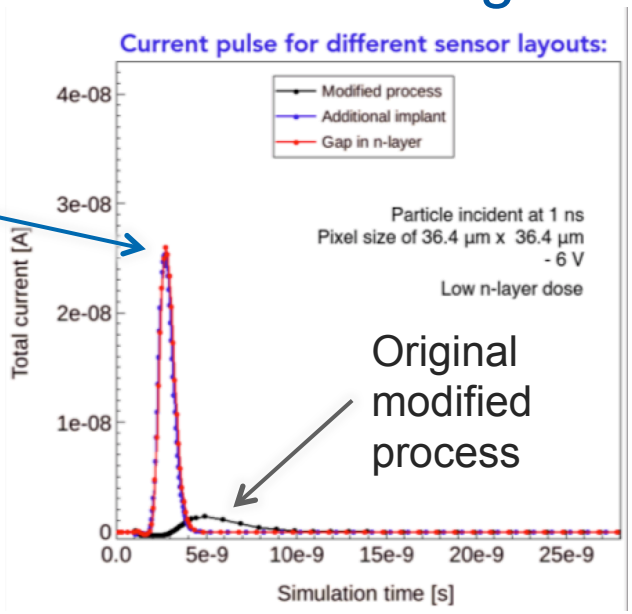


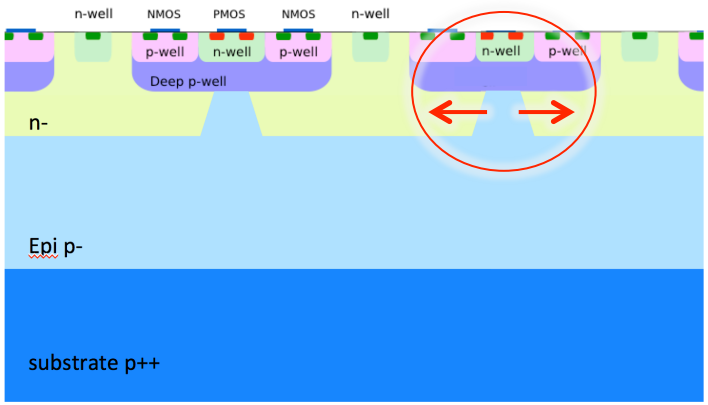
Fix corner efficiency for small electrodes

- Key for good radiation hardness/charge collection is to generate lateral field under DPW
  - See M. Munker's talk Wednesday
  - E.g. gap in n- layer to "focus" charges to electrode
- Optimized design in TCAD simulations
- Implemented in new sensor design and submitted

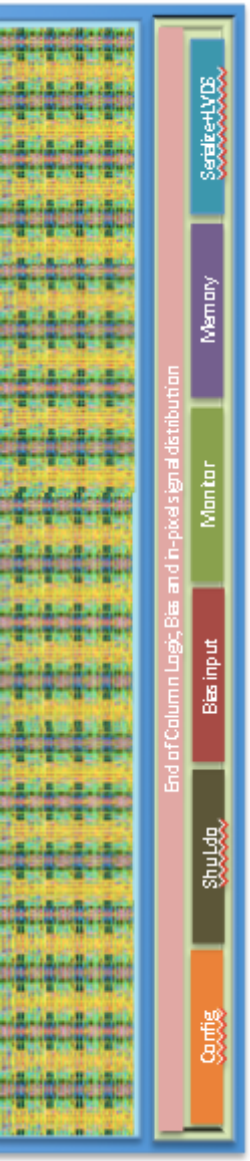


- Much **faster charge collection with fixes**
- **Less charge trapping ~4x more Q** after irradiation





ATLAS CMOS-1 Periphery



Key focus now is the realization of an ATLAS-ready ASIC: include essential RD53 functionality in monolithic sensor

Key topics : Hit data Memory and Trigger

- Analysing memory design in order to efficiently use bandwidth, distribute power and use little space
- Memory: efficient storage concept : local EoC hit memory plus global memory for trigger latency

Key topics : Serializer and output

- Data out after trigger is serialized with 1280 Mbps to go to aggregator with RD53 protocol
- Clock recovery from Clk/CMD 160MHz to receive from PP0

Key topics : Power and bias, configuration

- Submitted designs of blocks for serial power: use on CMOS sensor shunt regulators for serial powering
- Implement configuration with RD53 protocol

Beyond HL-LHC Phase 2 - Future Enhanced Performance

- Achieve **better spatial resolution**, **faster timing** and **higher rate capability** through higher integration density for future trackers

Now in 0.18 µm

Q/C > ~ 0.25 fC / 5 fF = 50 mV

- ALPIDE: 40 nW/pixel (analog)
- MALTA/Monopix: 1 µW /pixel (25ns)
- Analog power in matrix dominant

Pixel pitch ≈ sensitive layer thickness ≈ 30 µm

- Position resolution ~ 5 µm

Matrix hit rate capability:

- MALTA matrix > 100 Mhit/mm²/s (but cannot cope at periphery)

Deeper submicron

Q/C >>

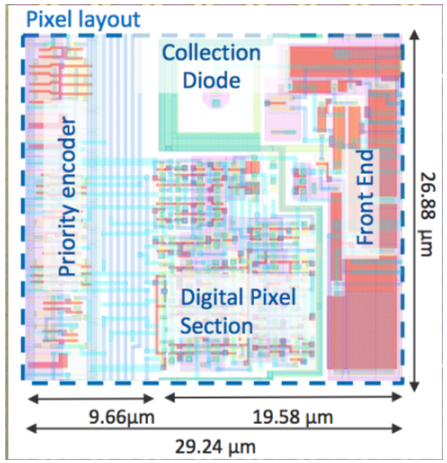
- Analog power will go close to zero

Pixel pitch ≈ sensitive layer thickness ≈ 5-10 µm

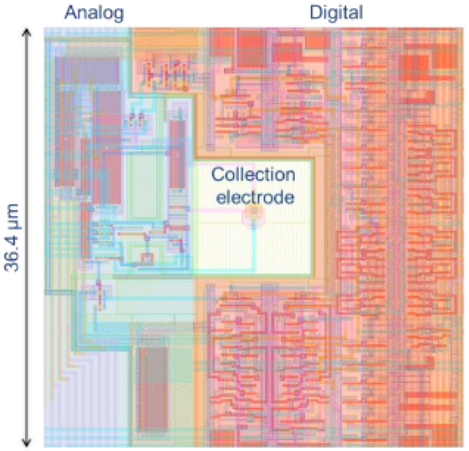
- Position resolution ~ 1-2 µm

Matrix hit rate capability:

- 10's of GHz/mm² (but need to cope at periphery)



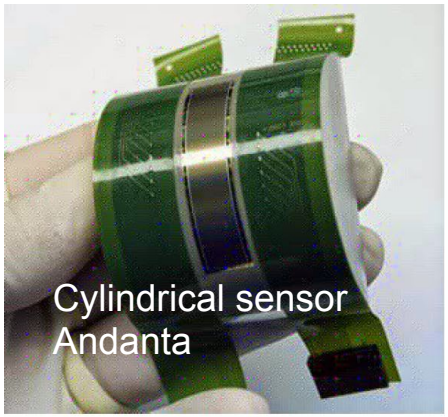
Alpide pixel



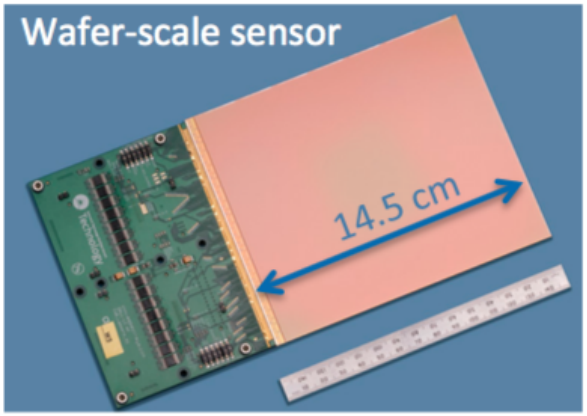
MALTA pixel

Large sensors & systems

- Developed **"stitched" designs for large sensors and special geometries**
  - Chain sensors for large area trackers and large acceptance
  - Exploit mechanical flexibility of thin sensors in cylindrical or spherical geometry (e.g. of interest for very low mass inner layer upgrade of ALICE ITS)



Cylindrically Curved CCD (Convex)



- CMOS sensor key advantage is large volume production on 200/300mm wafers
- Improve ratio between chip and total detector area through stitching

Explore new solutions for data aggregation and transmission for high data rates

E.g. demonstrator module with sensor to sensor interconnection and high-speed data readout via photonics chip

Summary

- The development of new **depleted monolithic CMOS sensors** in HR/ HV CMOS process progresses rapidly
  - Large CMOS trackers like ALICE ITS are under construction and future new trackers use monolithic CMOS sensors as their base-line design (HVCMOS sensor MuPix for Mu3e experiment at PSI, ALPIDE sensors for sPhenix at BNL)

- **Monolithic CMOS sensors** are being developed for **high-radiation environments at HL-LHC with complex readout architectures** for the future pixel system of **ATLAS**

  - CMOS sensors are considered as option for the ATLAS Pixel ITk outermost layer
  - Front-end designs with large and small collection electrodes have been realized in 3 different CMOS processes with very encouraging results
  - We have developed synchronous and asynchronous readout architectures for high hit rates (>>MHz/mm^2) and implemented them in large matrices

- Implementation of all ATLAS functionality into the ASIC is now the main activity together with **integrating these sensors to modules**

Summary

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