Review on depleted CMOS

VERTEX-2018 International Workshop on Vertex Detectors
Chennai, India
25/10/2018

Thanushan Kugathasan, CERN
Advantages of monolithic pixels for Vertex Detectors:

- Detector assembly and production cost.
  - Standard CMOS processing (larger wafer diameter, low cost per area)
  - No need for cost intensive fine pitch bump bonding
- Thin detectors (O(50 μm Si)) and high granularity (small pixel sizes)
- Better power-performance ratio for monolithic on the condition of better Q/C (cabling and cooling material reduction)
Detectors requirements

- Radiation tolerance
  - Ionizing radiation (TID) – circuit is more sensitive to TID
  - Non-ionizing radiation (NIEL - displacement damage) - affects the sensor
- Position resolution (~μm)
- Low power consumption is the key for low mass
  - Now tens of mW/cm² for silicon trackers and hundreds of mW/cm² for pixels
  - Even with enhanced detector functionality for upgrades, power consumption cannot increase too much because of the material penalty

<table>
<thead>
<tr>
<th></th>
<th>STAR RICH</th>
<th>ALICE-LHC</th>
<th>ILC</th>
<th>HL-LHC Outer layer</th>
<th>HL-LHC Inner layer</th>
<th>CLIC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Required Time Res. [ns]</td>
<td>200 000</td>
<td>20 000</td>
<td>350</td>
<td>25</td>
<td>25</td>
<td>~ 1</td>
</tr>
<tr>
<td>Particle Rate [kHz/mm²]</td>
<td>4</td>
<td>10</td>
<td>250</td>
<td>1000</td>
<td>10 000</td>
<td>&lt; 0.3</td>
</tr>
<tr>
<td>NIEL Fluence [n_{eq}/cm²]</td>
<td>&lt; 10^{12}</td>
<td>&lt; 10^{13}</td>
<td>10^{12}</td>
<td>10^{15}</td>
<td>10^{16}</td>
<td>&lt; 10^{12}</td>
</tr>
<tr>
<td>Total Ionizing Dose [Mrad]</td>
<td>0.2</td>
<td>0.7</td>
<td>0.4</td>
<td>50</td>
<td>1000</td>
<td>1</td>
</tr>
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<td>Particle Rate [kHz/mm(^2)]</td>
<td>4</td>
<td>10</td>
<td>250</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Non Ionizing Energy Loss Fluence [n(_{eq})/cm(^2)]</td>
<td>&lt; (10^{12})</td>
<td>&lt; (10^{13})</td>
<td>(10^{12})</td>
<td></td>
<td></td>
<td></td>
</tr>
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</table>

**MIMOSA28 (ULTIMATE)**
- IPHC Strasbourg
- First MAPS system in HEP
- 0.35 μm CMOS
  - Rolling shutter readout

**ALPIDE - First MAPS in HEP with sparse readout similar to hybrid sensors**
- 1.5 x 3.0 cm\(^2\) 0.5 Mpix (28 um pitch)
- In production

G. Aglieri et al, DOI 10.1016/j.nima.2016.05.016
ALICE ITS Upgrade

Installation of the new ITS during LHC Long Shutdown 2 (2019 - 2020)

Thin sensors (50 μm), high granularity (~30 x 30 μm²), large area (10 m²) and moderate radiation

Parameter | Inner Barrel
--- | ---
Chip size (mm x mm) | 15 x 30
Chip thickness (mm) | 50
Spatial resolution (mm) | 5
Detection efficiency | > 99%
Fake hit rate | << 10⁻⁶ evt⁻¹ pixel⁻¹
Integration time (ms) | < 10
Power density (mW/cm²) | ~35
TID radiation hardness (krad) (**) | 2700
NIEL radiation hardness (1 MeV nₑq/cm²) (**) | 1.7 x 10¹³
Readout rate, Pb-Pb interactions (kHz) | 100
Hit Density, Pb-Pb interactions (cm⁻²) | 18.6

(*) In color: ALPIDE performance figure where better than requirements
(**) 10x radiation load integrated over approved program (~ 6 years of operation)

VERTEX-2018 Serhiy Senyukov “Silicon tracker detector for the ALICE upgrade”

MONOLITHIC ACTIVE PIXEL SENSORS

Review on depleted CMOS - T.Kugathasan - VERTEX2018
ALPIDE Sensor Technology

- TowerJazz 180nm CMOS imaging sensor process
- Electronics outside the collection electrode: small electrode, large circuit area, no signal coupling

- Reverse bias to increase depletion volume (-6 V, the sensor is not fully depleted)
Minimum Ionizing Particle (MIP) creates ~ 60 e/h pairs per micron of silicon traversed (in case of thin silicon)

Example for 25 um thick layer: 1500 e/h $\Rightarrow$ 0.24 fC
Cluster size and resolution

Charge sharing depends on
- Hit position
- Sensor design and bias

Cons:
- Less signal in a pixel, more data
Pro:
- Better spatial resolution
**ALPIDE circuit**

- **Analog front-end continuously active** (40 nW/pixel)
  - analogue delay line (~2 µs peaking time)
  - Good threshold uniformity: \( Q_{th} = (64.6 \pm 11.4) \) e-
  - Low noise: ENC = (5.6 e ± 0.8) e-

- **Global threshold** for discrimination
  - => binary pulse OUT_D

- **Digital in-pixel circuitry** with three hit storage registers (multi event buffer)

- **Global shutter** (STROBE) latches the discriminated hits in next available register triggered or continuous readout

- **Zero suppressed readout**, no hits no power

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**C_d ~ 2.5 fF**

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D. Kim et al. TWEPP 2015, DOI 10.1088/1748-0221/11/02/C02042

G. Aglieri et al. NIM A 845 (2017) 583-587

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**1024 pixel columns**

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Review on depleted CMOS - T.Kugathasan - VERTEX2018
ALPIDE pixel matrix cross section and layout
Towards more demanding applications

Specifications for the ATLAS Inner Tracker Upgrade Phase 2 (HL-LHC)

<table>
<thead>
<tr>
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<th>ATLAS-HL-LHC</th>
<th>CLIC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Required Time Res. [ns]</td>
<td>20 000</td>
<td>25 Inner</td>
<td>~ 1</td>
</tr>
<tr>
<td>Particle Rate [kHz/mm²]</td>
<td>10</td>
<td>1000</td>
<td>10 000</td>
</tr>
<tr>
<td>Fluence [n₀e₂/cm²]</td>
<td>&lt; 10^{13}</td>
<td>10^{15}</td>
<td>10^{16}</td>
</tr>
<tr>
<td>Ion. Dose [Mrad]</td>
<td>0.7</td>
<td>50 Inner</td>
<td>1000</td>
</tr>
</tbody>
</table>

- Time resolution: fast collection by drift (<< 25 ns)
- High particle rate: short dead time (< 1 us)
- Tolerance to non-ionizing radiation (displacement damage): fast collection by drift to decrease signal charge trapping probability
- High Q/C for power optimization:
  - High Q : less charge sharing (small cluster)
  - Low C : smaller junction capacitance

VERTEX-2018 talk:
Heinz Pernegger
“Depleted CMOS for H-LHC”

VERTEX-2018 talk:
Magdalena Munker
“Status of silicon detector R&D at CLIC”

⇒ Full depletion
Approach to increase depletion: Circuit inside the collection electrode

- CMOS technology for high voltage switching electronics
- High reverse substrate voltage (~ 100 V)
- High resistivity p-substrate (> 2 kΩ cm)
- Charge is collected by drift, good for radiation tolerance
- Limited circuit area, large capacitance (C ~ 400 fF)
ATLASpixSimple (H18-AMS  Active area 3.25 mm x 2 cm)
Pixel matrix: 25 x 400 pixels of 130µm x 40µm size
Analog only in-pixel circuit:
No cross-talk induced by digital activity
Reduction of the circuit size for sensor capacitance reduction
Digital circuit at the periphery:
Clock signals (and time stamp signals) are limited to smaller area
smaller power consumption
One-to-one connection from pixel to R/O logic, complex routing
ATLASpix timing

Delay over sensor

delaymap_for_plane_1

Timewalk

ToT time Trigger Difference versus ToT

thr = 300 mV

Time stamp at the periphery, compensation for the position dependent latency.

Possible Time walk correction with ToT
LF-Monopix Column Drain architecture

- CSA + Discr. with 4-bit DAC
  - Aiming for < 25 ns time walk, Static current ~ 20 μA/pixel
- RAM cells to store 8-bit ToA + ToT
- Full-custom dig. Circuit
  - Minimized area => reduce $C_d$
  - Special low noise design to minimize substrate noise
  - Differential signal transmission

$Q_{th}$ 2500 e⁻, ENC 200 e⁻
No significant loss after irradiation (NIEL $2 \cdot 10^{15} n_{eq}/cm^2$, TID 150 Mrad)
Matrix digital signal transmission

Column bus R/O Differential signal transmission to remove digital switching

Standard SF readout
- LF-Monopix, TJ-Monopix
- 40μA/bit (differential)
- TJ-Monopix example:
  - 21 bits / DC
  - 125 DC / cm
  - 190 mW /cm²

Gated SF readout
- TJ-Monopix
- No current drawn during standby
- In the READ phase the bus is connected to the SF
- Static power eliminated

K. Moustakas – Uni Bonn
Large vs Small collection electrode

Large collection electrode (HV-CMOS)
- Large capacitance
- Higher power
- Practically uniform field
- Very high radiation tolerance

Small collection electrode (TJ)
- Small capacitance
- Lower power
- Less prone to coupling
- Longer signal travel path, process modification to increase radiation tolerance
Small Electrode - Modified process

Modified: full depletion, better radiation tolerance

55Fe measurements before irradiation (J. Van Hoorne): less charge sharing and more uniform time response

Note: here the circuit contributes significantly to the signal rise time!

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Small collection electrode – MALTA

- Analog power ≈ 1 μW per pixel (75 mW/cm²)
- Time-walk based charge information
- Novel asynchronous readout, no clock distribution over pixel matrix → reduced power
- Sensor radiation tolerance to be improved

512 x 512 pixels, 8 flavors

VERTEX-2018 talk:
Abhishek Sharma
“The Malta CMOS pixel detector prototype for the ATLAS Pixel ITK”
Digital architecture power and bandwidth

- Power per bit transmitted per hit as a function of hit rate
- Hit activity
  - If 1 bit (or rather one line toggle) is sent to periphery for every pixel hit *before* trigger
  - Average power = hit rate x column height/2 x 6.5 pJ/cm² = R x H x 6.5 pJ/2

<table>
<thead>
<tr>
<th>Layer</th>
<th>hit/BC/mm²</th>
<th>Mhit/mm²/s</th>
<th>Power/bit/cm² (H=2 cm)</th>
<th>Power (4.5 bit toggling)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0.68</td>
<td>27.2</td>
<td>17.7</td>
<td>79.6</td>
</tr>
<tr>
<td>1</td>
<td>0.21</td>
<td>8.4</td>
<td>5.5</td>
<td>24.6</td>
</tr>
<tr>
<td>2</td>
<td>0.043</td>
<td>1.72</td>
<td>1.1</td>
<td>5.0</td>
</tr>
<tr>
<td>3</td>
<td>0.029</td>
<td>1.16</td>
<td>0.8</td>
<td>3.4</td>
</tr>
<tr>
<td>4</td>
<td>0.021</td>
<td>0.84</td>
<td>0.5</td>
<td>2.5</td>
</tr>
</tbody>
</table>

T. Kugathasan et al TWEPP 2017

- Clock distribution over the matrix (needed if data kept in pixel):
  - 200 lines per cm (1 per double column) for 25 μm pixel pitch:
  - 200 x 6.5 pJ x 40 MHz = 50 mW/cm²

MALTA (matrix only)
• Hit information is transmitted using short pulses over a parallel bus
• This massive parallelism makes huge on-chip bandwidth available (Gb/s/μm !), but to conserve low power one needs to keep the activity down and cannot use this huge bandwidth continuously
Small collection electrode radiation tolerance

Unirradiated
$Q_{th} = 250 \text{ e}^-$

Irradiated $5 \times 10^{14} \text{n}_{eq}/\text{cm}^2$
$Q_{th} = 350 \text{ e}^-$

2x2 pixels
36.4 $\mu$m$^2$

Issue: Detection efficiency loss in the pixel corners

Solution
Increase lateral electric field in critical sensor regions (corners)
TCAD transient simulations

VERTEX-2018 talk: Magdalena Munker
“Status of silicon detector R&D at CLIC”

Simulation of MIP incident at lateral position of field minimum (worst case)

Un-irradiated sensor
Charge collection time improvement Eg. Qth 100 e- from ~ 7 ns to < 2 ns

Irradiated sensor [10^{15} n_{eq}/cm^2]
Charge collection time and signal after irradiation significantly improved after irradiation
## Monolithic pixel sensors - comparison

<table>
<thead>
<tr>
<th></th>
<th>Readout</th>
<th>Time Resolution</th>
<th>Capacitance</th>
<th>NIEL Radiation Tolerance [1 MeV n_{eq}/cm^2]</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>MAPS - 3T</strong></td>
<td>Analog signal to the periphery</td>
<td>&gt; 10 us</td>
<td>&lt; 10 fF</td>
<td>$10^{12}$</td>
</tr>
<tr>
<td><strong>MAPS – ALPIDE</strong></td>
<td>In pixel intelligence</td>
<td>1 us</td>
<td>&lt; 5 fF</td>
<td>$10^{13}$</td>
</tr>
<tr>
<td><strong>D-MAPS</strong></td>
<td>In pixel intelligence</td>
<td>&lt; 25 ns</td>
<td>~ 100 fF</td>
<td>$10^{15}$</td>
</tr>
<tr>
<td>(HV-CMOS, large electrode)</td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td><strong>D-MAPS</strong></td>
<td>In pixel intelligence</td>
<td>&lt; 25 ns</td>
<td>&lt; 5 fF</td>
<td>$10^{15}$ ?</td>
</tr>
<tr>
<td>(Small electrode)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Hybrid pixels</strong></td>
<td>In pixel intelligence</td>
<td>&lt; 25 ns</td>
<td>&gt; 50 fF</td>
<td>$10^{16}$</td>
</tr>
</tbody>
</table>
Monolithic CMOS sensors in HEP

ULTIMATE in STAR
IPHC Strasbourg
First HEP MAPS system

ALPIDE in ALICE
First MAPS with sparse readout similar to hybrid sensors
Chip-to-chip communication for data aggregation

ATLAS CMOS
Depleted radiation hard MAPS with:
Sparse readout
Chip-to-chip communication
Serial power
...

FCC, CLIC, ...
Large stitched fast radiation hard MAPS
with:
Sparse readout
Chip-to-chip communication
Serial power
...

Important steps in every iteration
Conclusion and outlook

- Increasing interest of **Monolithic in High Energy Physics**
- **ALPIDE** pixel chip in TowerJazz adopted for the ALICE ITS upgrade
  - Low sensor capacitance (< 5 fF, circuit + sensor) for low power operation
  - The sensor is not fully depleted (moderate radiation tolerance and speed)
- Present development CMOS pixel sensor targets:
  - 25 ns bunch crossing time and tolerance to NIEL fluence > $10^{15}$ (1 MeV n$_{eq}$/cm$^2$)
    => Full depletion
  - **Large collection electrode (HVCMOS):** Electronics in the collection electrode.
    - Good radiation tolerance
    - Power penalty due to large sensor capacitance (400 fF) and robust design to avoid cross talk.
  - **Small collection electrode:** TowerJazz process modification for full depletion combined with low C (< 5 fF, circuit + sensor)
    - Low power front-end (< 25 ns, < 1 µW)
    - MALTA, asynchronous readout, allows for large on chip bandwidth
    - New sensor design to improve both timing and radiation tolerance.
- Future challenges:
  - faster timing (~ ns), larger hit rate capability (~ 10 MHz/mm$^2$) and higher radiation tolerance (> $10^{15}$ n$_{eq}$/cm$^2$)
  - System level aspects: serial powering, sensor bias, stitching for large sensor area
Acknowledgements

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• ATLAS ITk CMOS collaboration
• STREAM