Interconnects and Assembly Technologies for Hybrid Pixel Detectors

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Fraunhofer IZM, Berlin, Dept. Wafer Level System Integration
Agenda

- Formation of Interconnects – A Wafer Level Packaging Technology
- Interconnection Technology
  - Solder Bumping
  - Transient Liquid Phase Bonding
  - Metal-Metal Bonding
- Application: 3D Integration Technology for Hybrid Detector Modules
Assembly of Hybrid Pixel Detectors

- Step 1: UBM deposition on sensor wafer
- Step 2: solder bump deposition on readout chip wafer
- Step 3: Flip Chip Assembly of readout chip to sensor chip

Advantages:
- Separate development and optimization of sensor and readout chip
- Variable use of different semiconductor sensor materials
Wafer Level Packaging: Micro Bumping and Hybridization Process

Seed Layer ➔ Resist Process ➔ Lithography ➔ Plating ➔ Strip / Etching ➔ Dicing ➔ Assembly

Sputter ➔ Spin Coater ➔ Mask Aligner ➔ Wafer Plating ➔ Wet Etching ➔ Dicing ➔ Flip Chip

- Resist Stripping and wet Etching of the Plating Base
- Sputter Etching and Sputtering of the Plating Base / UBM
- Spin Coating and Printing of Photoresist
- Electroplating of Cu and PbSn
- Reflow

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The 27th International Workshop On Vertex Detectors
Chennai, India, October 21 - 26, 2018
Hybrid Pixel Detectors - Requirements in HEP and Radiation Imaging

**Assembly Pixel Pitch**
- Low cost: >500µm
- Standard: >50µm
- Advanced: <50µm
- Challenging: <20µm

**Interconnect Material**
- Low Temp: Indium, Indium-Tin
- Standard: SnAg solder, Cu-pillar w solder cap
- High Temp: TLPB/SLID: AuSn, CuSn,
- Non-Melting: Au-Au, Cu-Cu, (Ni-Ni)

**Bonding Technology**
- Low Cost: Solder paste, conductive glue
- Standard: solder bump reflow
- Advanced: TLPB/SLID: AuSn, CuSn,
- Challenging: Metal-Metal, Metal-Oxide Hybrid Bonding

**Assembly**
- Standard: Chip to Chip Assembly
- Advanced: Chip to Wafer, Wafer to Wafer Assembly
Bonding Techniques

**Solder Bump Bonding**
- ECD UBMs and solder bumps (SnAg, In, InSn, AuSn, Cu-pillar/Sn cap)
- High temp and low temp solder
- Bonding without or low pressure

**Transient Liquid Phase Bonding (TLPB)**
- ECD Cu and Cu-Sn pads
- High melting Cu$_3$Sn IMC
- Bonding parameters: 220...280°C, 10...50MPa; $T=\text{min}$
- High planarity necessary

**Metal-Metal Direct Bonding**
- ECD Cu pads (Au, Ni)
- Planarized surfaces, pre-conditioning
- Bonding parameters: 300°C...400°C,
  ~10...100MPa, $t=\text{min...h}$, vacuum

**Metal – Oxide Hybrid Bonding**
- ECD Cu pads (or Ni)
- Surface planarization (CMP)
- Surface activation (plasma)
- Room temperature bond
- Annealing 175°C...400°C
Assembly Roadmap

<table>
<thead>
<tr>
<th>Bond Interface</th>
<th>Bond Parameter</th>
</tr>
</thead>
<tbody>
<tr>
<td>solder</td>
<td>no pressure</td>
</tr>
<tr>
<td>solder</td>
<td>low pressure</td>
</tr>
<tr>
<td>IMC</td>
<td>low pressure</td>
</tr>
<tr>
<td>Metal</td>
<td>high pressure</td>
</tr>
</tbody>
</table>

- Reflow Soldering, SnAg, Cu-Pillar/Sn, In
- TC Bonding, In, Sn
- TLPB („SLID“), Cu/Sn, Au/Sn
- Metal Diffusion Bonding (solid/solid), Cu/Cu, Au/Au

Pitch [µm]: 3 5 7 10 20 30 50 70 100
Solder Bumping on RD53A 300mm Wafer

- 300mm wafer, TSMC 65nm technology
- ~ 90 RD53A readout chips per wafer
- Bumping pitch 50x50 µm²
- Bump size and height ~25..30 µm
- SnAg solder bumping

- Assembly of single chip modules using
  - planar sensors 100µm, 150µm thickness: Hamamatsu, MPG HHL, FBK
  - 3D sensors: FBK, SINTEF

RD53A wafer

Details of RD53A ROC after bumping

RD53 collaboration
https://rd53.web.cern.ch/RD53/
Low Temperature Bonding of “high-Z” Sensors for X-ray Imaging

Materials:
- Cadmium Telluride
- Gallium Arsenide
- Germanium

Requirements:
- Bump Material adapted to GaAs and CdTe pad metallization
- Maximum process and bonding temperature below 120°C ... 150°C (CdTe, Ge)
- Low bonding pressure → Indium based solder bumps

Indium and Indium/Tin for Low Temperature Flip-Chip Assembly

- $T_M(\text{Indium}) = 156 \, ^\circ \text{C}; \ T_M(\text{In52Sn48}) = 117 \, ^\circ \text{C}$ for thermally sensitive bonding processes
- Electrochemical deposition of Indium or Indium/Tin
- Standard Pitch ~50µm, Bump size 25µm
- Realized minimum pitch so far 10µm/6µm bump size
- Flip chip bonding process In to In or In to Au pad surface, bonding temperature at 100°C evaluated

Indium Bumping 10 µm Pitch for IR image sensors
Process Evaluation: Indium Bump (Thermo)-Compression Bonding

- Bonding temperature below 100°C using a low temperature compression bonding process
- Daisy chain and single bump electrical resistance measurement design on MEDIPIX3 size test chip

**Compression of Indium bumps on**

**Passivation defined NiAu**

- Bonding temperature below 100°C using a low temperature compression bonding process
- Daisy chain and single bump electrical resistance measurement design on MEDIPIX3 size test chip

**Pad defined NiAu metal**

- Bonding temperature below 100°C using a low temperature compression bonding process
- Daisy chain and single bump electrical resistance measurement design on MEDIPIX3 size test chip
Detectors with “high-Z” Sensors for Hard X-rays

GaAs 3x2 HEXA_Mo35kV

CdTe IZM single 3 (Xn2017_05)

Ge 3x2 HEXA Detector

- Single Photon Counting ROC developed at CERN
- Bump size: 25…30µm
- Bump Pitch: 55µm (x, y)
- Chip Size: ~14 x 16 cm²
- Bump matrix: 256x257 (65792 per chip)
- Module Assembly using In-Bumps

All modules with MEDIPIX / TIMEPIX readout chip:

(Sarajlic, 2017 JINST 12 C01068)
Assembly Roadmap

- **bond interface**
- **solder**
- **IMC**
- **Met**

<table>
<thead>
<tr>
<th>pitch [µm]</th>
<th>bond parameter</th>
</tr>
</thead>
<tbody>
<tr>
<td>3 - 5</td>
<td>no pressure</td>
</tr>
<tr>
<td>7 - 10</td>
<td>low pressure</td>
</tr>
<tr>
<td>20 - 100</td>
<td>high pressure</td>
</tr>
</tbody>
</table>

- Reflow Soldering, Cu-Pillar/Sn
- TC Bonding, Cu-Pillar/Sn
- TLPB („SLID“), Cu/Sn, Au/Sn
- Metal Diffusion Bonding (solid/solid), Cu/Cu, Au/Au

- Low/medium pressure
- high Temperature
Transient Liquid Phase Bonding (TLPB) – Solid Liquid Interface Diffusion (SLID)

- ECD Cu and Cu-Sn pads
- High melting Cu₃Sn IMC (676°C)
- Bonding parameters: 220…280°C, 10…50MPa, T= min
- High planarity necessary
- Wafer to wafer assembly
- Chip to Chip in inert atmosphere

Hermetic Sealing

Silicon interposer: 2 half-shells forming a microchannel cooler

4-port fluidic interposer

chip sealing fluid port micro-channel

TSV micro sealing micro-channel

X-ray pictures
Transient Liquid Phase Bonding (TLPB)

Results CuSn

Results AuSn

remaining Sn left at the edge

Au

Intermetallic compound Au₅Sn
Assembly Roadmap

bond interface

solder

solder

IMC

Met

Reflow Soldering, Cu-Pillar/Sn

TC Bonding, Cu-Pillar/Sn

TLPB („SLID“), Cu/Sn, Au/Sn

Metal Diffusion Bonding (solid/solid), Cu/Cu, Au/Au

bond parameter

no pressure

low pressure

low pressure

high pressure
high Temperature

pitch [µm]

3  5  7  10  20  30  50  70  100
Metal-Metal Diffusion Bonding

- ECD Cu pads (Au, Ni)
- Planarized surfaces, pre-conditioning
- Bonding parameters:
  - 300°C...400°C,
  - 10...100 MPa
  - \( t= \) min...h
  - Vacuum, inert atmosphere
- Available for wafer to wafer bonding
- R&D for Chip to Chip assembly
Metal-Metal Diffusion Bonding

Cu-Cu

Au-Au

Bonding temperature 300°C
Bonding pressure 100 MPa

T = 250°C, P < 100MPa
fully bonded interface

T = 100°C, P < 100MPa
partly bonded interface
Assembly Roadmap

bond interface

solder

Reflow Soldering, Cu-Pillar/Sn

no pressure

tc bonding, Cu-Pillar/Sn

low pressure

IMC

TLPB („SLID“), Cu/Sn, Au/Sn

low pressure

Met

Metal Diffusion Bonding (solid/solid), Cu/Cu, Au/Au

high pressure

high Temperature

Met

Nanoporous Gold (NPG) / Gold Nanosponge

lower pressure

lower temperature

<table>
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<th>pitch [µm]</th>
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<td>3 5 7 10 20 30 50 70 100</td>
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</table>
R&D: Nano-Porous Gold (NPG) Bumps for Chip Interconnections

- Development electro-plating baths
  Ag/Au alloy deposition

- Prozess flow similar to conventional
  Au Bumping

- Skeleton formation due to dealloying
  by wet etching of Ag

- Average pore sizes adjustable from
  20 nm up to 500 nm

- TC-Bonding with reduced bonding parameters possible,
  typ. 10 Mpa / 200°C / 300s

- Sponge-like Au is fully compressible and able to compensate
  topography and inhomogeneities on chip and substrate
R&D: Nano-Porous Gold Bumps for Chip Interconnections

The advantage of compressible bonds:

- low T, low force
- low Youngs Modulus: low stress
- compressible: accommodate implantarities
- suitable for topography and thickness variation

→ Bonding process down to 15 MPa @ 150°C
**Metal – Oxide Hybrid Bonding**

**Process:**
- ECD Cu pads (or Ni)
- Surface planarization (CMP)
- Surface activation (plasma, chemicals)
- Room temperature bond
- Annealing 175°C…400°C
- Available for Wafer to Wafer bonding

**Motivation for DBI:**
- W2W, (D2W)
- Highest interconnect density
- I/O Pitch up to 1 µm
- High alignment accuracy
- No bumps
- No intermetallics
- No underfilling
- High reliability

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**Fraunhofer IZM-ASSID**

300 mm W2W Bonding:
<5µm alignment accuracy

Fraunhofer test chip with 4 µm pad /18µm pitch, Metal density: 4.5%


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<table>
<thead>
<tr>
<th></th>
<th>FhG IZM ASSID (Results)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Roughness beside TSV (Oxide) Ra</td>
<td>0,146 nm</td>
</tr>
<tr>
<td>Roughness on TSV (Cu) Ra</td>
<td>0,163 nm</td>
</tr>
<tr>
<td>Planarization</td>
<td>5nm @ 100µm</td>
</tr>
</tbody>
</table>
Application: Advanced Packaging - 3D Integration

- Low material budget
- Thin chip modules
- Multichip modules
- TSV technology

- Four side stitchable modules
- Heterogenous sensor integration
- Multichip modules
- TSV technology

Courtesy of DESY
**TSV Process for Ultra Fast Xray Pixel Matrix Chip**

- UFXC32k Readout Chip developed by AGH Krakow, Poland

**Process at IZM:**
- TSV-frontside process
- Completely-filled Cu-TSV
- Frontside and backside RDL
- Frontside Solder Bumps/Pillars
- Backside solderable Pad Metallization
- Hybridization to sensor
- 2nd level assembly to LTCC

Cross section of ROC-Sensor Module, with Cu filled TSV

ROC backside after TSV and backside RDL process
TSV Process for Ultra Fast Xray Pixel Matrix Chip

The tests of a detector module:

- measurement of a total power consumption (1.7 W @ 200 MHz)
- functionality verification of digital blocks in UFXC32k ICs (registers and counters readout),
- measurements of the effective offset spread from pixel to pixel before and after trimming,
- test with the charge injection circuit to verify the in-pixel analog front-end operation,
- test with X-ray radiation of different energy,
- measurement of example radiograms.

Summary

- Hybrid Detector Modules in HEP and Radiation Imaging
  - Pixel Pitch 50µm → 20…10µm
  - Bonding Temperature < 100°C and high-melting/ non-melting Interconnections
  - Reduction of bonding pressure
  - C2C, C2W, W2W Bonding

- Interconnection Technology
  - Reflow Soldering: Solder Bumps, Pillar with solder Cap
  - Solder Compression Bonding: Indium Bumps
  - Transient Liquid Phase Bonding / Solid Liquid Interphase Diffusion: CuSn, AuSn
  - Metal-Metal Diffusion Bonding: Au-Au, Cu-Cu, Nanoporous Gold (NPG)
  - Metal-Oxide Hybrid Bonding: Cu, Ni

- Application: 3D Integration using TSVs in thinned chips/wafers
Thank You