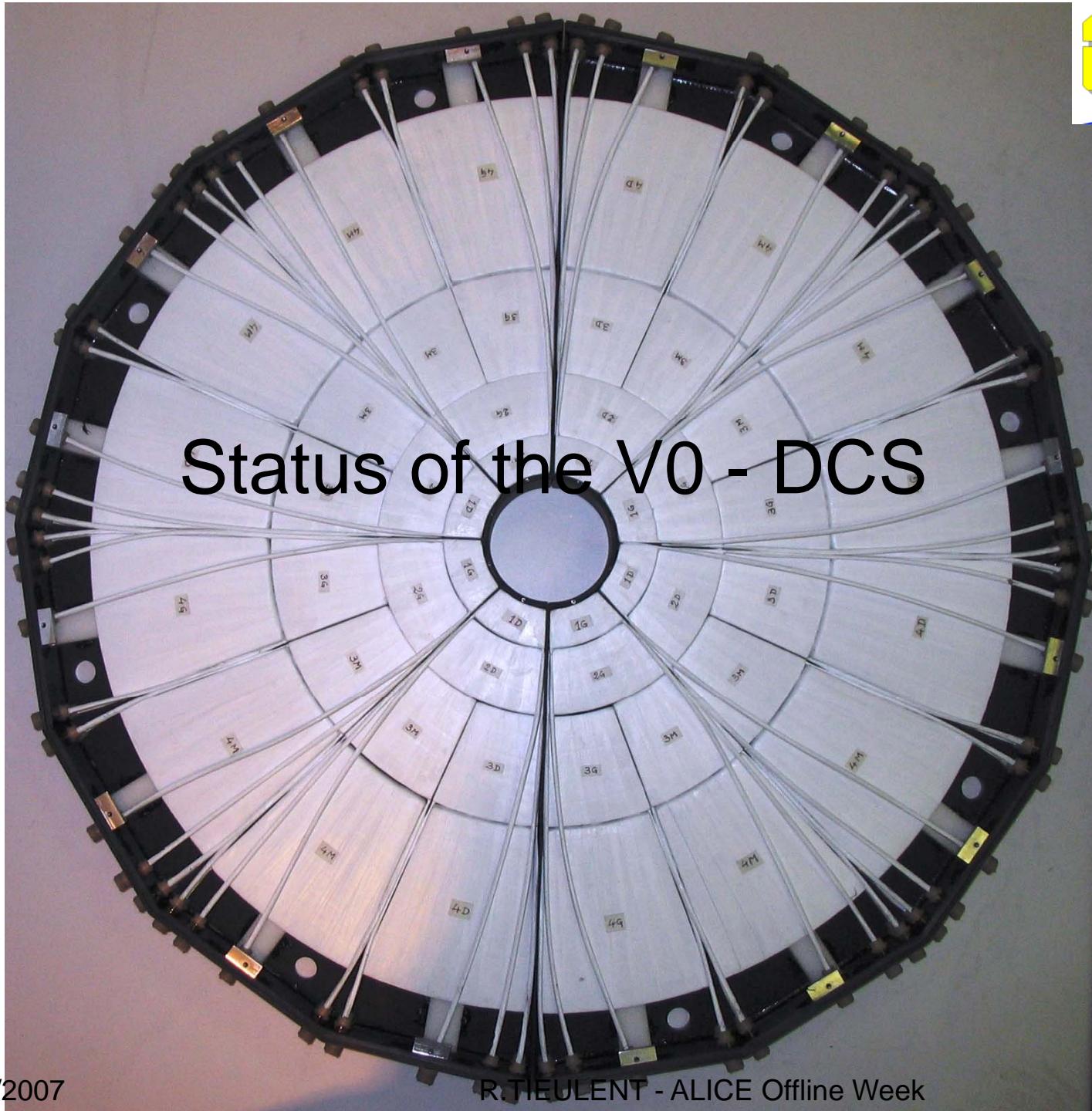




# Status of the V0 - DCS

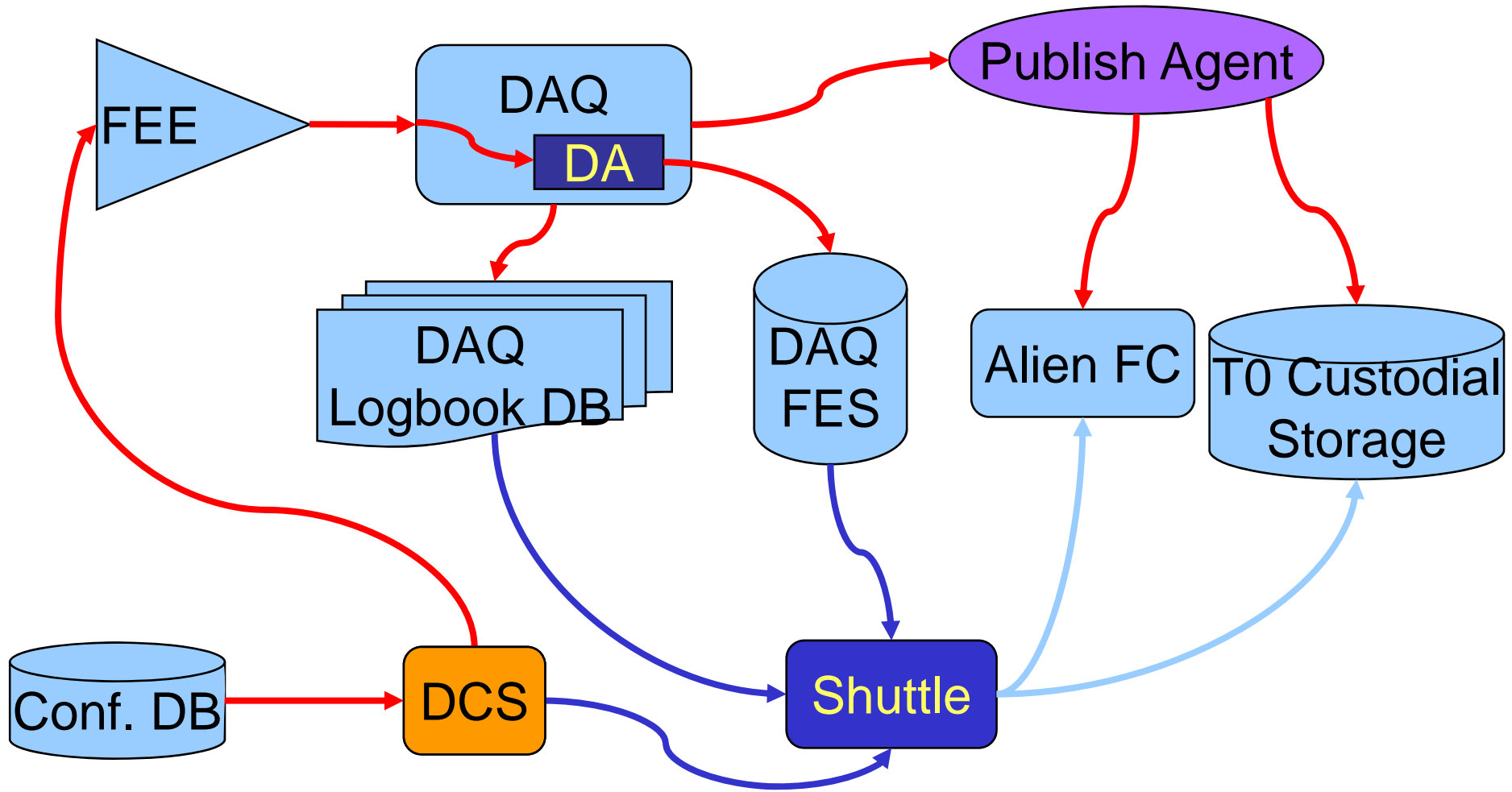


09/10/2007

R. TIEULENT - ALICE Offline Week



# On-Offline connection diagram (Use case6)





Counting room

Cavern

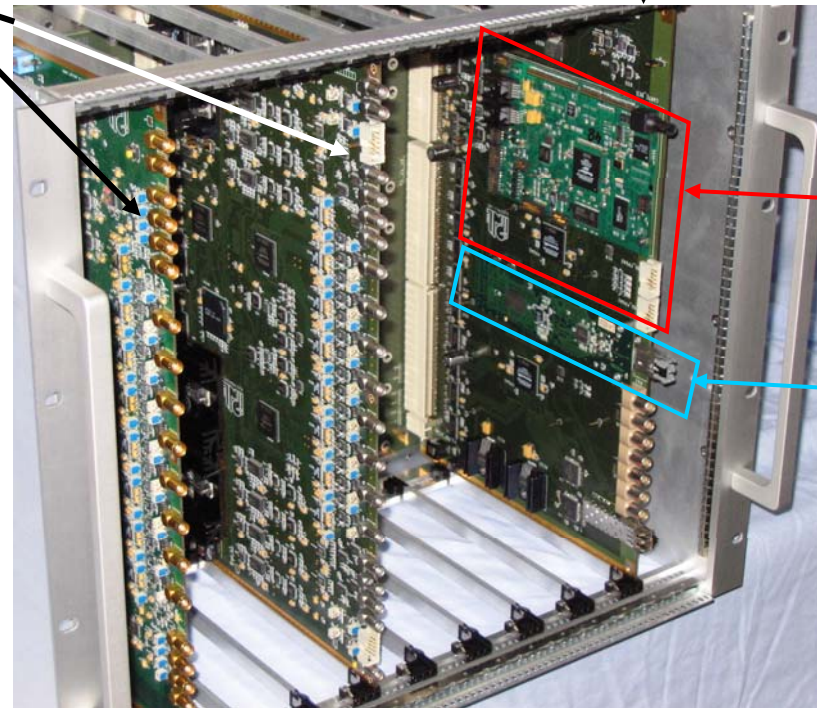
Inside magnet



# Front End Electronics



CIU, one board per ring  
- charge integration  
- time digitalization  
- trigger pre-processing



CCIU, pilot board  
- collects the CIU data  
- provides the final triggers  
- interface with the DAQ  
- interface with DCS

DCS board

SIU Mezzanine



# Installation and Commissioning Status



## What has been done:

- **V0C Detector installed and tested** (using custom FEE) 2-6 April 2007
- **LV and HV accessible from DCS at point 2**
- **Test in lab with DCS, DAQ, TRG** June 2007
  - test made with only 1 CIU board (corresponding to 1 ring of V0)

## Remaining Key Dates:

- **End of test and calibration of electronics boards in lab:** End of October
- **Test in lab with DCS, DAQ, TRG with final FEE:** End of November
- **Installation of DCS at point 2:** Beginning-December
- **Installation and configuration of FEE at P2:** Mid-December
- **Installation of V0A:** January 2008



# Development of the control



Vision\_1: TOP

11:12:36 28-09-07 data 300

root

FSM V00\_DET OFF

V00\_DET <<

- VOC
  - VOC\_QUAD0
  - VOC\_QUAD1
  - VOC\_QUAD2
  - VOC\_QUAD3
- V00\_INFR
  - VME
- V00\_FEE
  - CIU0\_memory\_zone
  - CIU1\_memory\_zone
  - CIU2\_memory\_zone
  - CIU3\_memory\_zone
  - CIU4\_memory\_zone
  - CIU5\_memory\_zone
  - CIU6\_memory\_zone
  - CIU7\_memory\_zone
  - CTP\_CCIU\_memory\_zone

VO M

Sector 0

Sector 1

Sector 2

Sector 3

Sector 4

Sector 5

Sector 6

Sector 7

Detector Monitoring Zone

High Voltage	Sector 0	Sector 1	Sector 2	Sector 3
High Voltage	Sector 4	Sector 5	Sector 6	Sector 7

V0 Expert Voltage Control

(NoName)

### VOA High Voltages Settings

Sec	Ring	V On	V Int	I On	I Int	IRU Full	IRU L...	IRU Hi...	IRD	V/s RUF	V/s RUL	V/s RUH	V/s RD	Trip -s	Delay
Sector0	Ring0	2000	1500	3.000	3.000	10.000	10.000	10.000	10.000	500	750	200	500	3	1
Sector0	Ring1	2400	1500	3.000	10.000	10.000	3.000	3.000	10.000	300	200	250	500	3	1
Sector0	Ring2	2500	1500	10.000	10.000	10.000	10.000	10.000	10.000	250	300	250	300	3	1
Sector0	Ring3	2500	1500	10.000	10.000	10.000	10.000	10.000	10.000	250	300	250	300	3	1
Sector1	Ring0	2500	1500	10.000	10.000	10.000	10.000	10.000	10.000	250	300	250	300	3	1
Sector1	Ring1	2500	1500	10.000	10.000	10.000	10.000	10.000	10.000	250	300	250	300	3	1
Sector1	Ring2	2500	1500	10.000	10.000	10.000	10.000	10.000	10.000	250	300	250	300	3	1
Sector1	Ring3	2500	1500	10.000	10.000	10.000	10.000	10.000	10.000	250	300	250	300	3	1
Sector2	Ring0	2500	1500	10.000	10.000	10.000	10.000	10.000	10.000	250	300	250	300	3	1
Sector2	Ring1	2500	1500	10.000	10.000	10.000	10.000	10.000	10.000	250	300	250	300	3	1
Sector2	Ring2	2500	1500	10.000	10.000	10.000	10.000	10.000	10.000	250	300	250	300	3	1
Sector2	Ring3	2500	1500	10.000	10.000	10.000	10.000	10.000	10.000	250	300	250	300	3	1
Sector3	Ring0	2500	1500	10.000	10.000	10.000	10.000	10.000	10.000	250	300	250	300	3	1
Sector3	Ring1	2500	1500	10.000	10.000	10.000	10.000	10.000	10.000	250	300	250	300	3	1
Sector3	Ring2	2500	1500	10.000	10.000	10.000	10.000	10.000	10.000	250	300	250	300	3	1
Sector3	Ring3	2500	1500	10.000	10.000	10.000	10.000	10.000	10.000	250	300	250	300	3	1
Sector4	Ring0	2500	1500	10.000	10.000	10.000	10.000	10.000	10.000	250	300	250	300	3	1
Sector4	Ring1	2500	1500	10.000	10.000	10.000	10.000	10.000	10.000	250	300	250	300	3	1
Sector4	Ring2	2500	1500	10.000	10.000	10.000	10.000	10.000	10.000	250	300	250	300	3	1
Sector4	Ring3	2500	1500	10.000	10.000	10.000	10.000	10.000	10.000	250	300	250	300	3	1
Sector5	Ring0	2500	1500	10.000	10.000	10.000	10.000	10.000	10.000	250	300	250	300	3	1
Sector5	Ring1	2500	1500	10.000	10.000	10.000	10.000	10.000	10.000	250	300	250	300	3	1
Sector5	Ring2	2500	1500	10.000	10.000	10.000	10.000	10.000	10.000	250	300	250	300	3	1
Sector5	Ring3	2500	1500	10.000	10.000	10.000	10.000	10.000	10.000	250	300	250	300	3	1
Sector6	Ring0	2500	1500	10.000	10.000	10.000	10.000	10.000	10.000	250	300	250	300	3	1
Sector6	Ring1	2500	1500	10.000	10.000	10.000	10.000	10.000	10.000	250	300	250	300	3	1
Sector6	Ring2	2500	1500	10.000	10.000	10.000	10.000	10.000	10.000	250	300	250	300	3	1
Sector6	Ring3	2500	1500	10.000	10.000	10.000	10.000	10.000	10.000	250	300	250	300	3	1
Sector7	Ring0	2500	1500	10.000	10.000	10.000	10.000	10.000	10.000	250	300	250	300	3	1
Sector7	Ring1	2500	1500	10.000	10.000	10.000	10.000	10.000	10.000	250	300	250	300	3	1
Sector7	Ring2	2500	1500	10.000	10.000	10.000	10.000	10.000	10.000	250	300	250	300	3	1
Sector7	Ring3	2500	1500	10.000	10.000	10.000	10.000	10.000	10.000	250	300	250	300	3	1

Ramping Speed from OFF to ON

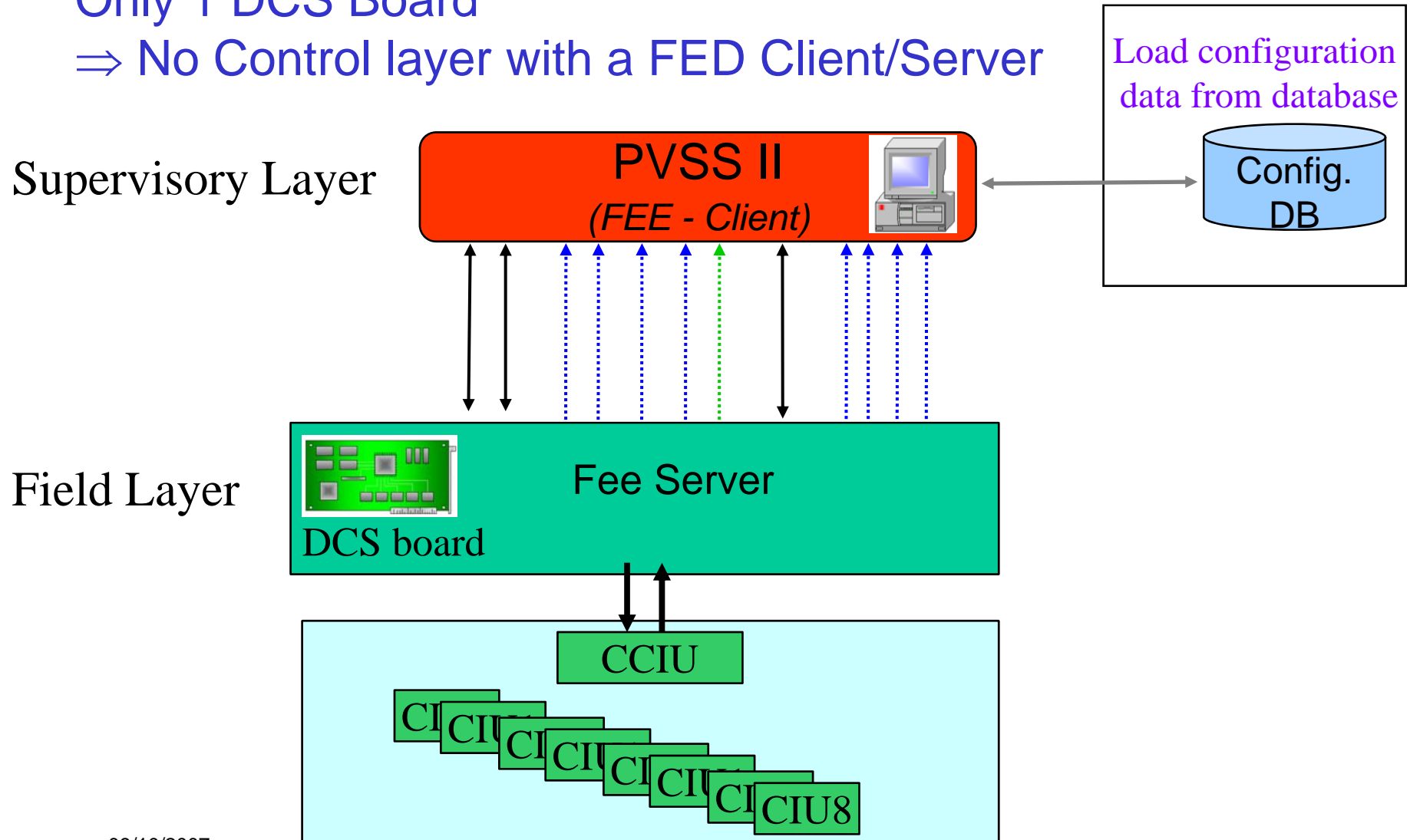
Reload Table Store Table STORE PARAM TO CHANNELS CLOSE



# Front-End-Electronics in DCS Control and monitor channels



Only 1 DCS Board  
⇒ No Control layer with a FED Client/Server





# FEE Control panels



Vision\_1: TOP

### CIU0 Manual Control

	Mean even	Mean Odd	Cut even	Cut Odd	Delay hit	Threshold	Q	T
1	0	0	0	0	2047	1100		
2	0	0	0	0	2047	1100		
3	0	0	0	0	2047	1094		
4	0	0	0	0	2047	1108		
5	0	0	0	0	2047	1119		
6	0	0	0	0	2047	1118		
7	0	0	0	0	2047	1116		
8	0	0	0	0	2047	1110		

Profil Clk1 win1  
 Profil Clk1 win2  
 Profil Clk2 win1  
 Profil Clk2 win2  
 Delay Clk1 win1  
 Delay Clk1 win2  
 Delay Clk2 win1  
 Delay Clk2 win2

Profil Reset  
 Test timing  
 Test charge  
 Test window  
 Pedestal Suppression  
 SelA FPGA1  
 SelB FPGA1  
 SelA FPGA2  
 SelB FPGA2

Update file    Update DP from FEE    Close

### CCIU

Minimum bias VQA threshold: 29    Random trigger rate: 1

Minimum bias VOC threshold: 3    Trigger Select 1: 1

Beam gas VQA threshold: 2    Trigger Select 2: 2

Beam gas VOC threshold: 2    Trigger Select 3: 3

BBA for beam gas trigger th: 0    TriggerSelect 4: 4

BBC for beam gas trigger th: 0    TriggerSelect 5: 5

Trigger delay: 15

Random trigger generator  
 Clock trigger source sel 1  
 Clock trigger source sel 0  
 Sel 1 clock DCS  
 Sel 2 clock DCS  
 Clock VQA source sel 0  
 Clock VOC source sel 1  
 Clock VQA sel 1  
 Clock VOC sel 1  
 Sel clock 1  
 Sel clock 2  
 Sel clock 3  
 Sel clock 4

Centrality trigger VQA threshold 1: 65535

Centrality trigger VQA threshold 2: 0

Centrality trigger VOC threshold 1: 1

Centrality trigger VOC threshold 2: 2

Multiplicity trigger VQA thr high: 2

Multiplicity trigger VQA thr low: 1

Multiplicity trigger VOC thr high: 0

Multiplicity trigger VOC thr low: 1

Update DP from FEE    Update file    Close

### CTP

Trigger sign

1	101
2	102
3	103
4	104
5	105
6	106
7	107
8	108
9	109
10	110
11	111
12	112
13	113
14	114
15	115
16	116

L1 trigger latency: 0

Option code: 2

Include hamming:

### CIU0 HPTDC Manual Control

HP TDC FileName

DLL tap		Offset	
0	0	16	0
1	0	17	0
2	0	18	0
3	0	19	0
4	0	20	0
5	0	21	0
6	0	22	0
7	0	23	0
8	0	24	0
9	0	25	0
10	0	26	0
11	0	27	0
12	0	28	0
13	0	29	0
14	0	30	0
15	0	31	0

Test select: Core clock

DLL clock source: PLL clock 320    DLL Mode: 320MHz  
 Core clock source: Clock 40    Dead time: 10ns  
 IO clock source: Clock 40    Max event size: No limit  
 Serial clock source: PLL clock 80    Leading res.: 100ps  
 Strobe select: No strobe    Readout FIFO size: 256  
 Readout single cycle sp.: 40Mbits/s    Width: 800ps

Roll Over: 4095  
 Charge pump Curr.: 4  
 Serial clk delay: 0  
 IO clk delay: 0  
 Core clk delay: 0  
 DLL clk delay: 0  
 RC tap 1: 0  
 RC tap 2: 0  
 RC tap 3: 0  
 RC tap 4: 0  
 Vernier offset: 0  
 DLL charge pump: 1  
 Coarse count offset: 0  
 Trigger count offset: 3836  
 Event count offset: 0  
 Search window: 47  
 Match window: 39  
 TDC lu: 9  
 Reject count offset: 3832  
 Serial delay: 0  
 Token delay: 0

Ch enable  
 Fixed pattern

Vermer  
 Coarse  
 Channel select  
 L1 buffer parity  
 Trigger FIFO parity  
 Trigger matching  
 Readout FIFO parity  
 Readout state  
 Setup parity  
 Control parity  
 JTAG inst. parity

Matching  
 Pair  
 TTL serial  
 TTL control  
 TTL reset  
 TTL clock  
 TTL hit  
 Test mode  
 Trailing  
 Leading  
 Mode RC  
 Mode RC comp  
 Power down mode  
 Test output  
 Inv Status conn  
 Low power mode  
 Test invert  
 Counters on bunch rst  
 Master reset code  
 Master rst on event rst  
 Reset ch. buffer on sep.  
 Sep. on event rst  
 Sep. on bunch rst  
 Direct event reset  
 Direct bunch reset  
 Direct trigger  
 Reject readout FIFO full  
 Readout occupancy  
 Readout separator  
 Overflow detect  
 Relative  
 Automatic reject  
 Fixed pattern  
 Local trailer  
 Local header  
 Global header  
 Global trailer  
 Keep token  
 Master  
 Byte-wise  
 Serial  
 JTAG readout  
 Select bypass inputs  
 Error mark  
 Error bypass  
 Readout speed sel

Update DP from FEE    Update file    Close

HP TDC FileName

Option code: 2

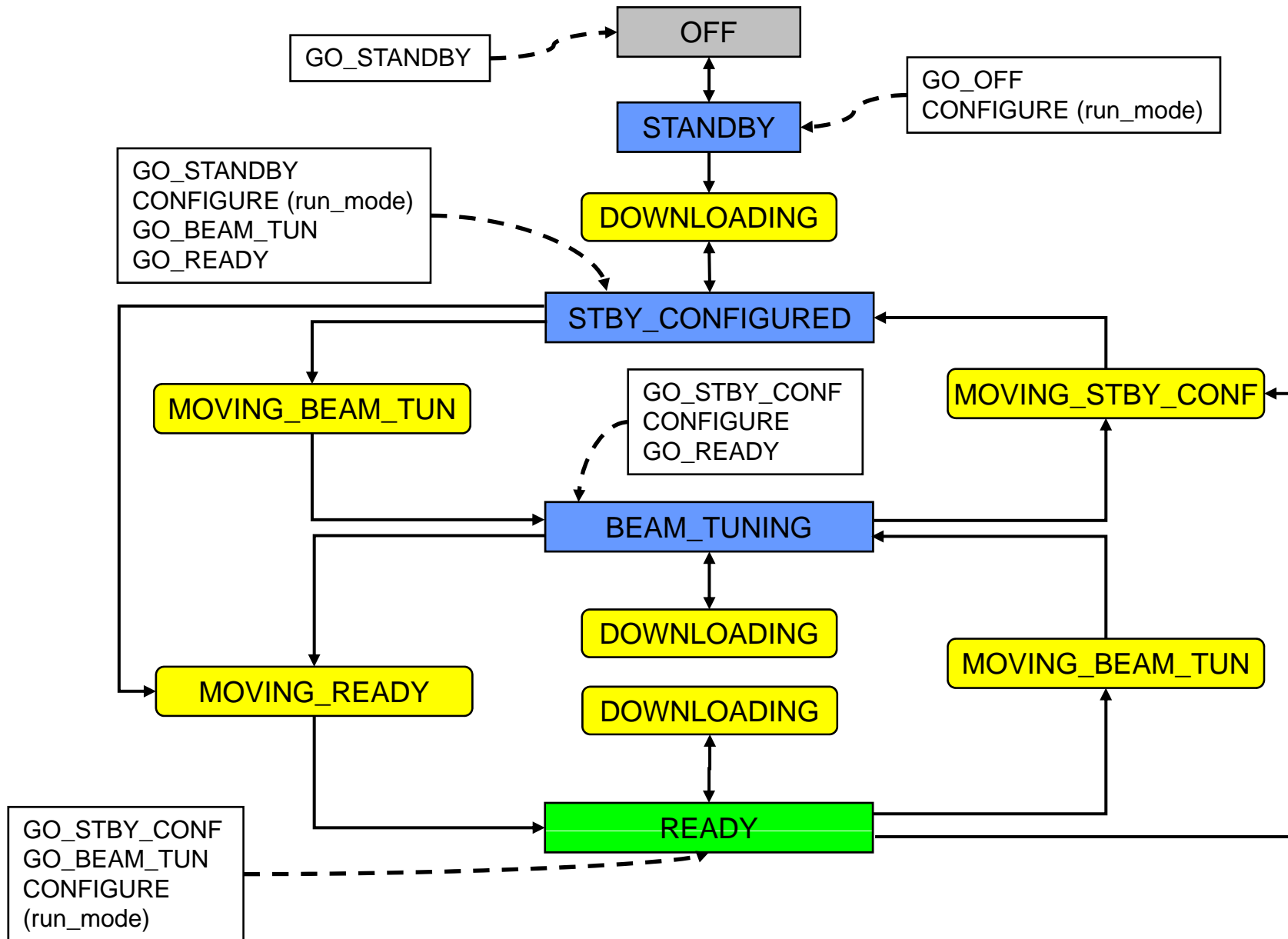
Include hamming:

CLOSE



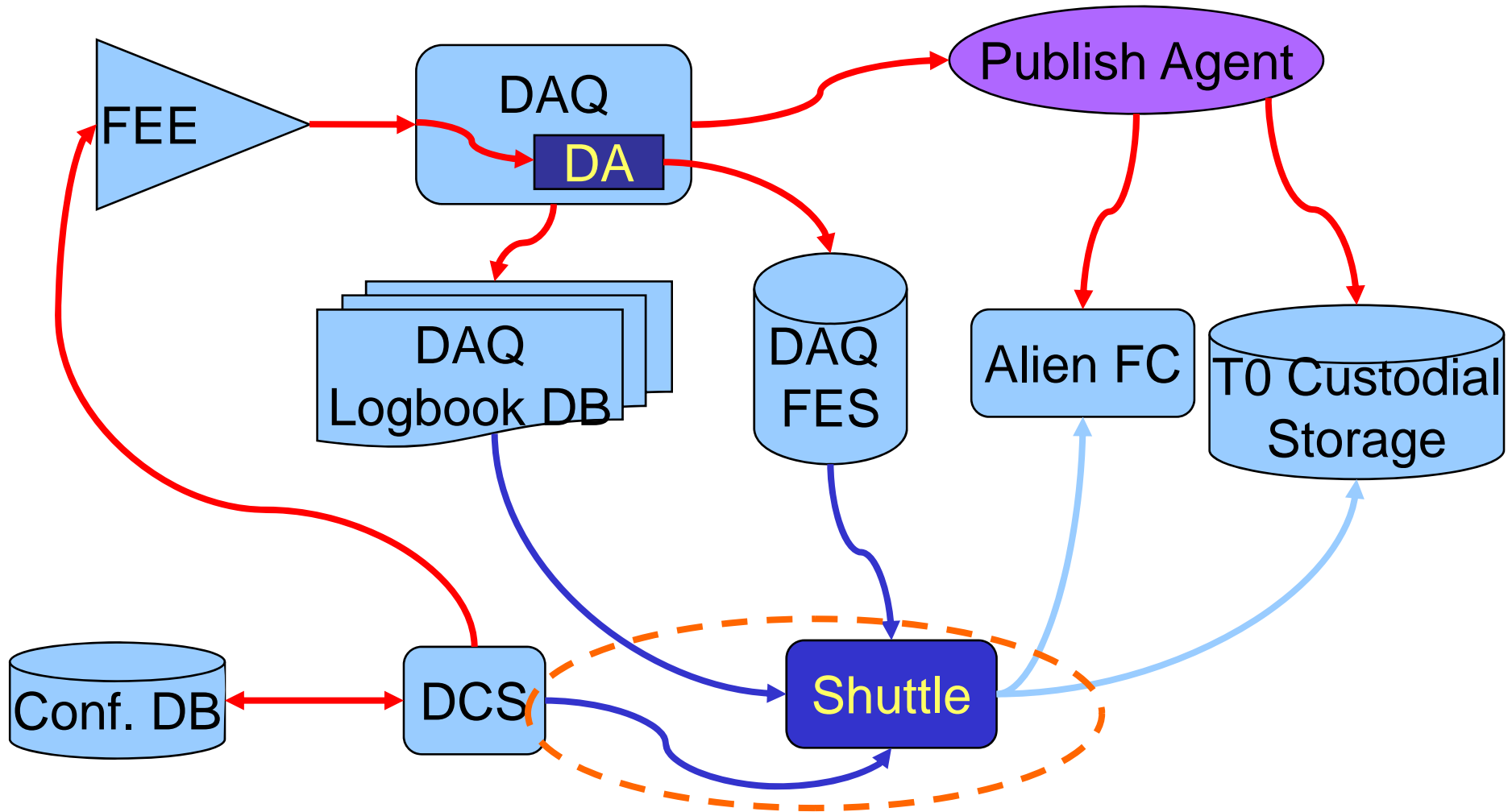


# V0-DCS State Diagram





# On-Offline connection diagram (Use case6)





# V0 - DCS Preprocessor



Add **AliVZERODataDCS** class to process DCS Data

Extract the Means and Widths during a physics run  
of the 64 HV Channels

Corresponding DCS Aliases:

**V00/HV/V0[A-C]/SECTOR[0-7]/RING[0-3]**

DCS alias	N of channels	Data type	Unit	Value	% fluctuation	Update Frequency (s)
<b>V00/HV/V0[A-C] /SECTOR[0-7] /RING[0-3]</b>	64	float	V	1800	1	10

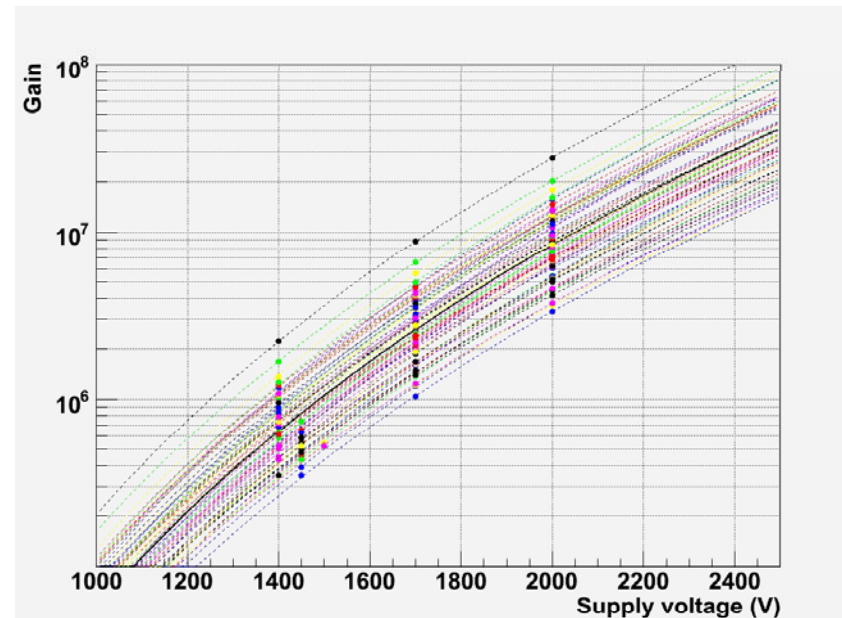


# Gain adjustment



V0 detector should run with a common gain on all channels

- DA will calculate from data gain, sigmas and pedestals
- All PMTs have been calibrated



V0Preprocessor will calculate the new voltages which should be apply via DCS panels



# Conclusions

---



- DCS Control of the V0 is well advanced
- It is used daily in lab for the test of the FEE boards
- DCS Preprocessor developed, tested and committed



# Backup





# V0 Node Synchronization table



V00_DET	V0 MODULE (V0A/V0C)	FEE	VME Crate
OFF	OFF	OFF	OFF
STANDBY	OFF	OFF	ON
DOWNLOADING	DOWNLOADING	DOWNLOADING	ON
CALIBRATING		CALIBRATING	ON
STBY_CONFIGURED	STBY_CONFIGURED	READY	ON
MOVING_READY	MOVING_READY	READY	ON
MOVING_BEAM_TUN	MOVING_BEAM_TUNING	READY	ON
MOVING_STBY_CONF	MOVING_STBY_CONF	READY	ON
BEAM_TUNING	BEAM_TUNING	READY	ON
READY	READY	READY	ON
TRIPPED	TRIPPED		
NO_CONTROL	NO_CONTROL		
NO_CONTROL		NO_CONTROL	
NO_CONTROL			NO_CONTROL
SYS_FAULT	SYS_FAULT		
SYS_FAULT		SYS_FAULT	
SYS_FAULT			SYS_FAULT



# VME Control panel



VISION\_1: TOP

11:12:59 28-09-07 dsU# 300

root

FSM VME NOT\_READY

VME DET

- VOC
  - VOC\_QUAD0
  - VOC\_QUAD1
  - VOC\_QUAD2
  - VOC\_QUAD3
- V00\_INFR
- V00\_FEE
  - CIU0\_memory\_zone
  - CIU1\_memory\_zone
  - CIU2\_memory\_zone
  - CIU3\_memory\_zone
  - CIU4\_memory\_zone
  - CIU5\_memory\_zone
  - CIU6\_memory\_zone
  - CIU7\_memory\_zone
  - CTP\_CCIU\_memory\_zone

V0 - VME Control Panel

LHC MACHINE DEVELOPMENT  
UNSTABLE BEAMS  
RAD. NO CONNECT

## VME Crate Control

### VME Crate

Commands: On Off

Temperature: Probe 1 21 °C

General Status:

- Power OFF
- Errors
- AC Power
- EEPROM
- Remote Control
- HW Write Protect

Power Supply:

Channel Name	Voltage	Current
+ 5 Volt	0.000	0.300
+ 8 Volt	0.000	0.140
+ 3.3 Volt	0.000	0.300
- 8 Volt	0.010	0.000

### CanBus

Commands: On Off

Reset Net

Reset Bus Off Count

Flush Read Queue

Flush Write Queue

Transmit/Receive:

- Tx Messages Pending
- Rx Messages Pending
- Tx Error Occured
- Rx Error Occured

Buffers:

- Buffer Overflow Occured
- Hardware Buffer Overflow Occured
- Software Buffer Overflow Occured

Bus Status:

- Error Active State
- Error Warning State
- Error Passive State
- Bus Off State

Parameter	Value	Details
Read Queue Length	0	Details
Write Queue Length	0	Details
Rx Error Count	0	Details
Tx Error Count	0	Details
Overrun Error Count	0	Details
Bus Off Count	0	Details

Detector Monitoring Zone

High Voltage	Sector 0	Sector 1	Sector 2	Sector 3
High Voltage	Sector 4	Sector 5	Sector 6	Sector 7

Info Panel not yet enabled!

v00\_dcs v00\_dcs

CLOSE





## V0 Front-End-Electronics in DCS Progress Status



- FEE server on DCS Board:
  - Driver for communication with CCIU: developed, tested and fully functional
  - FEE server: developed, tested, stable and fully functional
  - DIM server for CTP (to set CTP option code : developed, tested, stable and fully functional
- PVSS:
  - State machines defines and fully implemented
  - FEE Client (DIM) stable and fully functional
  - Front panels : completed
- VME Crate:
  - Control, FSM and panels completed using the work of Lionel Wallet.
- Remaining work:
  - Interface with the Configuration DB.



# Résumé of HV/LV Sub-system



## CAEN Crate:

- Crate installed in CR4 controlled by DCS
- Need to develop the operation of the crate by 2 operators (T0/V0)

## PVSS:

- All panels developed

## FSM:

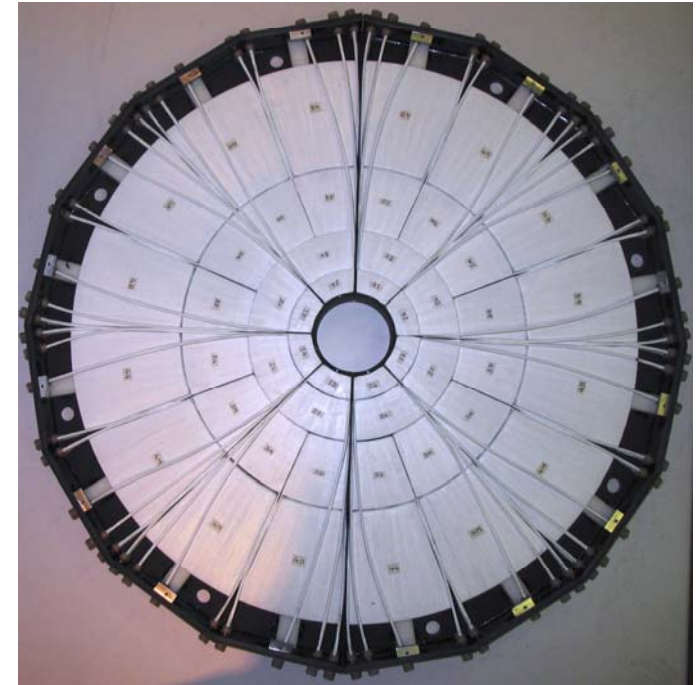
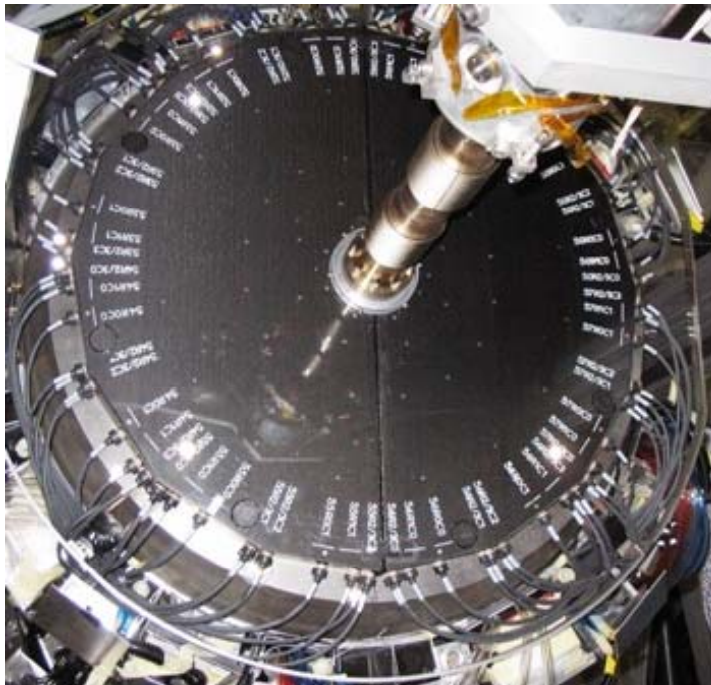
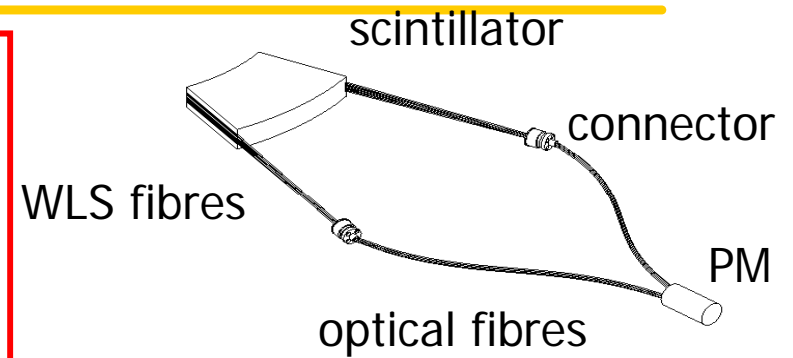
- FSM completed including the SW interlock between LV and HV.



# The V0 detector

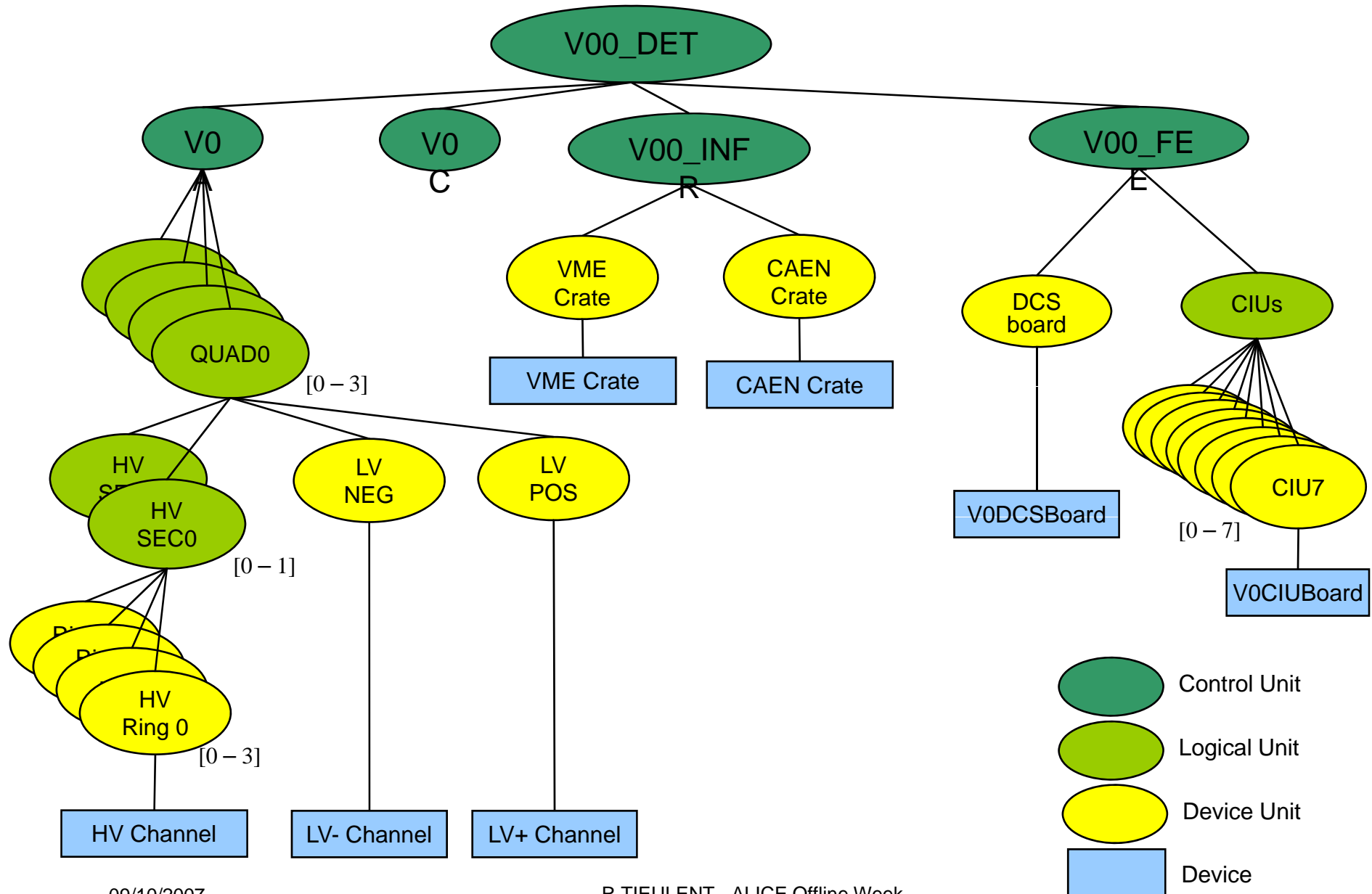


- Two scintillator hodoscopes at low angles
  - trigger for the central detectors
  - background filter for Muon
- 2 x 32 channels (VOA et VOC)
- 8 sectors of 4 channels per hodoscope



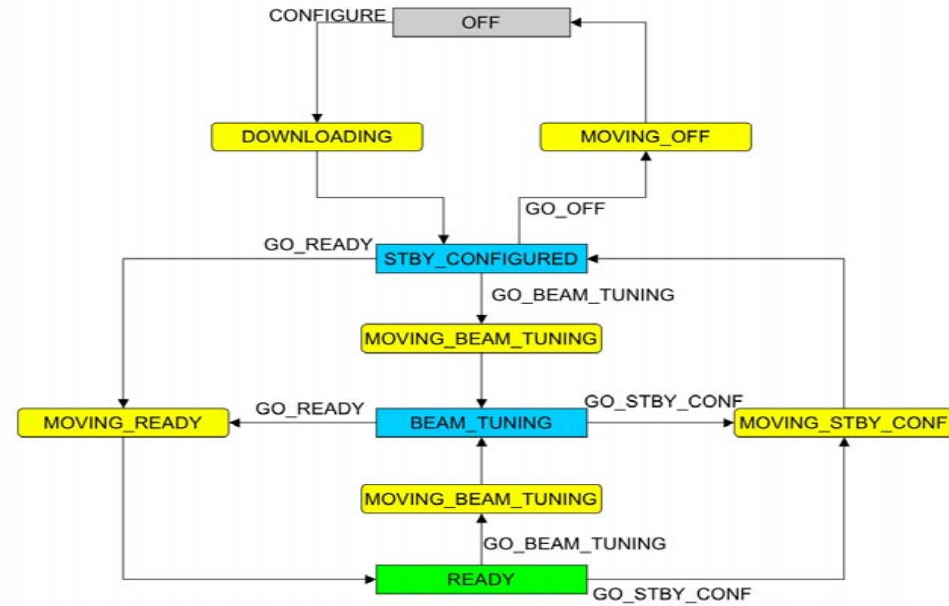
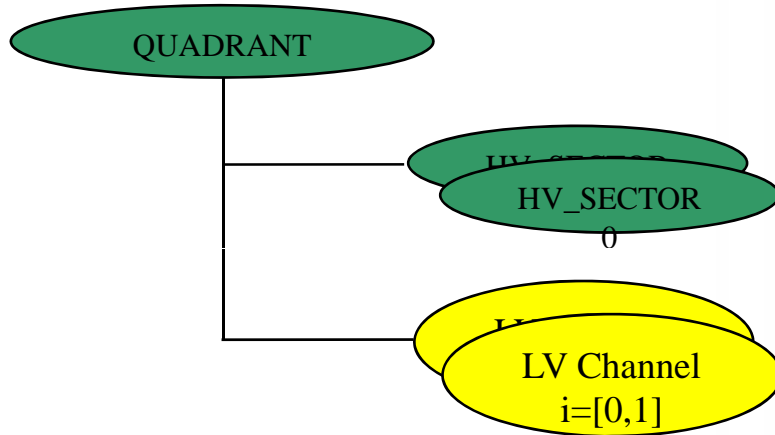


# The V0-FSM Tree





# Voltage Quadrant FSM



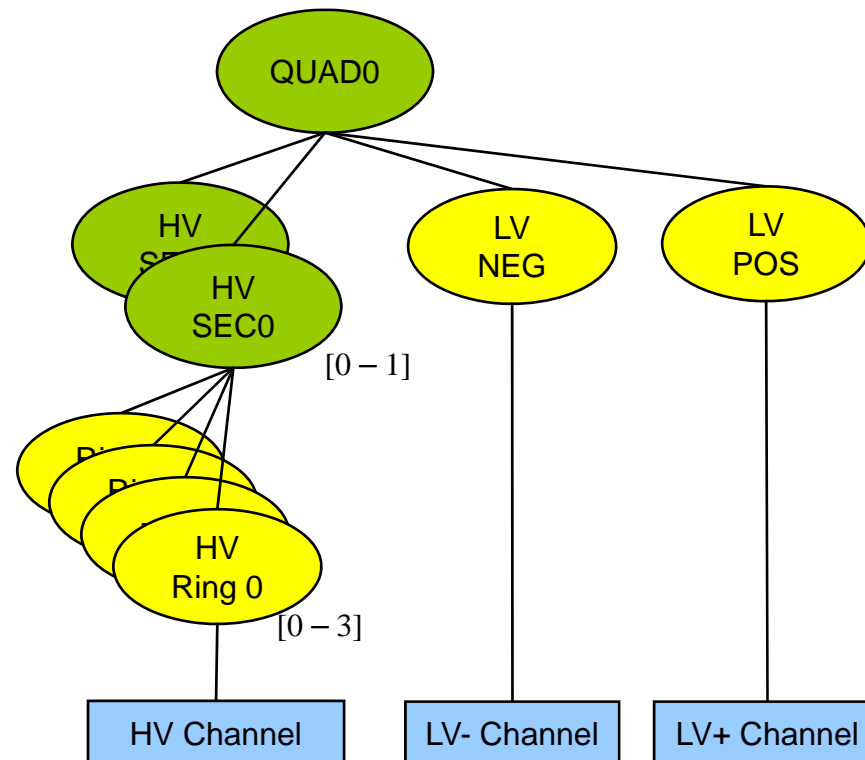
POWER MODULE	HV_SECTOR i <sup>th</sup>	LV Channel i <sup>th</sup>
OFF	OFF	OFF
DOWNLOADING	OFF	RAMP_UP
MOVING_OFF	OFF	RAMP_DW
STBY_CONFIGURED	OFF	ON
MOVING_READY	MOVING_READY	ON
MOVING_BEAM_TUNING	MOVING_BEAM_TUNING	ON
MOVING_STBY_CONF	MOVING_OFF	ON
BEAM_TUNING	BEAM_TUNING	ON
READY	READY	ON
NO_CONTROL	NO_CONTROL	
NO_CONTROL		NO_CONTROL
TRIPPED	TRIPPED	
TRIPPED		TRIPPED
SYS_FAULT	SYS_FAULT	
SYS_FAULT		CHAN_FAULT



# HV/LV Sub-system

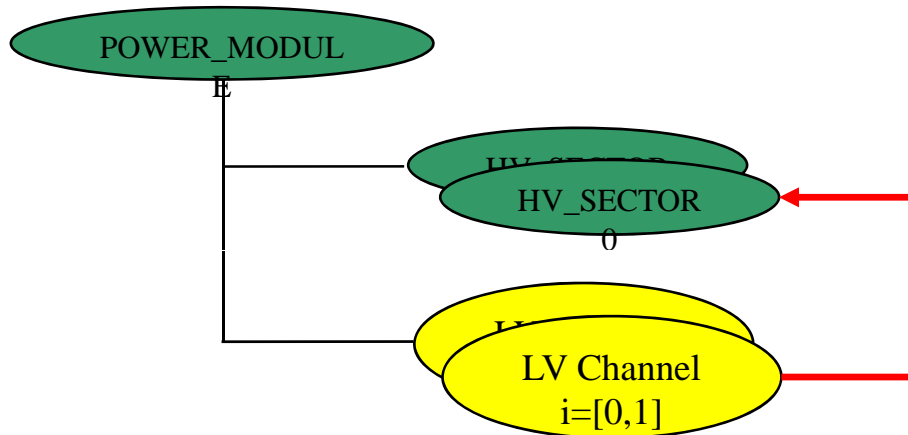


- Use the principle of Caen Channel Stock Settings developed by Antonio Franco for the HMPID. Will move to new FW component as soon as it becomes available.





# Voltage Quadrant Interlock



If (Any LvChannel != ON) and (Any Hv Sector !=OFF)  
Then SWITCH\_OFF HV Sectors



# Working principle



- Control of the DCS board components :
  - TTCRx registers (example : TTC channel B data output for the CCIU board)
- Control of the FEE boards (CCIU and CIU) components
  - HPTDCs
  - Modes
  - Pedestals
  - ...
- Collection and publication of monitoring data
  - DCS board
  - FEE





# Control panels proposal



- Main panel with :
  - Configure (from configuration file or database configuration parameters?)
  - Reset
- Child panel with status of the different components of the system controlled by the DCS board
  - HPTDC on DCS board
  - CCIU registers
  - CIU registers
- Sub-child panels with individual access to registers and functions of the previous components



# Summary of calibration procedure



Gains and pedestals computed by Online Monitoring using dedicated data (**minimum bias** and **+/- 10 around the event of interest** mini-events respectively) stored in the FEE and sent to the DAQ with the events of interest.

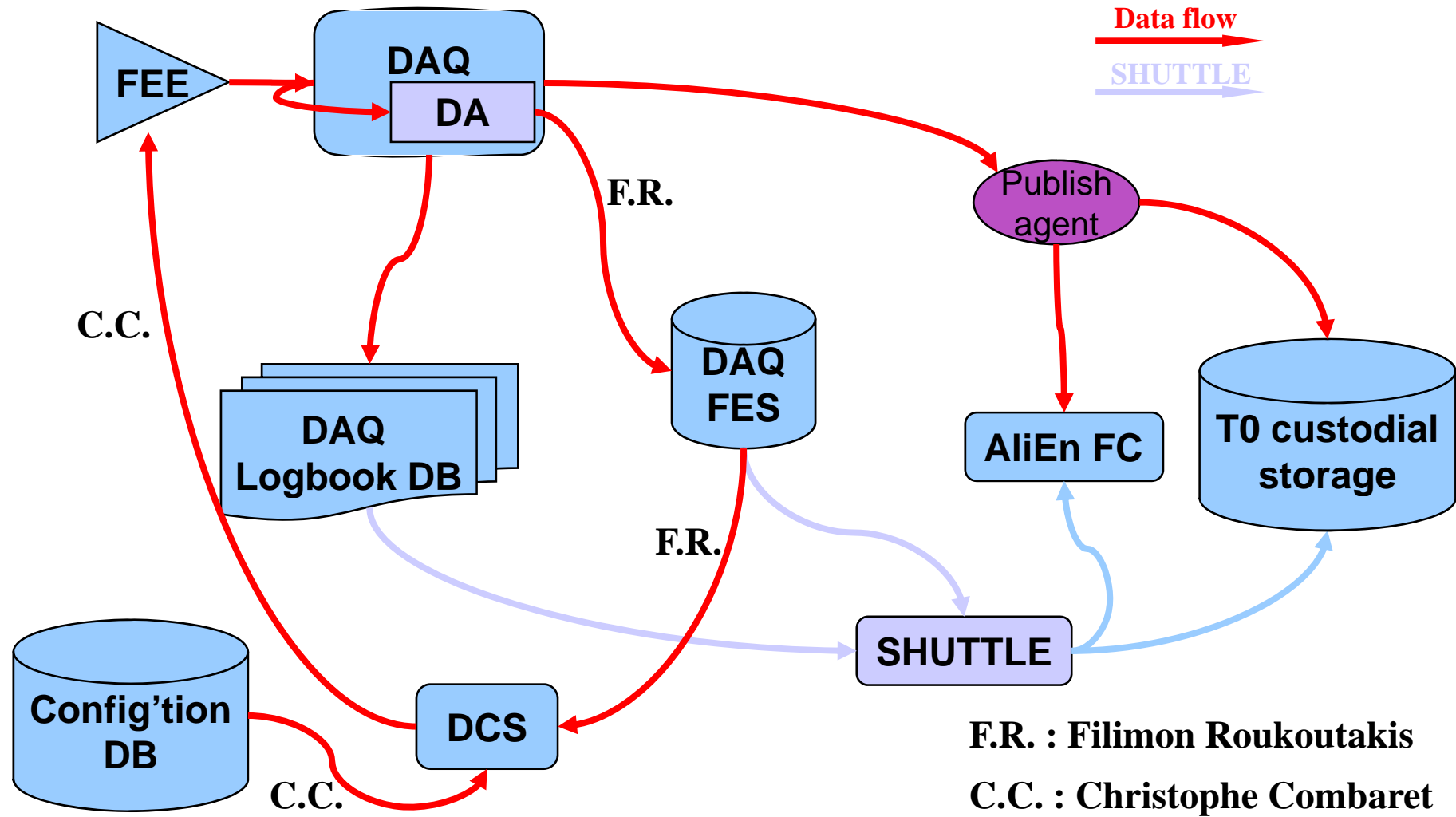
Note that this procedure is achieved by the FEE **independently of the Central Trigger Processor**.

These values will be written in the Calibration Data Base for later use by offliners and updated at each run change.

Validity period will be run interval unless a hardware failure occurs.



# Use case 6





# Calibration excel file



Par #	Parameter	Data format/size per channel	Data size (Total) Bytes		Update freq	Source	Confirmed
			in OCDB	reference			
1	gains	32 bits (TBC)	512	0	Run	DAQ (on line data) *	yes
2	pedestal means	32 bits (TBC)	512	0	Run	DAQ (on line data) *	yes
3	pedestal sigmas	32 bits (TBC)	512	0	Run	DAQ (on line data) *	yes
4	time gains	32 bits (TBC)	256	0	Run	DAQ (on line data) *	yes
5	time offsets	32 bits (TBC)	256	0	Run	DAQ (on line data) *	yes

Run type / Trigger type	# of required events/sampling rate	Processing level: sub-event or event	Results: FEE/Archive	Accessible by offline	Calib. Procedure in AliRoot	use case #
physics data *	at least 2000 L2 (TBC)	event and sub-event	DAQ FES / OCDB	yes	fall 2006	6
physics data *	at least 1000 L2 (TBC)	event and sub-event	FEE and DAQ FES / OCDB	yes	fall 2006	6
physics data *	at least 1000 L2 (TBC)	event and sub-event	FEE and DAQ FES / OCDB	yes	fall 2006	6
physics data *	at least 10000 L2 (TBC)	event	DAQ FES / OCDB	yes	Unknown	1
physics data *	at least 10000 L2 (TBC)	event	possibly FEE and DAQ FES / OCDB	yes	Unknown	6



# Online output data for DAQ and monitoring



An event as seen by the V0 Front End Electronics will be:

- Charges (64).
- Arrival times (64) and time response widths (64).
- Beam-Beam (BB) and Beam-Gas (BG) flags (64).
- States of the 5 triggers sent to the CTP (MinBias, BB, BG, Central, SemiCentral).

For each event triggered by a L2 signal coming from the CTP (called Event-Of-Interest), the following information will be sent to the DAQ:

1. The event of interest itself with all the parameters listed above, **for physics analysis**
2. The events between **Eol-10 to Eol+10** (charges and BB/BG flags), **for monitoring pedestals, pile-up...**
3. The **10 last V0 Minimum Bias** events (charges and BB/BG flags), **for monitoring gains**



# Calibration procedure



- Calibration parameters are computed online in the DAQ LDC from sampling dedicated data
- Results are made available as ROOT files in the DAQ FES
- DCS accesses the Root file in the DAQ FES, compares the parameter values to reference values stored in the DCS Configuration DB and updates the FEE values if needed.



# Calibration



Calibration **CDB file** has been created and CDB reading implemented.

Calibration parameters stored into CDB are :

- 128 gains, 128 pedestal means, 128 pedestal sigmas (2 QDC per channel)
- 64 time gains and 64 time offsets

i.e. 512 floats, **4 kB**

All these parameters are accessible through class **AliVZEROCalibData**