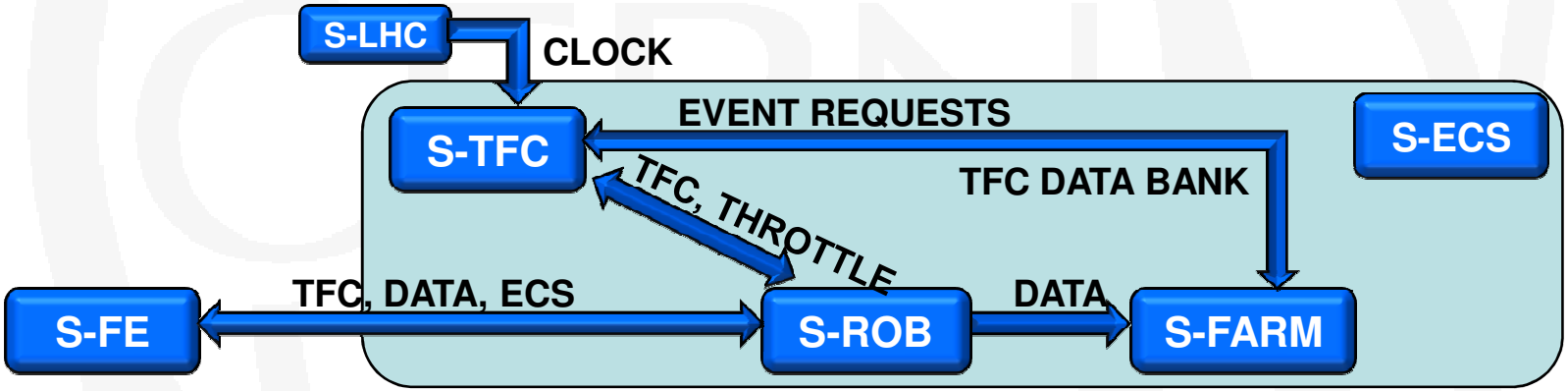
Simulation framework for TFC architecture and configurable FE-ROB model

LHCb Electronics Upgrade Meeting
26-10-09

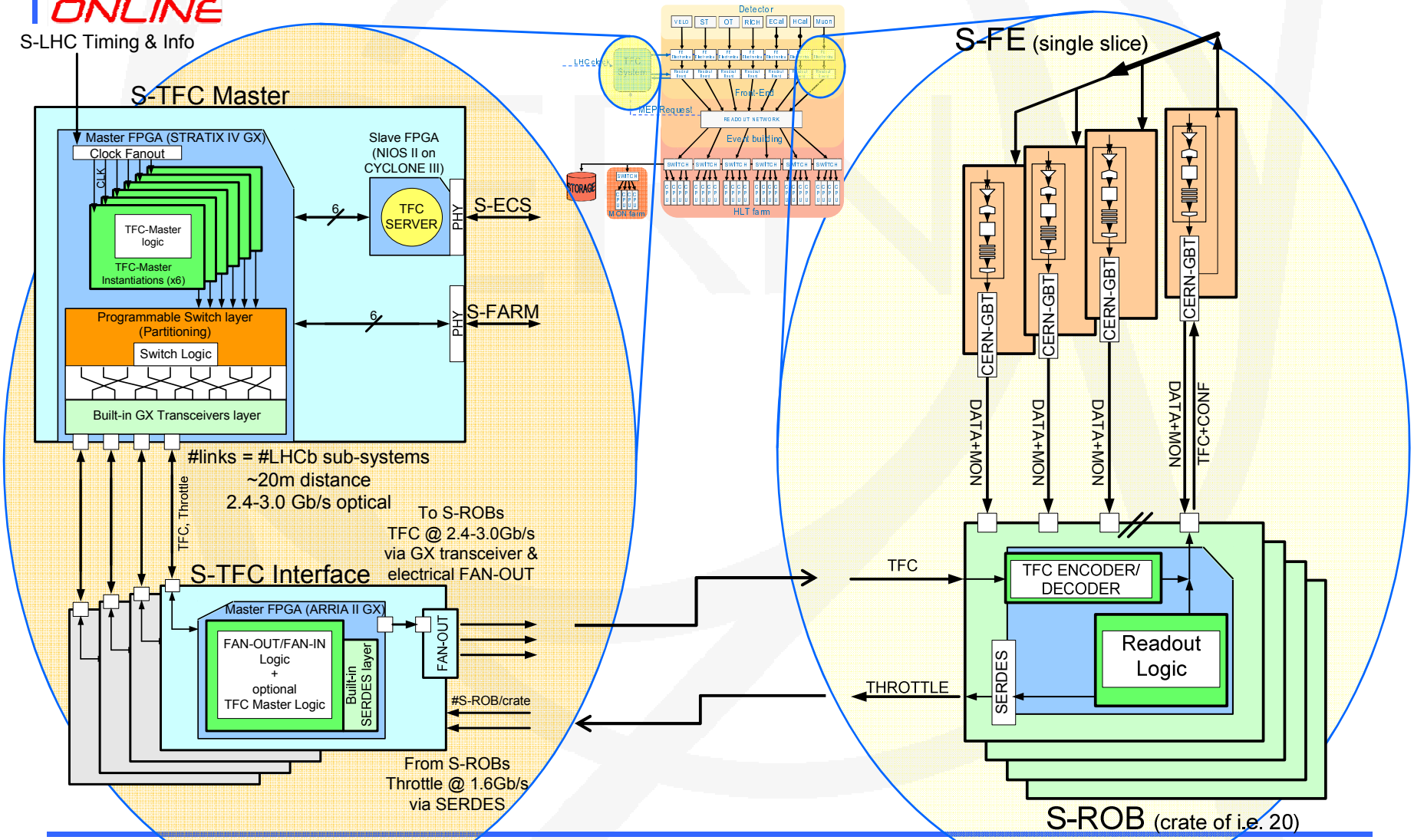
Federico Alessio, CERN
Richard Jacobsson, CERN

Quick reminder: Readout Architecture



- No L0-trigger
- Point-to-point bidirectional high-speed optical links
  - → Same technology and protocol type for readout, TFC and throttle
  - → Reducing number of links to FE by relaying ECS and TFC information via ROB

Elaborated S-TFC Architecture



Main S-TFC activities Q1-Q3/2009

- Build a full simulation framework based on the new Readout/S-TFC architecture

  1. synthesizable “clock level-fidel” simulation of S-TFC component and links (Thanks to Marseille for GBT simulation to startout from!)
  2. clock level emulation of FE+ROB model with variable parameters

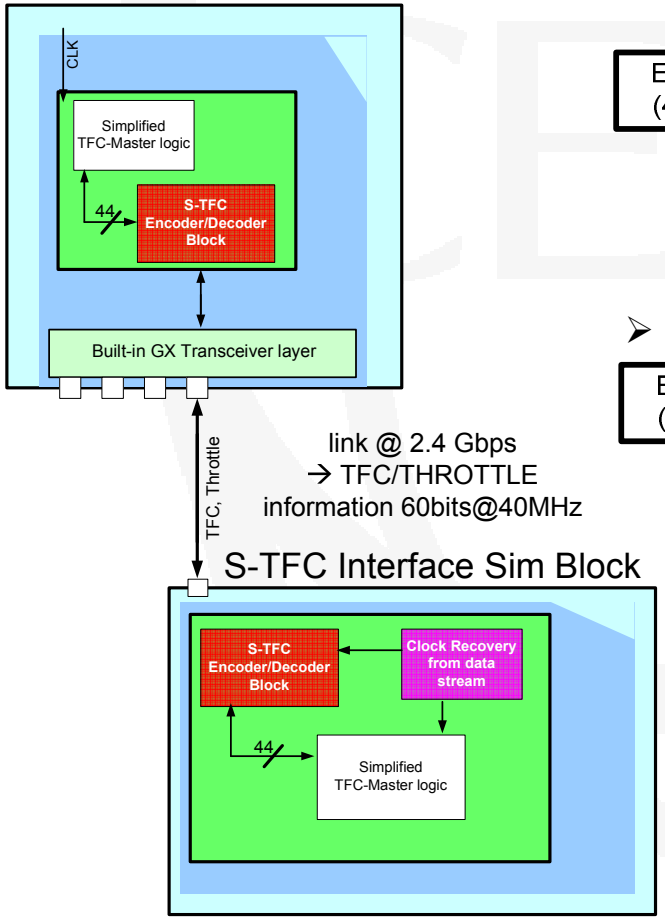
- Investigate (in theory for now) latency and phase control and stability of common Altera GX links with Marseille

- Based on mature ideas on new S-TFC architecture presented at IEEE Real Time Conference 2009 in Beijing, China

http://lhcb-doc.web.cern.ch/lhcb-doc/presentations/conferencetalks/postscript/2009presentations/Alessio-IEEE-NPSS.ppt

1. Simulating S-TFC links

S-TFC Master Simulation Block



S-TFC Master ←→ S-TFC Interface link **preliminary** protocol

- TFC control fully synchronous 60bits@40MHz → 2.4 Gb/s (max 75 bits@ 40 MHz → 3.0 Gb/s)

EVENT ID (4-12 bits)	TFC information (40-32 bits)	ReedSolomon-FEC (16 bits)

1. Reed Solomon-encoding used on TFC links for maximum reliability (header ~16 bits) (ref. CERN-GBT)
2. Asynchronous readout → TFC info must carry Event ID

- Throttle("trigger") protocol

EVENT ID (4-12 bits)	THROTTLE information (20 bits)	OTHERS	ReedSolomon-FEC (16 bits)

1. Must be synchronous and carry Event ID
   → Protocol will require alignment similar to TFC protocol

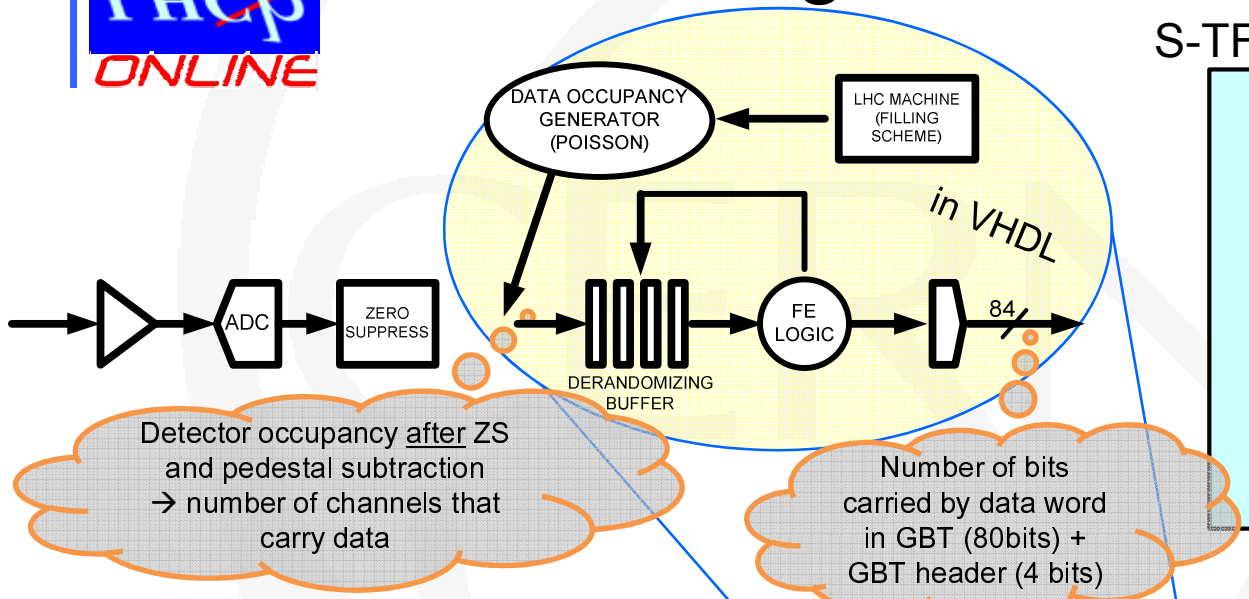
The links are successfully simulated

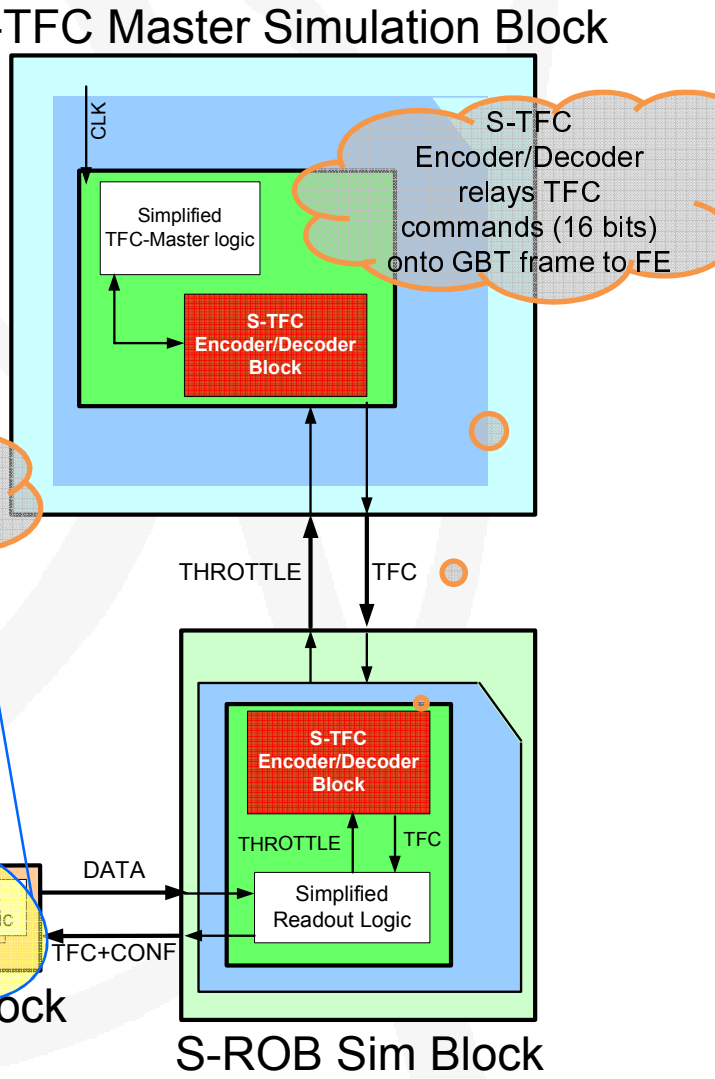
→ The clock recovery from data stream needs additional firmware logic (thanks for disclosed info from Altera) in order to control the latency and the phase of the clock w.r.t. the data stream

→ Plan to test the link with a (real) board developed in Marseille

N.B. in the full simulation framework, the links are not simulated for "time consuming" reasons but emulated

2. Simulating the RO architecture



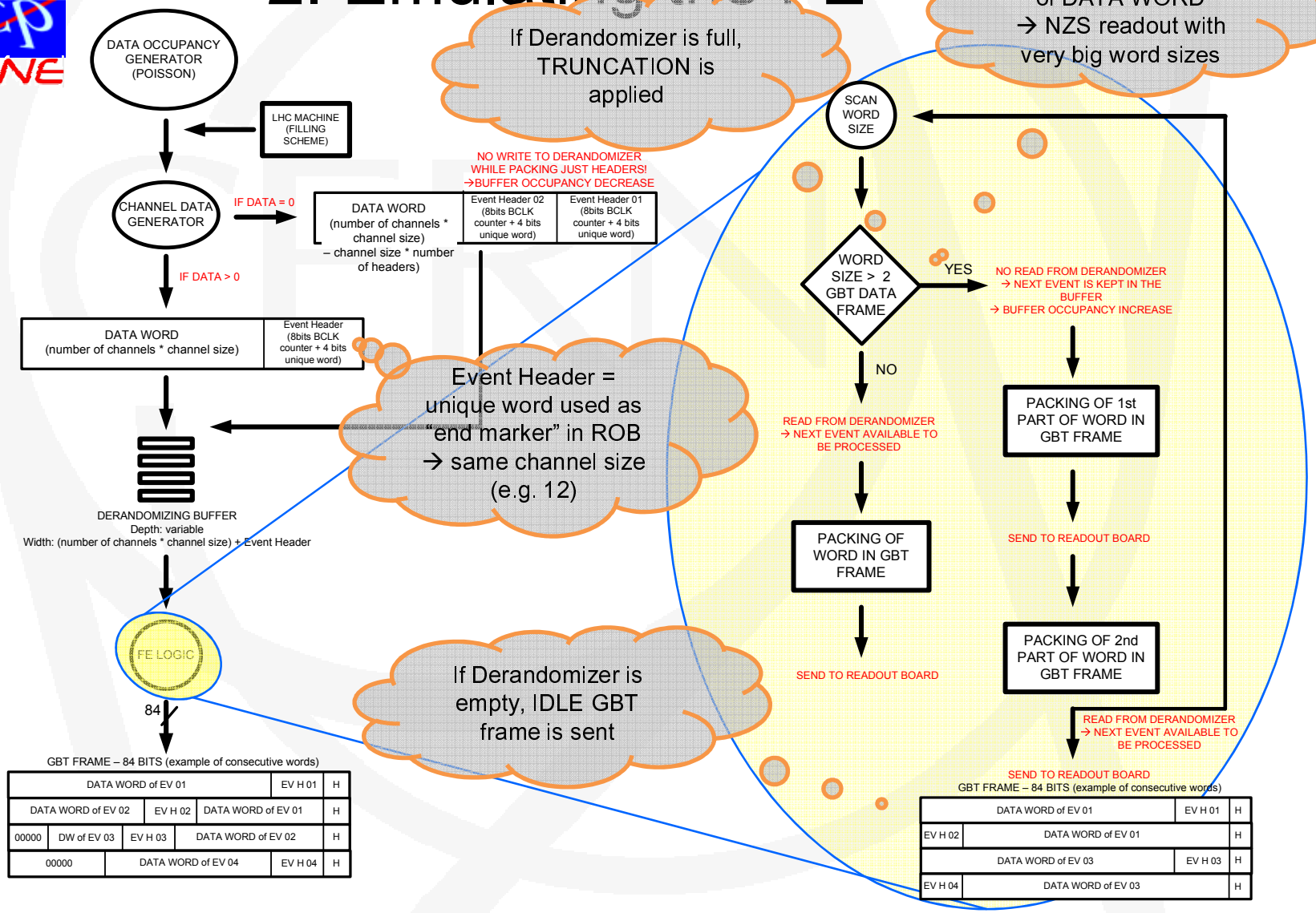


Customizable variables:

→Detector occupancy mean value
→Channel size
→ Number of channels per GBT link
→ Derandomizer depth

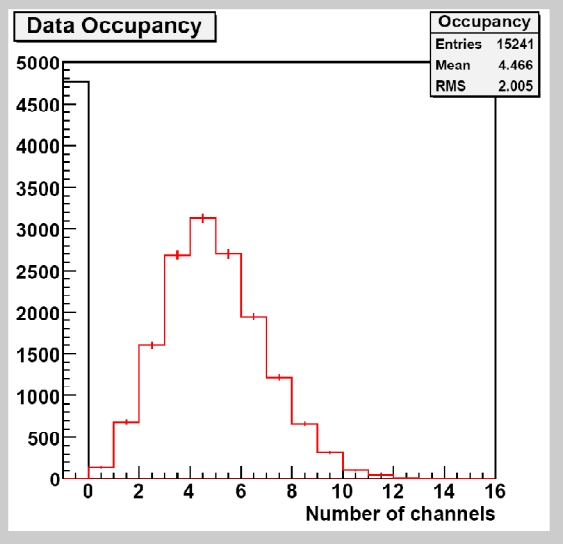
Nominal (2808/3564) LHC filling scheme at LHCb point 8 (collision scheme)

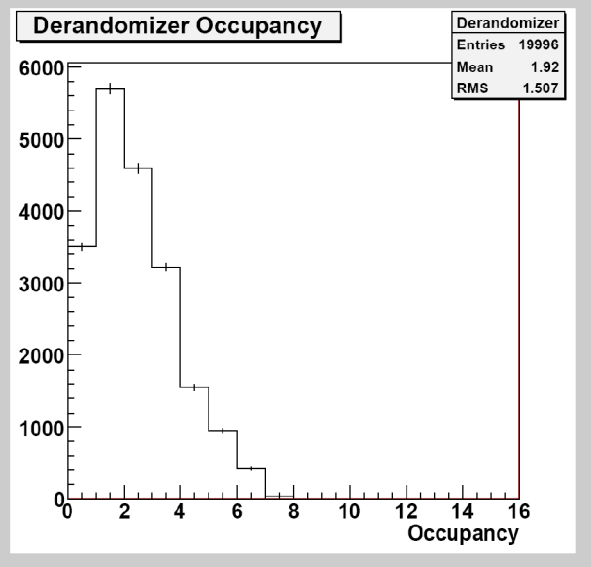
2. Emulating the FE

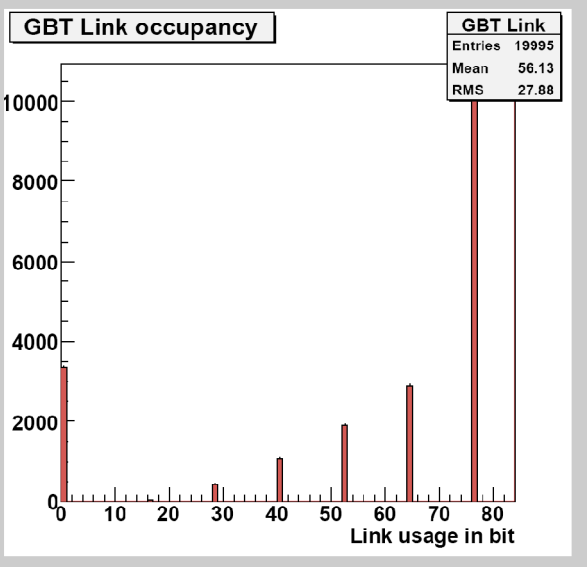


2. Results (Example 1)

Variables applied:
<Detector occupancy> = 30%
#channels / GBT link = 15
→ ~ 4.5 channels / GBT after ZS
Derandomizer depth = 16
Channel size = 12
(e.g. ADDR = 4bits + ADC_DATA = 8bits)



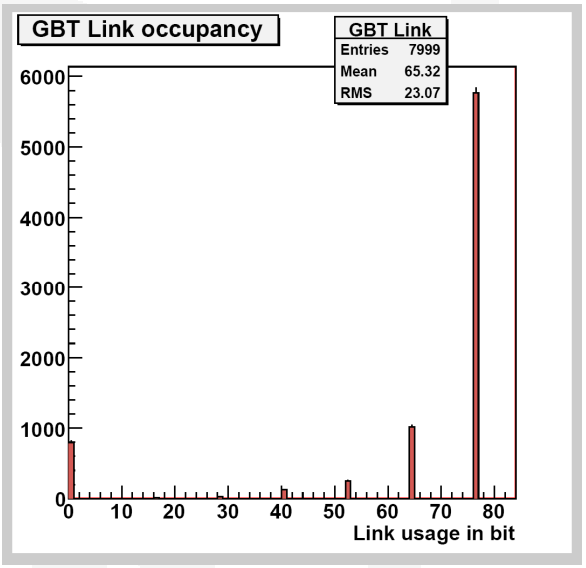


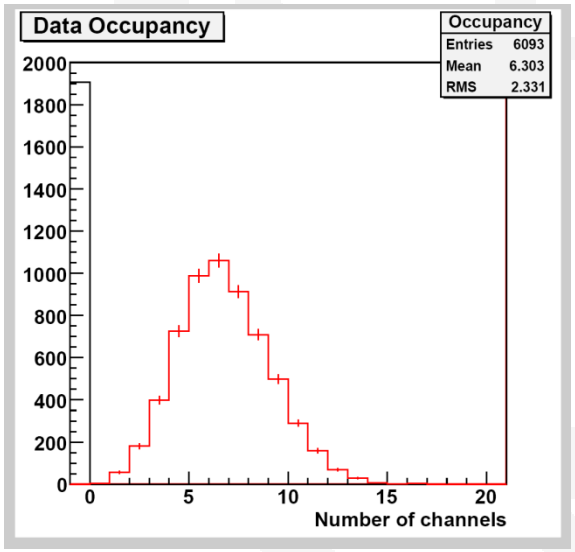


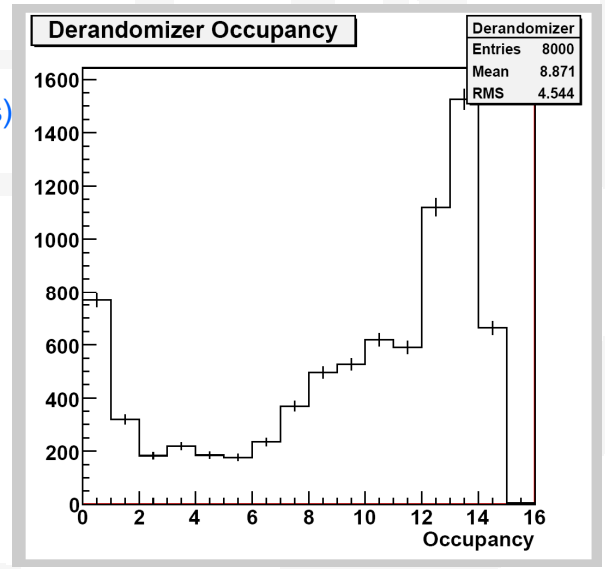
→ No truncation occurred: system undercommitted (overdesigned)
→ ~145kbits of channel data sent through one GBT link over full LHC turn: 48.3% of GBT link bandwidth + 14% Event Header + 4.8% GBT header (unavoidable)

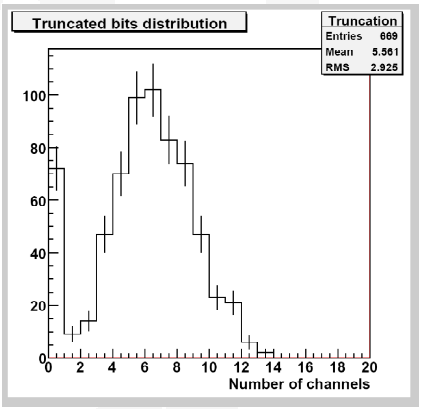
2. Results (Example 2)

Variables applied:
<Detector occupancy> = 30%
#channels / GBT link = 21
→ ~ 6.3 channels / GBT after ZS
Derandomizer depth = 16
Channel size = 12
(e.g. ADDR = 5bits + ADC_DATA = 7bits)









→Truncation occurred: "raw truncation" = 10.5%
"effective truncation" = 9.5%
→ Size of truncated events follows occupancy PDF, no bias!
→ 184~kbits of data sent through one GBT link over full LHC turn: 61.6% of GBT link bandwidth + 14% Event header + 4.8% of GBT header (unavoidable)

2. Results (Example 3)

Variables applied:

<Detector occupancy> = 30%

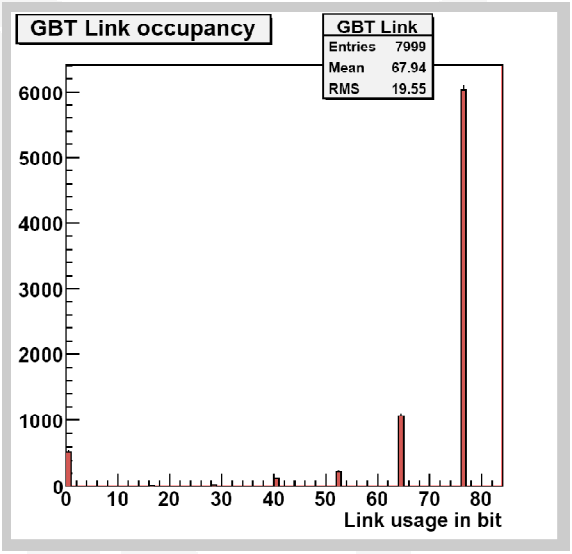
#channels / GBT link = 21

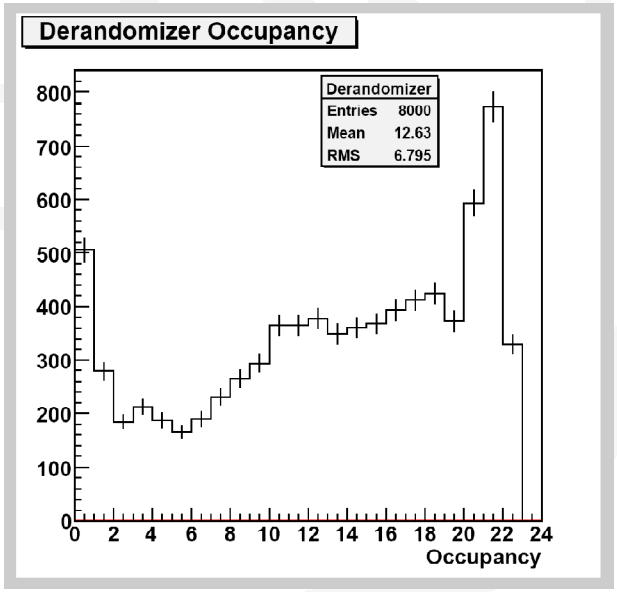
→ ~ 6.3 channels / GBT after ZS

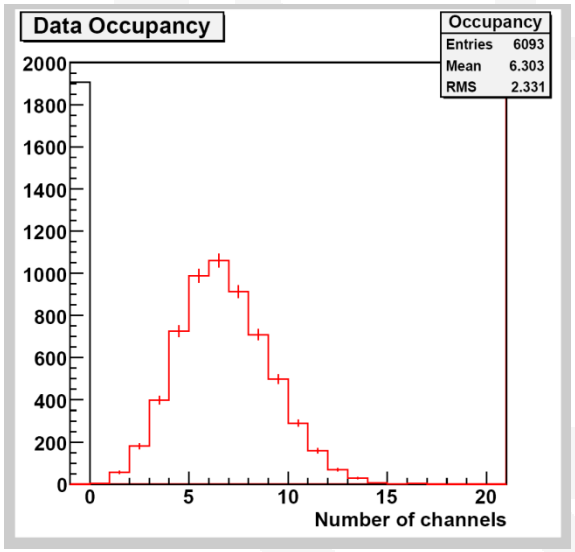
Derandomizer depth = 24

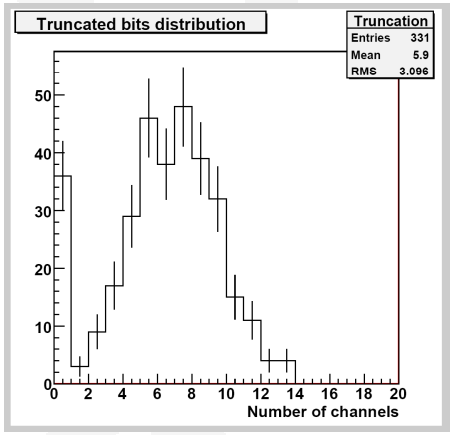
Channel size = 12

(e.g. ADDR = 5bits + ADC_DATA = 7bits)









→Truncation occurred: "raw truncation" = 5.4%

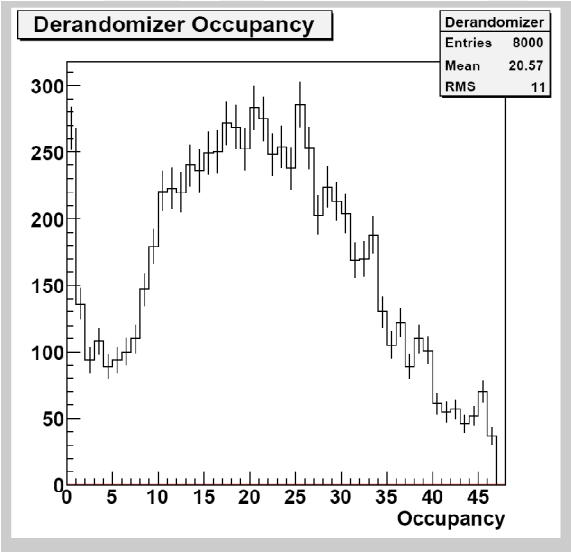
"effective truncation" = 4.7%

→ Size of truncated events follows occupancy PDF, no bias!

→ ~193kbits of data sent through one GBT link over full LHC turn: 64.4% of GBT link bandwidth + 14% Event header + 4.8% GBT header (unavoidable)

2. Results (Other examples)

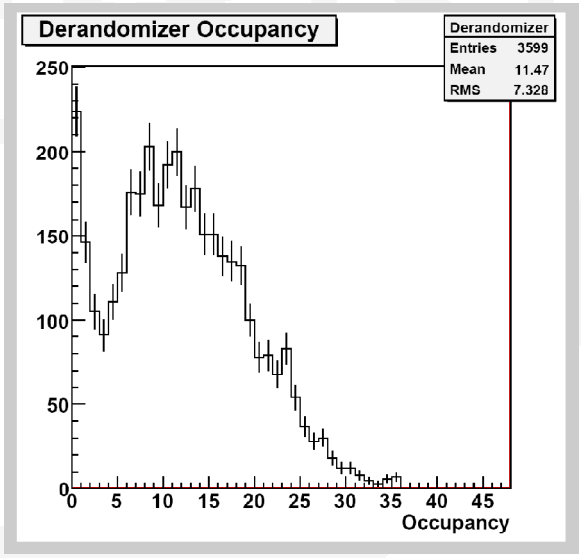
Variables applied:
<Detector occupancy> = 30%
#channels / GBT link = 21
→ ~ 6.3 channels / GBT after ZS
Derandomizer depth = 48
Channel size = 12
(e.g. ADDR = 5bits + ADC_DATA = 7bits)

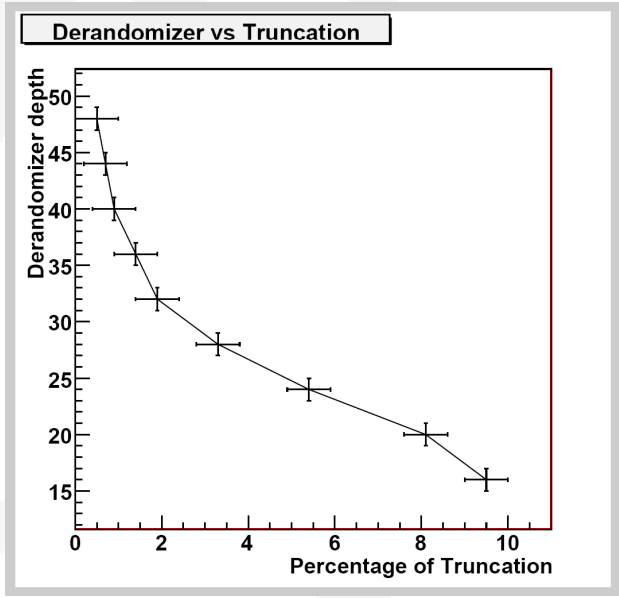


→Truncation occurred: "raw truncation" = 0.5%
"effective truncation" = 0.4%

→ ~200kbits of data sent through one GBT link over full LHC turn: 68.0% of GBT link bandwidth + 14% Event header + 4.8% GBT header (unavoidable)

Variables applied:
<Detector occupancy> = 30%
#channels / GBT link = 20
→ ~ 6.3 channels / GBT after ZS →NO Truncation occurred
Derandomizer depth = 48
Channel size = 12
(e.g. ADDR = 5bits + ADC_DATA = 7bits)





Conclusions

- We have now a *generic simulation* testbench for the Readout architecture

→ Starting point for discussion
→ Easily implement any detector design parameters and/or alternative model for ZS or data compression
→ Used to implement and verify TFC and Readout mechanisms in TFC-FE-ROB (synch checks, calibration, resets, NZS readout…
→ Already started implemented a CALO example with Jacques and Frederic: compression, packing, transmission over GBT (soon results and ZS!)

Please come to us with realistic numbers and requirements about ADC data sizes and distributions!

- Optimise FE model in VHDL (e.g. split channel data across different GBT frames, optimise buffer occupancies by merging small events together)

- Plan for the autumn is to test the TFC links with the Marseille board
- Start working on a first prototype for a TFC control board

Thanks for your attention