Technological blocks for 40 MHz readout

- Implementation
- Critical issues
- Board status
- Foreseen schedule

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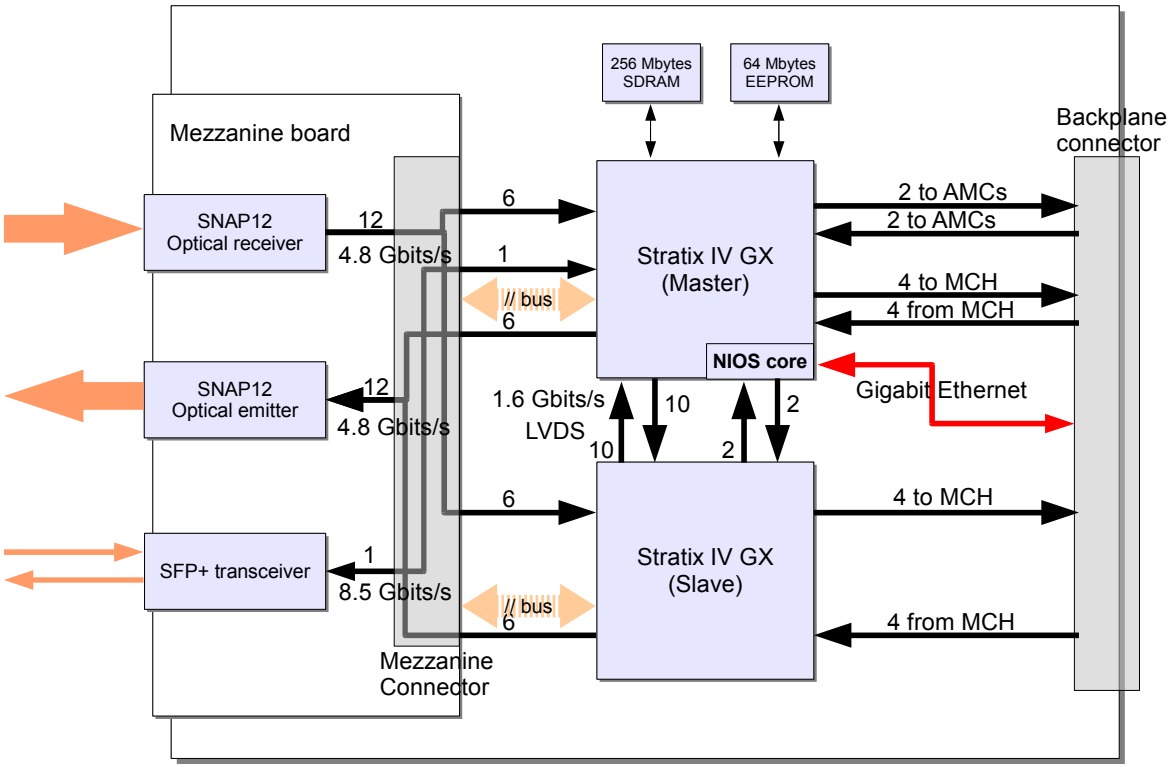
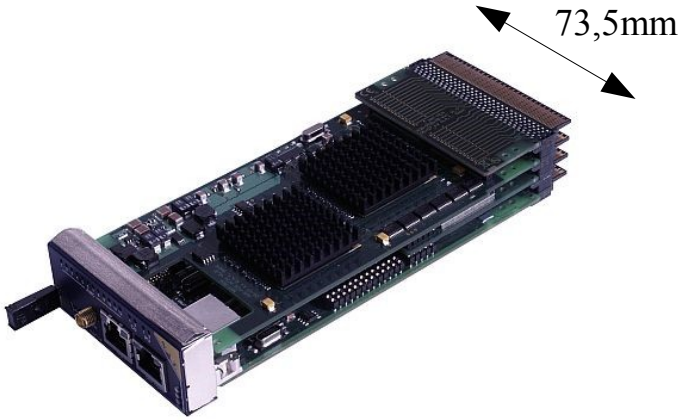
Implementation

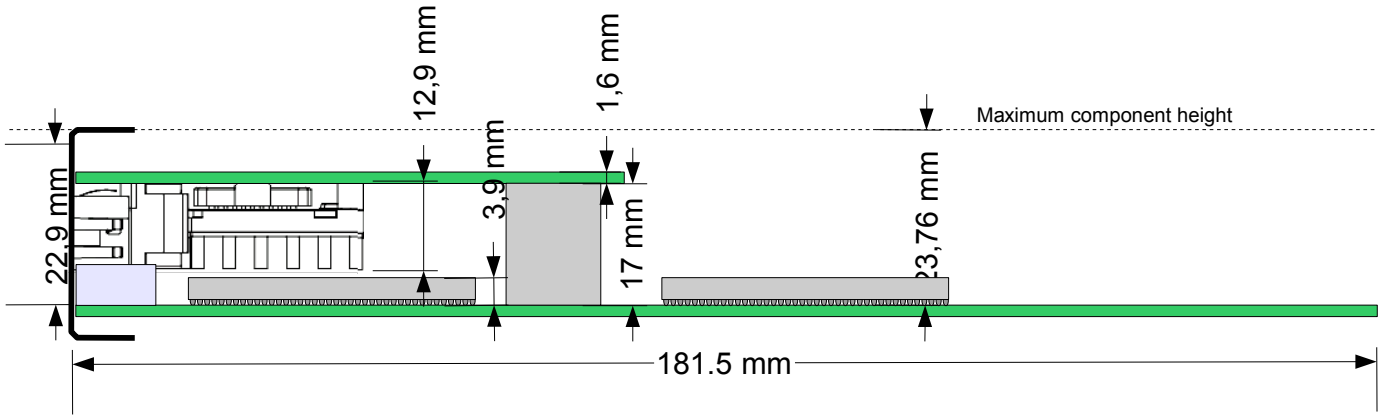
- **Main board :** 2 FPGAs Stratix IV GX
- **Mezzanine board :**
  - 1 SNAP12 receiver : 12 x 6.25 Gbits/s → emulation of GBT reception
  - 1 SNAP12 transmitter : 12 x 6.25 Gbits/s → emulation of emission toward GBT
  - 1 transceiver 8.5 Gbits/s → emulation of farm interface
    - availability of Stratix IV GT at 10-11 Gbits/s on 2010



Mechanics


ELMA


73,5mm


12,9 mm
1,6 mm
Maximum component height
22,9 mm
3,9 mm
17 mm
3,76 mm
181.5 mm

Critical issues

- **Power supplies for FPGAs :**

  25 power supplies required !!

Power supplies:

- V_{CC} : 0.9V core supply voltage
- V_{CCPT} : 1.5V power supply for programmable technology
- V_{CCPGM} : 3.0 V configuration pins power supply
- V_{CCAUX} : 2.5V Auxiliary supply for the programmable power technology
- V_{CCBat} : 2.5V Battery back up power supply (non utilisé dans ce design)
- V_{CCPD} : 3.0V I/O pre-driver (for 3.0V and 3.3V) power supply
- V_{CCPD} : 2.5V I/O pre-driver (For lower than 2.5V and equal) power supply
- V_{CCIO} : 1.8V I/O power supply
- V_{CCIO} : 2.5V I/O power supply
- V_{CCIO} : 3.0V I/O power supply
- V_{CC_CLKIN} : 2.5V differential clock input power supply
- V_{CCD_PLL} : 0.9V PLL digital power supply
- V_{CCA_PLL} : 2.5V PLL analog power supply
- V_{CCA_L} : 3.0V Transceiver high voltage power (left side)
- V_{CCA_R} : 3.0V Transceiver high voltage power (right side)
- V_{CCHIP_L} : 0.9V Transceiver HIP digital power (left side)
- V_{CCHIP_R} : 0.9V Transceiver HIP digital power (right side)
- V_{CCR_L} : 1.1V Receiver power (left side)
- V_{CCR_R} : 1.1V Receiver power (right side)
- V_{CCT_L} : 1.1V Transmitter power (left side)
- V_{CCT_R} : 1.1V Transmitter power (right side)
- V_{CCL_GXBLn} : 1.1V Transceiver clock power (left side)
- V_{CCL_GXBRn} : 1.1V Transceiver clock power (right side)
- V_{CCH_GXBLn} : 1.5V Transmitter output buffer power (left side)
- V_{CCH_GXBRn} : 1.5V Transmitter output buffer power (right side)

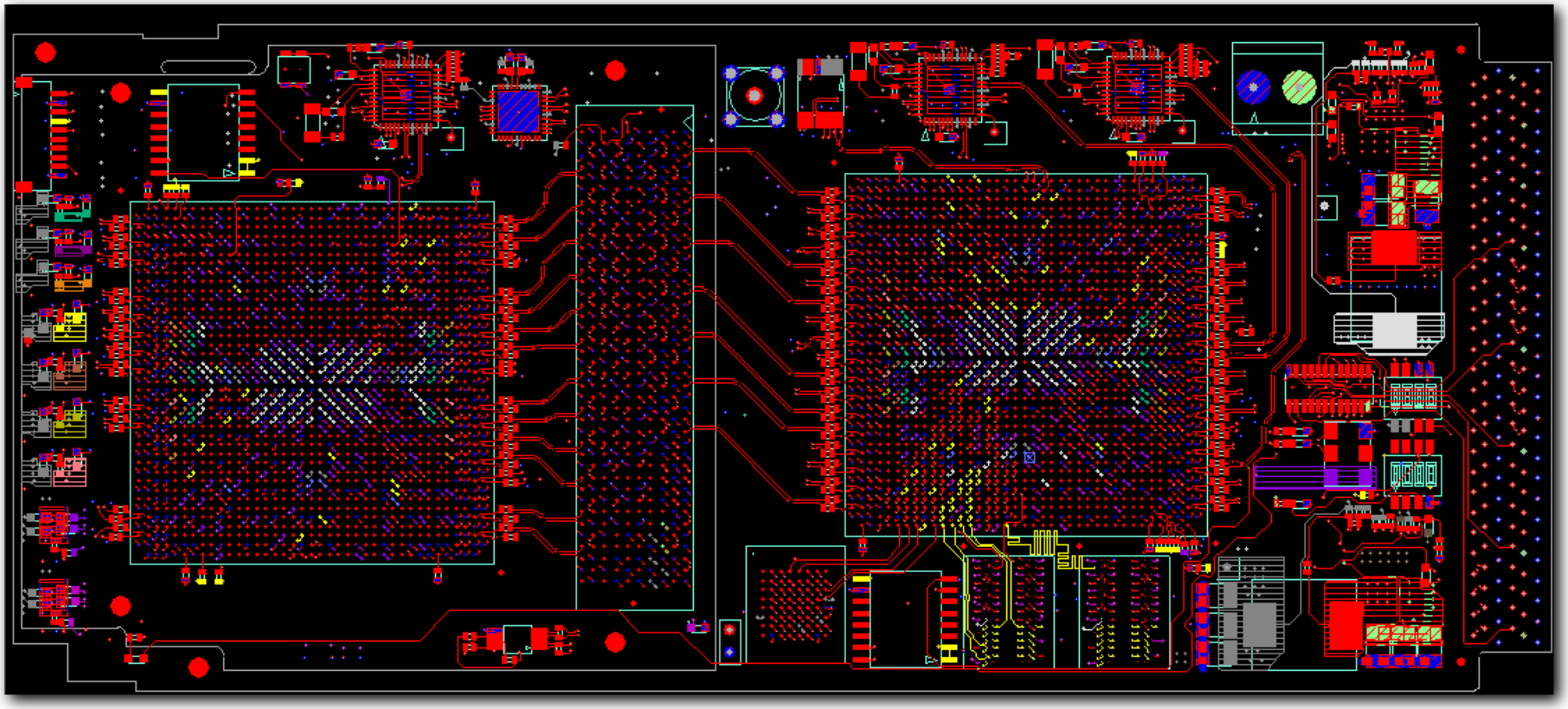
- **Decoupling scheme for FPGAs :**

  - Estimated consumption full charge = 15A for 0.9V
  - 200 decoupling capacitors required !
  - Only 75% of capacitors implemented
  - Not a problem for the prototype : limited design

    - Tests at full charge will be made to validate our decoupling scheme

Board Layout

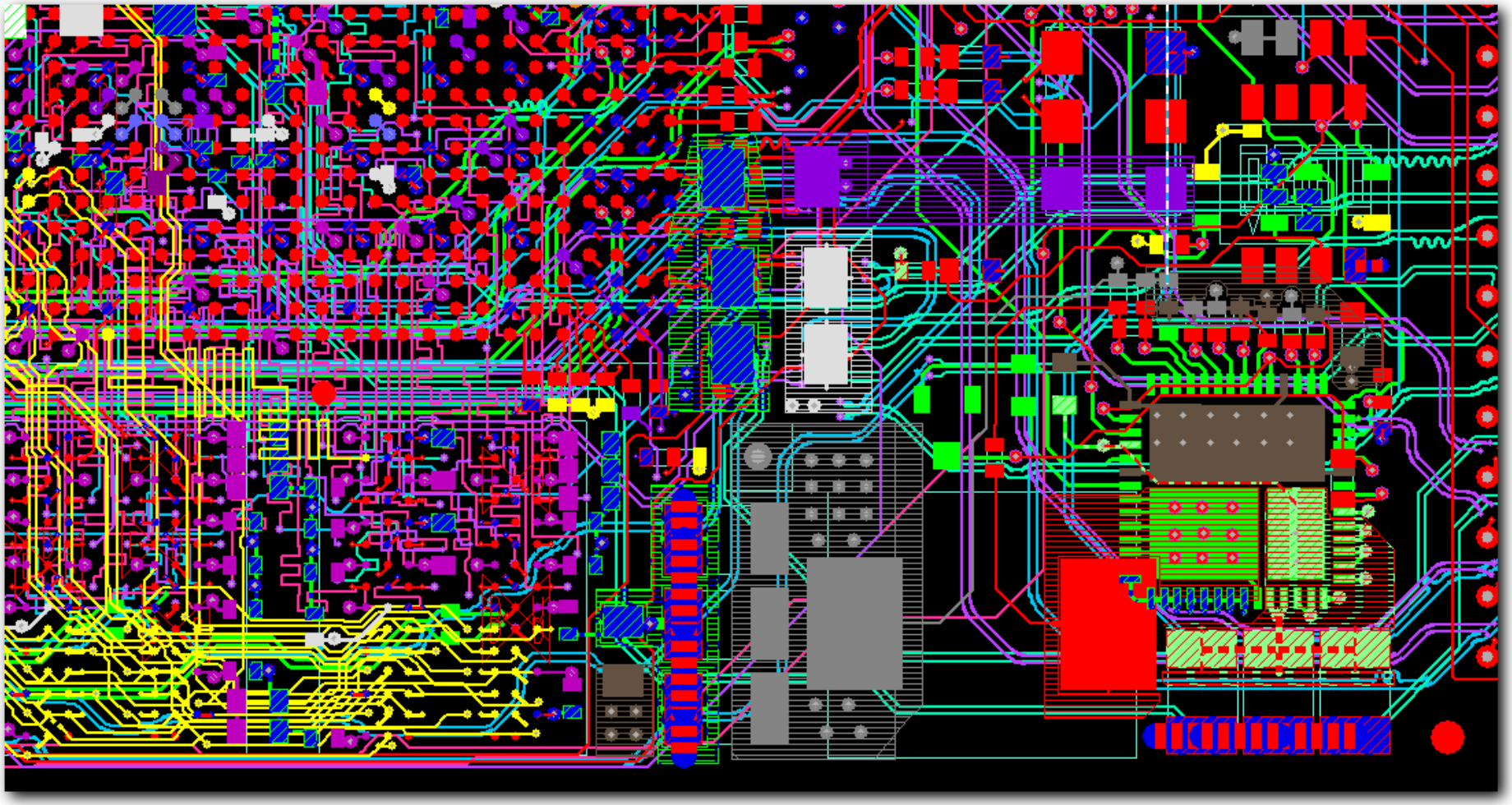
- 684 components, 2 FPGAs 1500 pins
- PCB dimension 73.5 x 181.5 mm



Prototype board top layer view

Board routing

- **Board and its mezzanine are routed: 14 layers, 900 signals, sequential PCB (buried and laser vias)**



Foreseen schedule

- November : **PCB manufacturing**
- December/January : **cabling**
- **Start debug** : mid January
- **First measurements** and results : Early March

Conclusion

- This board will allow us to test :

  - GBT protocol compliance at 4.8 Gbits/s

  - Signal integrity on copper through mezzanine connector up to 8.5 Gbits/s in and out

  - Density issues for implementing large FPGAs

- With this board we are able to validate all technologies required by the 40 MHz read-out board

- By the end of 2010 we will develop a prototype of the 40 MHz board with:

  - A 10 Gbits/s implementation

  - A form factor suitable for LHCb