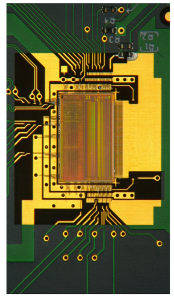
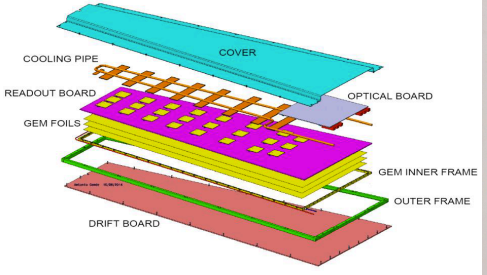
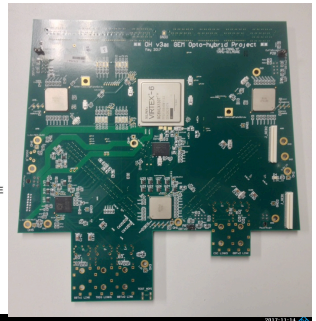
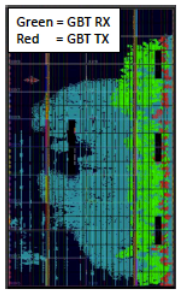
# Lessons learned from GE1/1

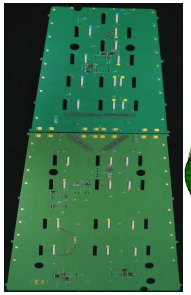
G. De Lentdecker (ULB)

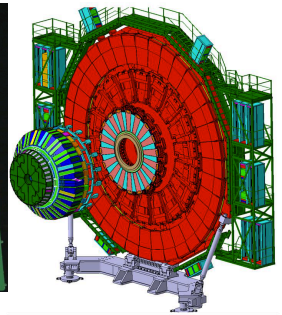


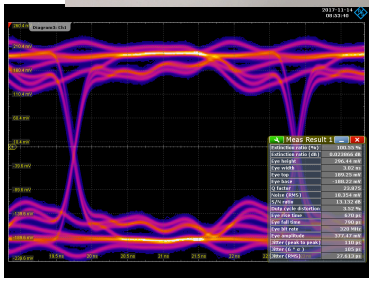






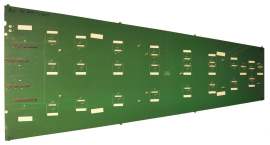


# Content

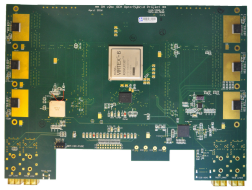
- GE1/1 achievements
- GE1/1, GE2/1 & ME0 common points
- Lessons learned
  - VFAT3 hybrid design
  - GEB design
  - OH design
  - Mechanics, power, …

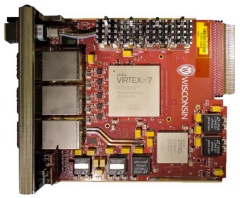
# GE1/1 prototyping steps

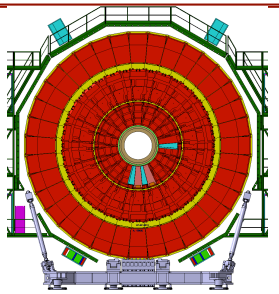
Prototype 2a (2015):
Full size GEB (one piece)
VFAT2
Opto-hybrid with Virtex-6, emulating GBT protocol
Back-end: GLIB board
Applications: Test Beam



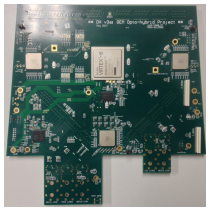
Prototype 2b (2016):
Full size GEB (one piece)
VFAT2
Opto-hybrid with Virtex-6 + 1 GBT + 1 SCA, VTTx and VTRx
Back-end: GLIB and CTP7 boards
Applications: Slice Test

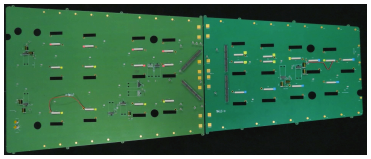


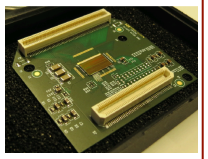




Prototype 3a (Q3 2017):
Full size GEB (two pieces)
VFAT3a
Opto-hybrid with Virtex-6 + 3 GBT + 1 SCA, VTTx and VTRx
Back-end: CTP7 boards



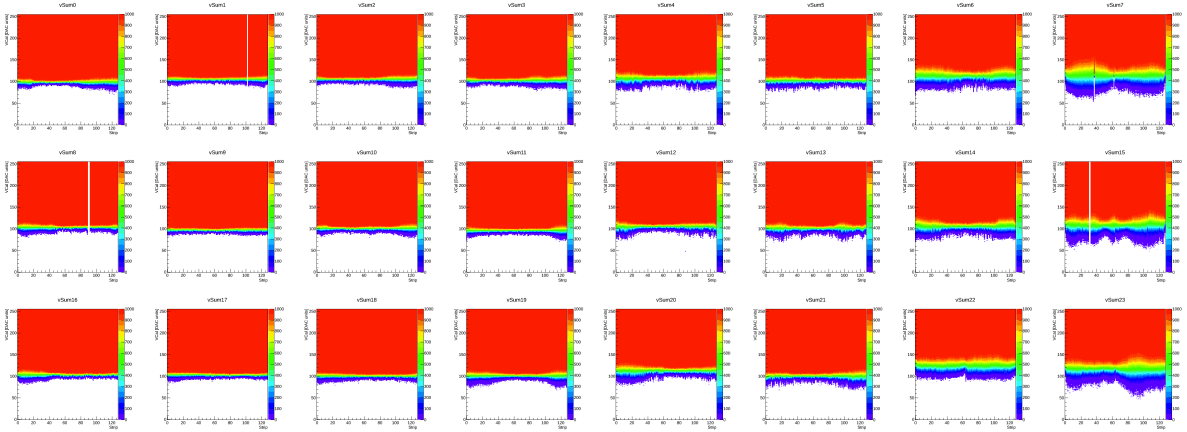




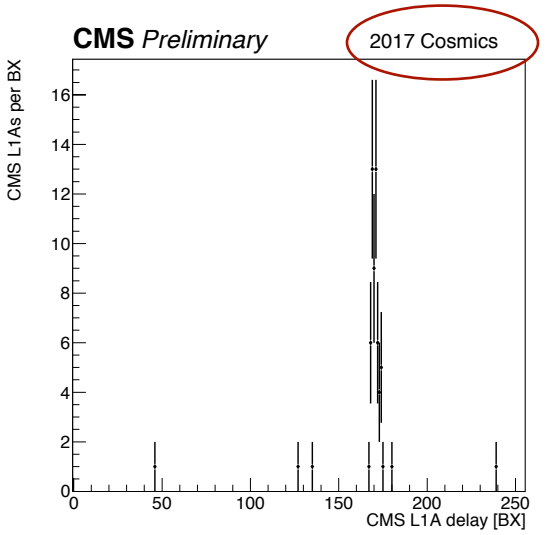
Prototype 3b (Q1 2018):
Full size GEB (two pieces)
VFAT3b
Opto-hybrid with Virtex-6 + 3 GBT + 1 SCA, VTTx and VTRx
Back-end: CTP7 boards
Applications: LS2

# Achievements: GEMs in P5

- 5 x v2 super-chambers since January 2017
  - VFAT2, Opto-Hybrid v2b (1 GBT+ 1 SCA)
  - In global runs since Nov. 2017.



S-curve after trimming of one chamber in P5



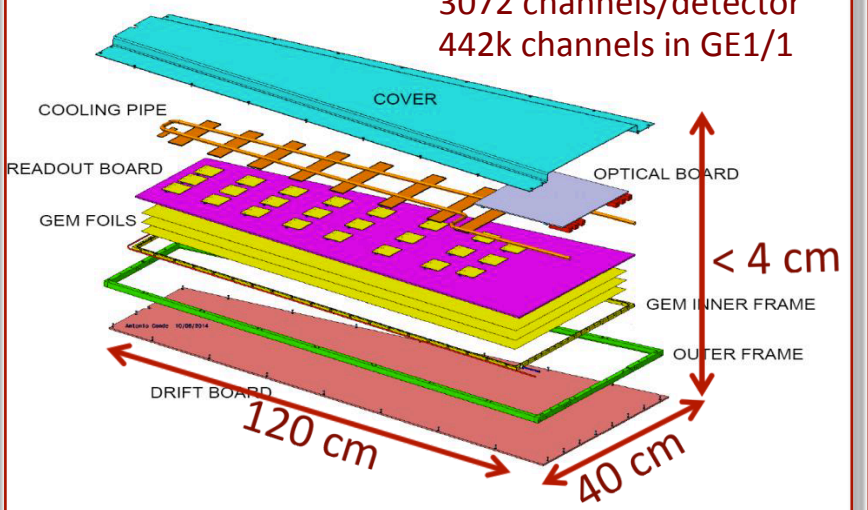

Latency scan

- 1 x v3 super-chamber since February 2018
  - Replacing one v2 super-chamber (Multi-channel HV)
  - VFAT3b, Opto-Hybrid v3 (3 GBT+ 1 SCA), FEAST, …

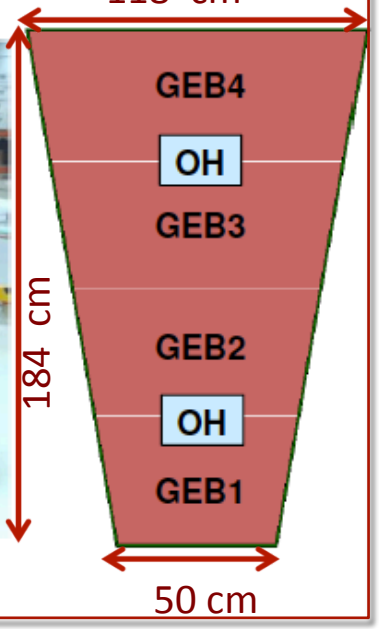
# CMS Triple-GEMs

## GE1/1 Triple-GEM

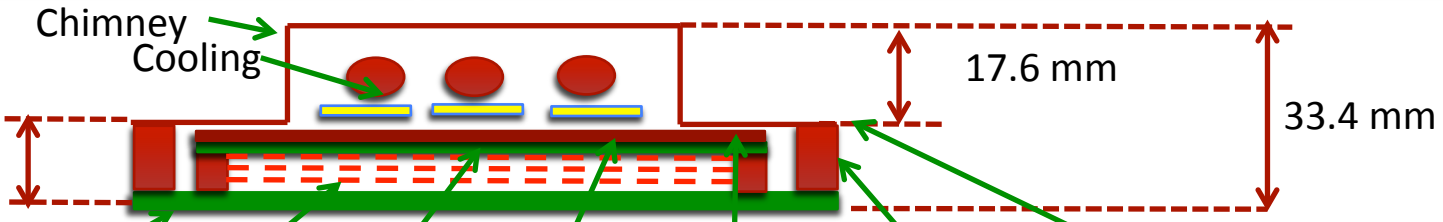
3072 channels/detector
442k channels in GE1/1




## GE2/1 Triple-GEM


## ME0 Triple-GEM




*GE2/1 & ME0 mechanic details, See Michele's talk*

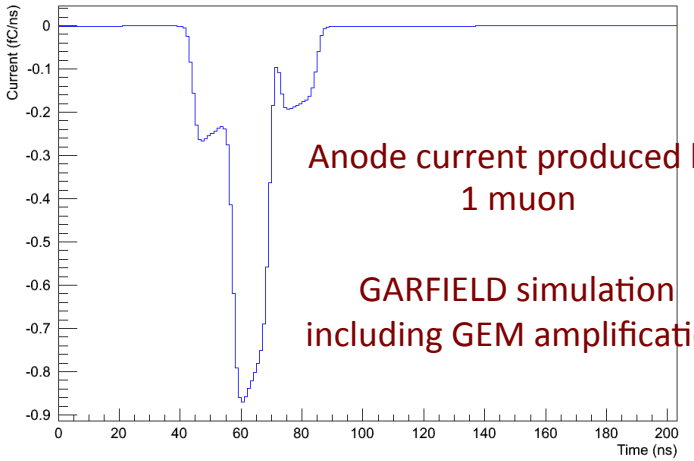
Drift 3.0 mm Stack 7.2 mm | GEBs 1.2 mm | Alu Frame 11.8 mm | Chimney 1 mm

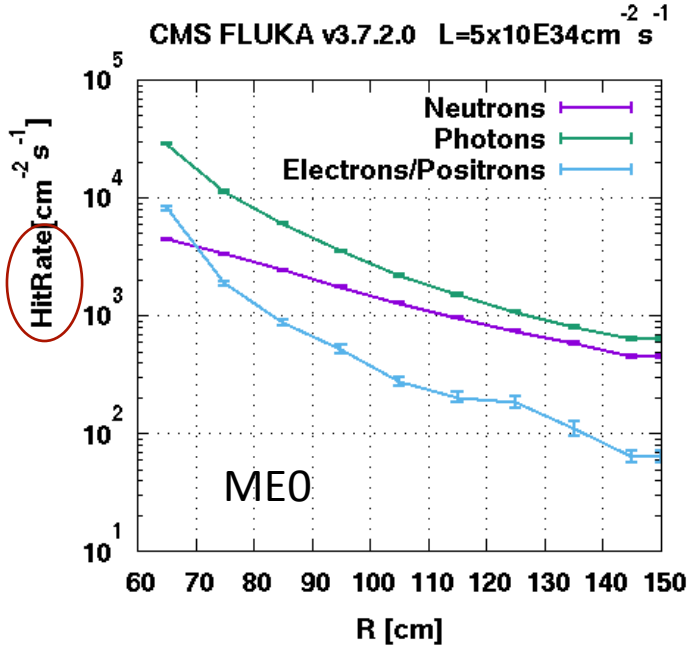
RO 3.0 mm | Clearance 0.4 mm

# GE2/1 and ME0 electronics requirements

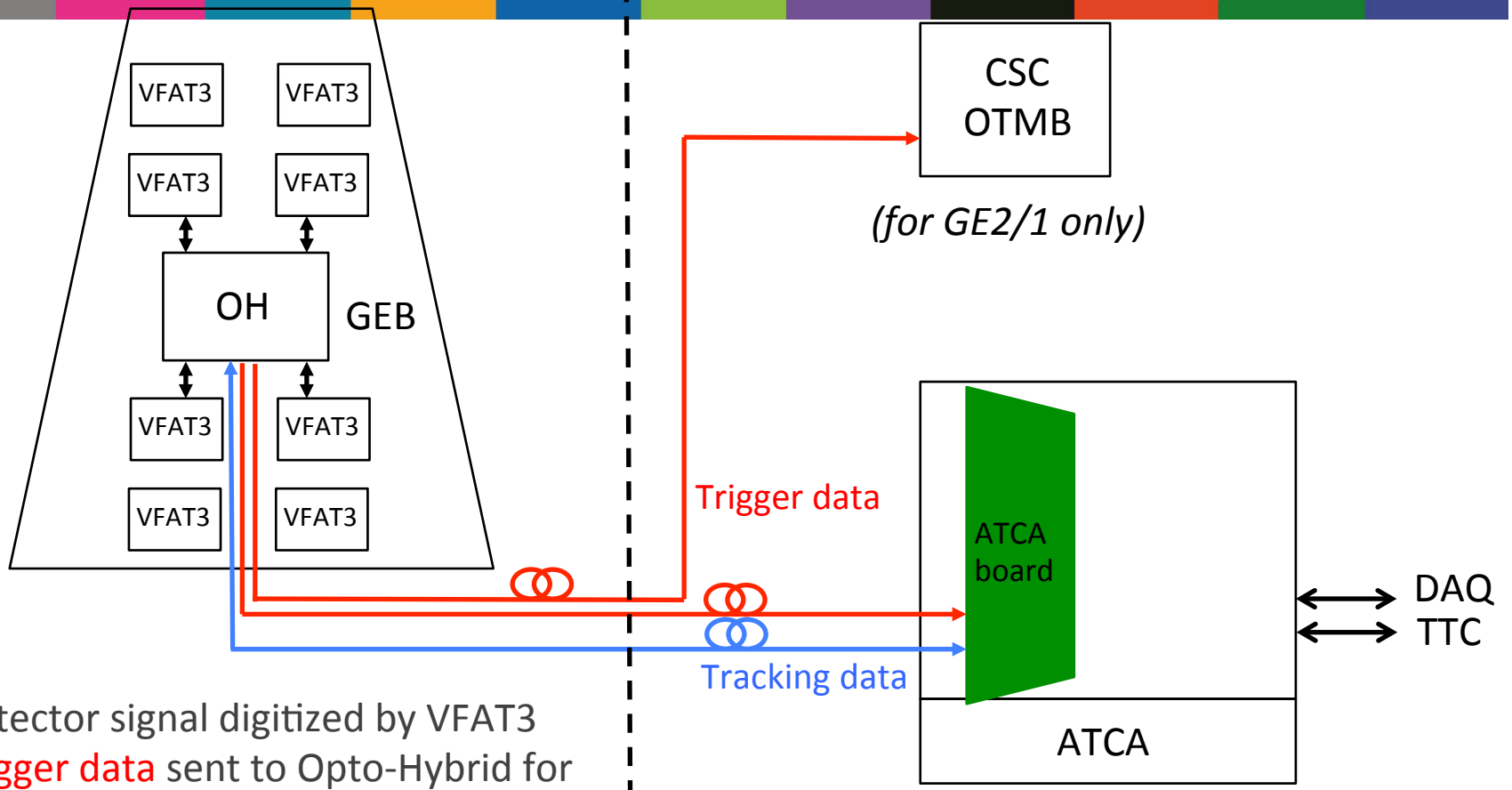
- CMS Triple-GEM
  - signal length: ~60 ns
  - detector capacitance > 30 - ? pF
  - charge range (MIP): 4-110 fC

    *More details on capa. & charge in Marcus' talk tomorrow*
- Expected particle rate
  - GE21: similar to GE11 (a few kHz/cm$^2$)
  - ME0: up to ~5MHz/cm$^2$ (one order higher than GE11)
- CMS Level-1 latency: 12.5 µs
- CMS Level-1 Accept rate: 750 kHz
- Total irradiation dose:
  - 5 krad - 1 Mrad (10 krad in GE11)



# Overview of the GEM electronics system



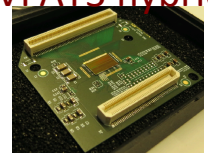

- Detector signal digitized by VFAT3
- Trigger data sent to Opto-Hybrid for cluster finding (+1 link to OTMB in GE21)
- Tracking data, slow ctrl and clock are handled by LpGBT

- Baseline plan based on CTP7-like ATCA board
- Running local trigger
- Event building and sending to DAQ

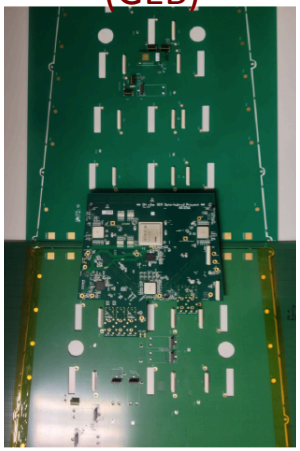
# GE1/1 Electronics overview

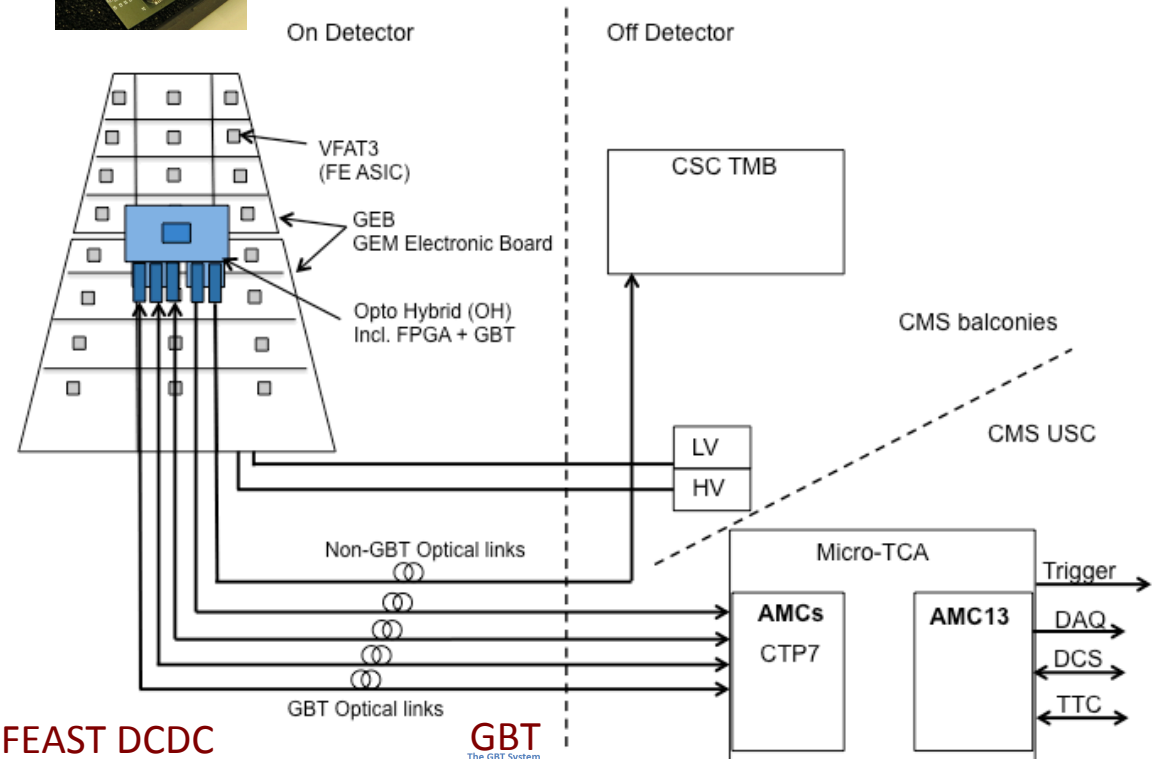
Use of many common developments such as GBT, Versatile Link, CTP7 and FEAST

VFAT3 hybrid

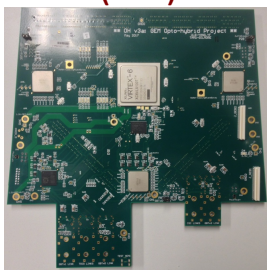


GEM Electronic Board (GEB)

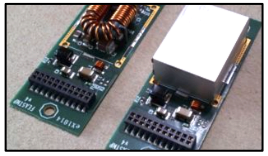




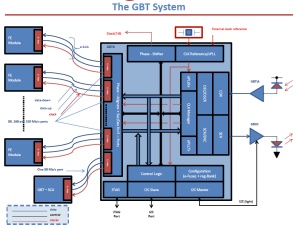

Opto-Hybrid (OH)



FEAST DCDC



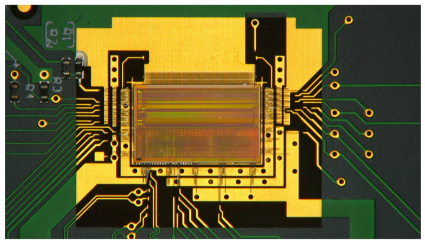
GBT




CTP7

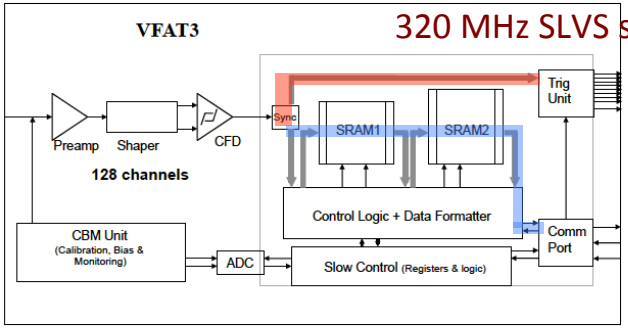
# VFAT3 & GE1/1 VFAT3 hybrid

**VFAT3**



**Some features**:

- Binary chip
- 320 MHz
- L1 latency: up to 12 µs
- Slow control: ePort, GBT compatible
- Trigger data:
  - 1bit= OR of 2 strips (+DDR option)

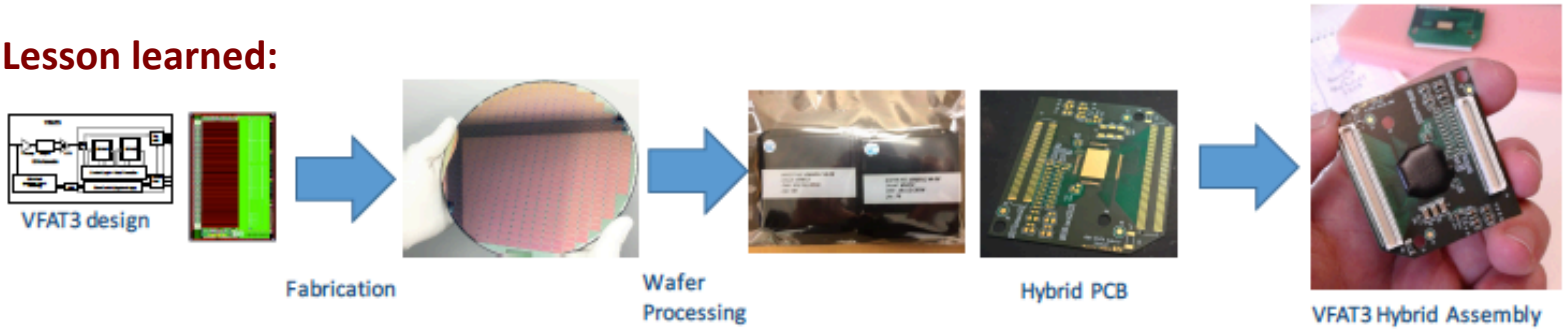



320 MHz SLVS signals:

Trigger data

Tracking data (upon L1A)

**Lesson learned:**



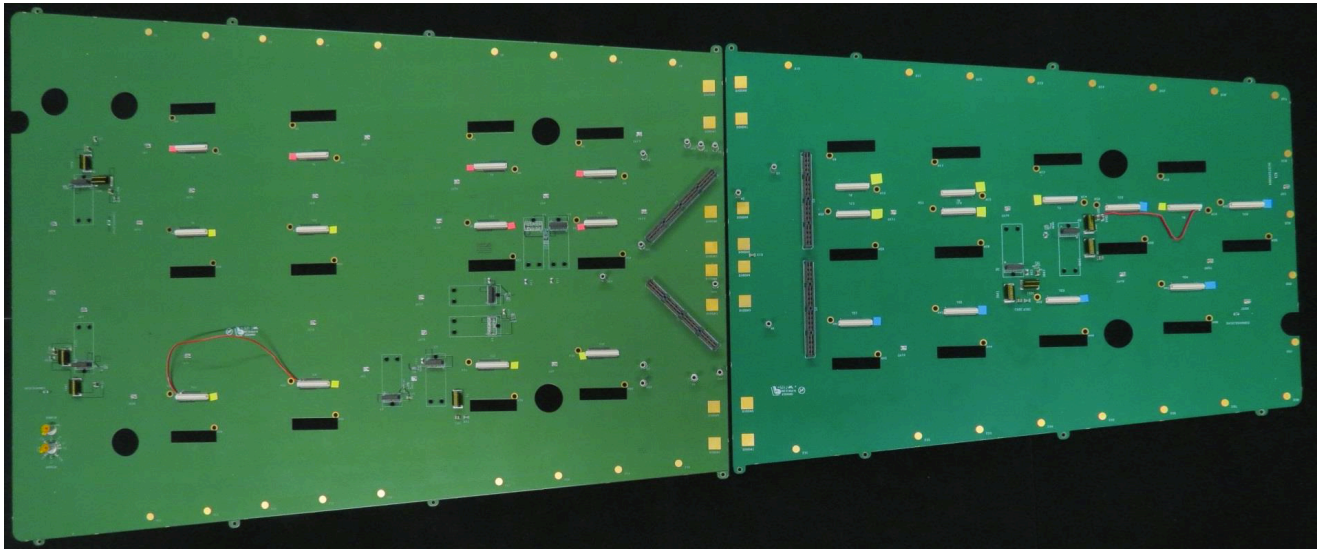

This procedure is complicated and difficult to do. At the limit of industrial capabilities.

Preference is to package VFAT3 for future use.

*VFAT3 details, see Paul's talk*

# The GEB board

The GEB
- 8-layer PCB
- Carry signals between VFAT3s and OH
- Carry power from FEASTs to VFAT3 and OH

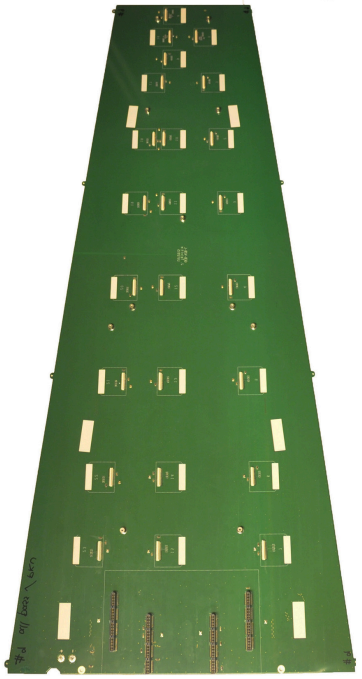


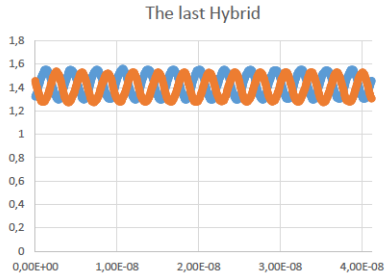

On paper it looks like just a passive PCB carrying signals, providing power and ground but it is much more complex:
- large number of connections (~500 differential signals, 10 FEASTs, AGND & DGND to every VFAT3)
- tight mechanical constraints
  - limited thickness ~1mm -> limited number of layers
  - Flatness
  - Many connectors -> mechanical stress

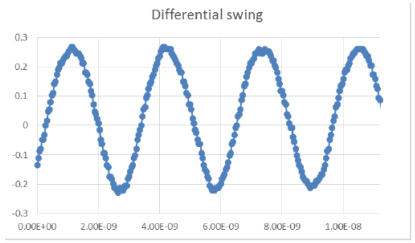
# GEB lesson learned

- Manufacturing >1m long PCB
  - At the limit of industrial capabilities
  - Very few companies can manufacture 120 cm long PCBs
    - Expensive, yield issues
  - Concerns about signal integrity
    - Reminder, we use 320 MHz SLVS signals
    - An example of a clock signal with 320 LVDS:

1 piece GEB
(Slice Test)





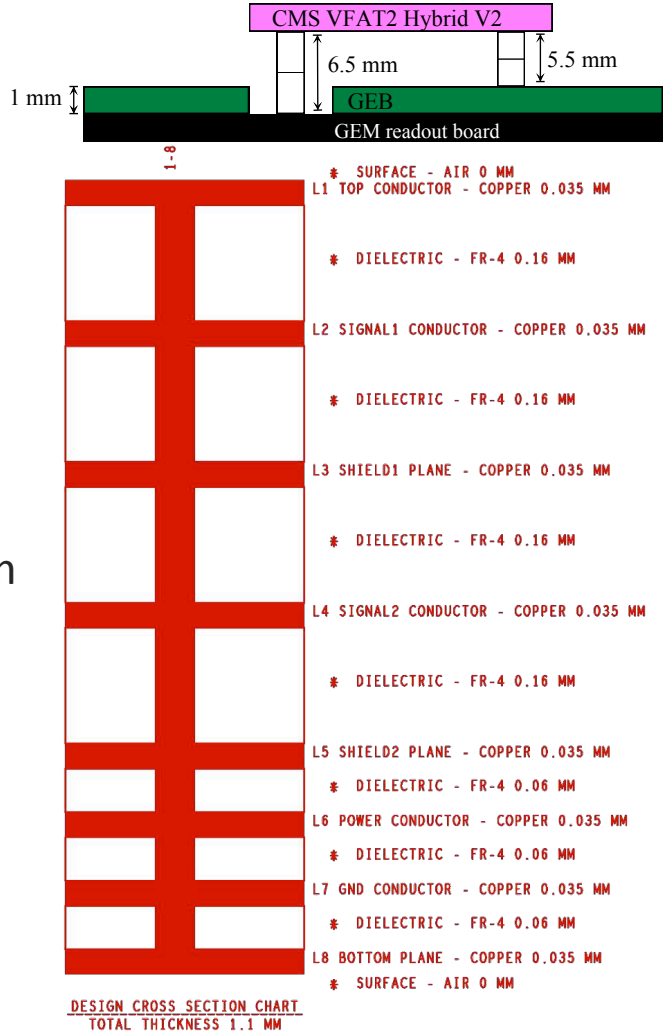

- Note: we did not investigate further but rather design a split GEB for GE1/1

# GEB lesson learned

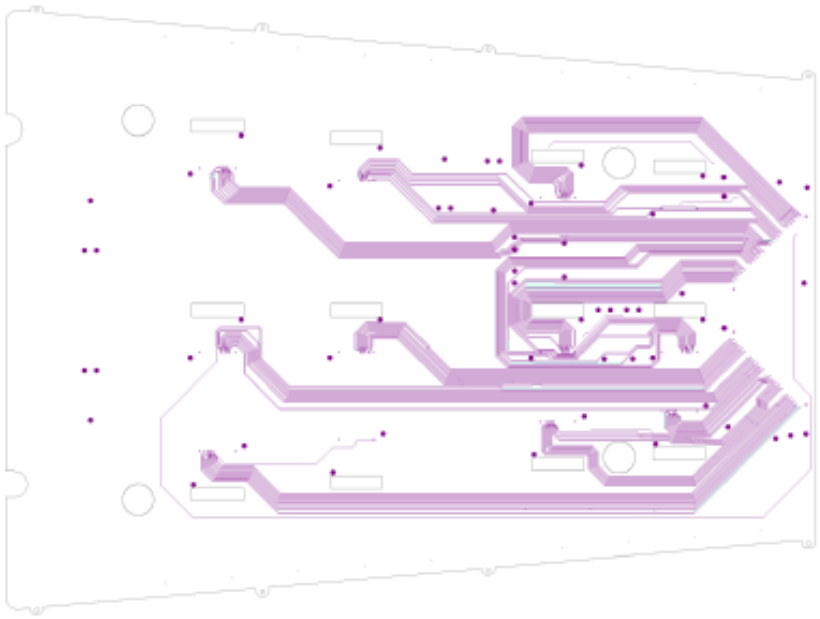
- GEB thickness limited to ~1mm
  - Limited number of layers in PCB
    - 1 power plane
    - 1 GND plane
    - 2 signal layers
    - 1 shield layer
      - This shield layer between GEB signal lines and Read Out Board (ROB) was added from our Slice Test experience

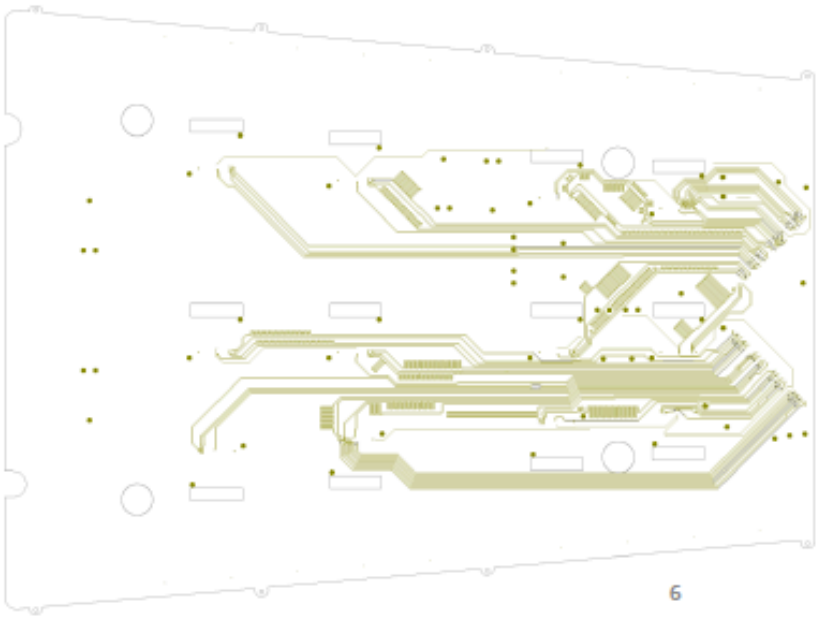
*More on Grounding in Cameron & Brian's talk tomorrow*

- Matching signal lines lengths for VFAT3s synchronization

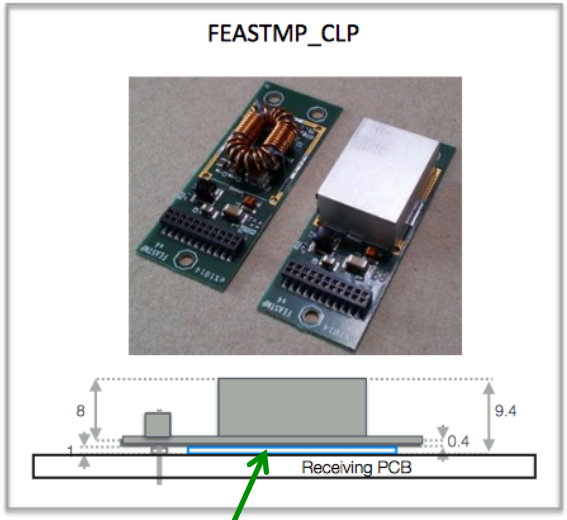


# GEB signal layers





# Power

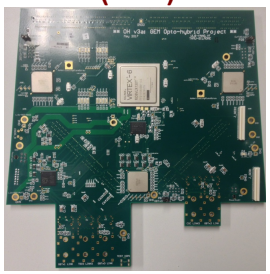


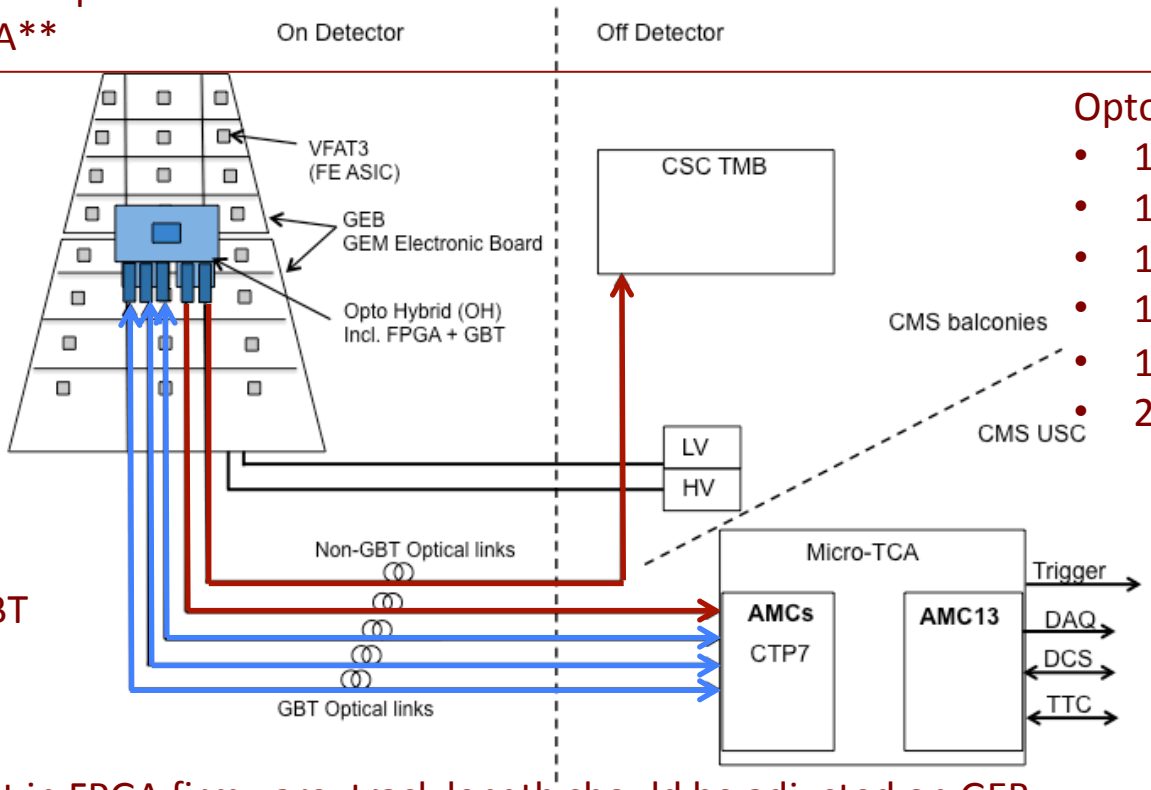

- All the FE components are powered from FEASTs
  - 4 x 1.2 V for 24 VFATs
  - 6 for OH
- Some key features of the FEASTS:
  - Input voltage: 5 to 12 V
    - Need an Enable Voltage (3 V)
  - Limited output current: 4A
  - Limited output power: 10 W
  - Maximum temperature: ~75°C
    - Beyond, FEAST shutdowns by itself
    - Need good contact with cooling; cooling from the bottom of the PCB
    - In GE1/1, FEAST are placed up-side down (see next page)
    - If you want to modify the PCB (to enlarge the holes or whatever) it is at your charge

# Opto-Hybrid (OH)

The Trigger data (FastOR) from 24 VFAT3s represent 61.44 Gbps => requires on-detector procesing*
In addition these data have to be transmitted to existing CSC Trigger Mother Board (oTMB) which is not compatible with GBT speed.
=> Need OH with FPGA**

Opto-Hybrid (OH)






Opto-Hybrid powering:

- 1.0 V, 2A
- 1.0 V, 4A
- 1.2 V, 2A
- 1.5 V, 3.5 A
- 1.8 V, 1A (EEPROM)
- 2.5 V, 3A

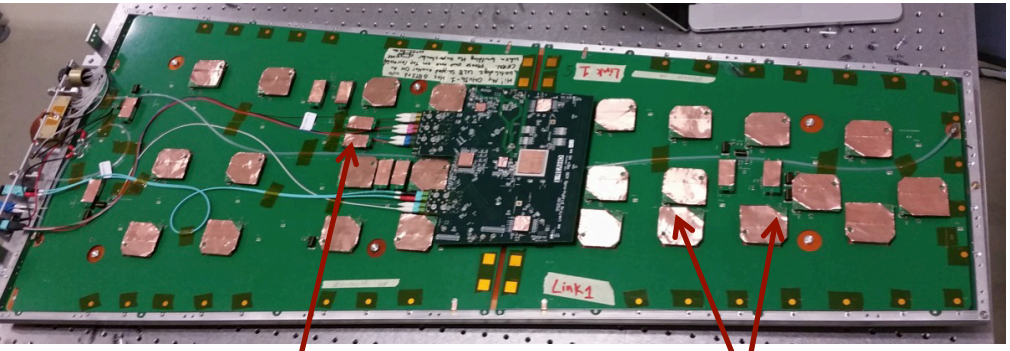
3 GBT*** links + 2 No-GBT links

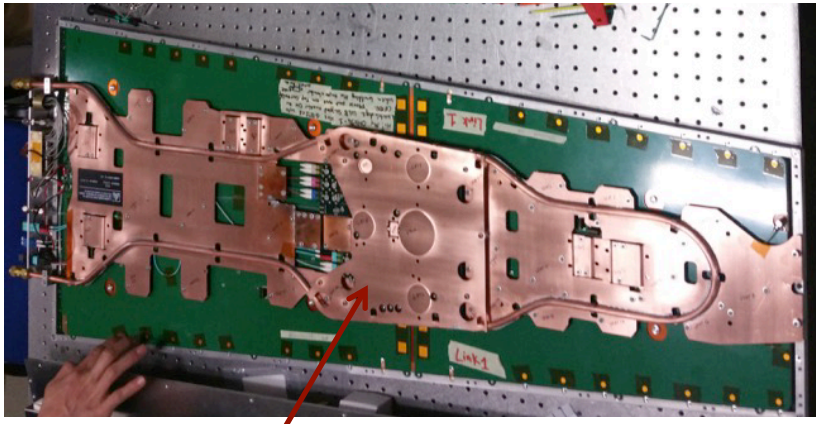
*To relax time adjustment in FPGA firmware, track length should be adjusted on GEB

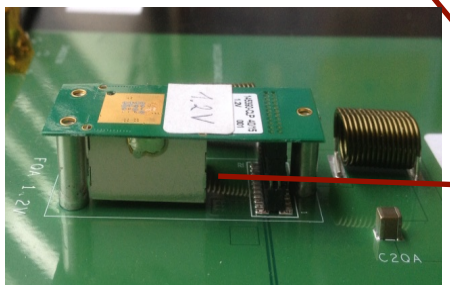
*** 1GBT can handle up to 10 VFAT3 ** Chosen FPGA (Virtex-6) is the same as used on CSC ME1/1 chambers

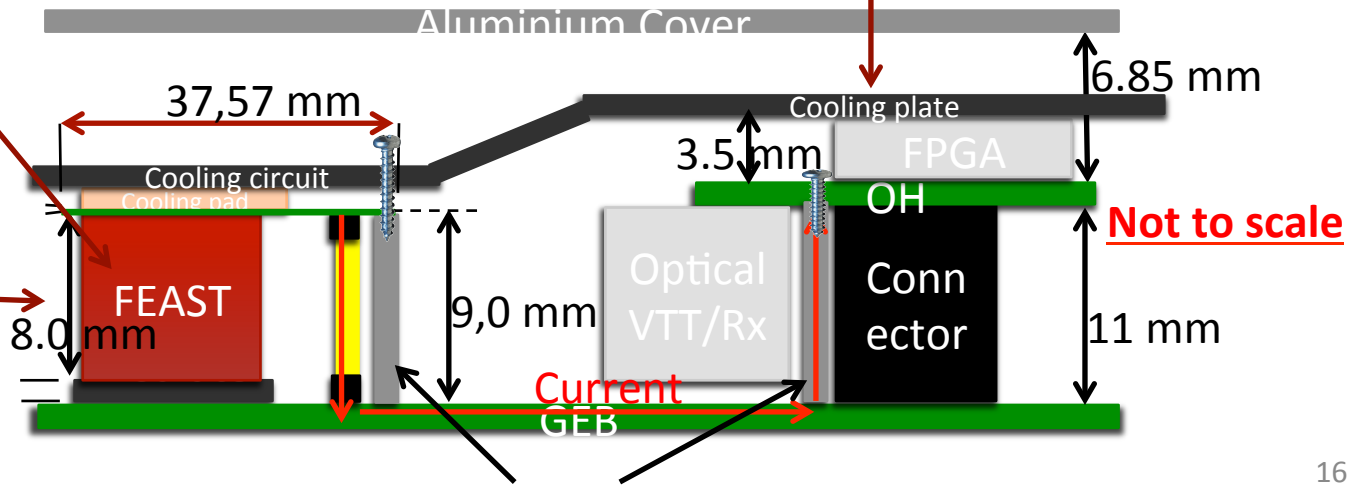
# Mechanics

With cooling plate:



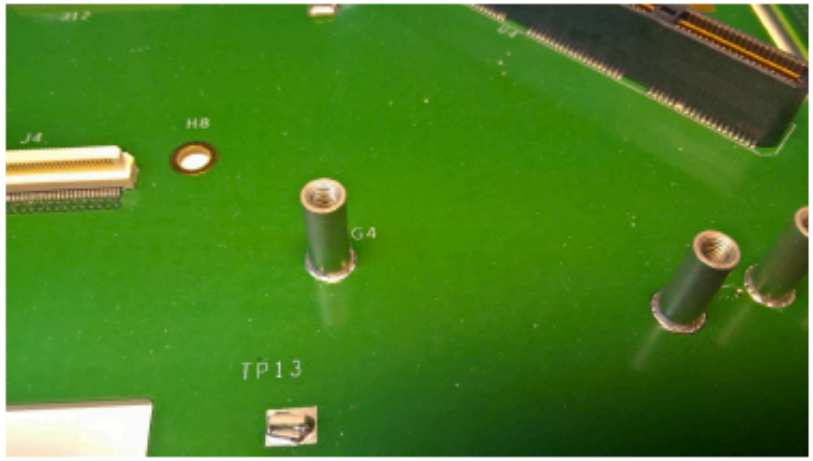





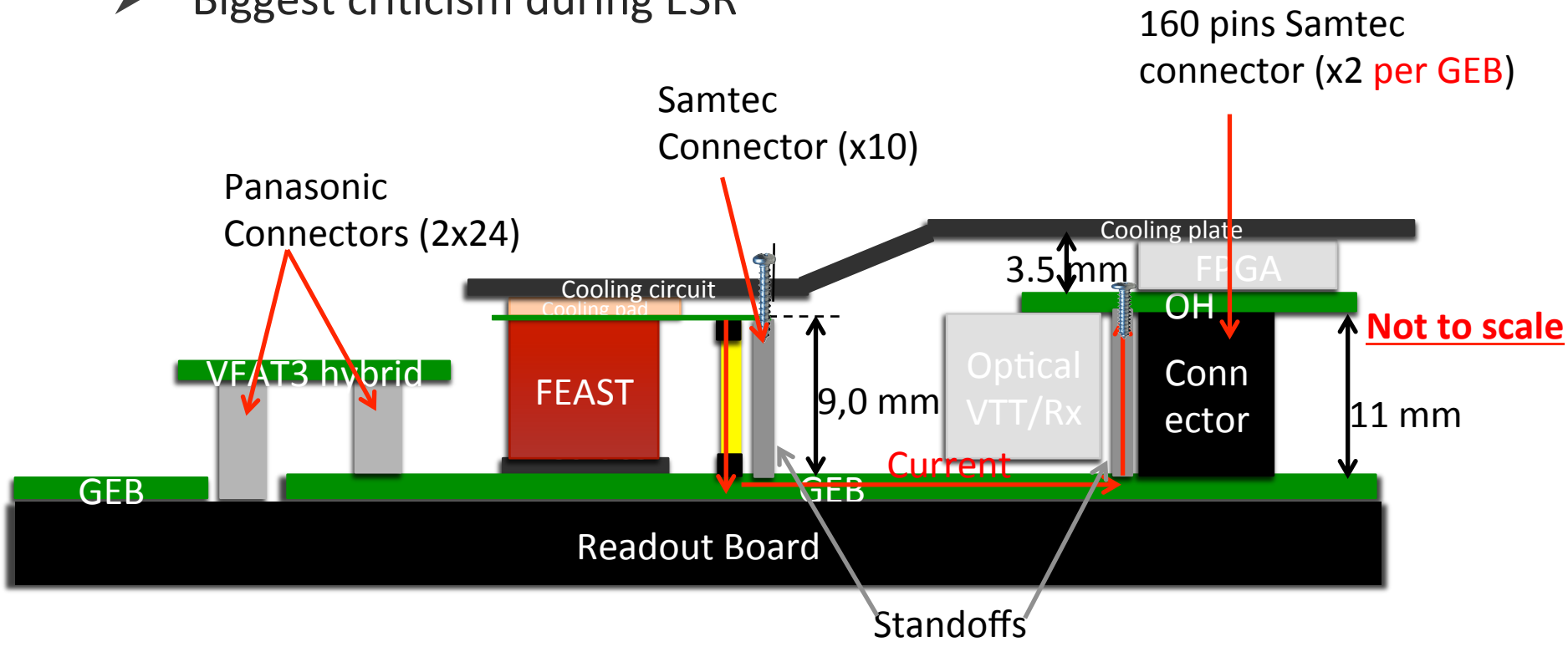
# Mechanics

- Many screws (90)
  - Some very small (M2 for FEAST)
- Standoffs are fragile
  - Difficult to solder
    - Some connected to GEB GND
  - Reinforced with Araldite



# Mechanics

- (Too) many connectors
  - Biggest criticism during ESR



# Other lessons

- Choose common design software (cadence/altium)
  - To allow other designers to review the designs
- Use repository and versioning to store and share design files
  - Keep track of changes

# Conclusions

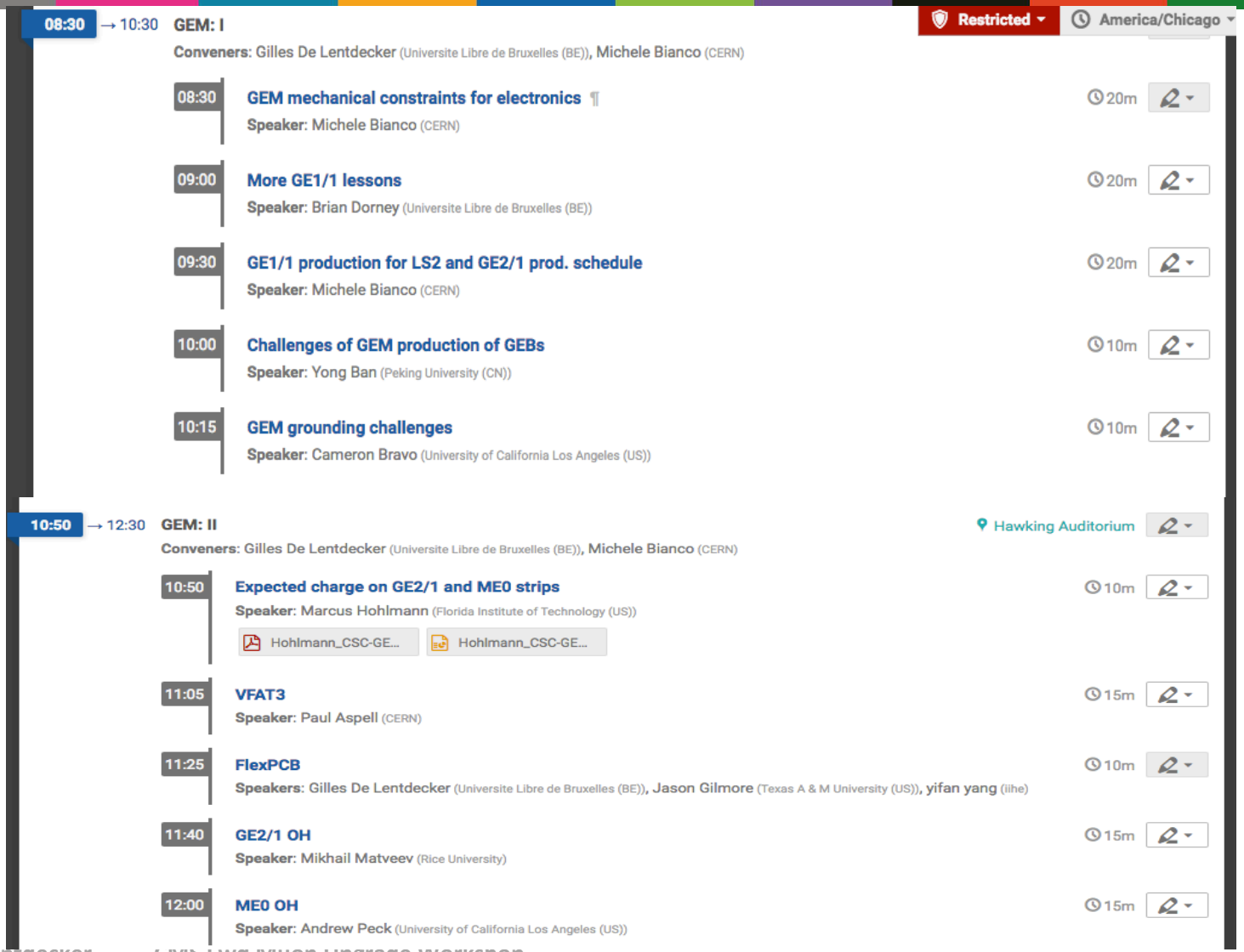
- Although GE2/1 and ME0 baseline is
  - LpGBT
  - Packaged VFAT3
  - FlexPCB

first GE2/1 prototypes will very much look like GE1/1 (in much larger)

- 4 GEBs with many mechanical constraints and many interfaces will require several prototype iterations

| | date | milestone description | status |
|---|---|---|---|
| **GE2/1** | 21 Mar 2017 | Key detector system design parameters are defined based on performance requirements | achieved |
| | 19 Jun 2017 | On-chamber electronics preliminary design completed and interfaces defined | achieved |
| | 12 Mar 2018 | Off-chamber electronics preliminary design completed and interfaces defined | on track |
| | 1 May 2018 | A full size GE2/1 prototype with partially instrumented readout built and tested | on track |
| | 8 May 2018 | Det. design parameter optimization completed, final design selected for demonstrator | on track |
| | 1 Jun 2018 | On-chamber electronics prototypes engineering design complete | on track |
| | 3 Aug 2018 | → GE2/1 PRR for the On-Detector Services | on track |
| | 18 Oct 2018 | On-chamber electronics prototype electronics manufacturing and testing is complete | on track |
| | 13 Nov 2018 | → GE2/1 PRR for the Foil Production | on track |
| **ME0** | 21 Mar 2017 | Key detector design parameters are defined based on performance requirements | achieved |
| | 11 Jun 2017 | Irradiation studies, assessment of performance/longevity with small prototypes completed | achieved |
| | 25 Jul 2017 | On-det. & off-det. electronics preliminary design complete and interfaces defined | achieved |
| | 18 Dec 2018 | Chamber (stack) prototype mechanical design completed | on track |

# More details tomorrow



08:30 → 10:30 **GEM: I** — Restricted — America/Chicago

**Conveners**: Gilles De Lentdecker (Universite Libre de Bruxelles (BE)), Michele Bianco (CERN)

| | | |
|---|---|---|
| 08:30 | **GEM mechanical constraints for electronics** ¶<br>**Speaker**: Michele Bianco (CERN) | 20m |
| 09:00 | **More GE1/1 lessons**<br>**Speaker**: Brian Dorney (Universite Libre de Bruxelles (BE)) | 20m |
| 09:30 | **GE1/1 production for LS2 and GE2/1 prod. schedule**<br>**Speaker**: Michele Bianco (CERN) | 20m |
| 10:00 | **Challenges of GEM production of GEBs**<br>**Speaker**: Yong Ban (Peking University (CN)) | 10m |
| 10:15 | **GEM grounding challenges**<br>**Speaker**: Cameron Bravo (University of California Los Angeles (US)) | 10m |

10:50 → 12:30 **GEM: II** — Hawking Auditorium

**Conveners**: Gilles De Lentdecker (Universite Libre de Bruxelles (BE)), Michele Bianco (CERN)

| | | |
|---|---|---|
| 10:50 | **Expected charge on GE2/1 and ME0 strips**<br>**Speaker**: Marcus Hohlmann (Florida Institute of Technology (US))<br>Hohlmann_CSC-GE... Hohlmann_CSC-GE... | 10m |
| 11:05 | **VFAT3**<br>**Speaker**: Paul Aspell (CERN) | 15m |
| 11:25 | **FlexPCB**<br>**Speakers**: Gilles De Lentdecker (Universite Libre de Bruxelles (BE)), Jason Gilmore (Texas A & M University (US)), yifan yang (iihe) | 10m |
| 11:40 | **GE2/1 OH**<br>**Speaker**: Mikhail Matveev (Rice University) | 15m |
| 12:00 | **ME0 OH**<br>**Speaker**: Andrew Peck (University of California Los Angeles (US)) | 15m |

# Backup

# GE2/1 Timeline

- GE2/1 chambers are foreseen to be installed into CMS during the EYTS 2022 and 2023 (one disk per year)
- Module pre-production is expected to start at the end of GE1/1 chamber production, end 2018, right after the EDR
- First GE2/1 electronics prototype (OH + GEB): Q2 2018
- Q3-Q4 2018: design second version (design & tests)
- Q1 2019: Validation with demonstrator
- 2019-2020:
  - final design
  - test & pre-prod.
  - prod

# MEo Timeline

- ME0 chambers are foreseen to be installed in to CMS during LS3 (2024-2025)
- Module pre-production is expected to start beginning 2021
- First ME0 electronics prototype (OH + GEB) by end of 2019
- 2020: second version (design & tests)
- 2021:
  - Q1: final design
  - Q2-Q3: test & pre-prod.
  - Q4: prod