CSC Electronics Upgrade – Overview and Open Questions

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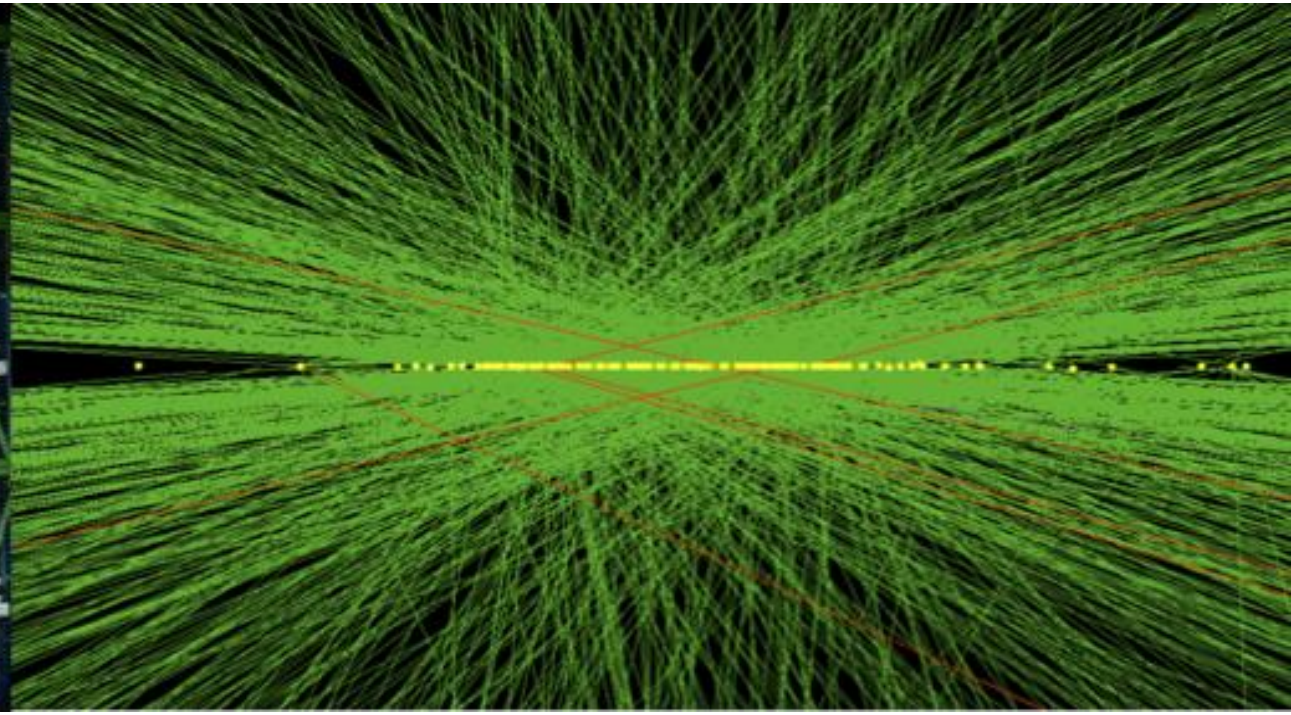
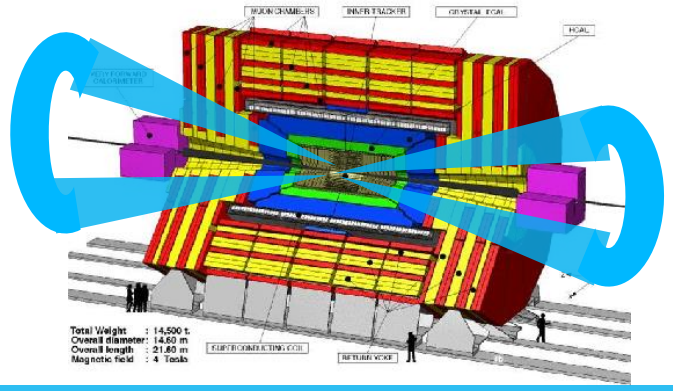
CSC/GEM Electronics workshop, TAMU 09-Apr-2018



Outline

- Overview
  - LS2, “on chamber electronics”
  - LS3, “off chamber electronics”
- Open questions
  - Not be be discussed exhaustively during this talk
  - Frames some goals for the week

CSC on-chamber electronics upgrades (LS2 Scope)

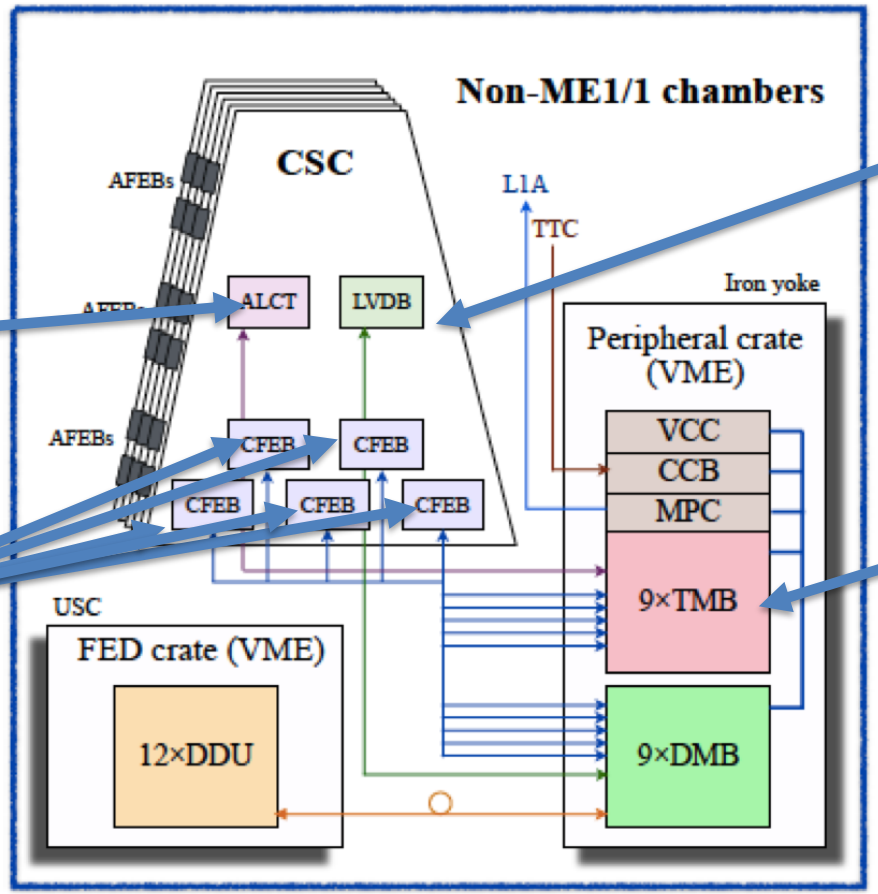


Approximate angular region of MEX/1

High data volumes/trigger rates and longer L1 latency require deeper buffering and an increase in the bandwidth for the front end electronics in the most forward/backward chambers.

Anode Local Charged Track electronics: replace mezzanine cards to increase latency capability and output bandwidth

Cathode Front End Boards: replace with Digital Cathode Front End Boards (latency and rate capabilities)

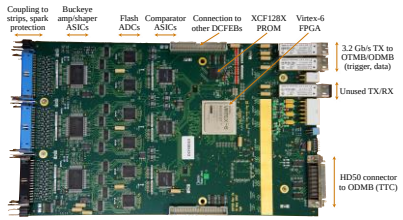


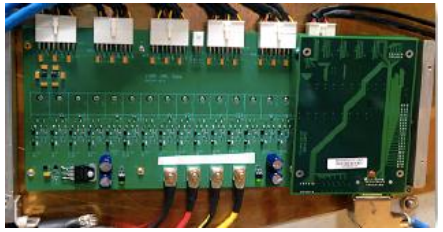
Low Voltage Distribution Board: replace to provide voltages and currents for DCFEBs

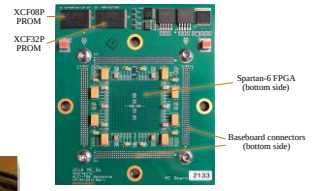
Trigger Motherboard (TMB): replace with optical TMB: needed to receive DCFEB trigger data; increased algorithmic power

Schedule overview – LS2 upgrades

- Electronics boards
  - 570 DCFEBs
  - 120 LX150T ALCT mezzanines
  - 320 LX100 ALCT mezzanines
  - 120 LVDB boards
  - 120 OTMB boards







- Power and infrastructure
  - HV system for ME1/1
  - 36 LV junction boxes
  - 12 Maraton LV supplies
  - 216 optical fiber cables

	2017				2018				2019				2020			
	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
Opt. fibers	On-chamber				Today	EDR				Start ME1/1 installation						
LVDB5																
DCFEB (+)																
DCFEB (-)																
ALCT-LX150T																
ALCT-LX100																
LV system	Off-chamber															
HV system																
OTMB																

Color code	Design	Engin. Prototype	Pre-production	Production	Float	Install. & Commiss.

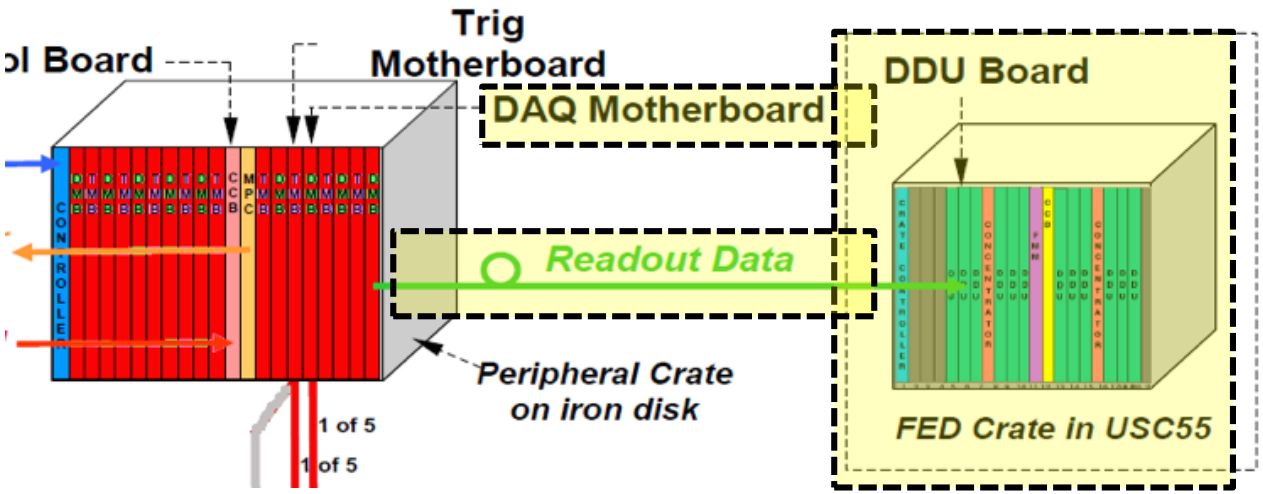
CSC off-chamber electronics (L3 scope)

High data volumes/trigger rate require an increase in the bandwidth of links connecting electronics on the detector with the counting room

Data rates up to 3 Gbps at HL-LHC, current links are 1.6 Gbps

- Replace DAQ motherboards in peripheral crates
  - Upgrade output bandwidth
- Replace Front End Driver (FED) crates
  - µTCA or ATCA system
- Additional optical fiber connections
- Other electronics are not changed during upgrade

Current Electronics Configuration for CSC Readout

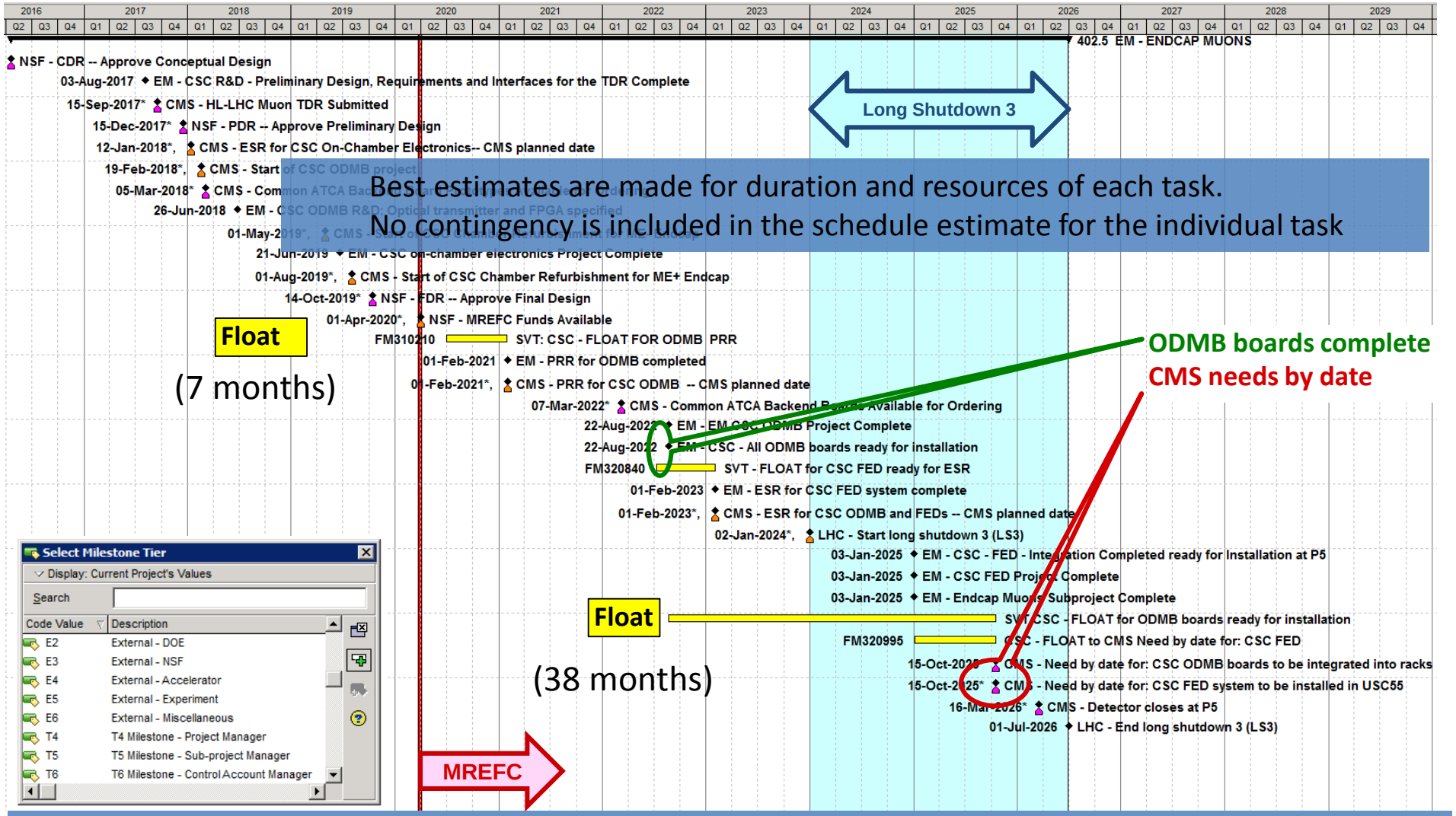


In Peripheral Crates: Replace DAQ mother boards (only) – one per chamber

Additional high bandwidth optical fibers

FED system is replaced with all new crates and modules

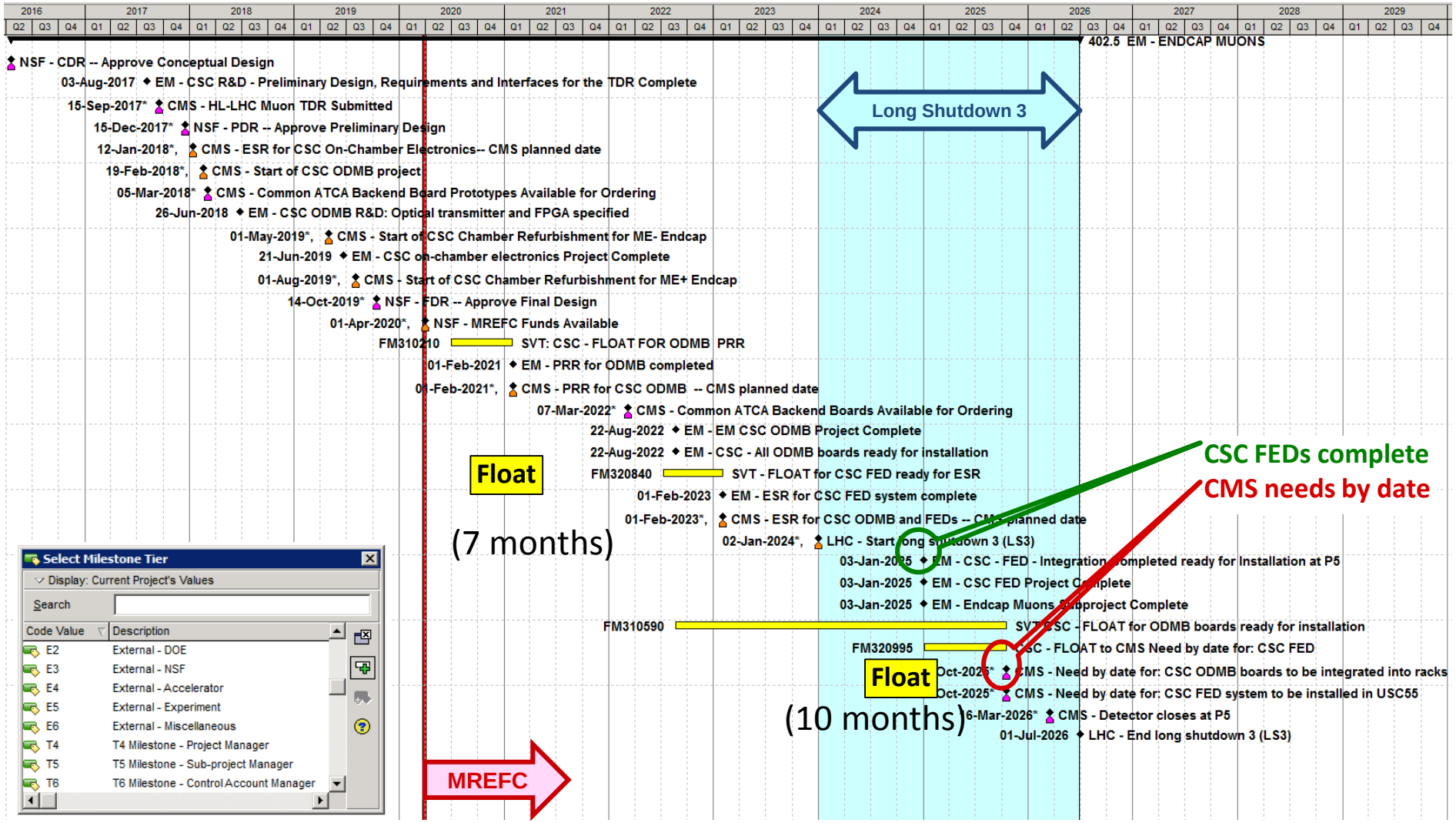
Schedule: CSC ODMB



Best estimates are made for duration and resources of each task.
No contingency is included in the schedule estimate for the individual task

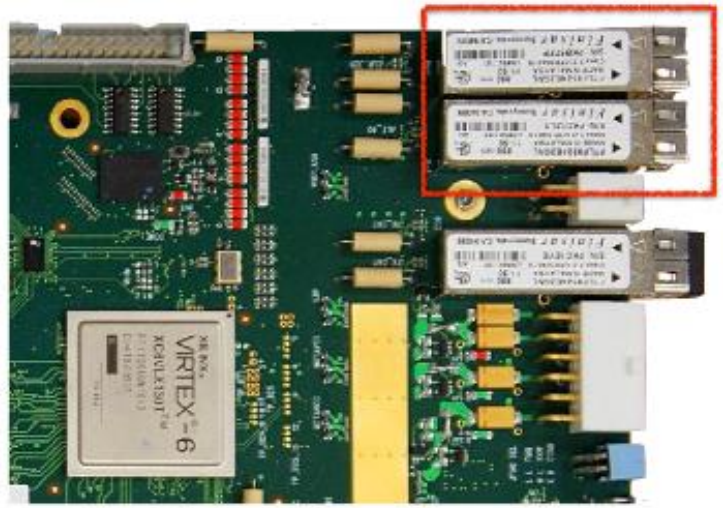
Schedule contingency is visible in floats between completion milestone and external “need-by” dates

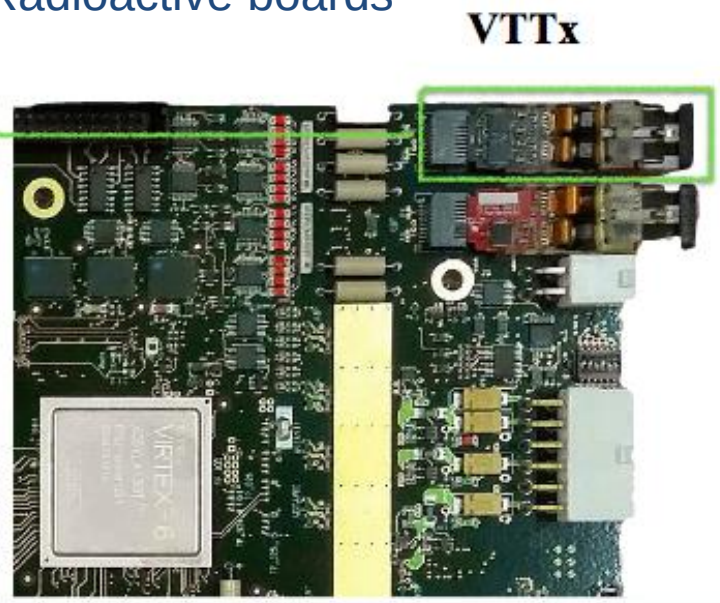
Schedule: CSC FEDs



Open questions: DCFEBs (1)

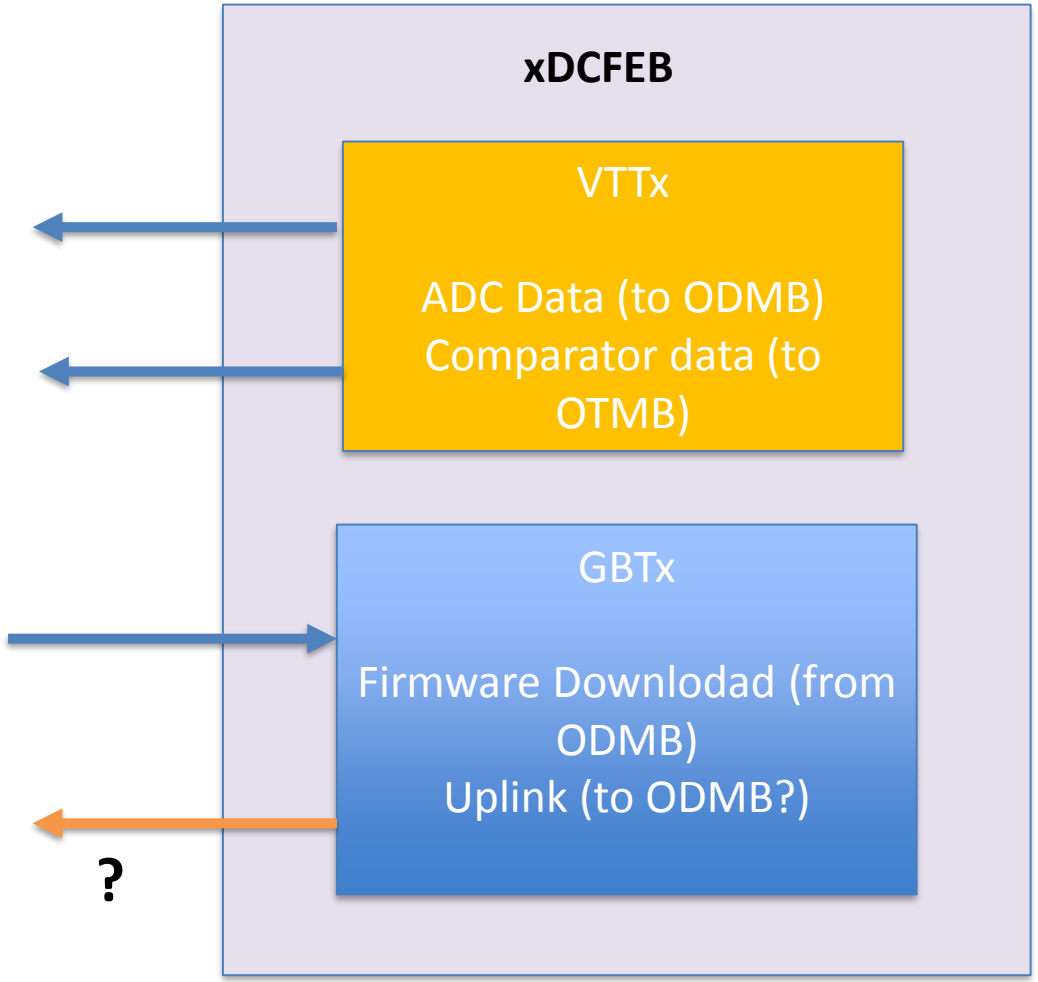
- **Replace Finisar optical transceivers on old DCFEBs from ME1/1?**
- Background:
  - 10 Finisar's died in 2017 run – not sure why
  - In CHARM rad testing, all Finisars were dead by ~20 kRrad
  - We are using VTTx's on new xDCFEBs – maybe replace?
- Considerations:
  - Not pin compatible
    - Would need adapter board to replace
  - Still need to unsolder old Finisars
    - Possible damage to boards?
  - Swap logistics
    - Narrow time window
    - Radioactive boards





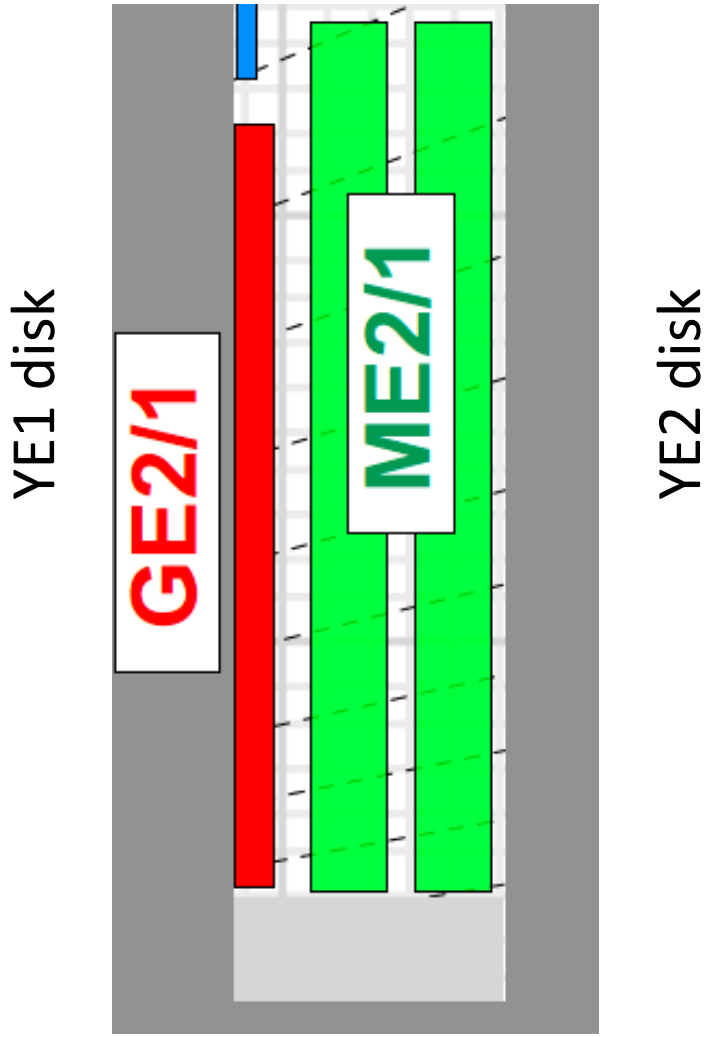
Open questions: DCFEB (2)

- **How to implement GBTx communication for xDCFEBs in ME1/1?**
  - Full duplex?
  - Affects the number of fibers , but don't need to decide until near LS3
- **Power down GTBx in Run 3?**



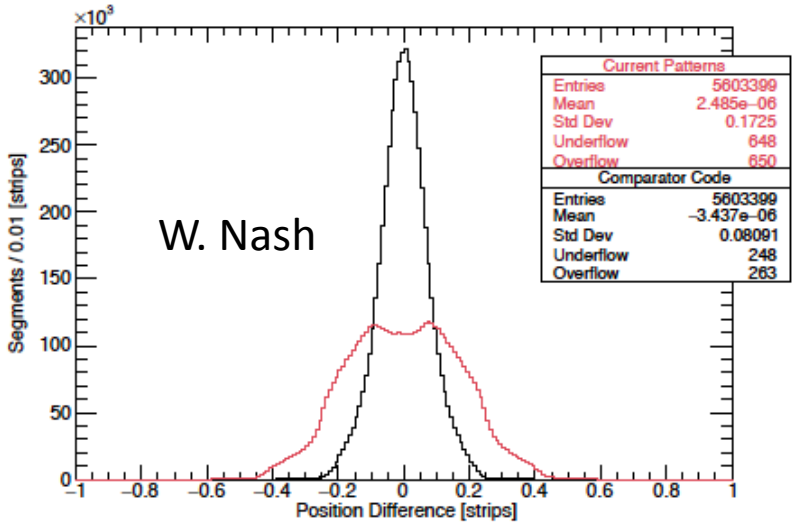
Open questions: OTMB (1)

- **How to connect fiber inputs from GE2/1 to OTMBs for ME2/1?**
  - Fiber from GE2/1→ME2/1, and then to the OTMB via a single 12-fiber bundle
    - Latency? Fiber routing?
  - Bundle from GE2/1→PC, merge with ME2/1 bundle into one bundle that connects to a single MTP12 RX on the OTMB
    - Requires custom fiber
  - Bundle from GE2/1→PC and connect to a second MTP12 RX on the OTMB
    - Additional flavor of OTMB
  - No direct GEM→CSC connection
    - Do everything in EMTF



Open questions OTMB (2)

- **Do we need to support legacy copper inputs on new OTMBs?**
- **Can improved LCT resolution from OTMB fitting algorithms help in triggering?**
- **How many spare fibers for OTMBs in ME2,3,4,/1?**



Open questions: ODMB

- **Which FPGA?**
- **Which optical transmitter?**
  - What speed? Affects the number of links and the headroom
- **Re-use (72) ODMBs from ME1/1 in ME3/1, ME4/1?**
- **How to program xDCFEB and ALCT FPGAs in ME1/1 – from ODMB or FED?**

TDR design – assuming 6.4 Gbps links

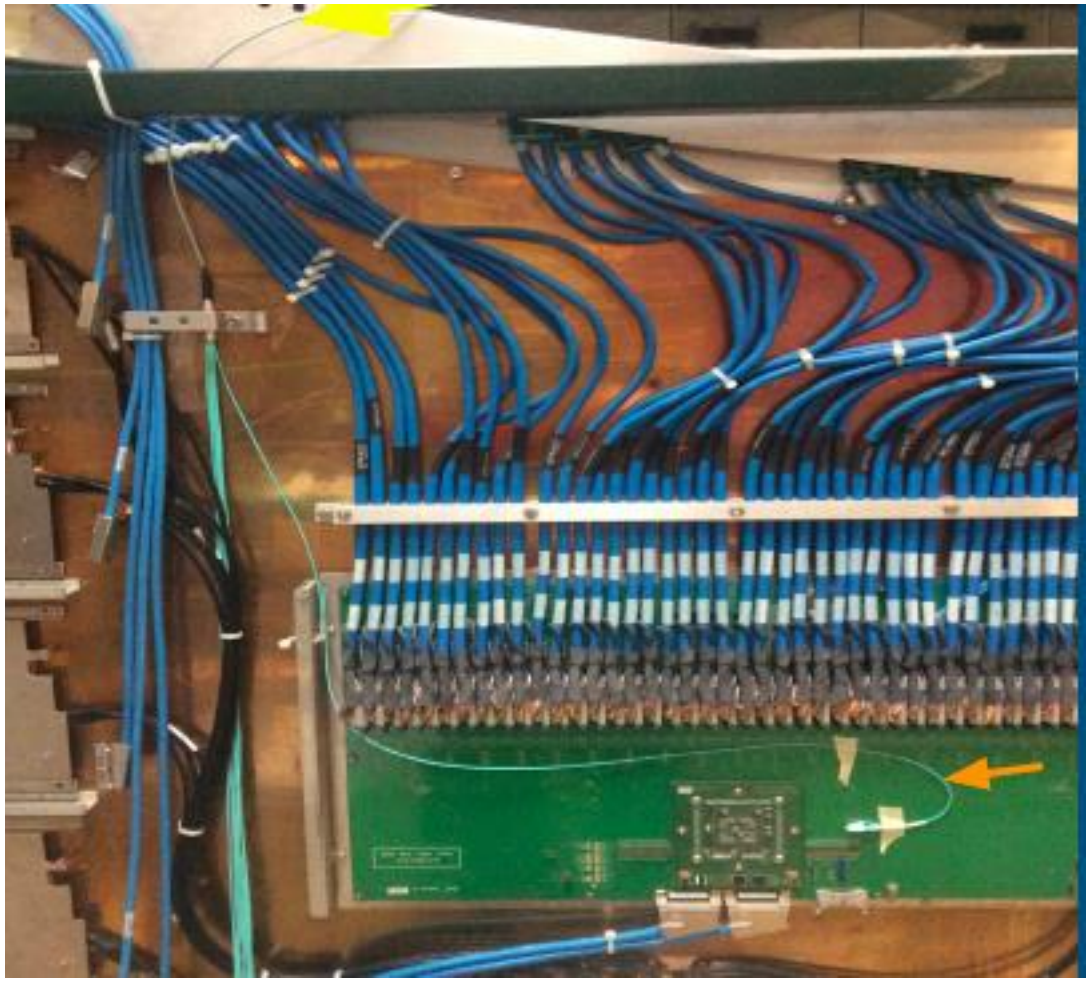
Station	Max. data rate (Gbps) baseline	# of Fiber	optical links occupation	
			Baseline HL-LHC	Ultimate HL-LHC
ME1/1	4.3	4	**21%**	**48%**
ME2/1	2.8	3	**18%**	**41%**
ME3/1	1.6	2	**16%**	**36%**
ME4/1	1.6	2	**15%**	**34%**
ME1/2	0.3	1	20%	45%
ME2/2	0.2	1	13%	29%
ME3/2	0.2	1	15%	34%
ME4/2	0.4	1	31%	70%
ME1/3	0.1	1	2%	5%

Open questions: FED system

- **Which ATCA module to use for CSC FED?**
  - The balance of I/O and processing might differ from other CMS projects (e.g. trigger)
  - Common with GEMs?
- **How to partition system and route fibers?**
  - 360 legacy fibers + 540 new fibers = 900 fibers
  - 60 peripheral crates
- **Do we need/want 2-way communication between ODMB and FED?**
  - If so, how should it be implemented?

Open questions: infrastructure

- **Layout/routing of fibers on ME234/1**
- **DCFEB cover design – cutout locations?**



Charge/plans

- This presentation merely introduced some of these question
  - We have a few minutes for discussion now, but we can identify any topics for detailed discussion later in the workshop
- I will revisit these questions at the end of the workshop
  - Note any questions that have been resolved ✓
  - Probably add some new questions as well