GEM/CSC backend segmentation options

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1. Overview

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- **General**
  - There are many variables, so this is just some preliminary proposals
    - CSC 6.4Gb/s links vs 10Gb/s links
    - GE2/1 LpGBT vs GBTX
    - Many options of the backend FPGAs and link counts
- **Andrew brought up a **very good** idea yesterday**
  - On the APd1 card, the mezzanine connector could be utilized to connect to a custom mezzanine board with cheap FPGAs to bring in the slow 1.6Gb/s CSC links
  - Turns out, this could reduce the total ATCA cards for CSC **by half!!**
    - Only 6 ATCA cards would be needed (100 link variant, preferably VU9P)
    - The mezzanine would have to have 60x 1.6Gb/s receivers
      - Could be done with 4 Artix7 FPGAs (~$200-$250 each)
        - Plus optical receivers e.g. 5x miniPODs ($136 each)
      - Send data to the main FPGA over 120 I/Os @ 640Mb/s
      - Most likely the board would have to be larger than dedicated envelope, so would have to stick out and take up the second slot
        - This is not a problem since we only have 6 cards in the crate
    - See next slide for more details
  - Question to Stephen: could this type of interface be included in BCP also?

2. APd1 with mezzanine for CSC FED

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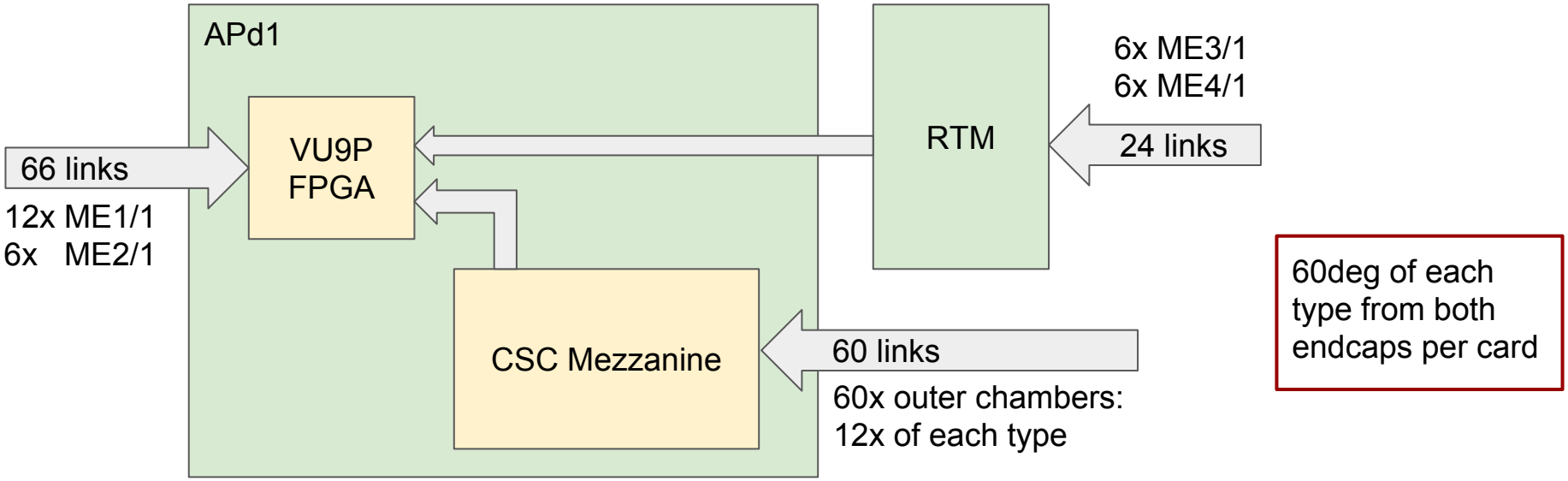

- **APd1 with VU9P and CSC Mezzanine (6 cards total)**
  - 90 out of 100 receivers used for high speed chamber links (new ODMB)
  - 60 slow links from outer chambers would be taken in by the CSC Mez
  - 8x 25Gb/s links used to interface with DTH (total = 200Gb/s)
  - 340Mbit of buffer space, plus 52Mbits of buffers on the CSC Mezzanine
  - With VU160 FPGA, buffer space = 115Mb, plus the mez buffers
- **Approximate total cost from $183744 to $193644**
  - 6x APd1 with VU9P: $29774 * 6 = $178644
  - 6x APd1 with VU160: $28124 * 6 = $168744
  - 6x CSC Mezzanines: around $2500 * 6 = around $15000

3. BCP with mezzanine for CSC FED

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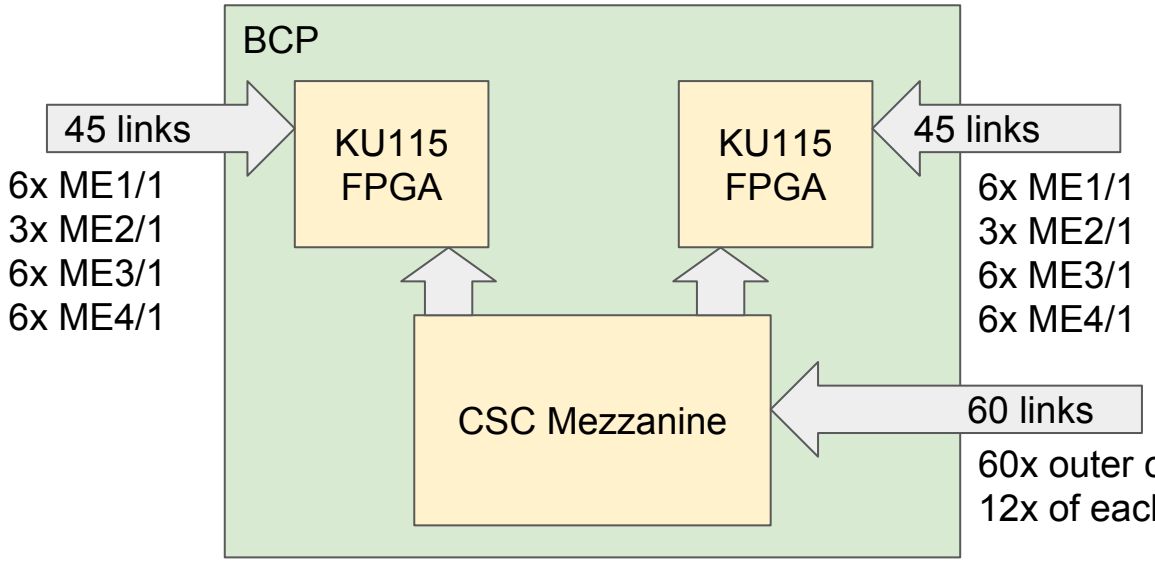

Is it possible with BCP?

40deg of each type from both endcaps per card

- **BCP with KU115 and CSC Mezzanine (6 cards total)**
  - 90 out of 96 receivers used for high speed chamber links (new ODMB)
  - 60 slow links from outer chambers would be taken in by the CSC Mez
  - 16x 15.7Gb/s links used to interface with DTH (total = 251Gb/s)
  - 152Mbit of buffer space, plus 52Mbits of buffers on the CSC Mezzanine
  - KU095 FPGA would give 118Mb of buffer space, plus the mez buffers
- **Approximate total cost from $128130 to $137730**
  - 6x BCP with KU115: $20455 * 6 = $122730 (removed 2 TX modules)
  - 6x BCP with KU095: $18855 * 6 = $113130 (removed 2 TX modules)
  - 6x CSC Mezzanines: around $2500 * 6 = around $15000

4. Considerations for the mezzanine option

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- **Caveat: eliminating station overlap with just 6 cards**
  - To eliminate station overlap would have to mix two endcaps in same card
    - Otherwise there would only be 3 cards to cover 4 stations
  - But even having some overlap is not a big problem given the amount of RAM we have in these cards (especially in VU9P)
    - Still should do queue depth simulations of course, in any case
      - This would drive the backend FPGA choice

5. CSC Options without the mezzanine

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- **9 BCP cards with KU095 or KU115**
  - Use 100 RX and 20 TX for chamber interfaces
  - Use 12x 15.7Gb/s links for DTH interface (total = 188.4Gb/s)
  - KU095 = 118Mb buffers, KU115 = 152Mb buffers
  - Both FPGAs would have the same number of each chamber type
  - Caveat: one card with chambers from plus and minus endcaps
    - Not a big deal since we never really run half of the system in local and the other half in global
  - Total cost with KU095: $18335 * 9 = $165015 (removed 4 TX modules)
  - Total cost with KU115: $19935 * 9 = $179415 (removed 4 TX modules)

- **APd1**
  - Cannot have 9 cards because there's not enough links
    - All links would be used up by chamber interfaces, and no left for DTH
  - Could use 10 cards, but chamber types would be distributed unevenly
    - Would have to take care in balancing the bandwidth
    - Total cost with VU160: $28124 * 10 = $281240
    - Total cost with VU9P: $29774 * 10 = $297740

6. GEMs

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- **Biggest concern is ME0 logic resources**
  - So number of boards needed is driven by logic rather than optical links
  - Adding a CSC mezzanine card would help mitigate that by taking up the GE2/1 processing and leaving the main FPGA just for ME0 processing
  - So the two options presented yesterday still hold
    - Either 2 ME0 chambers + 4 GE2/1 layers per card
    - Or 3 ME0 chambers + 6 GE2/1 layers per card
    - 4 ME0 chambers + 8 GE2/1 layers processed by the mezzanine is probably too tight for the logic resources (except maybe largest FPGAs)

Logic cells for each ME0 chamber (not considering the logic needed for GE2/1):

	BCP KU095 $19375	BCP KU115 $20975	APd1 VU160 $28124	APd1 VU190 $29944	APd1 VU9P $29774	APd1 VU11P $32675	APd1 VU13P $37988
2x ME0	1176k	1451k	1013k	1175k	1293k	1417k	1890k
3x ME0	(!) 784k	(!) 967k	676k	783k	862k	945k	1260k
4x ME0	588k	725k	507k	588k	646k	709k	945k

(!) means that the logic could be hard to divide, because one FPGA would have half of ME0

  - 2 ME0 chambers + 4 GE2/1 layers require 18 cards
  - 3 ME0 chambers + 6 GE2/1 layers require 12 cards
  - 4 ME0 chambers + 8 GE2/1 layers require 9 cards and 9 CSC Mezzanines

7. GE2/1 GBTX option

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- **Note on GBTX fallback on GE2/1**
  - The 18 card option (with 2 ME0 per card) can accomodate the GE2/1 even if it uses GBTX
  - The 12 card option (with 3 ME0 per card) can accomodate the GE2/1 GBTX option, but only if using a mezzanine

8. ME0 and GE2/1 links version 1

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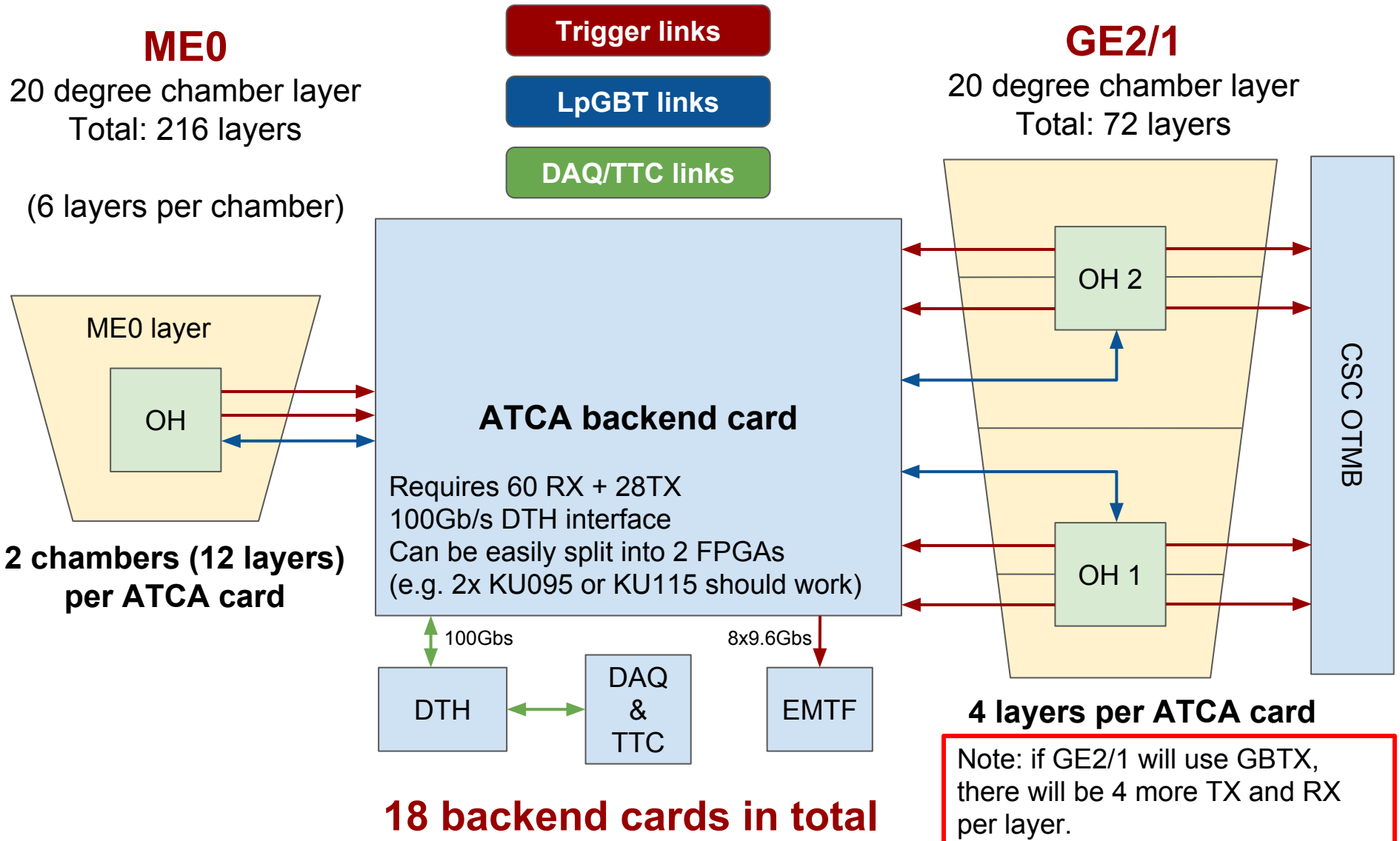
ME0 and GE2/1 as a common system, based on CTP7 link counts



9. ME0 and GE2/1 links version 2

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ME0 and GE2/1 as a common system, with more links than CTP7