CSC FED Open Questions

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CMS GEM/CSC Forward Muon Upgrade Workshop 10.04.2018

1. Overview

Evaldas Juska (TAMU)

- **Main question -- which ATCA card, and how many?**

- **Andrew brought up a very good idea yesterday**
  - On the APd1 card, the mezzanine connector could be utilized to connect to a custom mezzanine board with cheap FPGAs to bring in the slow 1.6Gb/s CSC links
  - Turns out, this could reduce the total ATCA cards for CSC by a lot
    - Only 6 ATCA cards would be needed (100 link variant, preferably VU9P)
    - The mezzanine would have to have 60x 1.6Gb/s receivers
      - Could be done with 4 Artix7 FPGAs (~$200-$250 each)
        - Plus optical receivers e.g. 5x miniPODs ($136 each)
      - Send data to the main FPGA over 120 I/Os @ 640Mb/s
      - Most likely the board would have to be larger than dedicated envelope, so would have to stick out and take up the second slot
        - This is not a problem since we only have 6 cards in the crate
    - See next slide for more details

  - Question to Stephen: could this type of interface be included in BCP also?

2. Which ATCA card?

Evaldas Juska (TAMU)

- **Which ATCA card? Best options (all RX channels occupied):**
  - 6x APd1 with VU9P + custom mezzanine for outer chambers ($193644)
    - Buffer space = 392Mb per card
  - 9x BCPs with KU115 ($179415)
    - Buffer space = 152Mb per card
  - 9x BCPs with KU095 ($165015)
    - Buffer space = 118Mb per card
  - 6x BCPs with custom mezzanine
- **Is it ok to mix chambers from plus and minus endcaps?**
  - This is the case when using 9 BCPs
  - Also could mix endcap in case of 6 APd1 to avoid station overlap
  - Not a big deal from my experience - never run half the system in global and other half in local
- **Is it ok to have some station overlap?**
  - This is the case when using 6 APd1 and not mixing endcaps
  - Probably wouldn’t have a big impact given the huge buffers
- **In any case, should do queue depth simulation**
  - Have a better idea of the buffer space requirements

3. APd1 with mezzanine for CSC FED

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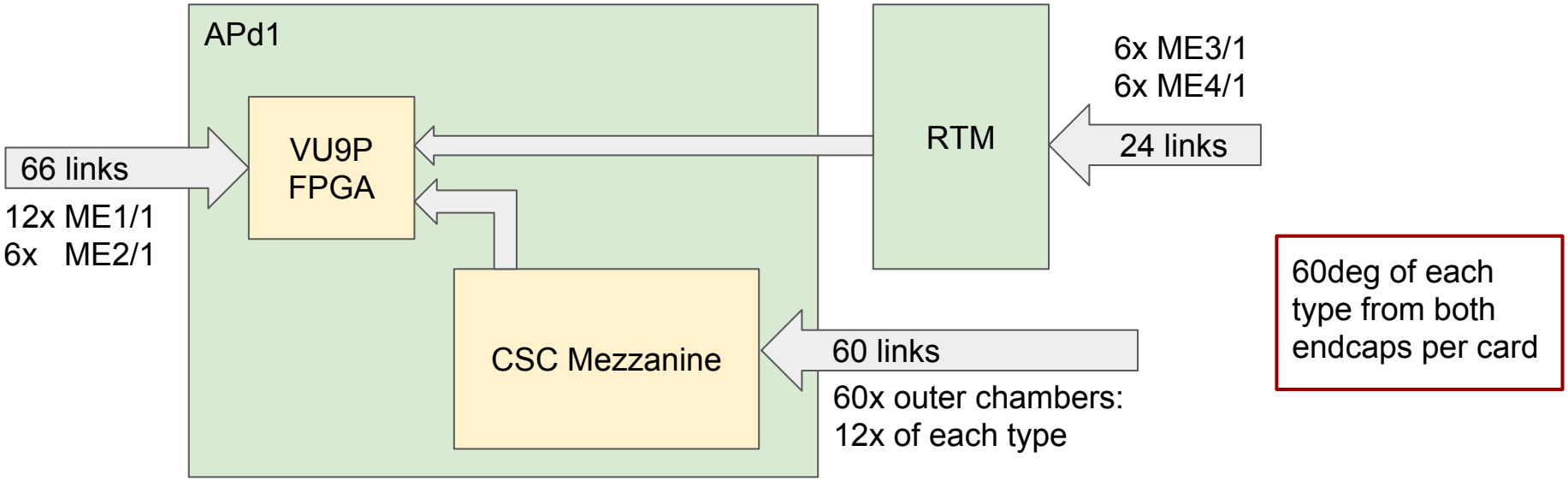

- **APd1 with VU9P and CSC Mezzanine (6 cards total)**
  - 90 out of 100 receivers used for high speed chamber links (new ODMB)
  - 60 slow links from outer chambers would be taken in by the CSC Mez
  - 8x 25Gb/s links used to interface with DTH (total = 200Gb/s)
  - 340Mbit of buffer space, plus 52Mbits of buffers on the CSC Mezzanine
  - With VU160 FPGA, buffer space = 115Mb, plus the mez buffers
- **Approximate total cost from $183744 to $193644**
  - 6x APd1 with VU9P: $29774 * 6 = $178644
  - 6x APd1 with VU160: $28124 * 6 = $168744
  - 6x CSC Mezzanines: around $2500 * 6 = around $15000

4. BCP option

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- **9 BCP cards with KU095 or KU115**
  - 40 degrees of each chamber type from both endcaps per card
  - Use 100 RX and 20 TX for chamber interfaces
  - Use 12x 15.7Gb/s links for DTH interface (total = 188.4Gb/s)
  - KU095 = 118Mb buffers, KU115 = 152Mb buffers
  - Both FPGAs would have the same number of each chamber type
  - Caveat: one card with chambers from plus and minus endcaps
    - Not a big deal since we never really run half of the system in local and the other half in global
  - Total cost with KU095: $18335 * 9 = $165015 (removed 4 TX modules)
  - Total cost with KU115: $19935 * 9 = $179415 (removed 4 TX modules)

5. Two way communication with ODMB

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- **Do we need two way communication with ODMB?**
  - I would say absolutely yes for two reasons:
    - Backpressure to ODMB would extend buffer space by a lot
      - 13-16Mb per chamber (depending on FPGA) -- this is huge
      - Would be a shame to waste that
    - PROMless programming of xDCFEBs and ALCT LX100

6. Bandwidth for ME4/2?

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- **Some ME4/2 chamber have significantly higher occupancy**
  - More of an ODMB question, but closely related to FED too
  - Have to check carefully if we really don't need an ODMB there with a faster link to FED

7. Worst case scenario data rate

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- **Worst case scenario data rate = 1.38Tb/s**
  - Not 0.6Tb/s as stated in TDR
  - From Manuel's presentation yesterday:

	6.4 Gb/s links 900 fibers			**10 Gb/s links** 720 fibers			**10 Gb/s links** 900 fibers		
Chamber	Rate [Gb/s]	Link [Gb/s]	Util. [%]	Rate [Gb/s]	Link [Gb/s]	Util. [%]	Rate [Gb/s]	Link [Gb/s]	Util. [%]
ME1/1	9.6	4×6.4	47	9.6	3×10	40	9.6	4×10	30
ME2/1	6.4	3×6.4	42	6.4	2×10	40	6.4	3×10	27
ME3/1	3.6	2×6.4	35	3.6	1×10	45	3.6	2×10	22
ME4/1	3.5	2×6.4	35	3.5	1×10	44	3.5	2×10	22
ME1/2	0.6	1×1.6	45	0.6	1×1.6	45	0.6	1×1.6	45
ME2/2	0.4	1×1.6	28	0.4	1×1.6	28	0.4	1×1.6	28
ME3/2	0.4	1×1.6	35	0.4	1×1.6	35	0.4	1×1.6	35
ME4/2	0.9	1×1.6	70	0.9	1×1.6	70	0.9	1×1.6	70
ME1/3	0.1	1×1.6	5	0.1	1×1.6	5	0.1	1×1.6	5

  - If you add up the "Rate" column, you get **1.38Tb/s** (!)
    - While TDR uses **0.6Tb/s** because 5x10^34 was used instead of 7.5x10^34

8. Worst case scenario data rate

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- **This changes things a bit**
  - 6x APd1 + mezzanine is much better option in this case
- **6x APd1 (VU160 or VU9P) + mezzanine option**
  - Total system output capability to DTHs = **3Tb/s**
  - Total cost (including mezzanine production cost) = **$183744 - $193644**
  - Compatible with 1 or 2 DTHs
    - Fits into one crate even with 2 DTHs
  - **167Mb - 392Mb** of buffer space per card
- **9x BCP without mezzanine option**
  - Total system output capability = **1.68Tb/s**
  - Total cost = **$169695 - $184095**
  - Adding bandwidth would mean adding 3 cards (additional cost = ~$60k)
    - Otherwise cannot be balanced
    - This probably needs also additional crate
    - Total output bandwidth after adding 3 cards = up to **3Tb/s**
    - Total cost after adding 3 cards = **$226260 - $245460**
- **Mezzanine card in general can help GEMs too**
  - Provide additional links for GE2/1 in GBTX scenario without BE increase
  - Offload GE2/1 processing from the main FPGA, leaving resources to ME0