Optohybrid Board for GE21

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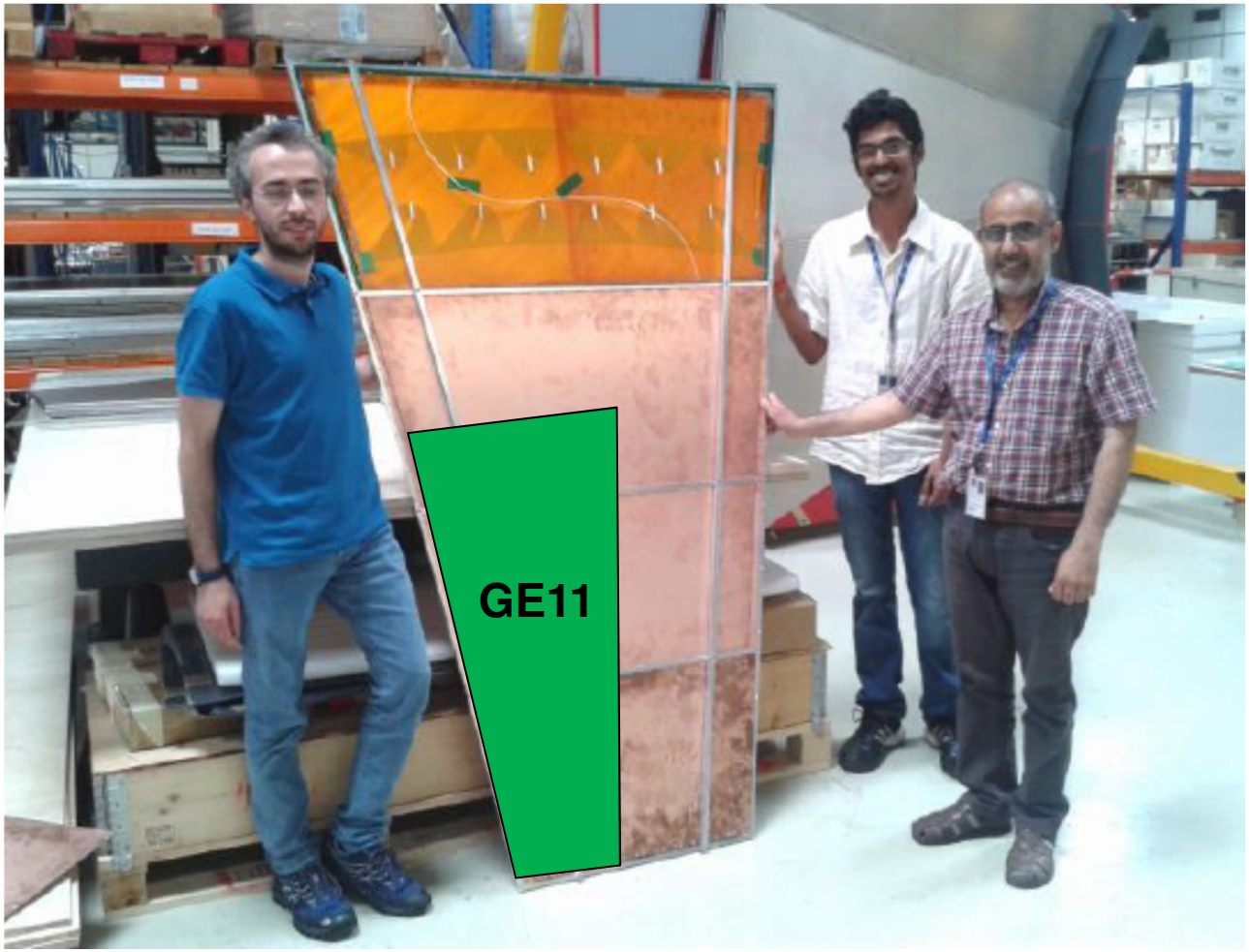
GE11 Readout and Trigger Links

- VFAT3 requires one 320MHz E-link to communicate with the GBTx
  - Each E-link comprises 3 differential pairs (input + output + clock)
- One GBTx ASIC can maintain only 10 E-links at 320MHz.
  - 3 GBTx are needed to read out 24 VFAT3 ASICs on GE1/1 chamber (OHv3 design)
- VFAT3 provides 8 trigger bits at 320MHz + 1 clock to the trigger path;
  - 24 VFAT3 x 9 pairs = 216 pairs = 432 signal inputs to the Virtex-6 FPGA
  - Existing differential pairs are as long as 80 cm
- Compressed trigger bits are sent at 3.2Gbps to OTMB (2 fibers) and uTCA CTP7 (2 fibers)
- For 144 10 degree GE11 chambers this architecture requires:
  - 144 x 3 = 432 GBTx links with Versalink protocol at 4.8Gbps for readout and control
  - 144 x 2 = 288 fibers to OTMB with 8B/10B protocol at 3.2Gbps for trigger data
  - 144 x 2 = 288 fibers to CTP7 with 8B/10B protocol at 3.2Gbps for trigger data

GE21 Chamber

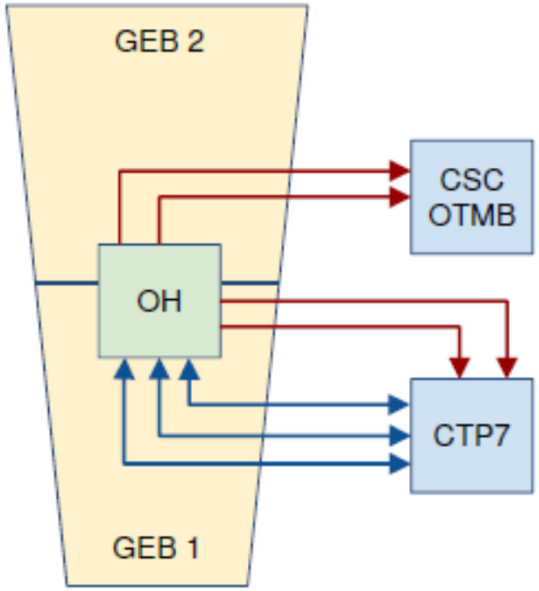


- Slide borrowed from A.Sharma's presentation at the CMS Week, February'18

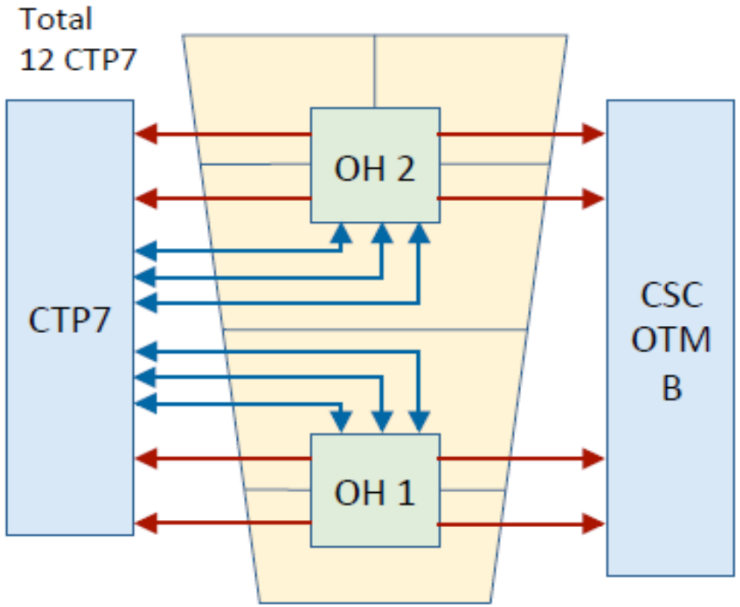
GE21 Readout and Trigger Links

- 72 large 20 degree (~1.8 x 1.2 m) GE21 chambers; will utilize 4 GEB boards and 2 Optohybrid boards
- One OH board will handle 24 VFAT3 ASICs
- GE21 OH functionality is close to GE11 OH, but readout and control links may be different:
  - GBTx
  - LpGBTx

GE1/1



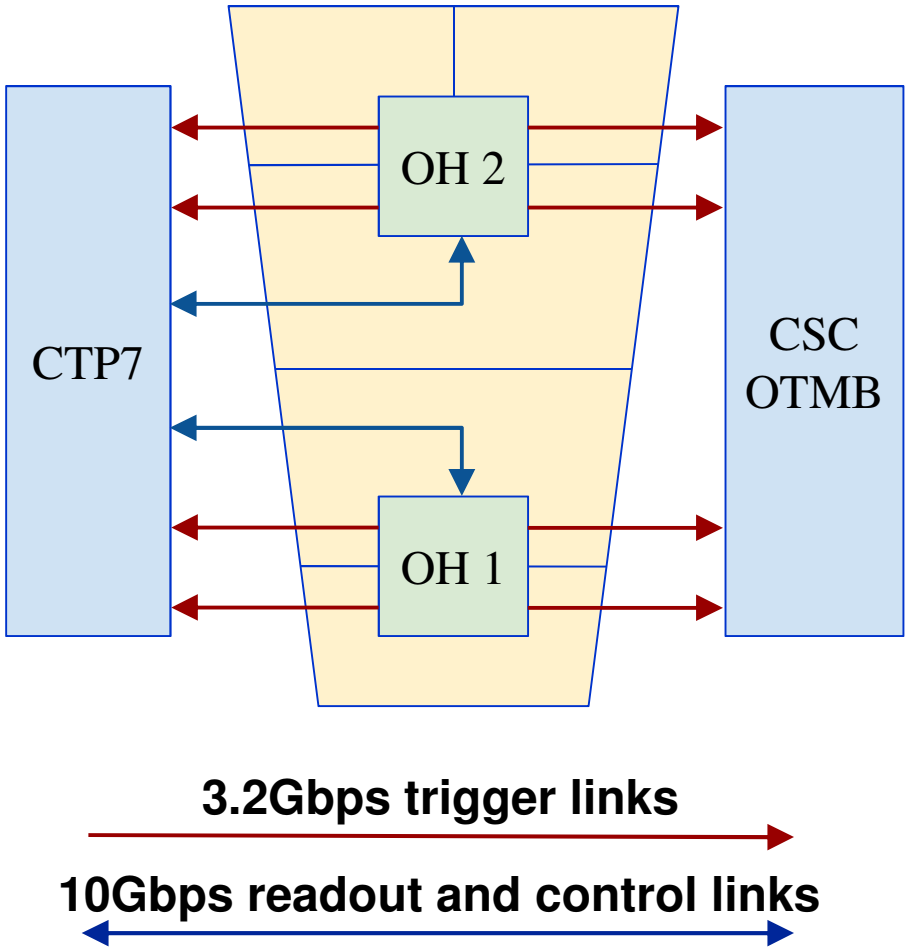
GE2/1



GE21 Readout with LpGBTX

- One LpGBTx could handle all 24 VFAT3 in place of 3 GBTx
  - Has 28 E-link inputs @ 320MHz
  - But only 4 E-link outputs @ 320MHz. These E-links should provide connections to 24 VFAT3s.
  - Optical link running at 10Gbps

- The biggest advantage of using LpGBTx instead of GBTx would be the reduction of readout and control GBT links from 432 to 144 and also reduction of CTP7 boards (or their future successor) from 12 to 8



GBTx and LpGBTx ASICs

	GBTx	lpGBTx
Optical Link	4.8Gbps User bandwidth 3.28-4.48Gbps	Down-link (Rx): 2.56Gbps (64-bit frame). User bandwidth 1.44Gbps Up-link (Tx): 5.12Gbps (128-bit frame). User bandwidth 4 (4.56) Gbps 10.24Gbps (256-bit frame). User bandwidth 8 (9.13) Gbps
E-Links	40 bidirectional E-links at 80Mbps 20 bidirectional E-links at 160Mbps 10 bidirectional E-links at 320Mbps 40 E-link clocks 40/80/160/320 MHz	Down-link (outputs): 16/8/4 at 80/160/320Mbps Up-link (inputs): 28/14/7 or 24/12/6 at 160/320/640/1280Mbps 28 E-link clock outputs 40/80/160/320/640/1280MHz
Package	BGA400 (17 x 17 mm)	BGA289 (9 x 9 mm)
Power dissipation, mW	2200 (worst case)	500 @ 5.12 Gbps 750 @ 10.24 Gbps
Radiation Hardness	100 MRad	200 MRad
Other features	Requires external crystal oscillator Requires SCA ASIC for control functions	Doesn't require external crystal oscillator Performs a reduced set of SCA functions
Status	Available, $35/pc	Samples: end of 2018 Engineering run: Q3 2019 Production complete (~100K chips): Q3 2021

VTRx ans VTRx+ Rad Hard Optical Transceivers

	VTRx	VTRx+
Companion to	GBTX ASIC	lpGBTX ASIC
Number of channels	1 Rx + 1 Tx (VTRx) 2 Tx (VTTx)	1 Rx + 1 Tx 1 Rx + 4 Tx (under consideration) 4 Tx (under consideration)
Wave Length, nm	1310 Single Mode, 850 Multi Mode	850 Multi Mode
Data Rate, Gbps	Tx: 5 Rx: 5	Tx: 5 and 10 Rx: 2.5
Dimensions, mm	55 x 14.5 x 10	20 x 10 x 2.5(4)
Radiation Tolerance, MRad	50	100
Status	Available, $150/pc	Prototyping and tests: 2017-2018 User evaluation and engineering run: 2019 Production: 2nd half of 2020

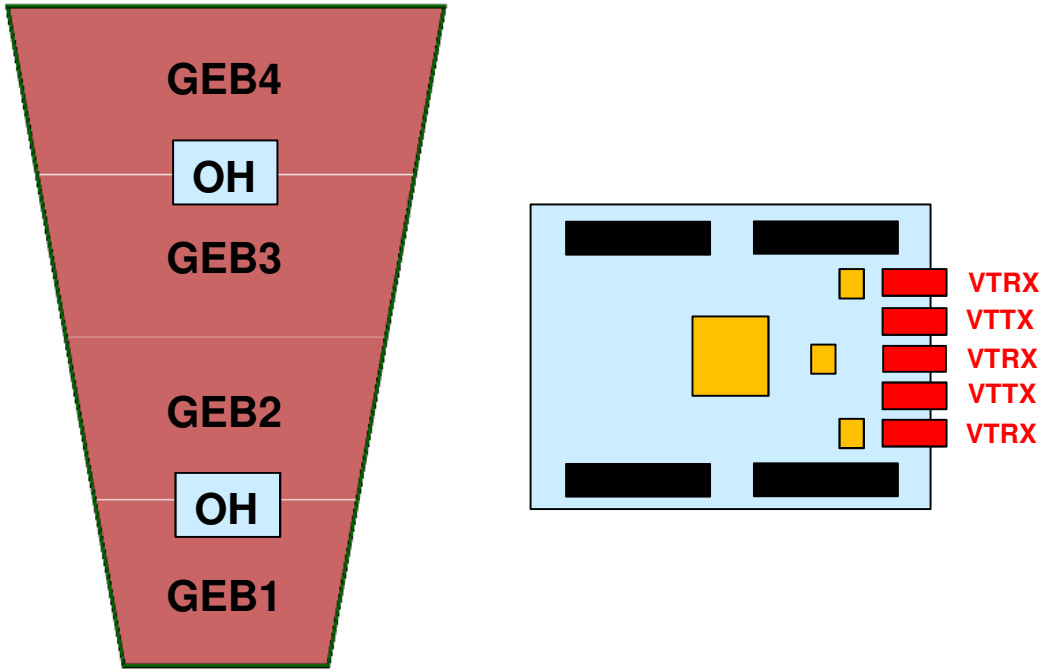
VTRx+ info is based on Jan Troska's presentation at TWEPP-17, September 2017

https://indico.cern.ch/event/608587/contributions/2614150/attachments/1522297/2378758/VTRxplus_TWEPP_13sep2017.pdf

LpGBTx Issues

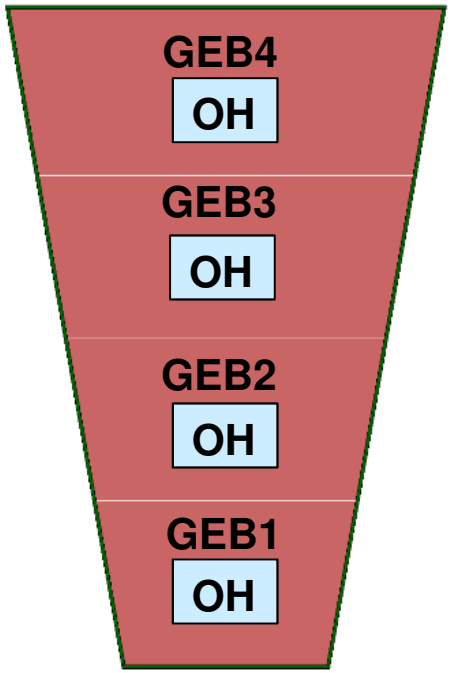
- Availability of first samples no earlier than in the fall of 2018
  - incompatible with the current aggressive GE2/1 electronics schedule
- Absence of LpGBTx core for Xilinx FPGA
  - possible additional delay w.r.t. ASIC samples
- Will need VTRx+ transceiver to fully utilize 10Gbps bandwidth
  - not available, samples no earlier than in the fall of 2018
- Very small package (9x9 mm) in comparison with GBTx (17x17 mm)
  - more complicated PCB design
  - pin assignment is unknown at this time
- How to distribute four 320MHz E-links from LpGBTx to 24 VFAT3?
  - SLVS interface supports multi-drop configurations, but this is challenging for 1 source with 6 loads and long traces at 320MHz
  - commercial SLVS fan-out buffers do not exist
  - need addressing scheme in the VFAT3… does it exist?
  - may use the FPGA as a fan-out with controllable delays (may be useful), but this would add additional complications:
    - less reliable due to SEUs
    - need 50 extra pins
    - Virtex-6, Spartan-6 and Artix-7 do not support true SLVS buffers

GE21 Readout with GBTX



- **Functionally similar to OHv3 for GE11. Serves 24 VFAT3 (two GEB boards).**
  - **Same proven Xilinx XC6VLX130T-1FFG1156C FPGA**
  - **~550 out of 600 i/o pins are in use**
  - **XCF128X EPROM + GBTx path to load the FPGA**
  - **3 GBTx + SCA**
  - **pin compatibility with the GE11 OHv3b where possible**
- **Mechanically different from GE11 OH. PCB traces from VFAT3 to the FPGA will be (much) longer; signal integrity and propagation delays worse.**

GE21 Optohybrid with "Light" FPGA



- One OH per GEB, serves 12 VFAT3 ASICs
- Need 2 GBTx + 1 SCA (or 1 LpGBTX)
- Need to provide 12 VFAT3 x 9 pairs = 108 diff pairs to FPGA
- One 3.2Gbps link (one fiber) to OTMB
- One 3.2Gbps link (one fiber) to uTCA processor
- Need 2 VTRx (GBTx) and 1 VTTx (trigger links)
- Few S6/V6/A7/K7 candidates, the cheapest <$100

Advantages

- Simpler mechanical design, installation and maintenance
- Simpler PCB design, shorter traces, better signal integrity
- Potential saving in FPGA cost

- **System Overview**
  - 72 chambers x 4 small FPGA = 288 small FPGA [144 large FPGA]
  - 72 x 4 x 2 = 576 [432] GBTx ASICs or 72 x 4 = 288 [144] LpGBTx
  - 72 x 4 = 288 [288] fibers to OTMB (four 3.2Gbps inputs to OTMB)
  - 72 x 4 = 288 [288] fibers to CTP7
  - 14 [12] CTP7 boards (GBTx) or 8 CTP7 boards (LpGBTx) [Assuming 68 Rx per CTP7]

Questions and Near Future Plans

- **What is needed for the schematic design**
  - **mechanical specification (GEB arrangements, number of connectors and connector part numbers, list of signals)**
  - **power connections (again, need more details from GE21 GEB designs) Will all powers (+2.5V, +1.8V, +1.5V, +1.2V, +1.0V) be provided from GEBs?**
  - **successful tests of GE11 OHv3 (to prove all the interfaces between VFAT3, Virtex-6 FPGA and GBTx, especially the long SLVS lines… BER? Eye pattern?)**
- **When all these issues are resolved, the GE21 OH schematic can be done in ~1 month, PCB layout in ~1 month (commercially), PCB prototype fabrication and assembly in ~2 months (4 boards?)**
- **Major components (FPGA, GBTx, SCA, EPROM…) are already known and can be ordered (or borrowed from the GE11 project if possible)**

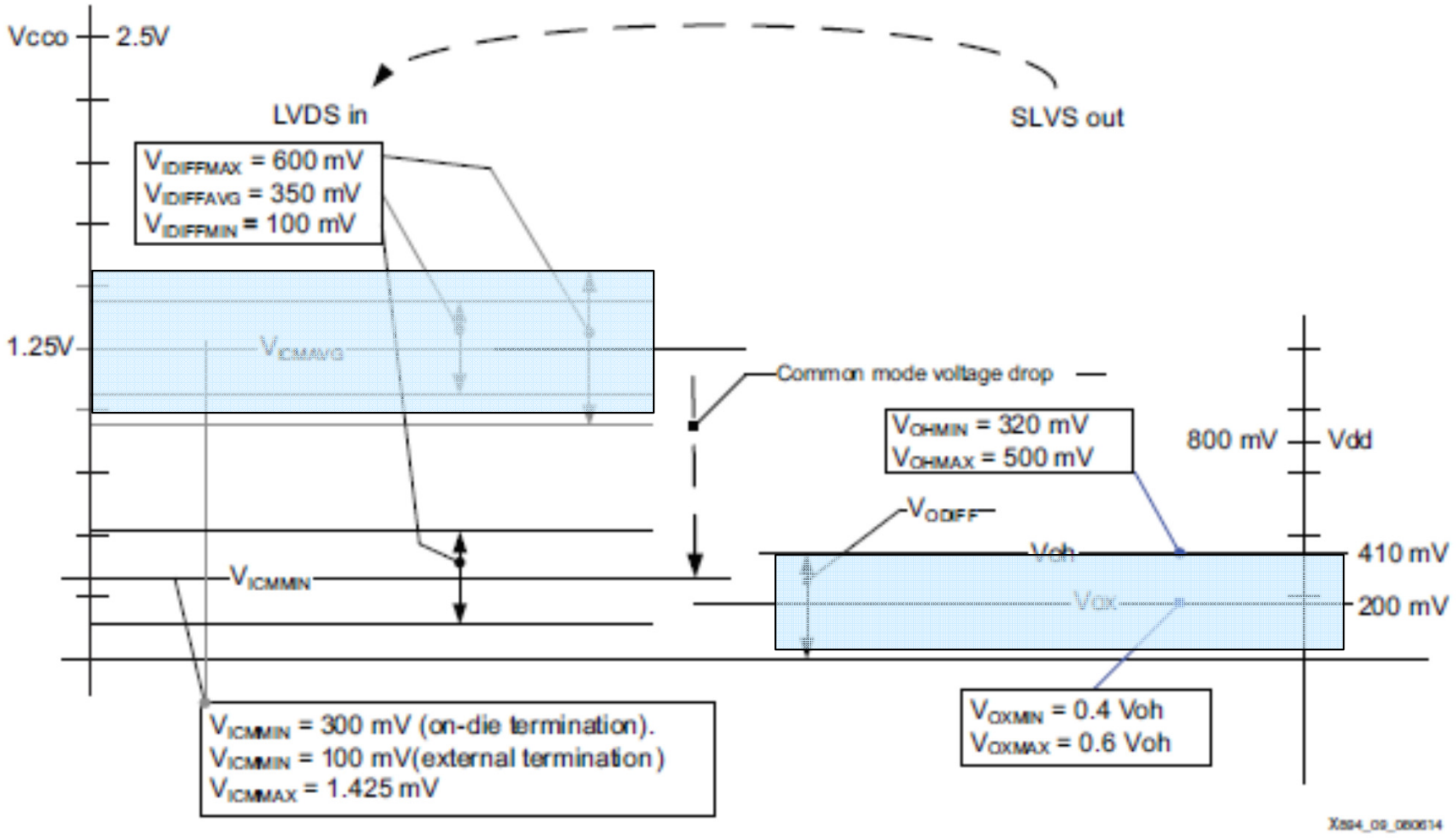
Backup Slides

SLVS vs LVDS

TABLE 1 SLVS INPUT- AND OUTPUT-SPECIFICATION CONFORMANCE

Characteristic	Device LVDS input (mV)	SLVS output (mV)
Minimum common-mode voltage	50	150
Maximum common-mode voltage	2350	250
Minimum differential voltage	100	140
Maximum differential voltage	2400	270
Characteristic	**Output with resistor network** (mV)	**SLVS input** (mV)
Minimum common-mode voltage	150	70
Maximum common-mode voltage	280	330
Minimum differential voltage	180	140
Maximum differential voltage	280	450

SLVS vs LVDS


Vcco
2.5V
LVDS in
SLVS out
$V_{IDIFFMAX}$ = 600 mV
$V_{IDIFFAVG}$ = 350 mV
$V_{IDIFFMIN}$ = 100 mV
1.25V
V_{ICMAVG}
Common mode voltage drop
V_{OHMIN} = 320 mV
V_{OHMAX} = 500 mV
800 mV
Vdd
V_{ODIFF}
Voh
410 mV
Vox
200 mV
V_{ICMMIN}
V_{ICMMIN} = 300 mV (on-die termination).
V_{ICMMIN} = 100 mV(external termination)
V_{ICMMAX} = 1.425 mV
V_{OXMIN} = 0.4 Voh
V_{OXMAX} = 0.6 Voh

SLVS Driver in GBTX ASIC

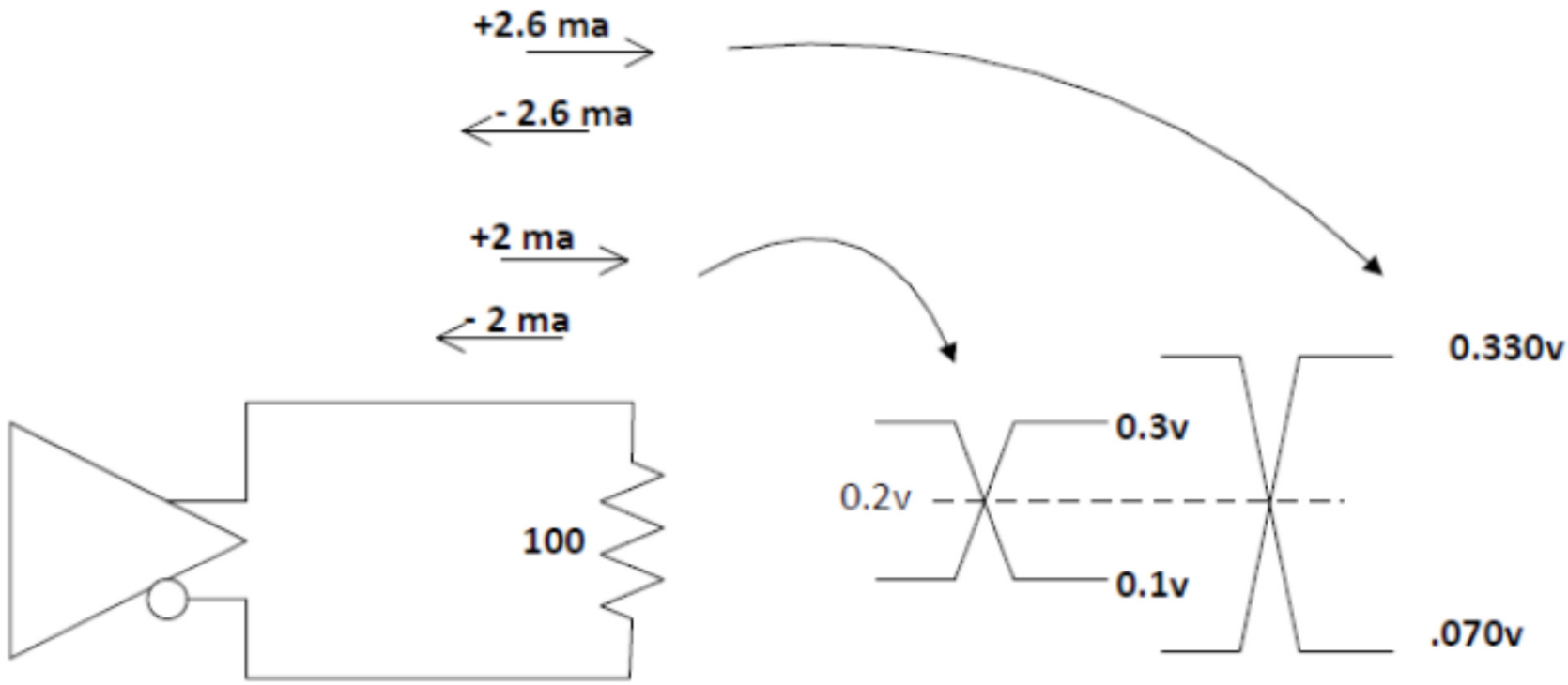


Figure 35 illustrates the differential swing and common mode for two different settings: SLVS levels, cset[3:0] = 10 and Maximum swing cset[3:0] = 00.

Virtex-6 LVDS_25 DC Parameters

LVDS DC Specifications (LVDS_25)

Table 9: **LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.825	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage for XC devices	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.075	1.250	1.425	V
	Output Common-Mode Voltage for XQ devices		1.000	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input Common-Mode Voltage		0.3	1.2	2.2	V

Simulated GBTX S-bits