ME0 Optohybrid

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ME0 Readout and Trigger Links

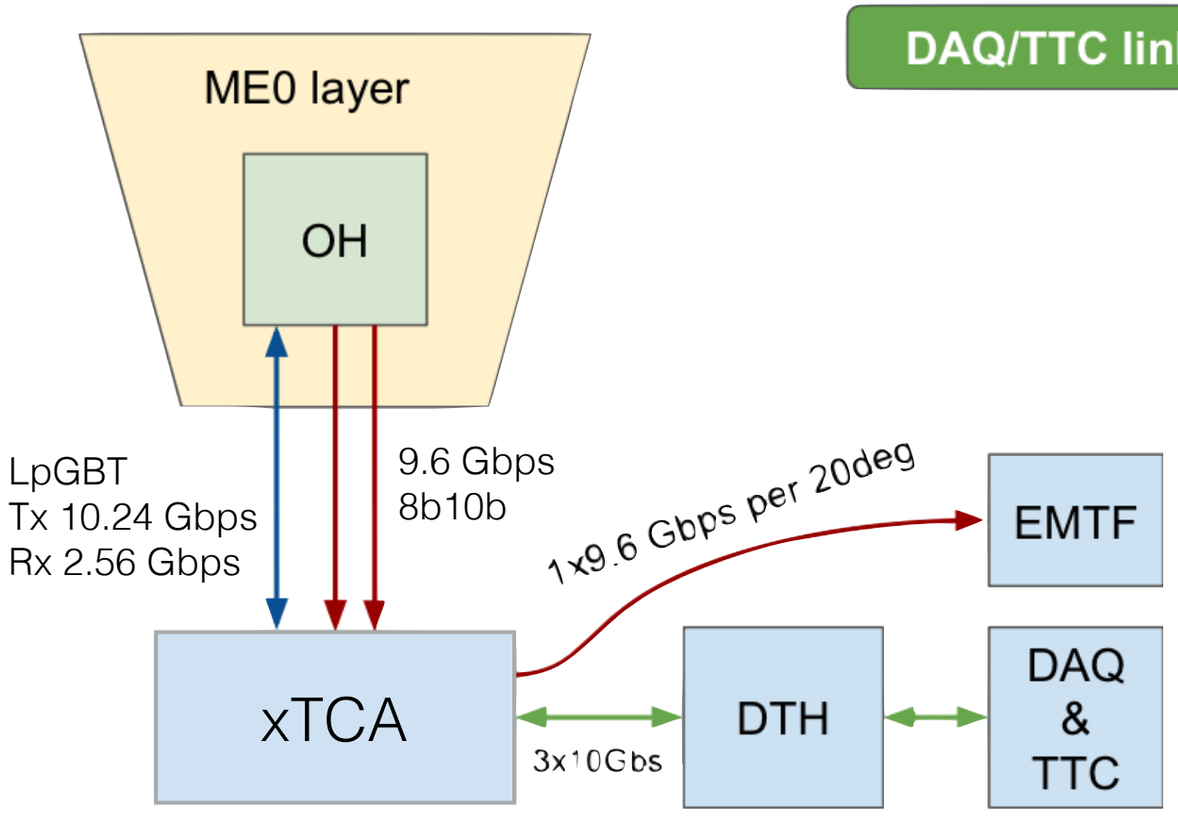
- 36 ME0 Modules (stack of 6 individual layers)
- Each layer has one optohybrid, 216 optohybrids total
  - Nominally, each has 1x LpGBT, 2x 8b10 trigger links per Optohybrid
- General similarity to GE1/1 Optohybrid, but a few changes:
  - GBTx → LpGBT (higher speed Serializer)
    - ✦ See Mike's slides for complexities of LpGBT
  - Removal of SCA (Slow Control Adapter)
    - ✦ Does not seem necessary
  - VTTX → VL+ (new CERN optics)
    - ✦ e.g. 3 TX + 1RX module
  - Virtex-6 → Kintex-7
    - ✦ Needed for higher trigger bandwidth, more logic
  - Change of dimensions, pinouts, connectors, mounting etc
  - **Radiation environment much harsher**
  - **Rates much higher**

ME0
20 degree layer
Total: 216 layers

Trigger links

LpGBT links

DAQ/TTC links



LpGBT Complexities

LpGBT design introduces complexities to control and configuration of VFAT

- Only 4 RX e-links @ 320 Mbps per LpGBT
  - ✦ c.f. Mike's talk for more details: https://indico.cern.ch/event/712520/contributions/2944468/attachments/1621966/2581115/GE21_OH_03_23_2018.pdf
  - ✦ c.f. LpGBT preliminary specs presentation: https://espace.cern.ch/GBT-Project/LpGBT/Specifications/LpGbtxSpecifications.pdf

- How to control 24 VFATs, provide EEPROMless programming, and FPGA control on one LPGBT?
  - ✦ 1x e-link @ 320 Mbps fans out to all VFATs (need to use HDLC addressing)
    - VFAT has 8-bit address… need 5 for 24 VFATs => OK
    - Need to find a suitable way to fanout SLVS signals => Find IC, or use FPGA
  - ✦ 12x e-link @ 80 Mbps provide EEPROMless programming + misc
    - e.g. 8-bit data bus, 1 bit prog_b, 1 VFAT reset, 2x TTC
  - ✦ Need e-link for readback from Optohybrid. Two options:
    - 1) Operate GBTx in FEC5 (lower quality error correction scheme)
      - Provides 4 additional 320 Mbps uplinks, but lose some error correction
    - 2) Or drop the SCA and use 80 Mb/s EC port

LpGBT Complexities, part 2

- Specs of LpGBT:

E-Links:

- Down-link:
  - Bandwidths: 80/160/320 Mb/s
  - Number of links*: 16/8/4
    - "Mirror" function:
      - 80 Mb/s: no;
      - 160 Mb/s: each channel is available on 2 outputs;
      - 320 Mb/s: each channel is available on 4 outputs.
  - One EC channel @ 80 Mbit/s

- "Mirror" function is added, allowing each e-link to drive 4 cloned outputs
  - ✦ Need to fanout 4 x (1 → 6) instead of 1 → 24
  - ✦ Might help.. might not.. but it is good to know about

SCA

- CERN GBT-SCA (SCA = Slow Control Adapter)
  - SCA provides JTAG
    - Do we really need JTAG? We have PROMless programming & no EEPROM
    - LpGBT has programmable IO—can run JTAG on those
  - SCA provides ADC. Do we really need ADC?
    - The FPGA has analog inputs
    - LpGBT includes 10 bit ADC, 8 inputs
  - SCA is complicated, adds expense, space
  - SCA occupies the External Control (EC) channel (80 Mb/s SLVS tx/rx)
    - EC channel can be used for FPGA TX/RX path
    - Else we need to give up FEC12 error correction

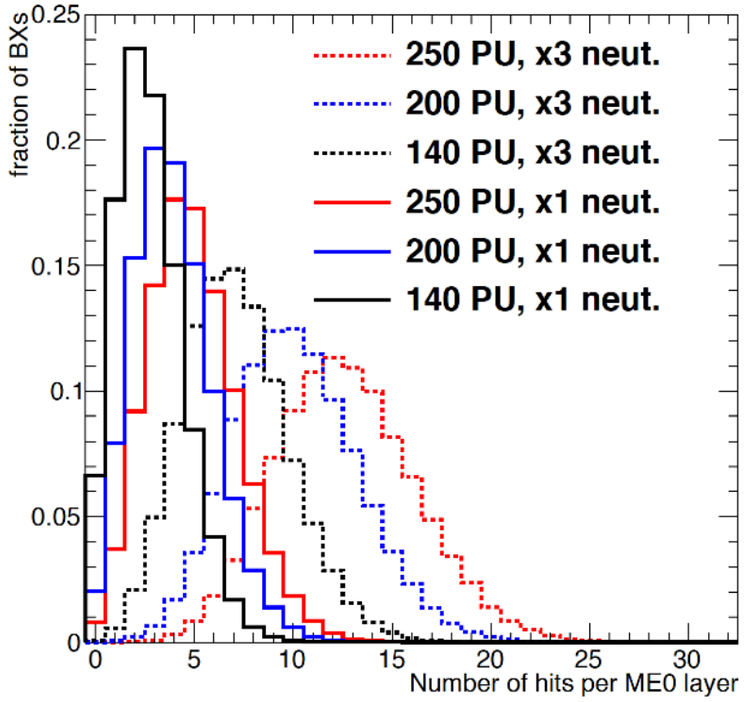
Reduced set SCA already built-in to LpGBT

- Choice: do we want FEC12, or do we want an FEC5 + SCA (lose SEU robustness)?

- Current plan: drop the SCA, use the EC channel for FPGA control

FPGA Choice

- Optohybrid concentrator card compresses trigger bits by encoding "clusters"
  - Each cluster requires at least 14 bits (11 bits position, 3 bits size)
  - Current design (Virtex-6, 2 fibers) allows transmission of only 8 clusters per bx
    - 8 clusters give high overflow rates in ME0 => **Need faster or more links**
    - Adding enough links could be prohibitively expensive in backend card costs
      - Don't want to add additional cards just to accommodate old chip
  - TDR suggests using Virtex-6 + 2x LpGBT as trigger link serializers
    - Probably not possible due to number of IO required
    - Should be confirmed.. but it is a complicated solution in any case
    - Trigger compression is very logic intensive
      - Virtex-6 Logic is also small to handle the # of clusters
      - Probably won't work as designed



Very likely need to change FPGA…

Firmware Requirements

- Latency & logic requirements scale with # of clusters being found
  - Finding large numbers of clusters becomes very difficult
- ex. GE1/1: finding 8 clusters in 1536 S-bits
  - ~65% of Virtex 135T = ~87k logic cells
- ME0: finding 24 clusters globally in chamber
  - scaling to ~260k logic cells; necessitates e.g. Kintex 325t or larger
  - Logic will get REALLY complex → SEU issues abound
  - Not trivial, not guaranteed to fit, especially not with full resolution
  - Should consider adding more trigger links to reduce compression ratio & simplify logic, reduce latency
    - 4 links / ME0 layer makes the firmware much simpler by allowing the chamber to be partitioned

ME0 OH firmware HAS to be prototyped before committing to a design

Common Firmware

- With care, it seems like a common OH firmware could be used for GE1/1, GE2/1, and ME0
- If possible can this be planned to reduce redundant work ?
- Single owner probably easiest ?

Design Resolution

Full resolution in trigger: <u>is this something we want/need</u>?

- VFAT3 can support full resolution trigger data using DDR mode (640 Mbps)
- Planning of Optohybrid and GEB needs to be done carefully
  - Higher deserialization ratio (16:1) and line rates require more care in clocking, routing
  - OH Logic requirements are increased (~doubled)
  - Backend logic requirements are increased (~doubled)
    - Cluster format changes (15 bits / cluster)
      - 3.2 Gbps links can now only encode 3 clusters, 6.4 Gbps and 9.6 Gbps do not change
    - GEB design is significantly more challenging w/ 640 Mbps signals
- For FPGA logic:
  - Prefer splitting chamber into fourths; 768 S-bits each, 12 clusters per quadrant per bx
- This needs to be decided and planned for

ME0 Trigger: Full Design vs 1/2 Resolution

Max p_T ID: 30 GeV vs 15 GeV

More flexibility in L1 menu and HLT track seeding

~1/2 L1 trigger rates

Better p_T resolution + ID: lower single and double muon rates

Online neutron bkg. rejection

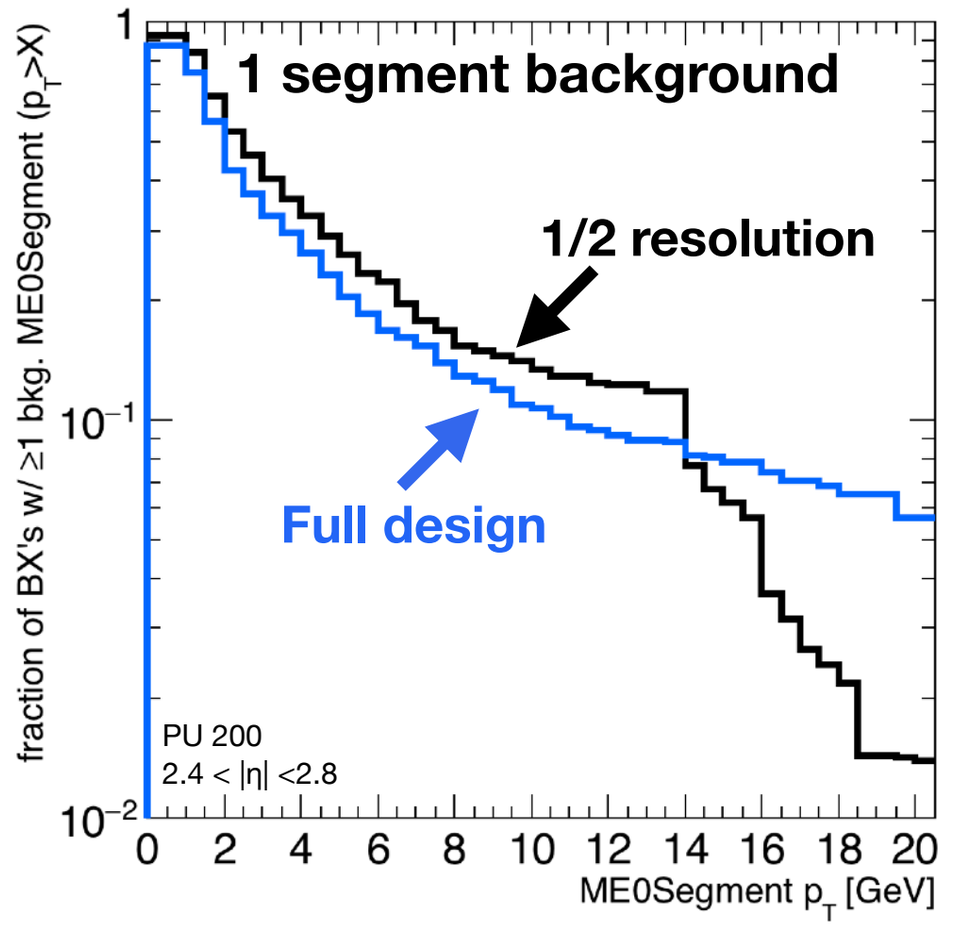
Neutron induced hits → wide clusters that can be cleaned on backend board

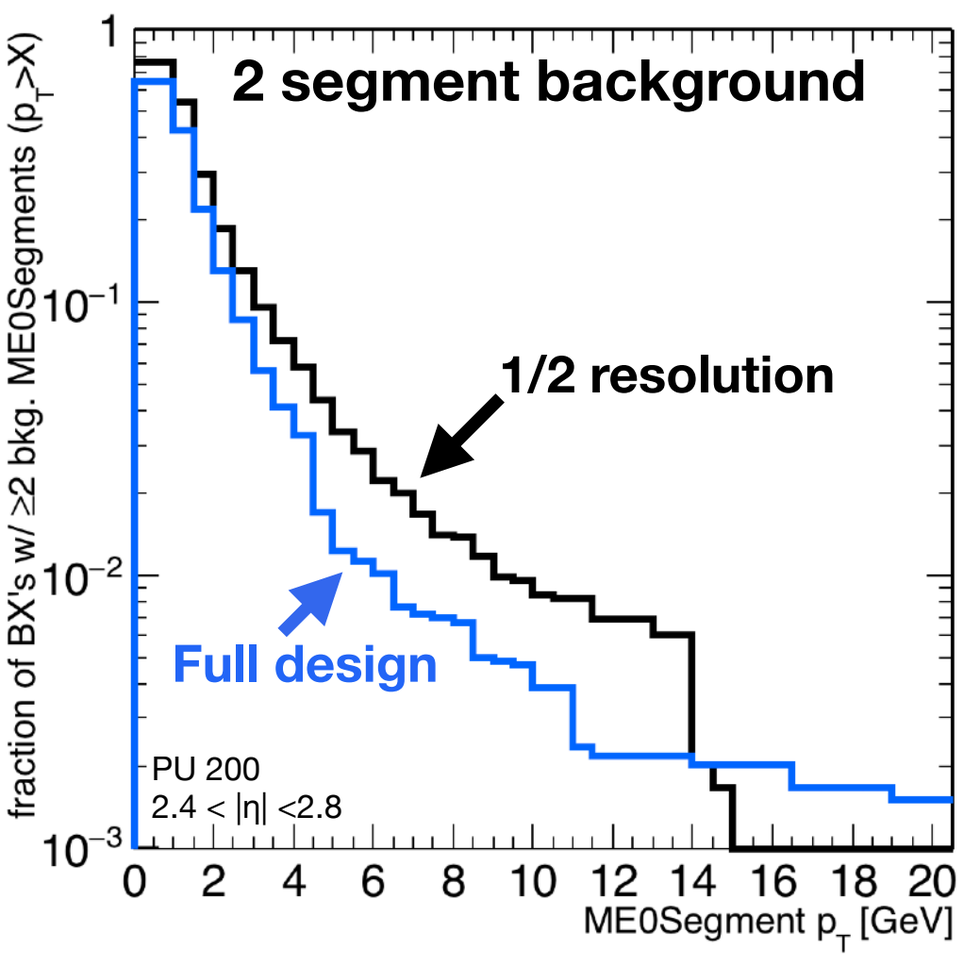
1/2 resolution: ≤ 4 strip clusters must enter segment reconstruction

ME0 is designed for L1:

Need full design for maximum versatility @ HL-LHC

(this slide=Nick McColl)





FPGA Choice

my increasing preference 

	V6 130T XC6VLX130T-2FF1156C	(ge11 fpga) V6 130T XC6VLX130T-1FF1156C	A7 200T XC7A200T-1FFG1156C	K7 325T XC7K325T-2FFG900C	**2 of** K7 160T XC7K160T-2FBG484C
Speed grade	-2	-1	-2	-2	-2
Logic Cells	**128k**	**128k**	**215k**	326k	162k x2
Link Speed	6.4 Gbps	3.2 Gbps	6.4 Gbps	9.6 Gbps	9.6 Gbps
# clusters / link / bx	8	4	8	12	12
# links needed	3	6	3	2	4
# of TX links per ME0 module (trig + data)	24	**42**	24	18	30
IO Available (>486 needed)	600	600	500	500	285 x2
FPGA Price (per board)	$1647	$1054	$293	$1343	$520
FPGA Cost (total, 240 boards)	$395280	$252960	$70320	$322320	$124800
Link Cost (est $100 per link)	300	600	300	200	400
Cost (OH + Links), not including backend	**460080**	382560	135120	365520	211200

FPGA Summary

- 1x Artix-7 200T
  - ✓ Most inexpensive
  - ✳ Needs more links… ok unless it changes backend card requirements
  - ✳ Logic is most likely insufficient for ME0 (good choice for GE2/1?)
- 1x Kintex-7 325T
  - ✓ More logic and faster links than Artix-7
  - ✓ Monolithic FPGA is most flexible (but firmware will be a challenge)
  - ✳ FPGAs are expensive
- 2x Kintex-7 160T
  - ✓ Inexpensive
  - ✓ Simple firmware, handling only half-chamber, most logic of any option
  - ✓ 70 additional spare pins—eases routing and provides capabilities for additional features (e.g. SLVS fanout)
  - ✓ Small packages / two FPGAs are easier to route (less congestion)
  - ✳ Trigger compression logic and routing partitioned into half-chamber; need more trigger links
    - ✳ 12 clusters per 1/2 chamber is insufficient for ME0 → need 4 trigger links (still fits well into backend)

Decisions

- Choice of FPGA:
  - If it fits into the backend (30 tx links per ME0)
    - ✦Use dual Kintex-7 160T (24 clusters / bx / half-chamber)
  - else
    - ✦Use single Kintex-7 325T (24 clusters / bx / full-chamber)

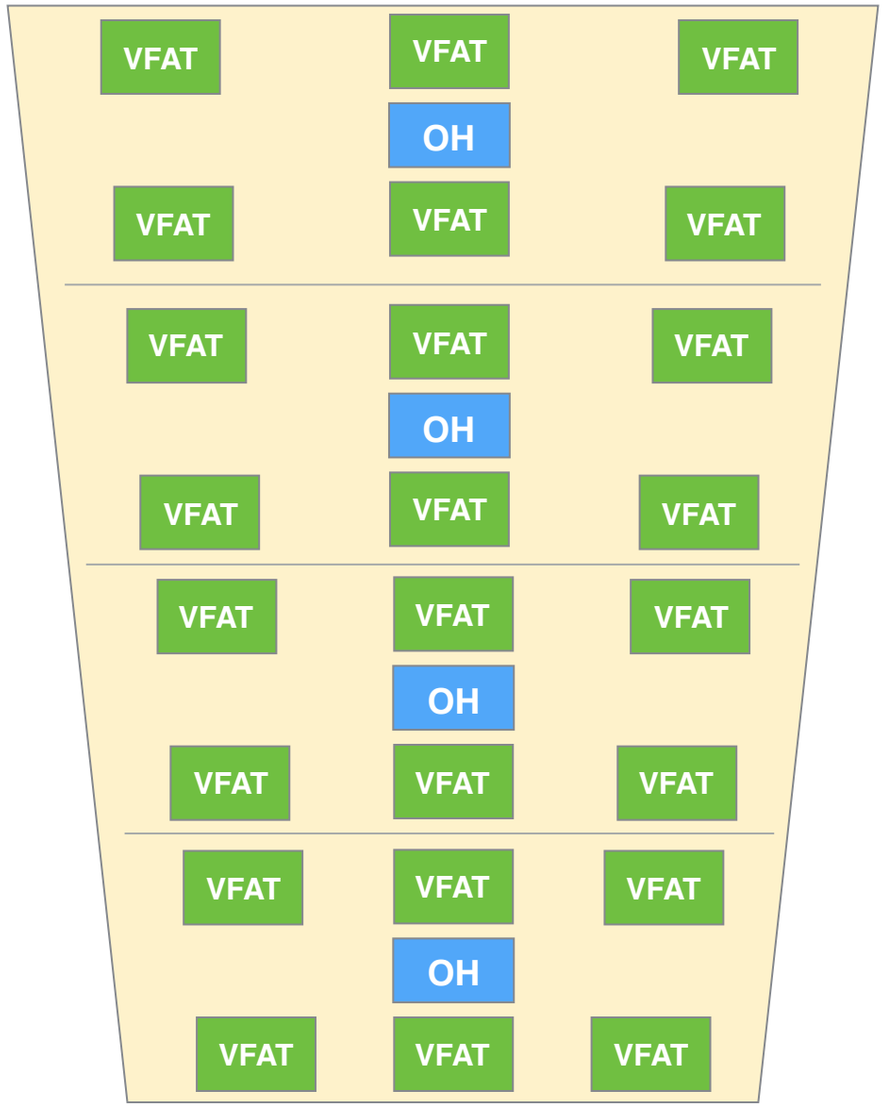
- Or… ask: why do we have an FPGA?
  - FPGA not doing anything fancy… just reducing link count
  - Complex logic on FPGA in harsh radiation environment is unhappy
  - Is there a way to eliminate the FPGA entirely?

FPGA-less ME0 at 1/2 Resolution

One LpGBT can handle trigger/DAQ from 3 VFATs

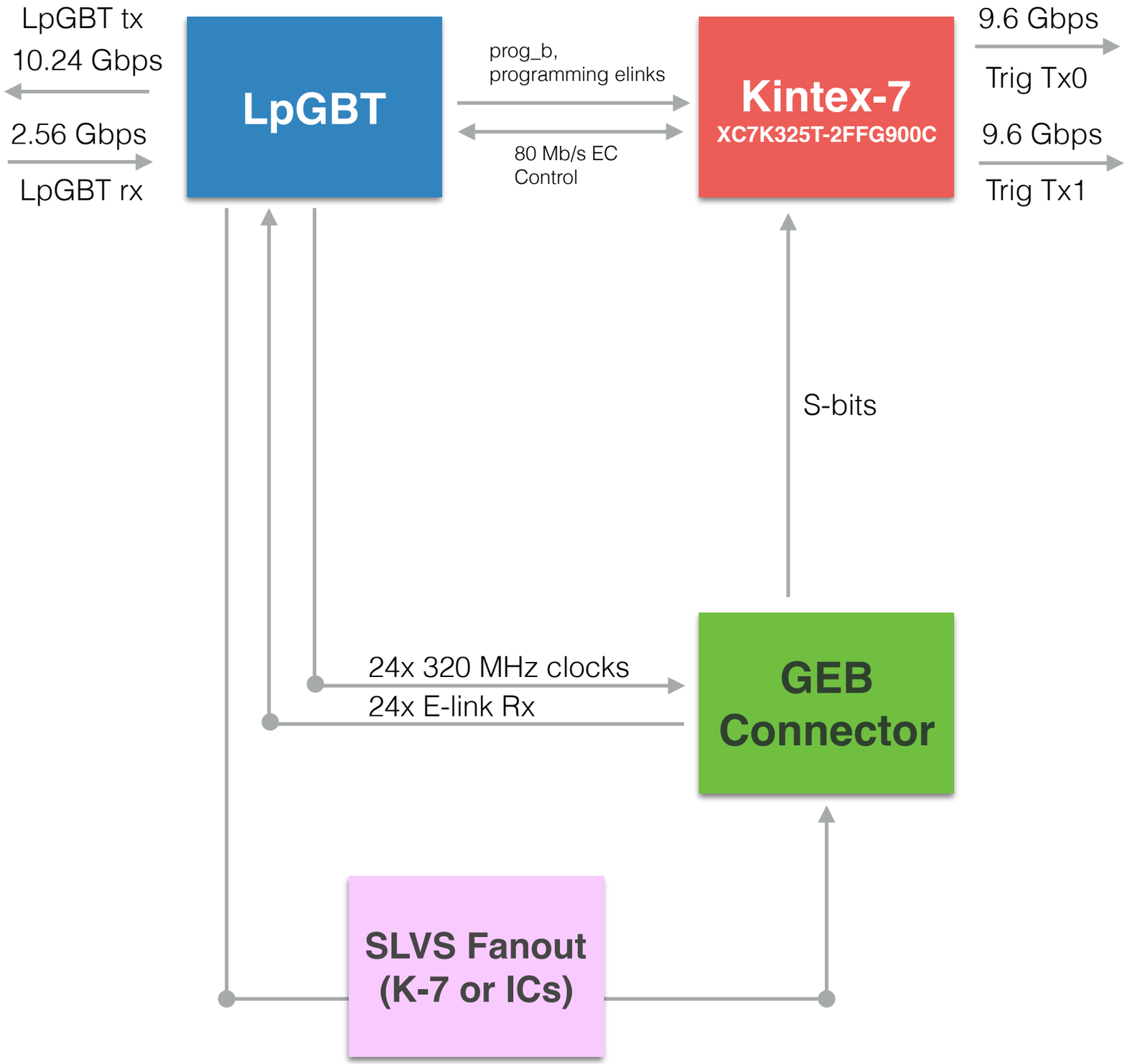
- 3 VFATs * 9 elinks per vfat (1 rxd, 8 trigger bits) = 27 e-links needed
- Operating GBT in FEC5 gives us 28 e-links
- Give up SoT… easy enough to reconstruct it on our own in firmware

- Use a very small (~vfat hybrid sized), very simple Optohybrid
  - Implementing only 2x LpGBT + Optics + baseboard connectors
  - Very low cost per unit
  - Covers only 1 or 2 ME0 partitions
  - Individual Rx elinks for each VFAT
- Needs 8 fiber / layer → 48 fibers per ME0
  - **LpGBT receiver links complicated by asymmetric backend links e.g. in BCP.** APD transmitter mezzanine ???

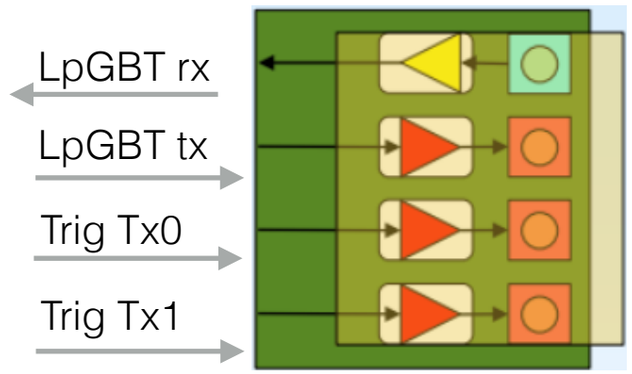


- No high speed signals crossing entire GEB… localized to very small portions of chamber
  - **GEB is functionally split in 4—only DC crossing partition boundaries**
- **All** components on detector are rad hard by design; distributed design has no single point of failure
- Crude cost estimates show ~no change in price (extra link cost offset by savings in OH FPGAs)

Monolithic FPGA Block Diagram

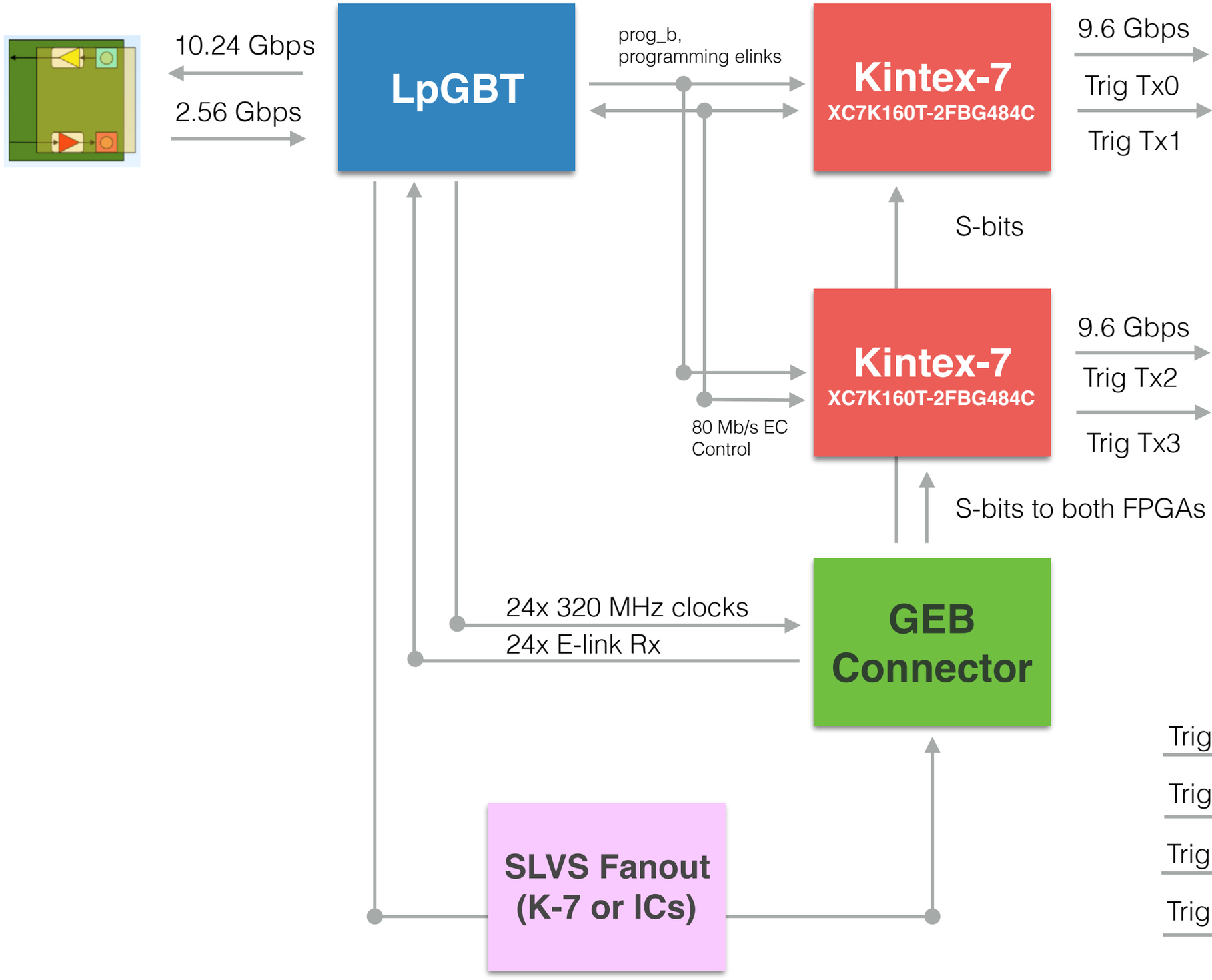


CERN VL+ Optics

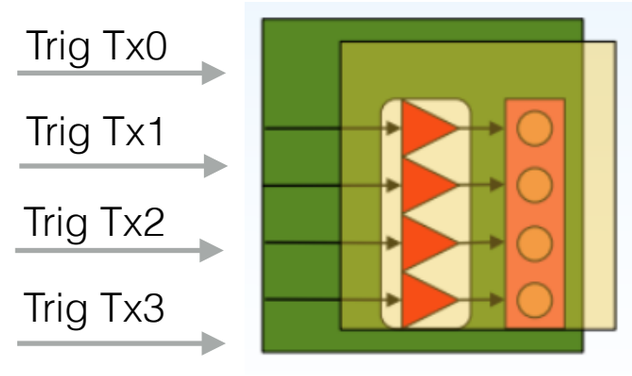


3 TX (single channel LDDs) + 1 RX

Dual Kintex-7 Block Diagram



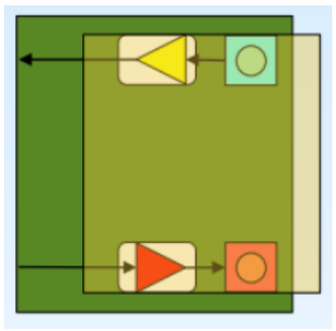
CERN VL+ Optics



4 TX

FPGA-less Optohybrid

CERN VL+ Optics



LpGBT tx
10.24 Gbps

2.56 Gbps
LpGBT rx

LpGBT

trig 320 Mbps x24

clock 40 MHz x3

tx/rx 320 Mbps x3

GEB Connectors

ME0 OH Prototyping Proposal

Dependence on timelines of (1) LpGBT, (2) VL+, and (3) ME0 GEB will slow progress of development…

- Propose de-coupling part of the R&D from these external dependencies and developing an intermediate design

- 1st generation prototype:
  - Target full compatibility with GE1/1 GEB
    - GBTx chip, match existing pinout and form factor, re-use much of the existing layout
    - Allows testing & development far ahead of likely GEB schedule
  - Upgrade FPGA & use commercial 10 Gbps optics (e.g. a 4x 10Gbps QSFP+)
    - Can test fanout of SLVS output control signals to VFAT3, verify SLVS input compatibility of new FPGA family
    - Can test and gain experience w/ new FPGA & port firmware to new FPGA
    - Can verify SEU rates and TID robustness of new FPGA family
    - Can validate design on existing, working electronics systems and detectors; no dependence on new GEB / mechanical specs
      - Should be plug and play with current GE1/1

- 2nd/3rd generation prototypes:
  - When VL+ is ready… upgrade optics
  - When LpGBT is ready: leave FPGA design alone from 1st generation, upgrade GBTx —> LpGBT
  - When GEB prototype specs are ready: update w/ real mechanical dimensions, pinouts of new GEB

Summary & Discussion Points

1. LpGBT control fanout
    - FPGA or IC
2. SCA
    - OK to remove?
3. FPGA choice, # of trigger fibers
    - Kintex-7?
4. no FPGA
    - Will this work? do we want it?
5. Full or degraded resolution
    - 640 Mbps signal integrity on GEB?
    - Implications for logic requirements

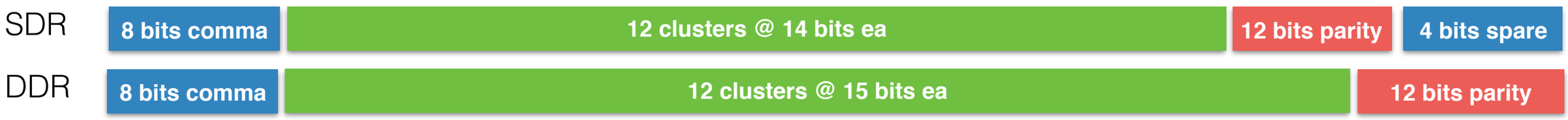
Backup & References

7 Series Radiation Tests

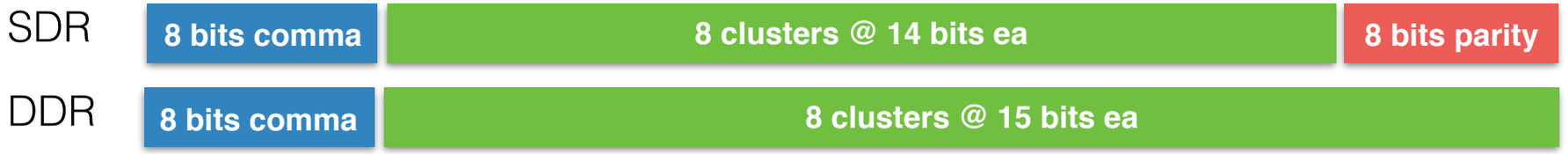
- Kintex-7 Radiation Tests
  - http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=7004593
  - https://indico.esa.int/indico/event/59/session/8/contribution/28/material/slides/0.pdf
  - http://iopscience.iop.org/article/10.1088/1748-0221/9/01/C01025/pdf
  - http://cds.cern.ch/record/1995019/files/AIDA-CONF-2015-018.pdf?subformat=pdfa
  - https://indico.cern.ch/event/489996/contributions/2291854/attachments/1345433/2030665/Kintex-7_irradiation_results_IFIN-HH.pdf
  - https://indico.gsi.de/event/5137/contribution/6/material/slides/0.pdf

Examples of Trigger Data Formats

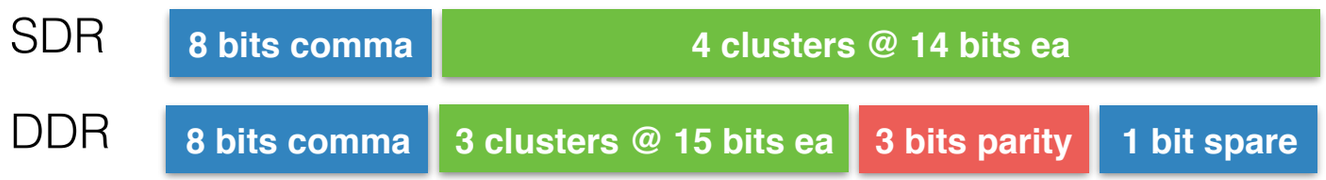
9.6 Gbps provides 192 bits / bx



6.4 Gbps provides 128 bits / bx



3.2 Gbps provides 64 bits / bx



GE1/1 Format

FPGA-less Option at Full Resolution

One LpGBT can handle trigger/DAQ from 3 VFATs

- Much more data
  - **Trigger:** 2x LpGBTs handle 3 VFATs
  - **Control:** 1x LpGBT handles 24 VFATs
- Per layer, 17 LpGBT. 102 per ME0.
  - Yikes!
  - Full BCP per ME0
  - Control link (backend → lpgbt) is complicated by asymmetric link quantity

Xilinx Product Tables

- 7 Series Product Table:
  - https://www.xilinx.com/support/documentation/selection-guides/7-series-product-selection-guide.pdf

- Virtex 6 Product Table:
  - https://www.xilinx.com/support/documentation/selection-guides/virtex6-product-table.pdf

Artix-7

Symbol	Description	Output Divider	Speed Grade								Units
			-3 (1.0V)		-2 (1.0V) -2LE (1.0V)		-1 (1.0V) -1LI (0.95V) -1Q (1.0V) -1M (1.0V)		-2LE (0.9V)		
			Package Type								
			FF FB SB	FG FT CS CP	FF FB SB RB RS	FG FT CS CP	FF FB SB RB RS	FG FT CS CP	FF FB SB	FG FT CS CP	
F_{GTPMAX}	Maximum GTP transceiver data rate		6.6	6.25	6.6	6.25	3.75	3.75	3.75	3.75	Gb/s

Virtex-6

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
F_{GTXMAX}	Maximum GTX transceiver data rate	6.6	6.6	5.0	5.0	Gb/s
$F_{GPLLMAX}$	Maximum PLL frequency	3.3(1)	3.3(1)	2.7	2.7	GHz
$F_{GPLLMIN}$	Minimum PLL frequency	1.2	1.2	1.2	1.2	GHz

Kintex-7

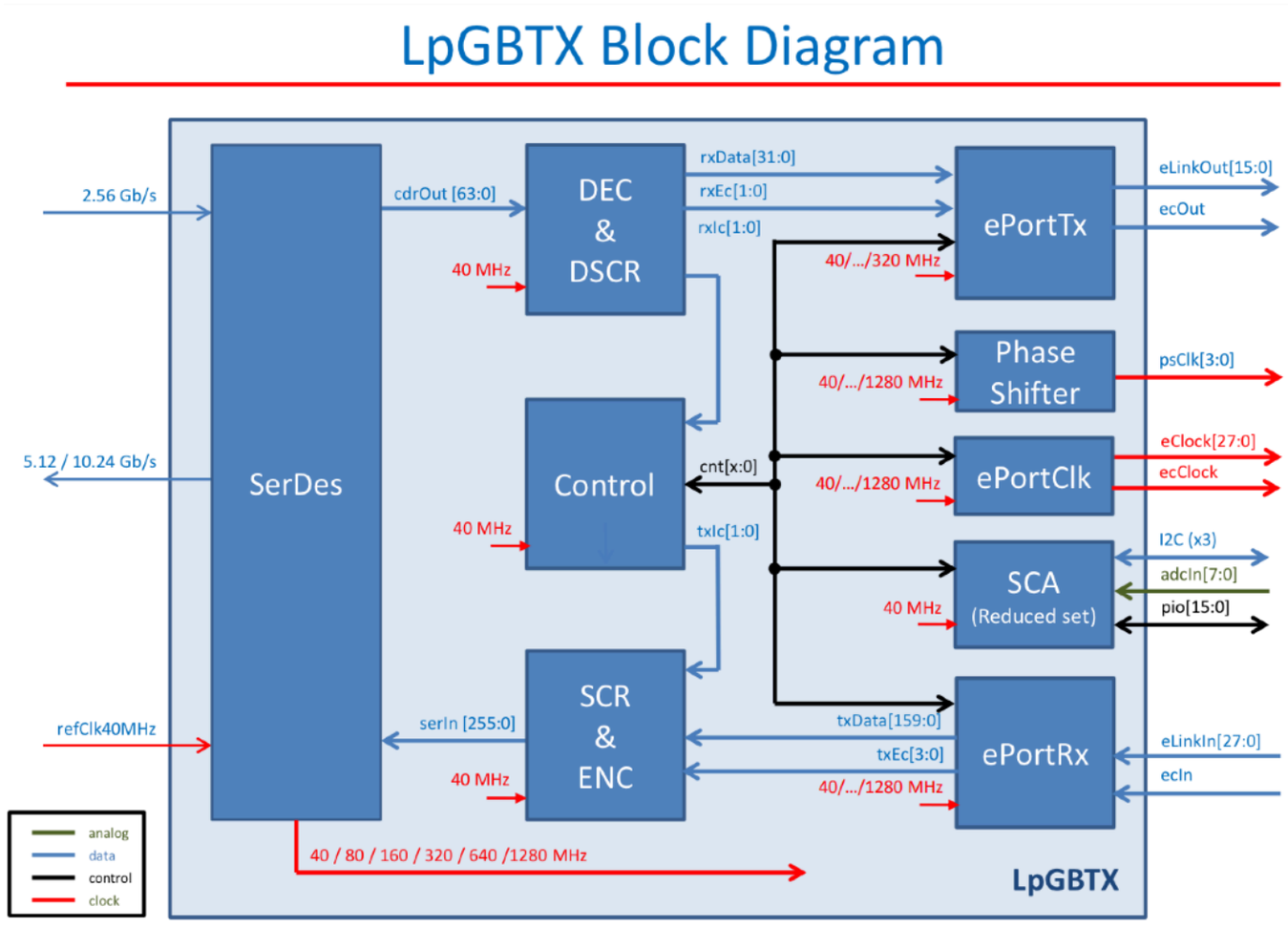
Symbol	Description	Output Divider	Speed Grade(1)								Units
			-3 (1.0V)			-2 (1.0V) -2LE (1.0V) -2LI (0.95V)		-1 (1.0V)(2) -1M (1.0V)(2) -1LM (1.0V)(2)		-2LE (0.9V)(3)	
			Package Type								
			FF	FBG484	FBG676 FBG900	FF RF FBG484	FBG676 FBG900	FF RF	FB	FF RF	FB
F_{GTXMAX}(4)	Maximum GTX transceiver data rate		12.5(5)	10.3125(6)	6.6	10.3125(6)	6.6	8.0	6.6	6.6	6.6	Gb/s

LpGBT Specs Summary

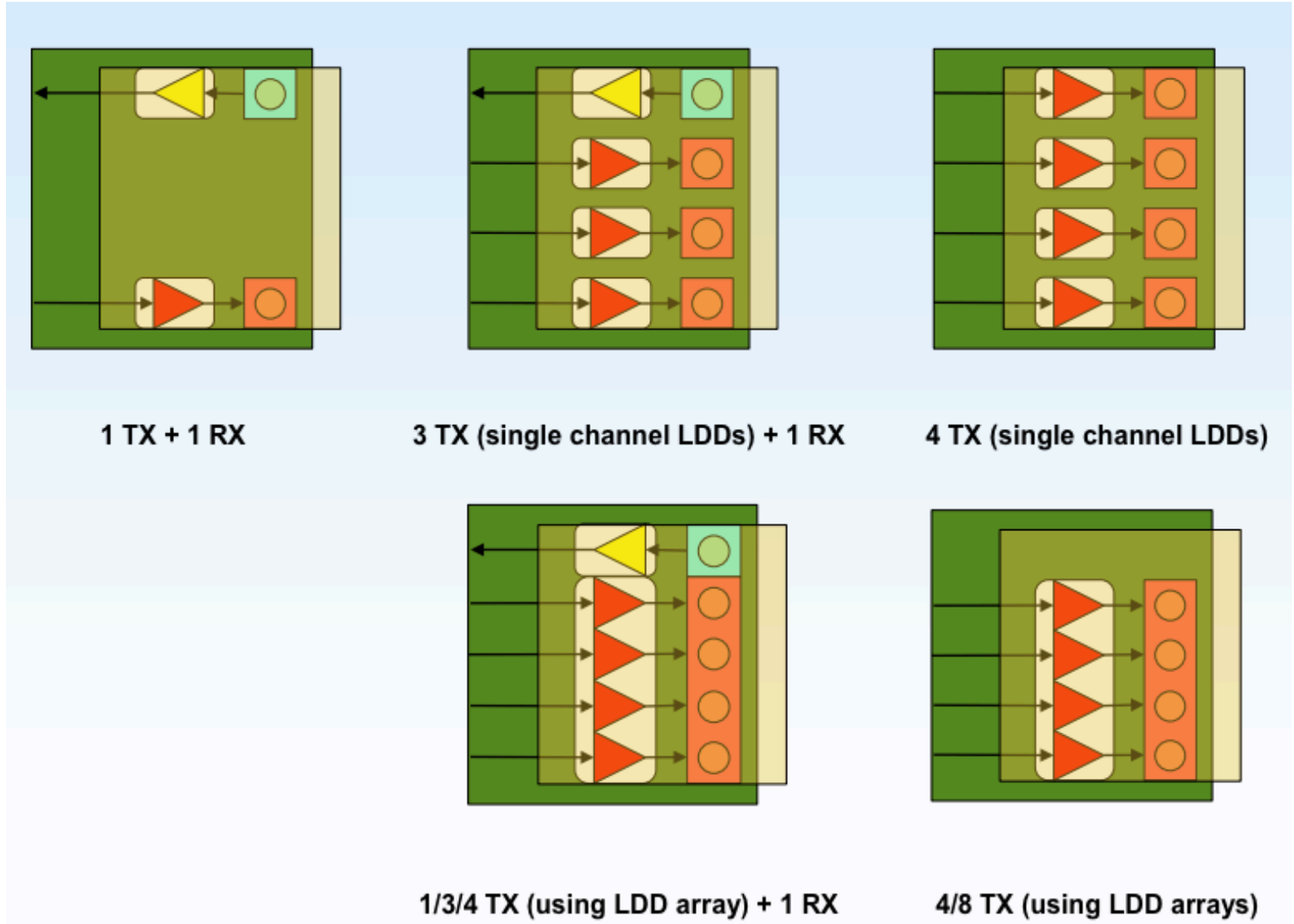
E-Links:

- Down-link:
  - Bandwidths: 80/160/320 Mb/s
  - Number of links*: 16/8/4
    - "Mirror" function:
      - 80 Mb/s: no;
      - 160 Mb/s: each channel is available on 2 outputs;
      - 320 Mb/s: each channel is available on 4 outputs.
  - One EC channel @ 80 Mbit/s
- Up-Link:
  - FEC5 @ 5.12 Gb/s:
    - Data rate: 160 / 320 / 640 Mb/s
    - # eLinks*: 28 / 14 / 7
  - FEC5 @ 10.24 Gb/s:
    - Bandwidth: 320 / 640 / 1280 Mb/s
    - # eLinks*: 28 / 14 / 7
  - FEC12 @ 5.12 Gb/s:
    - Bandwidth: 160 / 320 / 640 Mb/s
    - # eLinks*: 24 / 12 / 6
  - FEC12 @ 10.24 Gb/s:
    - Bandwidth: 320 / 640 / 1280 Mb/s
    - # eLinks*: 24 / 12 / 6
  - One EC channel @ 80 Mbit/s
  - Phase alignment on a per channel basis:
    - User programable phase
    - Automatic phase tracking

✦ https://espace.cern.ch/GBT-Project/LpGBT/Specifications/LpGbtxSpecifications.pdf



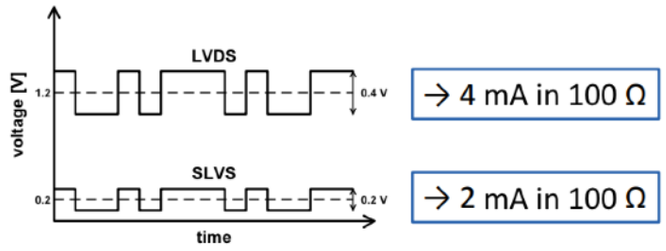
CERN VL+ Specs Summary



https://espace.cern.ch/project-Versatile-Link-Plus/Shared%20Documents/Presentations/2016_VLplus_AtlasUpgradeWeek_17Nov16.pdf

Voltage Standards & SLVS

Differing specs on LVDS (supported on FPGA) and SLVS (on VFAT/GBT). Uhg..



https://indico.cern.ch/event/225746/contributions/475189/attachments/371268/516635/IPblocks.pdf

Kintex-7 and Virtex-6 standards are very similar…

- Virtex-6 works.. so Kintex should be ok.. but not sure
- VFAT3 manual has no specs

	Virtex-6 LVDS_25	Kintex-7 LVDS	Kintex-7 LVDS_25	VFAT3 SLVS Requirement
Output Voltage High (Max), V	1.675 V	1.675 V	1.675 V	?
Output Voltage Min (Min)	0.825 V	0.825 V	0.7 V	?
Vdiff Out (Min/Typ/Max) mV	247/350/600 mV	247/350/600 mV	247/350/600 mV	?
Vcommon Out (Min/Typ/Max) V	1.075/1.25/1.425 V	1/1.2/1.425 V	1/1.2/1.425 V	?
Vdiff In (Min/Typ/Max) mV	100/350/600 mV	100/350/600 mV	100/350/600 mV	? / 200 / ?
Vcommon In (Min/Typ/Max) V	0.3/1.2/2.2 V	0.3/1.2/1.425 V	0.3/1.2/1.5 V	?