GE2/1 & ME0 Readout Boards

1. Producing the layout: challenges and current setup
2. Current specifications and related open questions

Ana Ovcharova (UCSB)

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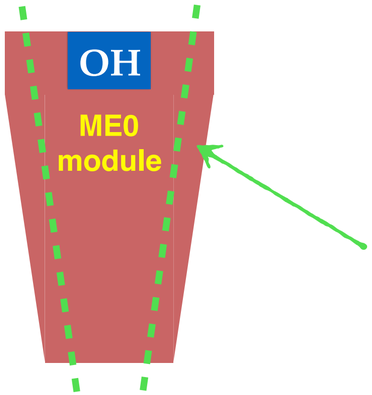
RO board layout challenge

★ ME0 and GE2/1 contain **9 different RO board geometries**
- ✦ cannot modify and reuse finished layouts → **each RO board has to be designed independently**
- ✦ Altium (PCB design software) not well suited for the challenge of odd-angle geometry combined with high density of traces → **need creative solutions to get done efficiently**

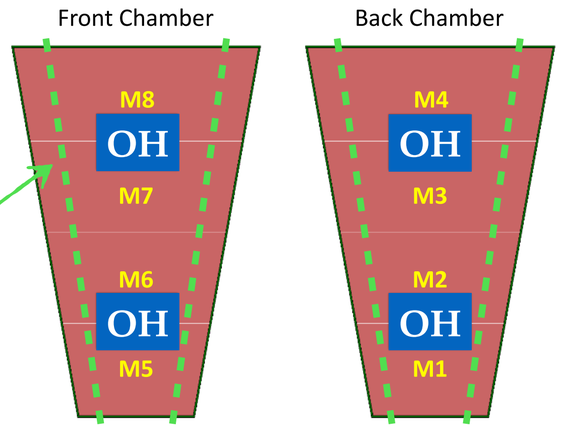
★ Very **tight geometrical constraints** for ME0 and the smaller GE2/1 modules
- ✦ connector placement constrained by chimney, OH and FlexPCB+VFAT hybrid dimensions

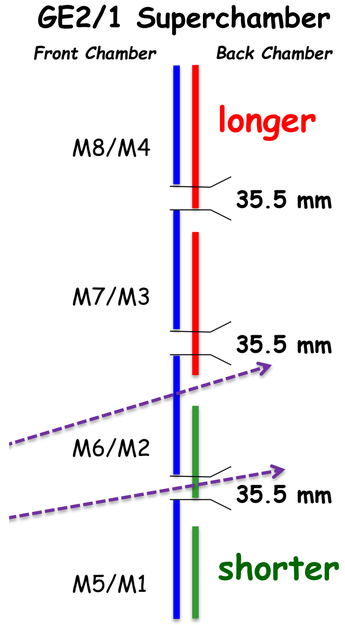
ME0 → same RO board geometry for all modules w/ 24 VFATs



chimney constraints

GE2/1 → 8 different RO boards w/ 12 VFATs each

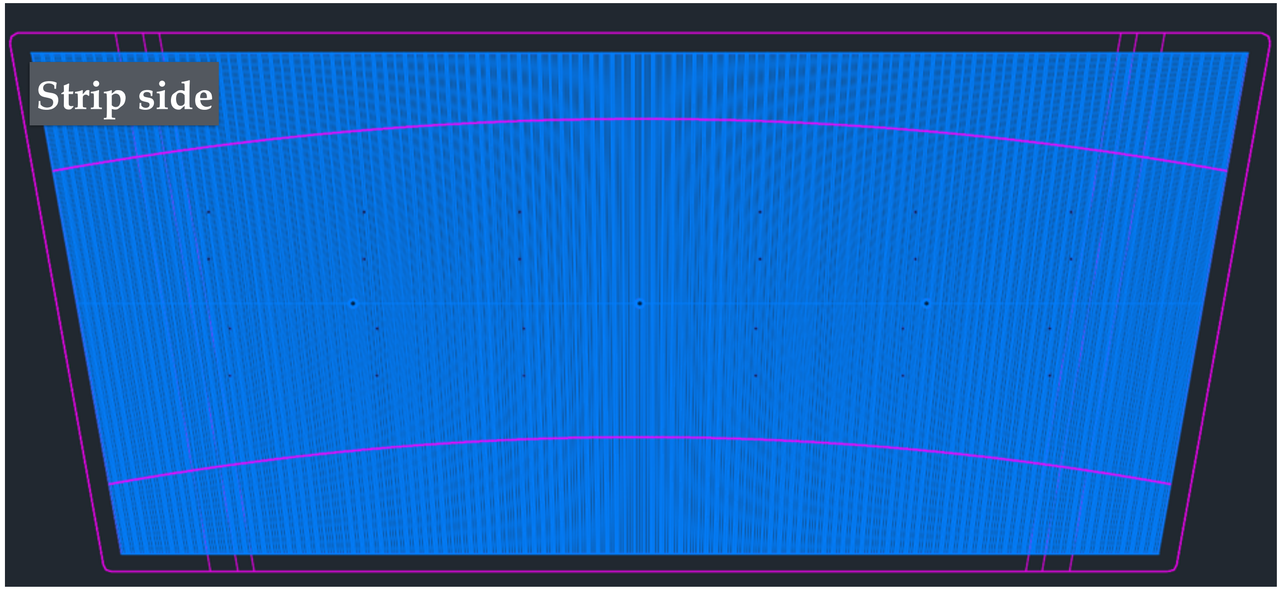


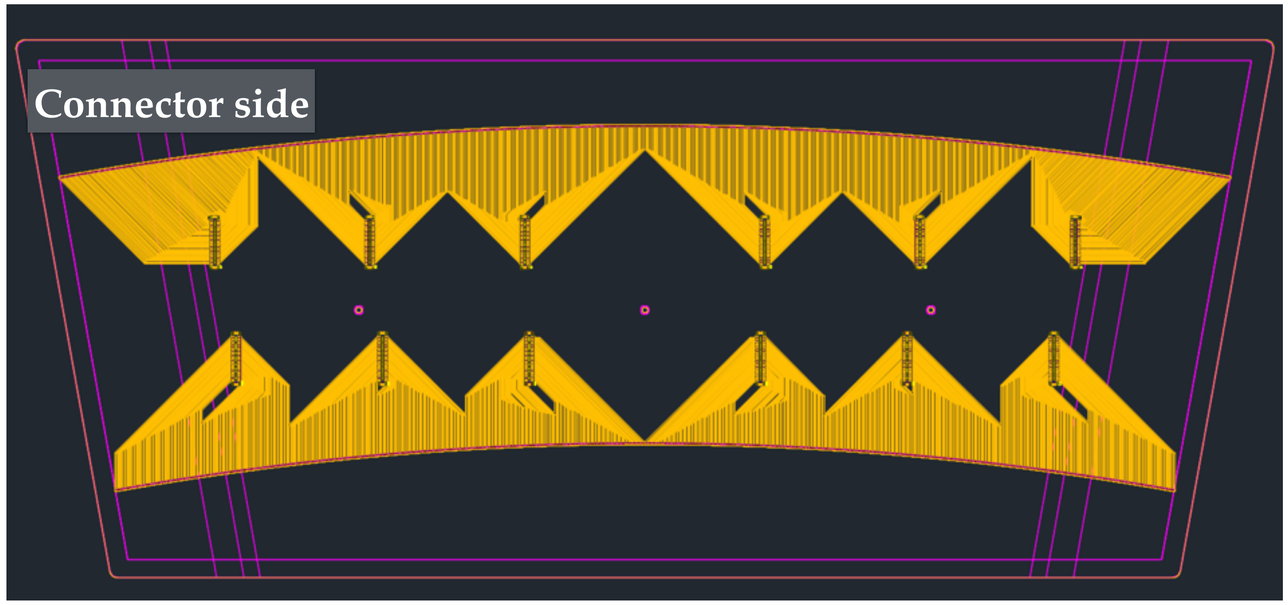


Not drawn to scale

Workflow: Overview

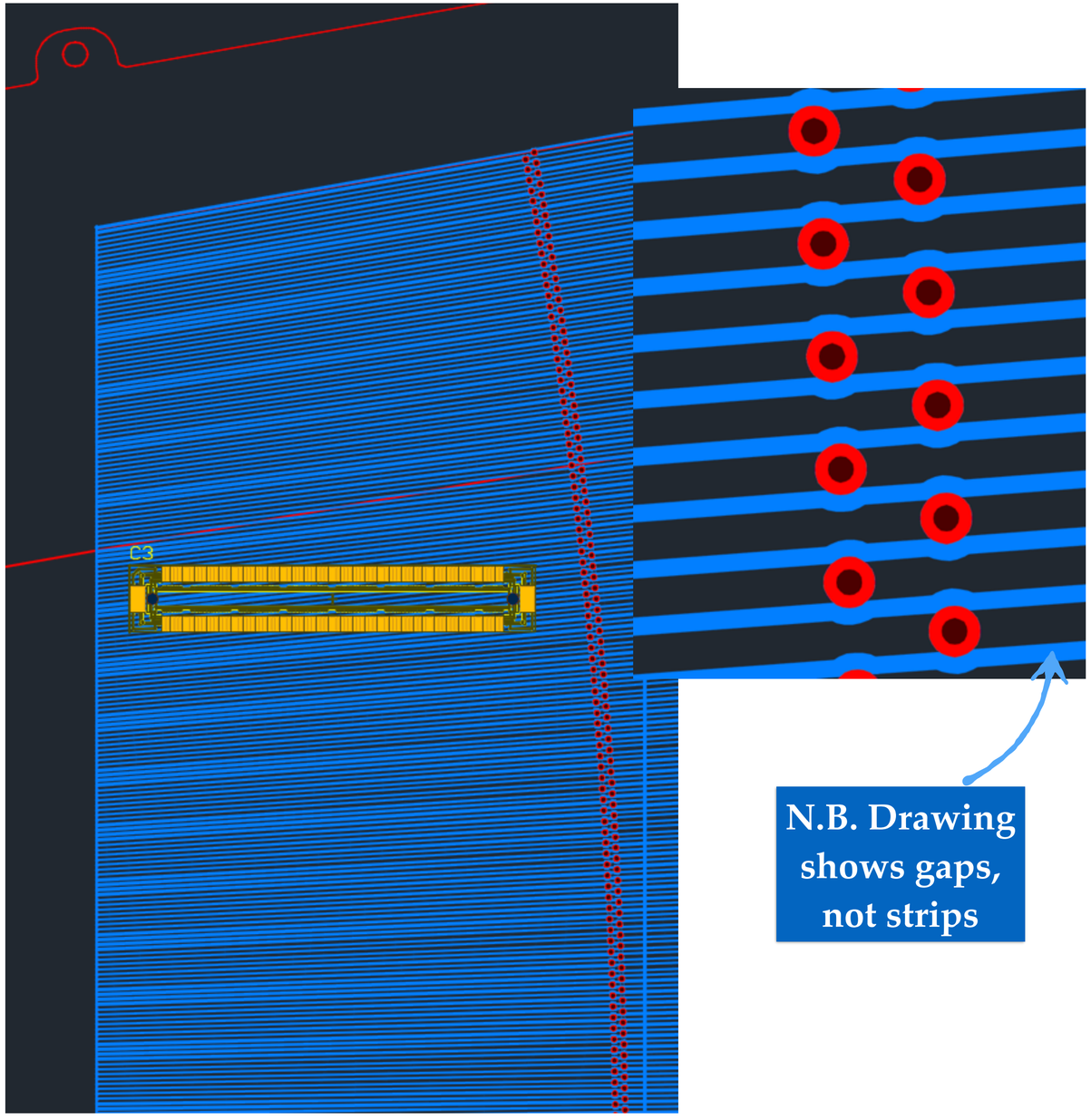
- ★ Readout Board 101
  - ✦ Bottom: radial strips with constant spacing
  - ✦ Top: signals routed to connectors
  - ✦ Density:
    - GE2/1 boards → 1536 traces
    - ME0 board → 3,072 traces
- ★ Workflow
  - ✦ produce technical drawing of strip side (DXF)
  - ✦ import in Altium and build up connector side
  - ✦ “finishing touch” - screw holes, copper plane, grounding
- ★ Producing layout “by hand” very time consuming
  - ✦ order of operations matters → even small changes may require redoing significant amount of work
  - ✦ critical to automate as much as possible





Workflow: Strips & component placement → automated

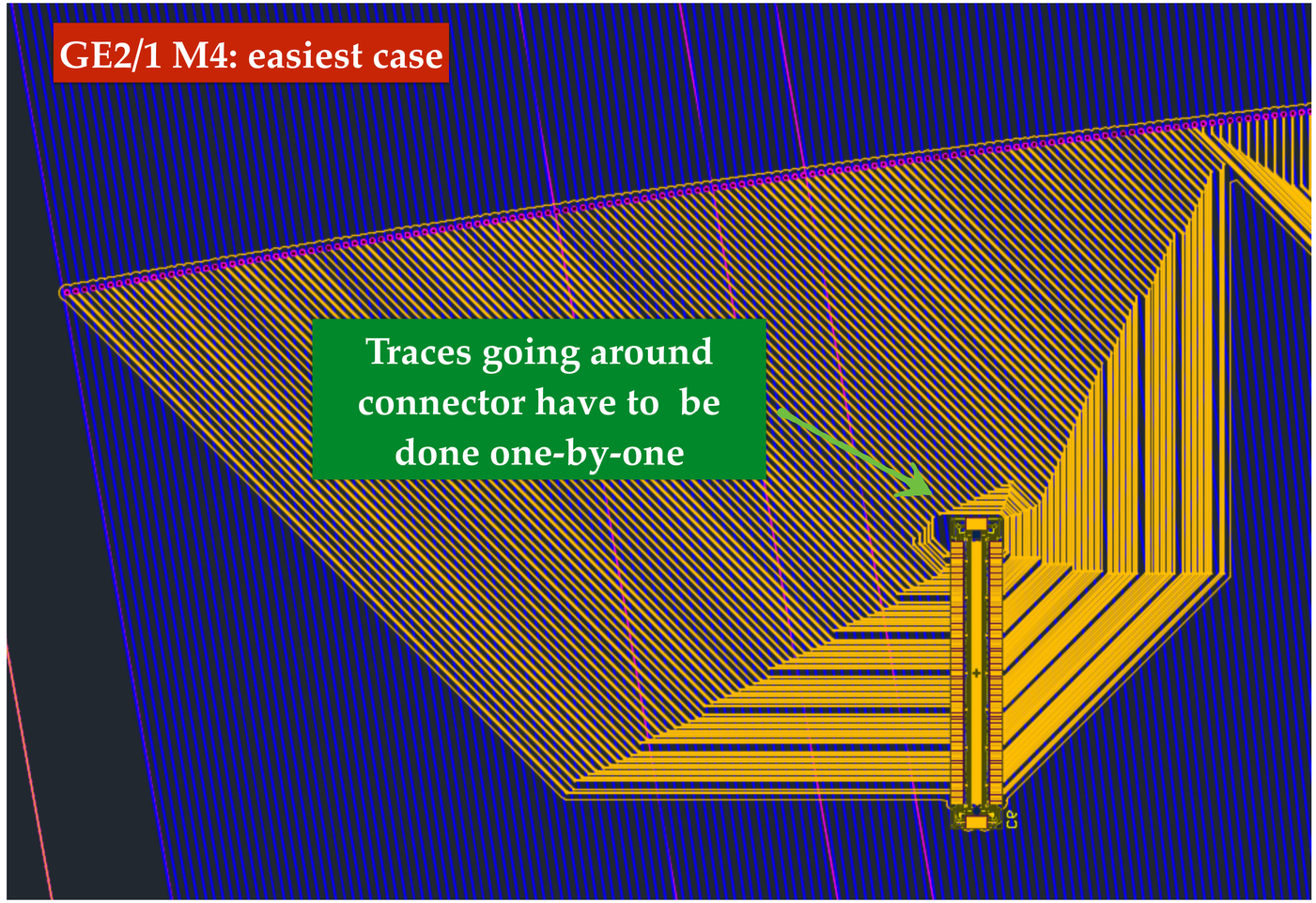
- ★ Technical drawing of strips including via overlap “drawn” in python
  - ✦ calculates if double via row needed
  - ✦ calculates if and how strip gaps need to curve around vias
- ★ PCB schematic
  - ✦ define connectivity for routing
  - ✦ generated via Altium JavaScript API
- ★ Vias and connectors placement
  - ✦ generated via Altium JavaScript API
  - ✦ caveat: flipping/rotating connectors requires extra care to retain sensible mapping between pins and vias



Workflow: Routing signals → manual

- Most time-consuming step
  - GE2/1 boards → 1536 traces
  - ME0 board → 3,072 traces

- If route has >2-3 turns, often have to do individual traces manually; else 10-20 at a time



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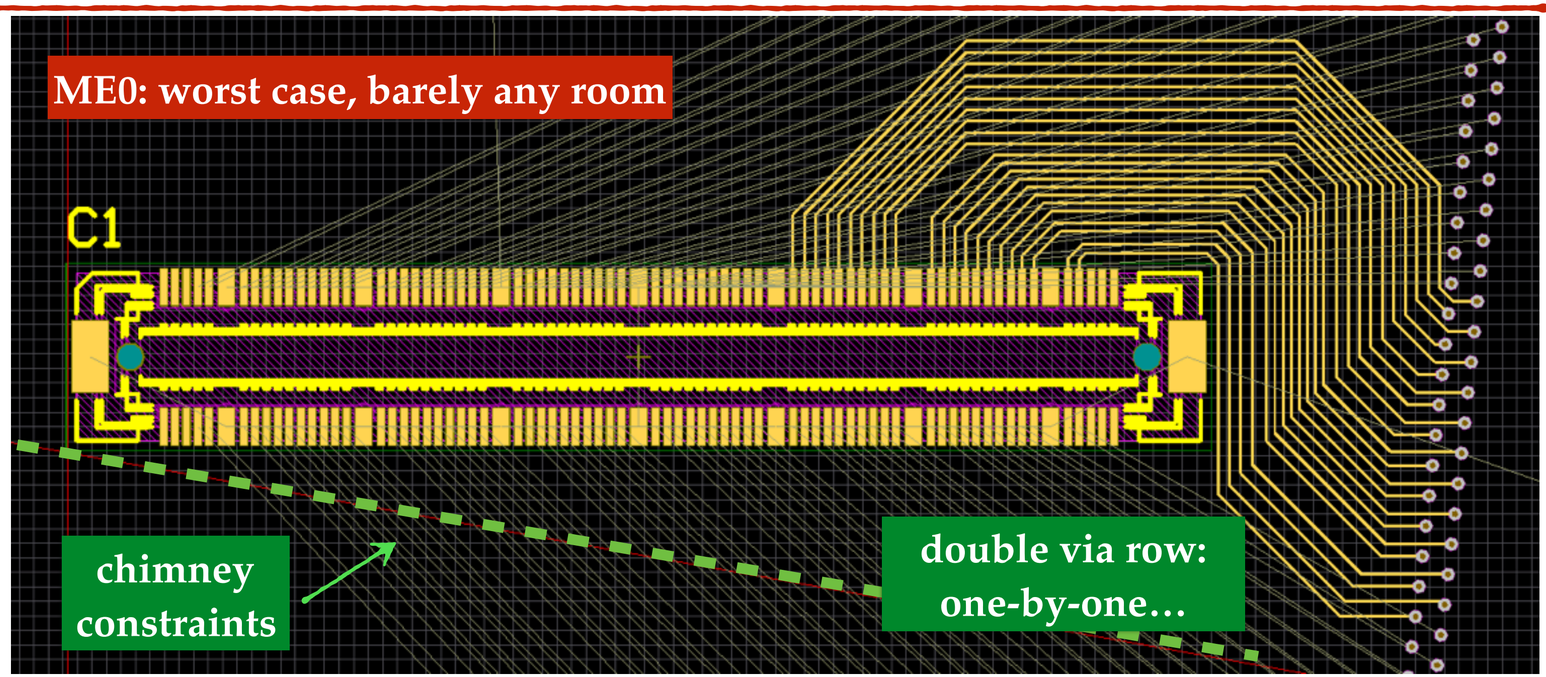
  - brainstorming if there is a solution…



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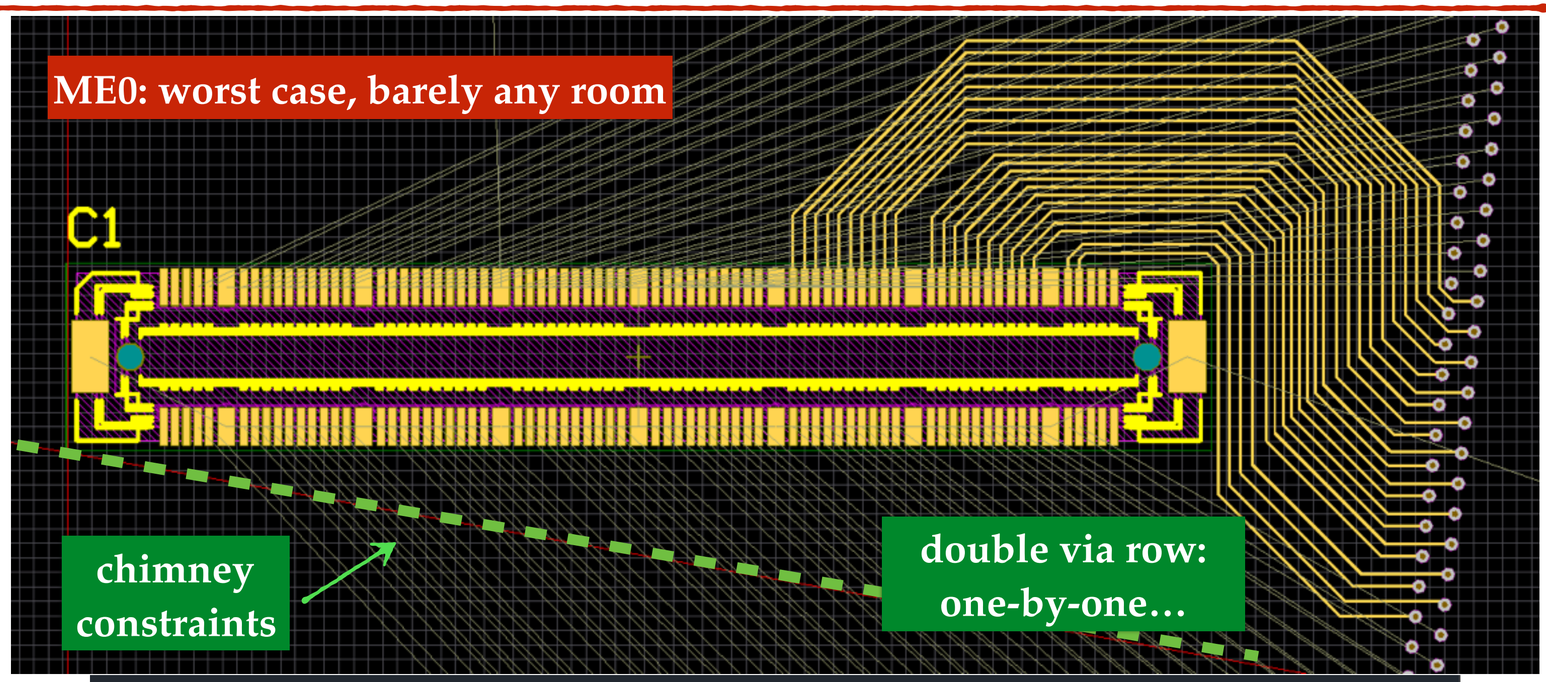
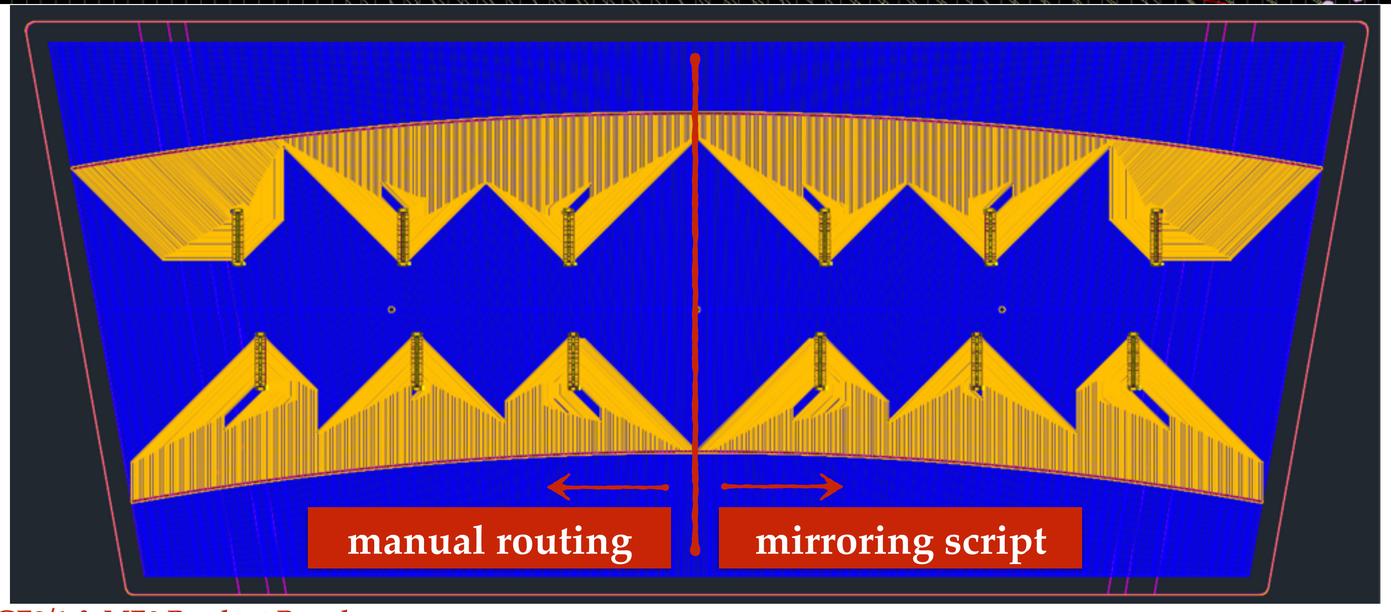
  - ✦ brainstorming if there is a solution…
- ★ When possible, trying to exploit symmetry of board to mirror routing traces with scripts
  - ✦ may not be possible for ME0, smaller GE2/1 modules

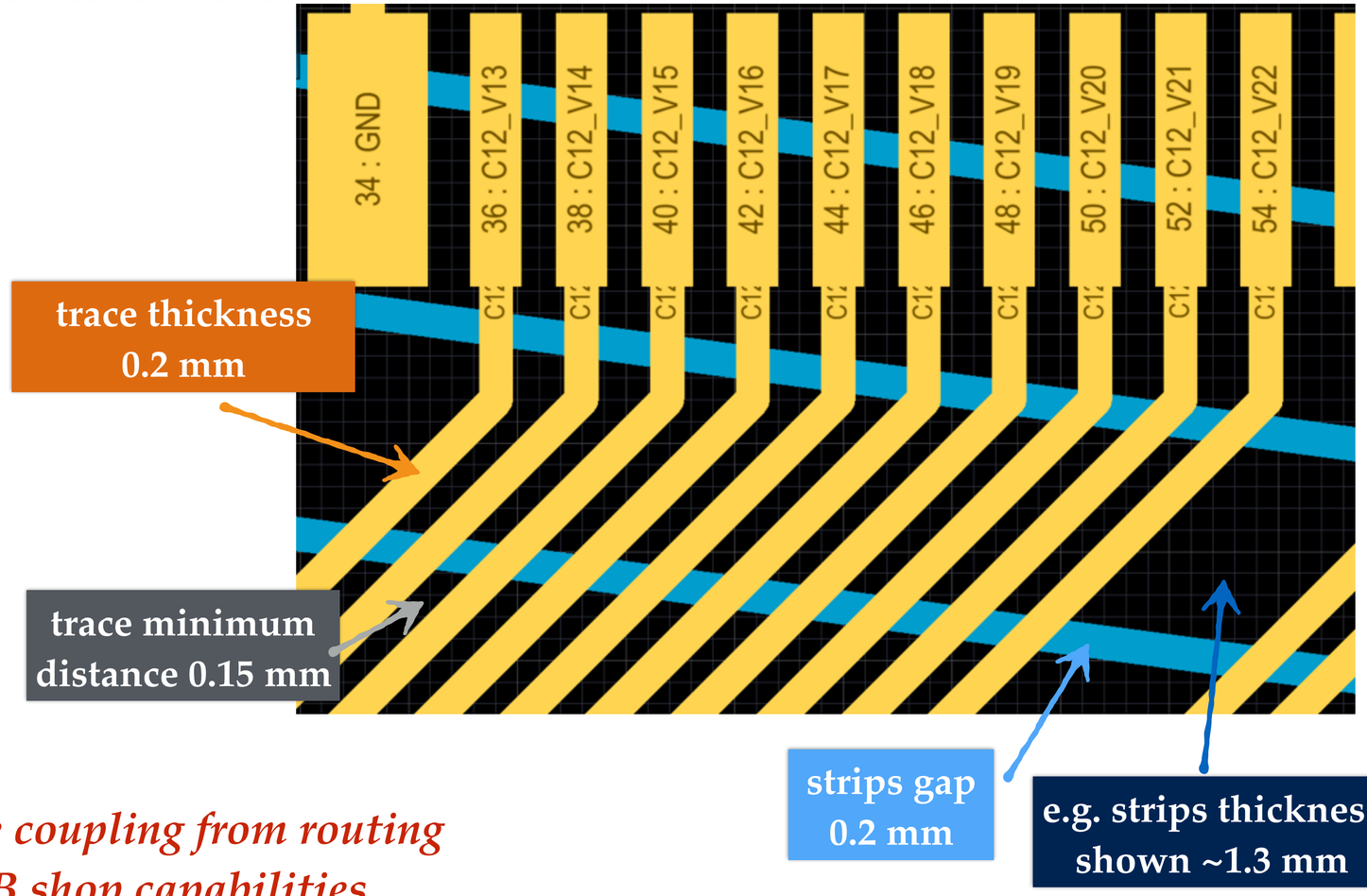




Current specifications: strips and traces

★ Strip side
- ✦ strip gaps - constant width 0.2 mm
- ✦ via diameter - hole: 0.3 mm, total: 0.6 mm
  - based on board thickness of 3.2 mm

★ Connector side
- ✦ trace thickness 0.2 mm
  - up from 0.13 mm in M4 prototype based on PCB shop request
- ✦ minimum trace gap 0.15 mm
  - increasing this makes traces longer!



Q: Is there significant contribution to capacitive coupling from routing traces? Need to optimize keeping within PCB shop capabilities

Related strip capacitance discussion by Markus (next) and Paul (next session), but not clear (to me) whether routing contributes significantly

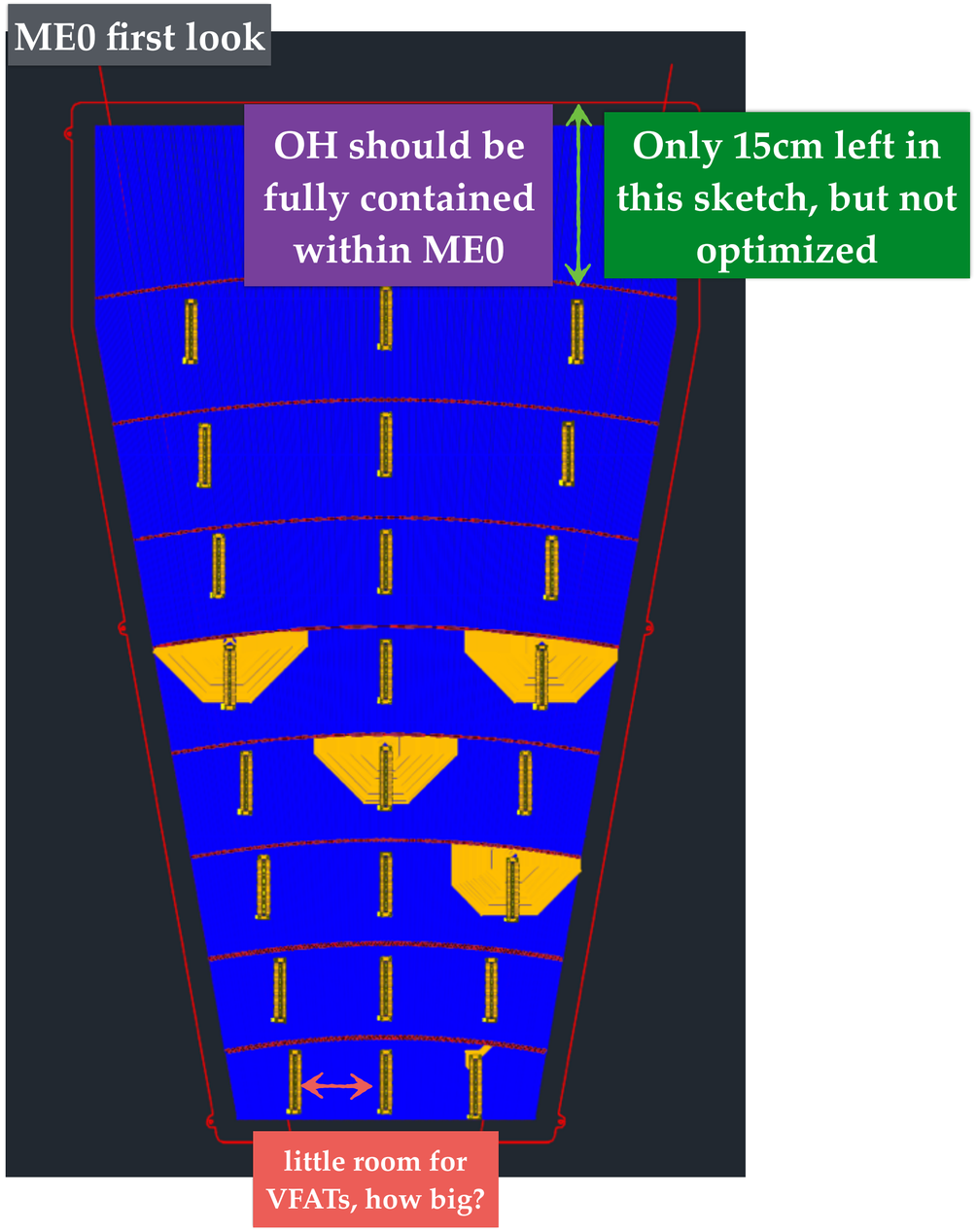
Current specifications: OH & VFAT-h dimensions

- ★ GE2/1 assumptions
  - ✦ OH height - 200 mm
    - • only half need be on the board
  - ✦ FlexPCB+VFAT hybrid - 65 mm x 78 mm

N.B. TBD this week if can fit on the smaller GE2/1 modules

- ★ ME0 first look
  - ✦ not feasible with dimensions given for GE2/1

Q: How much room do we need for ME0 OH and VFAT?
(required to check feasibility)



Current specifications: Grounding

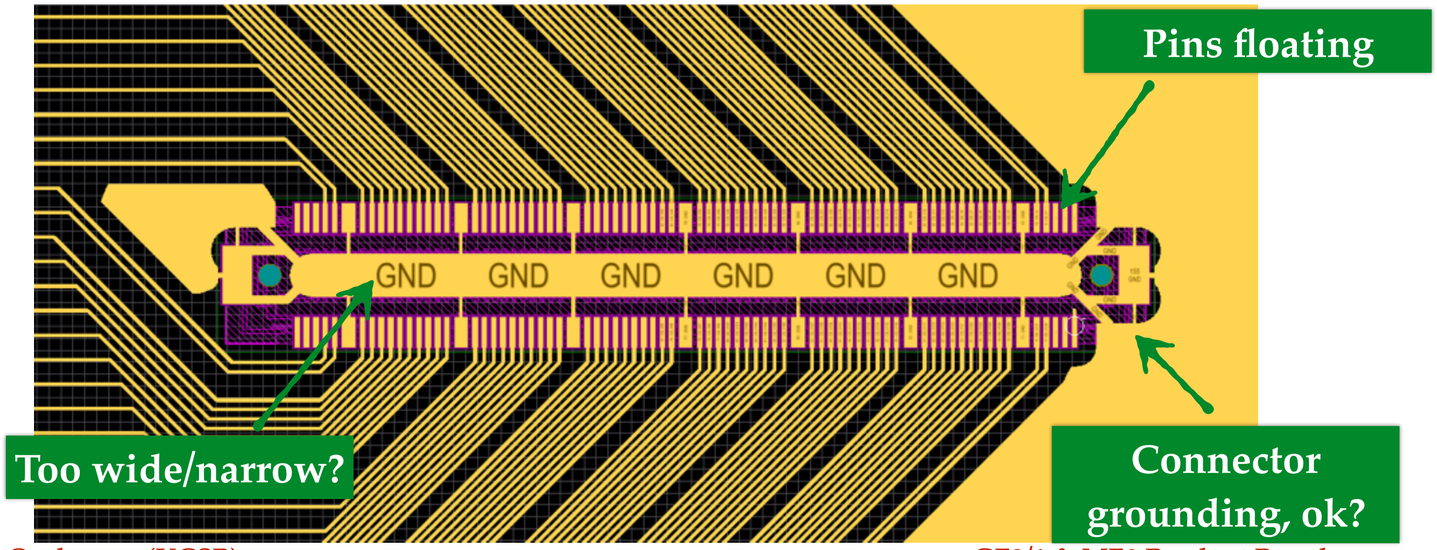
- ★ Grounding
  - ✦ 2.3 mm trace under connector feeds GND pads via 0.2 mm "whiskers"
    - connected to copper plane with 0.5 mm "whiskers"
  - ✦ copper islands retained
  - ✦ clearance between traces & GND plane: 1 mm

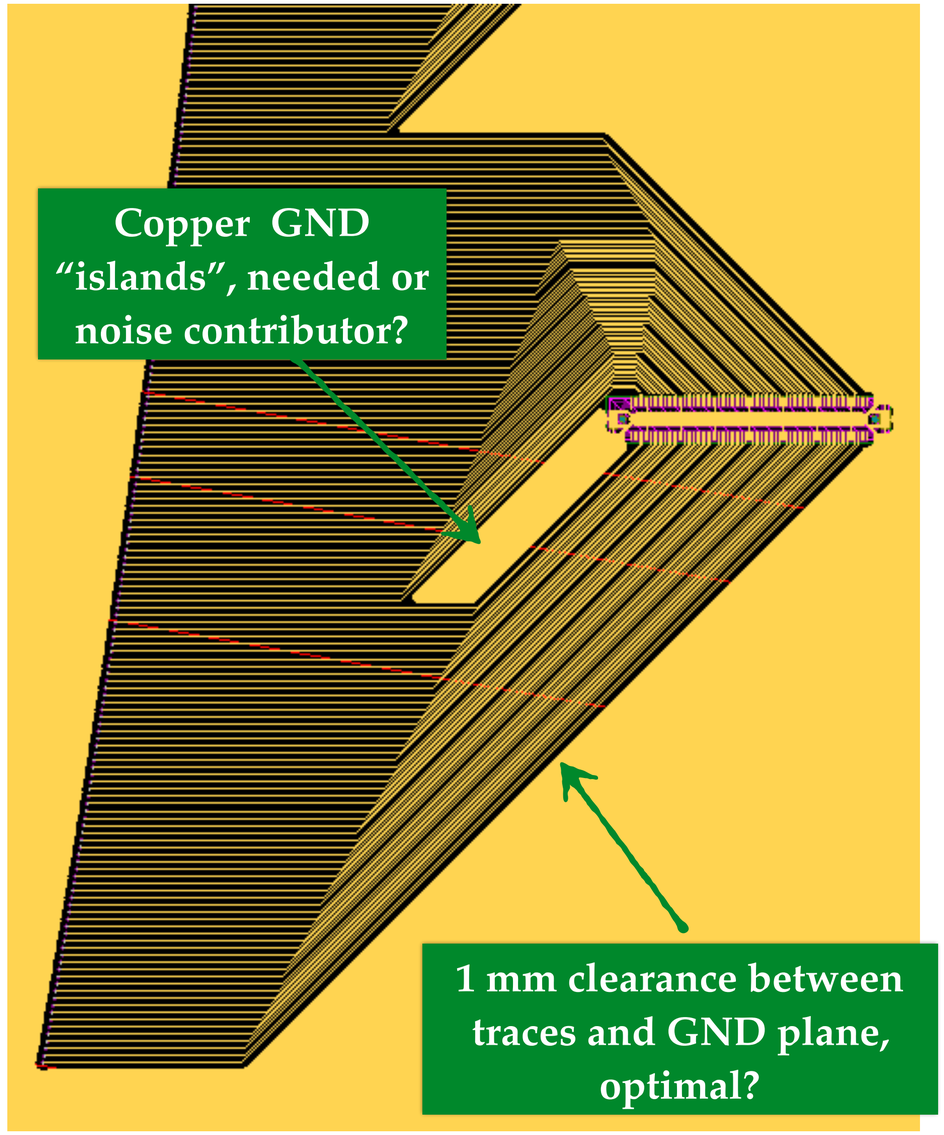
Q: Can we improve based on previous test results?

Related discussion

Cameron's talk: "noise in edge strips decrease as spacing between trace and ground plane was increased"

Tuure's talk on M4 prototype tests: "No clear difference between slots" [with 1, 2 or 3 mm clearance to ground plane]





Conclusion

- **Workflow** for producing the layouts is **in place**

- **GE2/1 status**
  - layout for **M4 done** - delivered to CERN PCB shop yesterday
  - next, proceed with **remaining modules, aim to finish by mid-May**

- **ME0 status**
  - first look at layout demonstrates that constraints will be **very tight**
  - **need exact dimensions** to assess if at all possible to fit all components

- **Questions** in optimizing specifications
  - what are the **trace thickness and spacing** constraints, while keeping board manufacturable
  - (close-to) **final VFAT and OH dimensions** for GE2/1 and ME0 each
  - **grounding scheme**
    - clearance between traces and ground plane
    - should we keep copper islands given concerns for noisy strips close to the ground plane?
    - optimal connector grounding