Decisions to be made/R&D plans

Readout Board:

both: How do we address possible noise issues on next board? Shielding layer?
GE2/1: Address sufficient S/N for VFAT3 (higher gain? change strip width(length?)
GE2/1: check cross-talk
Options: prepare multilayer PCB for RO board and add ground planes. Build a different one for each of the 8 modules and see what works best.   Adding prepreg/airgap to see if helps reduce cross-talk.
Try making a read-out board with/without a ground plane
Option: review of grounding/shielding plan
Action: optimize strip readout signals routing on RO board (eg rotate connector by 90)
Option: prepare RO board with different low-profile connector prototypes
Action: decide on how input protection to VFAT3 will be implemented

Task 1: make a prototype readout board w/o copper layer to reduce noise coupling (uncontrolled currents etc.)

- Need to include GEB and need to have a comparison – thus, this is a GE11 variant of ROB w/o copper layer
- Make measurements to confirm (compare with identical standard ROB)

Task 2: make a prototype ROB with multiple layers and no copper layer (increase the distance between the top layer strips on ROB from the shield layer on GEB):

- First, we can just take measurements where we insert "spacers" (could be various options – air or materials) and evaluate how noise level measures versus the distance. Get curve and find optimal distance is.
- Second, design a prototype where there is a top FR4 layer of about "optimal;" thickness provided the overall thickness of ROB is constant. Again, needs to be GE11-size to allow measurements with GEBs
- Compare to Task 1 to evaluate the results
- Seems like there could be reasons to make it with copper layer

Task 3: make a special prototype of GEB with an extra layer of prepreg material on the bottom as an alternative to re-designing the ROB (ROB cost increase is significant – we are checking the cost impact)

- We should really know what the optimal thickness is, but we are motivated by the measurements showing that 100 μm paper layer was giving large reductions in noise, measure noise with different thicknesses of the extra layer
- Verify that GEB manufacturing remains reliable (concerns that this increase warping of the boards)

Task 4: make a special ROB prototypes of GE11 size with the strip lengths corresponding to GE2/1 and ME0 (optional, but would be nice) to emulate capacitances for GE21

- Measure noise with full chain to ensure noise levels on VFAT3 are acceptable (measure most probable S/N value)
- Test alternative solutions (as opposed to re-designing the chip or modifying strip layout), e.g. higher gain (measure S/N)

ME0 Readout Board:

Task 1: Evaluate the design of ME0 ROB with varied connector positioning (horizontal vs vertical) to reduce lengths of signal lines and cross-talk etc.

- Determine if it is feasible from mechanical constraints standpoints etc.
- This can make ME0 design much more feasible/routable (shorter lines, less cross-talk etc.)
- Brian’s proposal is a variant of this type of alternating designs
- Need to make sure we can still plug in APVs, which is required for testing chambers at production sites

FlexPCB & Connectors:

Task 1: Evaluate performance FLEX with no shielding
Task 2: Evaluate performance FLEX with shielding
Task 3: Evaluate performance FLEX with reference ground layer on one side
Task 4: Evaluate performance FLEX with 4 layer double space signal
Task 5: Evaluate Design and then eventually evaluate performance Rigid + Flex

Requirement: Special GEB for Test of FLEX

Evaluate Connector FH43B /FH26W

VFAT3 tests of suitability for GE21 and ME0

Protection of VFATs (there is a report of VFATs being damaged in normal operations, the new VFAT3b has improved protection, but it is possible that more protection may be necessary)
ROB Task 1

Task 1: demonstrate that protection works with HV on / LV off

Task 2: perform testing of VFAT3 high voltage spark protection

- Turn the gain up to induce sparks and observe performance

GEB:

Task 1: Max dimensions for manufacturing
Task 2: Characterization performance Vs lengths with different length pairs: VFAT control signal for each pair (Each VFAT need 3 pair)(Max length to evaluate from M4 GEB layout +15%)

Task 3: Characterization for ME0 performance Vs lengths with different length pairs: Multi VFATs (6 VAFTs) sharing control lines (Max length ~ 90 cm to evaluate from M4 GEB layout +15%)
Task 4: Characterization for GE2/1 performance Vs lengths with different length pairs: Multi VFATs (4 VAFTs) sharing control lines (Max length ~ 70 cm to evaluate from M4 GEB layout +15%), testing FPGA driving control bits multi drop connections
*** Task 2-3-4 could be done with a small single test GEB
Task 5: Explore option to have full shield outside the chimney (overlap area)
Task 6: Make sure that the power standoffs has the right size on the GEB PCB
Task 7: Specs for GEB flatness and manufacturing (particular attention to the soldering)

**** Standard GEBs for prototype needs large slots to accommodate the GE1/1 Hybrids adapters

Optohybrid:

Task 1: Consider Master – Slave OH solution for GE2/1
Task 2: Check Mechanical constraint for OH on GE2/1-M1
Task 3: Decide on FPGA+1 GBTx option or using 3 GBTx option (Only for GE2/1), to confirm the LpGBT timeline
Task 4: Evaluate for alternative to standoffs for electrical power
Task 5: Specs to apply the correct torque to each fixation screws
Task 6: Space for no FPGA OH on ME0 (up to 4 ~ 8x10 cm small OH or 8 ~ 5x5 cm) or LpGBT embedded on to the GEB
Task 7: ME0 In case of FPGA solution firmware and radiation studies are needed
Task 8: Check possibility to read the VFAT data without the start of transmission signal

Backend:

Task 1: Check number of available link for no FPGA case in ME0

Task 2 : ME0 DPG has to have more accurate charge deposition for GEM detector?

Task 3: ME0 Minimal logic to reconstruct the segments

OH straddling between GEB boards is problematic?
Standoffs require rigid connections to work between boards.
Some question of whether it is wise to use the standoffs for electrical power vs. using a connector designed for this,
GE2/1: Decide on the 1 OH/per GEB option.
GE2/1: Decide on FPGA+1 GBTx option rather than wait for LpGBT or using 3 GBTx option
ME0: Need to prototype firmware
ME0: set up prototype of FPGA-less ME0 OH

Reviews:
need to make at least Gerber files etc. available in advance.