Optoboard Development for Inner Tracker of High Luminosity ATLAS Detector

SPS Annual Meeting 2018

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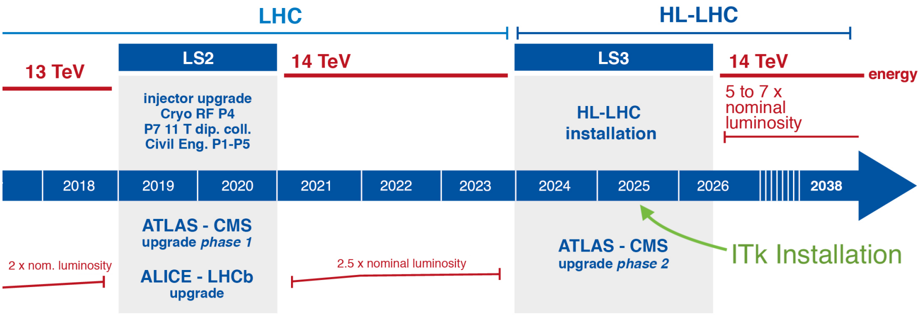
High Luminosity LHC program



Timeline of the LHC and High Luminosity LHC programs

- The Inner Tracker (ITk) replaces current Inner Detector of ATLAS

Read-out challenge

Higher instantaneous luminosity puts demands on read-out of ITk Pixel Detector

Bandwidth

Up to 5 Gb/s per pixel front end ($\sim$ 90 Tb/s in total)

Radiation tolerance

Sustain up to 1 GRad of radiation

Signal quality

Reliable transmission over long distances

Material budget

Keep number of electric cables minimal

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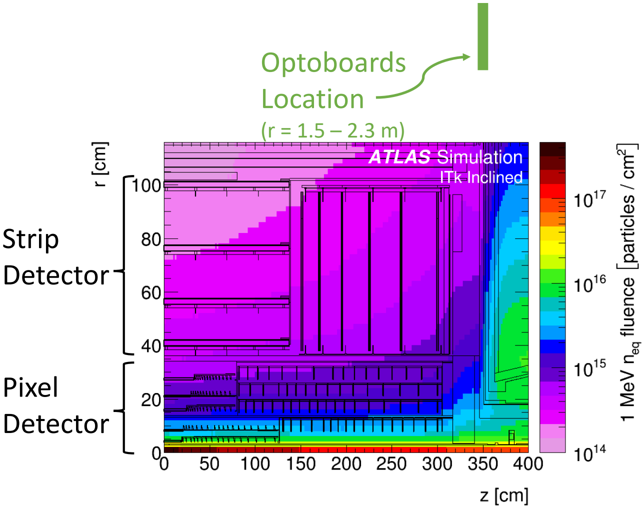
Optical fibres are favorable for bandwidth, signal quality and material budget
$\rightarrow$ Electrical to optical conversion stage: **Optoboard**



From ITk Strip TDR

Pro

- Reduce radiation damage to optoboard

Con

- Long electrical links

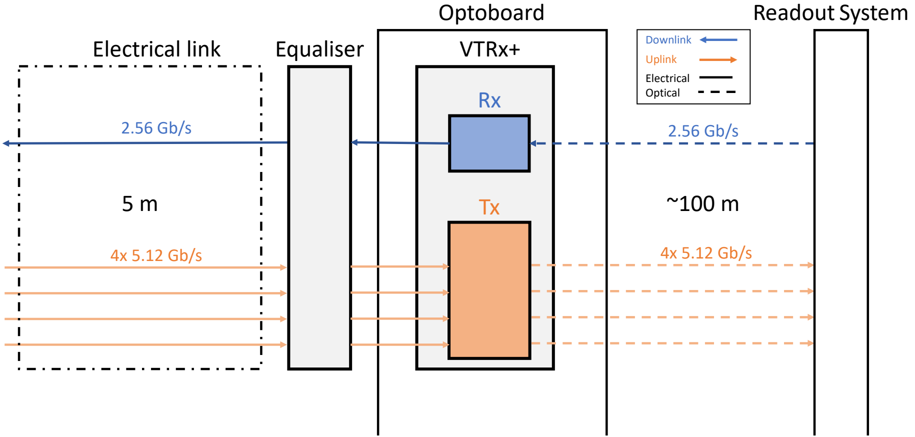
Optical read-out layout

Uplinks

Hit data

Downlinks

Clock, command and trigger



VTRx+

Versatile Link Plus project to develop radiation hard optical link system

- Endure $\sim 100\,\text{MRad}$, 10^{15} 1 MeV $n_{eq.}$
- Main component of optoboard

Rx (Receiver)

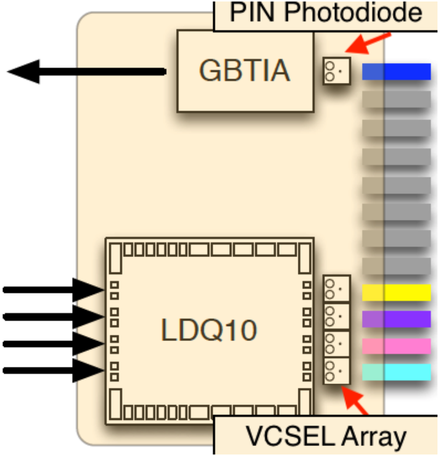
p-i-n photodiode

Transimpedance amplifier (GBTIA)

Tx (Transmitter)

Laser diode driver array (LDQ10)

VCSEL's (Vertical-cavity surface-emitting laser)



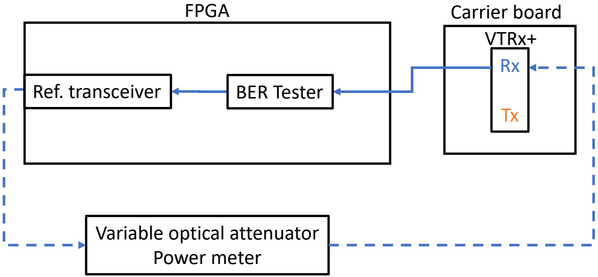
VTRx+ in 4 Tx + 1 Rx configuration

VTRx+ test

- BER $\overset{!}{<} 10^{-12}$ over whole communication chain
- First test only VTRx+ with pseudo-random bit sequence

Bit error rate

$$\text{BER} = \frac{\text{bit errors}}{\text{bits transferred}}$$



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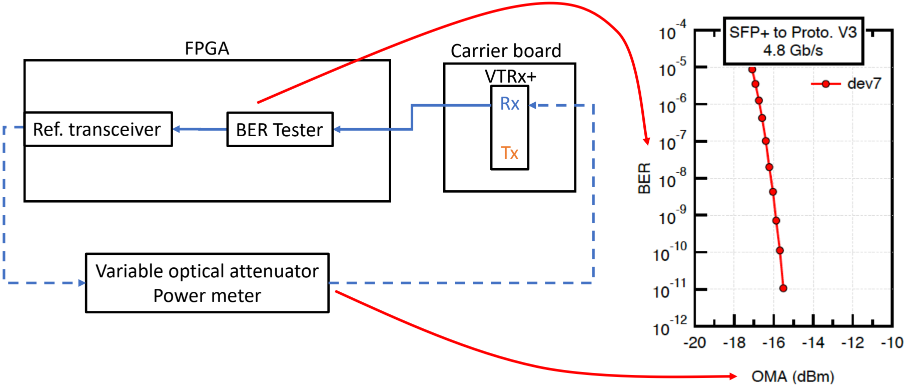
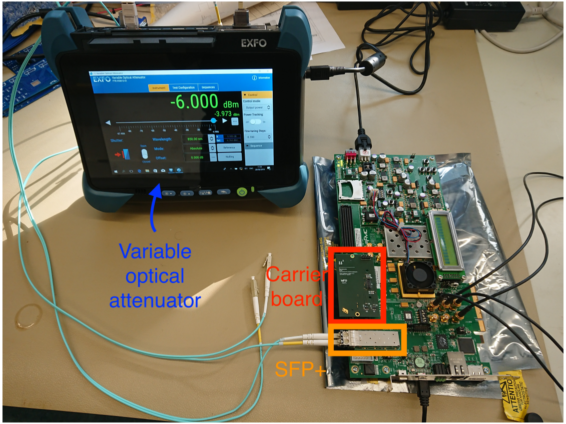


Setup ready for BER test

- Developed carrier board for VTRx+
- Waiting for first VTRx+ module to arrive
- Loopback test with reference transceiver and attenuator

Eye diagram tests are also necessary to understand possible transmission issues



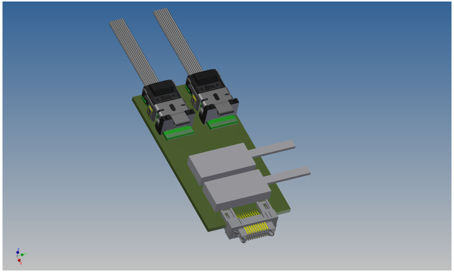
Optolink design

Optoboard

Hosts several VTRx+ depending on

- different data rates per pixel detector layer
- serial powering modularity of pixel sensors

→ 2 VTRx+/Optoboard in current design

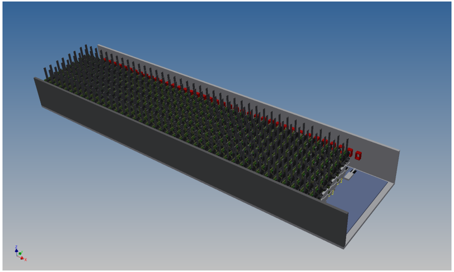


Optobox

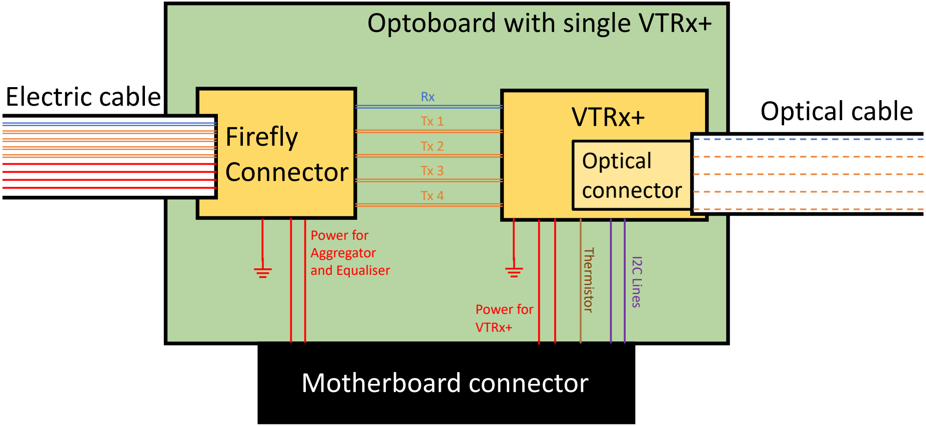
Hosts optoboards, provides

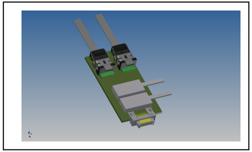
- power, control and monitoring
- cooling and interlock

Available space: $800 \times 200 \times 75\,\mathrm{mm}^3$

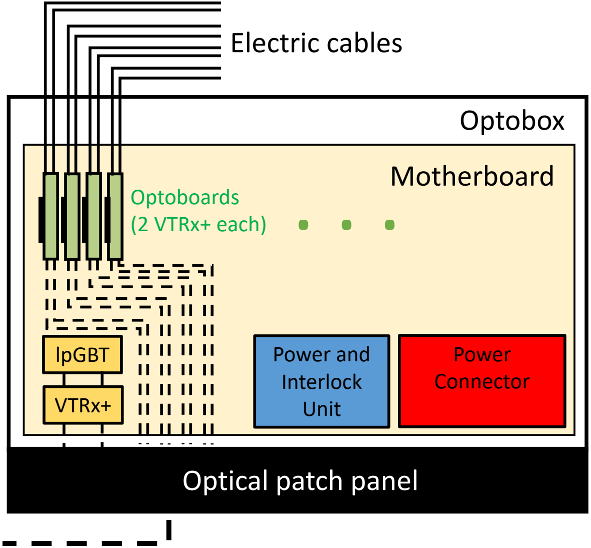


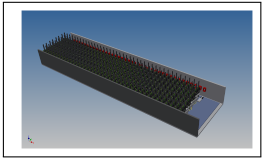
Optoboard functionality





Firefly: Link

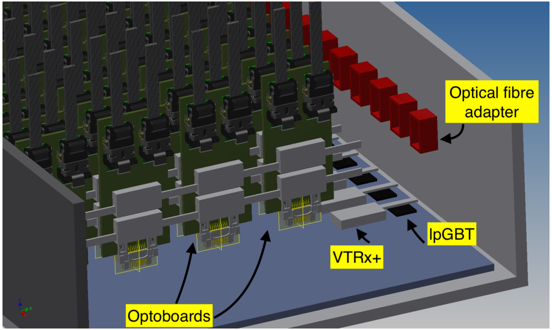




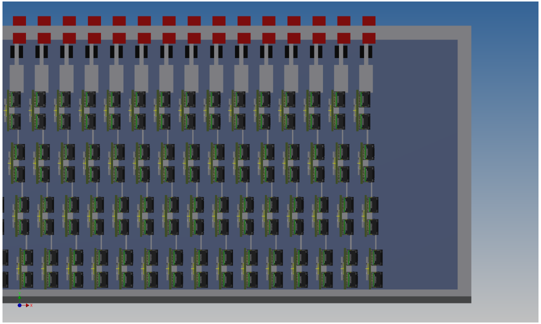
lpGBT chip

- I2C control and thermistor ADC
- Can serve 8 VTRx+

Optobox design



Front view, four optoboards per row



Top view

- Tight space constraints (especially height)
- Challenging cable management

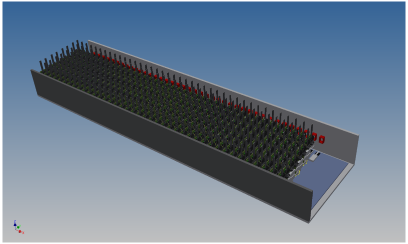
Estimation of needs

Optoboxes	16
Optoboards/Optobox	147

Outlook

Current status

- Design of first optoboard and optobox prototypes
- BER tests and eye diagram of VTRx+ starting soon



What comes next?

- Design of cooling system and power unit
- Production of first prototype, testing

First design review mid-2019

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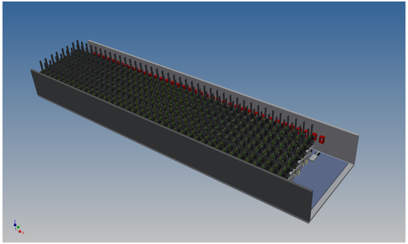

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Final optoboard production April 2021

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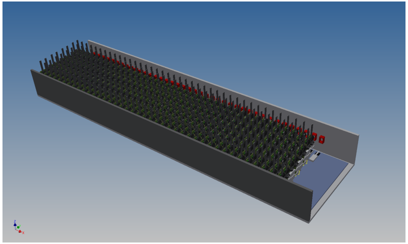

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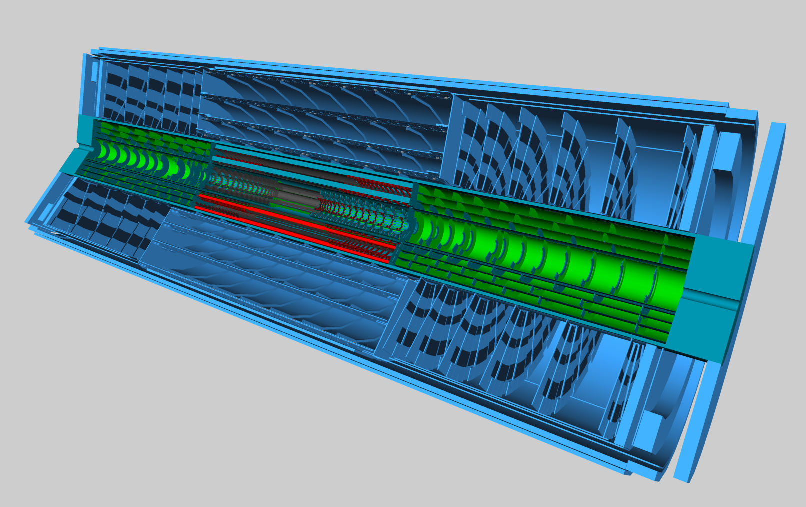
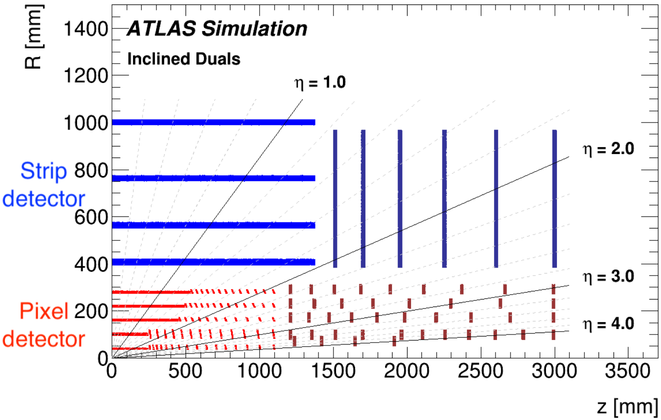
Final optoboard production April 2021

Next year I take the prototype with me!

Thank you!



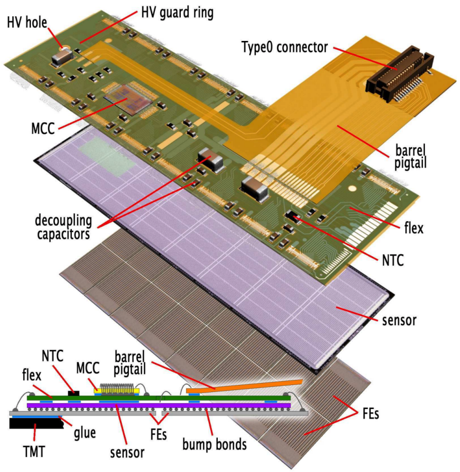
ATLAS Inner Tracker



Replaces current Inner Detector

- Ensures and improves track reconstruction at HL-LHC
- All-silicon design
- Low material budget of < 1.5 radiation lengths at all η

Inner Tracker



- Ensures and improves track reconstruction at pile-up of up to 200
- Pixel detector: Have to provide ∼ **90 Tb/s** of bandwidth
- Data transmission over electrical and optical links: **Optoboard**

Bandwidth

Trigger scheme

Baseline:

- 1 MHz for full pixel detector

Alternative:

- Fast clear for Layer 0+1 (< 800 kHz)
- 4 MHz for Layer 2-4

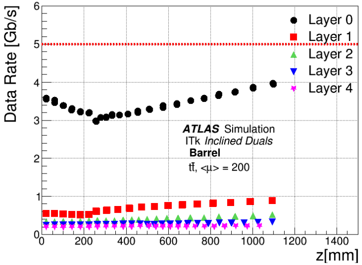
RD53 front end (FE) chip sends data over up to four 1.28 Gb/s lines

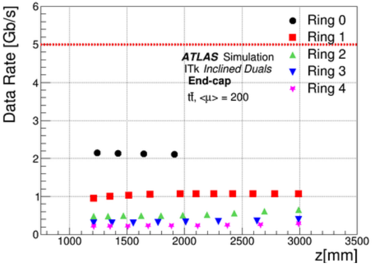
Layer/Ring	Data rate (1 MHz L0) (Gb/s)	Data rate (4 MHz L0) (Gb/s)	Design data rate per FE chip (Gb/s)
Layer 0	3.97	-	5.12
Layer 1	0.89	-	2.56
Layer 2	0.52	2.08	5.12
Layer 3	0.32	1.28	2.56
Layer 4	0.22	0.88	1.28
Ring 0	2.15	-	5.12
Ring 1	1.07	-	2.56
Ring 2	0.65	2.60	5.12
Ring 3	0.39	1.56	2.56
Ring 4	0.27	1.04	1.28

Uplink data rate per front end chip in ITk Pixel detector. (ITk Pixel TDR)

Uplinks: Bandwidth estimation

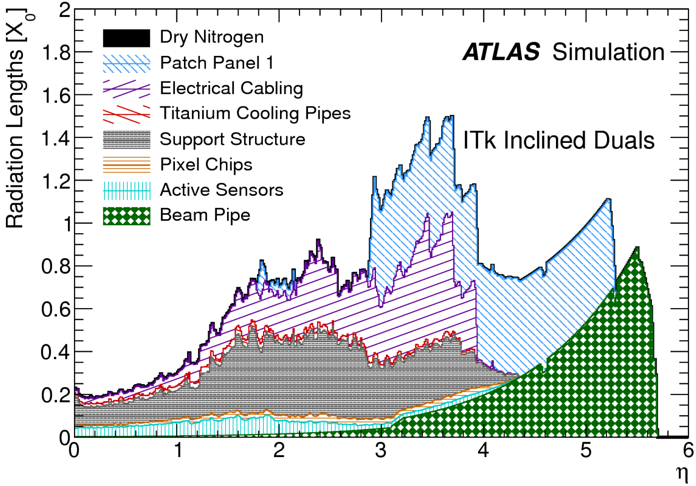
- Bandwidth $= \underbrace{\text{overhead}}_{=1.05} \cdot \underbrace{\text{word size}}_{=32\,\text{bit}} \cdot \underbrace{\text{trigger rate}}_{=1\,\text{MHz}} \cdot \text{occupancy}$
- occupancy $= \frac{<\text{hits/chip}>}{<\textit{regions}/\text{chip}>}$ (chip readout in regions of 4×1 pixels)
- Simulation of $t\bar{t}$ events in ITk with 200 minimum bias events superimposed, pass through ATLAS reconstruction



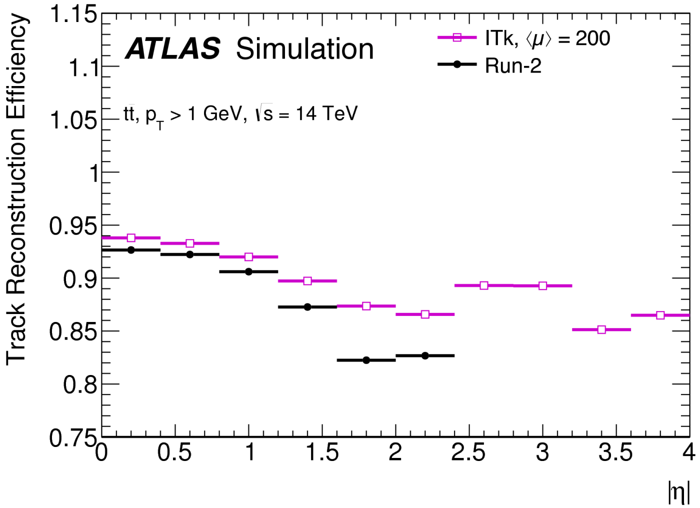


ITk Pixel TDR (http://cds.cern.ch/record/2285585)

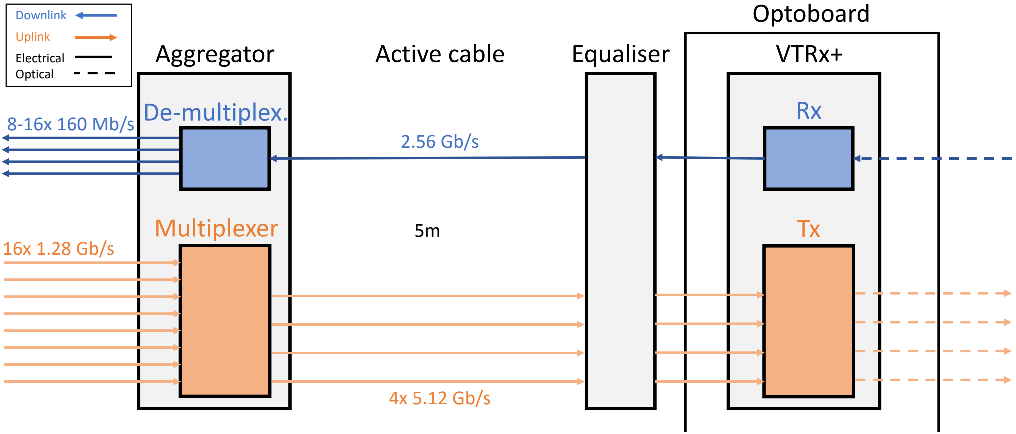
Material budget



Track reconstruction efficiency

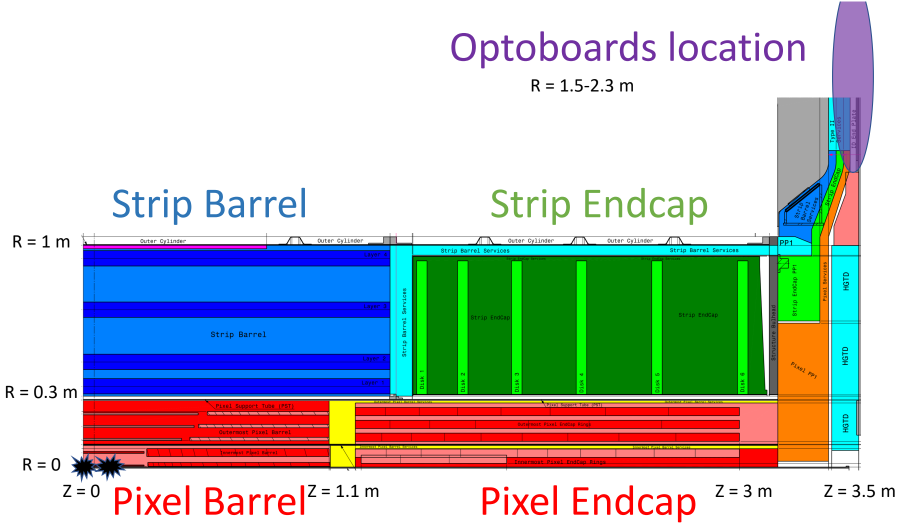


Link architecture



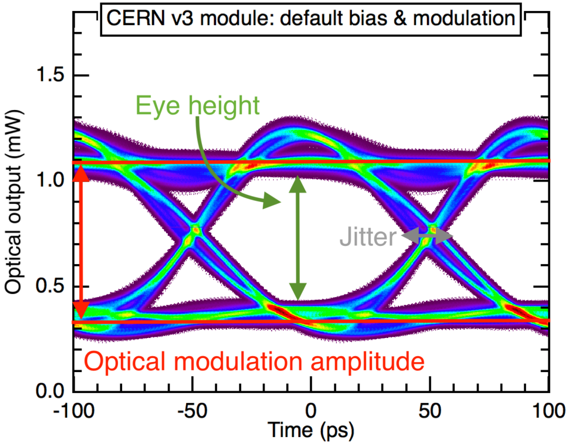
Attenuation in electric links puts high demands on equaliser and VTRx+ transmitter

Technical layout of the ITk



VTRx+ test: Eye diagram parameters

The more open the eye, the better the analog signal can be digitised



VTRx v3 Tx eye diagram, 10.22323/1.313.0048

VTRx+ specifications

#	Specification	Min.	Typ.	Max.	Unit
4.1.1	Tx OMA	-5.2			dBm
4.1.2	Tx Extinction Ratio	3			dB
4.1.3	Tx Eye Opening	60			%[a]
4.1.4	Tx rise/fall time[b]			35	ps
4.1.5	Tx Total Jitter[c,d]			25	ps
4.1.6	Tx Deterministic Jitter[e]			12	ps
4.1.7	Tx Eye Mask		TBD		
4.1.8	Tx output wavelength	840	850	860	nm
4.2.1	Tx Differential input voltage	100		1200	mV
4.2.2	Tx Input rise/fall time[b]		30	40	ps
4.2.3	Tx Input Total Jitter[c]			0.26	UI
4.2.4	Tx Input Deterministic Jitter			0.14	UI
4.2.5	Tx Input Eye Mask		TBD		
4.2.6	Tx Differential input impedance	90	100	110	Ω
4.3.1	Rx input Total Jitter[c]			0.48	UI
4.3.2	Rx input Deterministic Jitter			0.28	UI
4.3.3	Rx Sensitivity[c]			-13.1	dBm
4.3.4	Rx input wavelength	840		855 (TBC)	nm
4.4.1	Rx Differential output voltage	200		600	mV
4.4.2	Rx rise/fall time[b]			40	ps
4.4.3	Rx Total Jitter[c,f]			34	ps
4.4.4	Rx Deterministic Jitter[g]			14	ps
4.4.5	Rx Eye Mask		TBD		