DEVELOPMENT OF RESISTIVE MICROMEGAS TPCs FOR THE T2K EXPERIMENT

A. Delbart, on behalf of the ND280/HA-TPC collaboration,
CEA-Saclay/DRF-IRFU, Univ. Paris – Saclay
The goal of T2K-II phase (2022-) data taking after main ring upgrade is to measure $\delta_{CP}$ at $3\sigma$ thanks to a decrease in systematic errors in ND280 from 6% to 4%.

Super-Kamiokande (SK)
22.5 kt $\rightarrow$ ~200 kt (Hyper-K)

Goal of ND280
- Measure the flux & spectrum of neutrinos
- Measure $\nu_e$ contamination
T2K/ND280 PERFORMANCES & LIMITATIONS

NEED FOR AN UPGRADE

Reconstructed momentum and angle for $\mu$ selected at ND280 (left) and $e^-$ selected at SK

V-TPC spatial resolution 6.9x9.7 mm² pads

CURRENT ND280

Proposed ND280 upgrade

HA-TPC should be as performant as V-TPC

Good acceptance only for forward tracks

+ 6 TOF planes surrounding the new tracker

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Enlarged efficiency at high angles with respect to current ND280

- Drift volume + field cage
- MicroMegas Resistive
- Module Frame (MF)
- Central cathode

HA-TPC

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Overall x × y × z (m)</td>
<td>2.0 × 0.8 × 1.8</td>
</tr>
<tr>
<td>Drift distance (cm)</td>
<td>90</td>
</tr>
<tr>
<td>Magnetic Field (T)</td>
<td>0.2</td>
</tr>
<tr>
<td>Electric field (V/cm)</td>
<td>275</td>
</tr>
<tr>
<td>Gas Ar-CF$_4$-iC$<em>4$H$</em>{10}$ (%)</td>
<td>95 - 3 - 2</td>
</tr>
<tr>
<td>Drift Velocity cm/$\mu$s</td>
<td>7.8</td>
</tr>
<tr>
<td>Transverse diffusion ($\mu$m/$\sqrt{cm}$)</td>
<td>265</td>
</tr>
<tr>
<td>Micromegas gain</td>
<td>1000</td>
</tr>
<tr>
<td>Micromegas dim. z×y (mm)</td>
<td>340×420</td>
</tr>
<tr>
<td>Pad z × y (mm)</td>
<td>10 × 11</td>
</tr>
<tr>
<td>N pads</td>
<td>36864</td>
</tr>
<tr>
<td>el. noise (ENC)</td>
<td>800</td>
</tr>
<tr>
<td>S/N</td>
<td>100</td>
</tr>
<tr>
<td>Sampling frequency (MHz)</td>
<td>25</td>
</tr>
<tr>
<td>N time samples</td>
<td>511</td>
</tr>
</tbody>
</table>

HA-TPC V-TPC

MF with 8 micromegas

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Choice of the Resistive foil technology for the HA-TPC micromegas readout
- Charge spreading which should enable keeping the ~600 μm spatial resolution with larger pads and improves it at short drift distance → less electronic channels, cost reduction
- ASIC spark protection no longer needed → more compact FEE, maximize HA-TPC acceptance
- Encapsulated mesh @ GND + insulating layer → potentially lower track distortions & better S/N

Standard bulk-mm

Resistive-bulk-mm

Gaussian spreading as a function of time with:

\[ \rho(r, t) = \frac{RC}{2t} \exp\left[-\frac{r^2}{4t}\right] \]

\[ t \approx \text{shaping time (few 100 ns)} \]

\[ \sigma_r = \sqrt{\frac{2t}{RC}} \]

For pads of ~11x10 mm², the Kapton foil resistivity could be around 0.4 MΩ/□ and glue thickness ~75 μm for a good charge spreading (σ~ 2.6 mm) (spark protection to be checked)
To keep $\Delta E/E \leq 10^{-4}$ confined at $<1\text{cm from FC walls}$, the TPC cage requirements are:

- Cathode flatness better than 0.1 mm,
- Micromegas plane flatness better than 0.2 mm,
- Cathode/Anode planes parallel to within 0.2 mm,
- Field Cage walls flatness better than 0.3 mm.

Voltage divider resistors matched within rms $\sim 0.1\%$.
Ref: G. Collazuol (INFN Padova)

**TPC CAGE**

**FEA & ELECTRIC FIELD SHAPING**

<table>
<thead>
<tr>
<th>Layer of the wall</th>
<th>Material</th>
<th>thickness d (mm)</th>
<th>average X₀ (mm)</th>
<th>d/X₀ (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 (inner layer)</td>
<td>Double layer strip foil (+glue)</td>
<td>0.05</td>
<td>14.3 (Cu)</td>
<td>~0.07</td>
</tr>
<tr>
<td></td>
<td>→ Copper strips</td>
<td>~0.005</td>
<td>~240</td>
<td>0.70</td>
</tr>
<tr>
<td>2</td>
<td>Aramid Fiber Fabric (Twaron)</td>
<td>2.0</td>
<td>14300</td>
<td>0.17</td>
</tr>
<tr>
<td>3</td>
<td>Aramid honeycomb panel (Nomex)</td>
<td>25</td>
<td>14300</td>
<td>0.17</td>
</tr>
<tr>
<td>4</td>
<td>Aramid Fiber Fabric (Twaron)</td>
<td>2.0</td>
<td>~240</td>
<td>0.70</td>
</tr>
<tr>
<td>5</td>
<td>Kapton tape (+glue)</td>
<td>0.125</td>
<td>285</td>
<td>0.04</td>
</tr>
<tr>
<td>6 (outer layer)</td>
<td>Aluminized Mylar (+glue)</td>
<td>0.05</td>
<td>89 (Al)</td>
<td>~0.02</td>
</tr>
<tr>
<td></td>
<td>→ Aluminum layer</td>
<td>0.01</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total</td>
<td></td>
<td>~30</td>
<td>~89 (Al)</td>
<td>~1.6</td>
</tr>
</tbody>
</table>

**Thin & low Z composite materials**

Max 0.01 mm MF deformation under 4 mbar overpressure

Ref: H. Przybilski (IFJ PAN)

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HA-TPC READOUT ELECTRONICS
A NEW AFTER-BASED ARCHITECTURE

Main concepts
- AFTER chip designed for T2K (511 bucket SCA sampling@25 MHz, 120fC-600 fC, 100ns-2μs peaking time)
- New FEC with 8 AFTER chips which digitizes pad signal with an 8 ch. ADC (minimum dead time of 3.3 ms)
- FEM provides control (&trigger), synchronization, data aggregation, data buffering & data zero suppression
- The TDCM is a generic clock and trigger distributor and data aggregator (FPGA+2 xilinx CPU+1 GB DDR3)

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Epoxy (~0,02 mm) is used to fill the gap between copper pads. A 75 μm thick glue layer is used for the 50 μm Kapton+0.4 MΩ/DLC pressing, same process as for the MM0-DLC3.
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FULL-SIZE MM-DLC DESIGN
DLC+BULK-MICROMEGAS

7 x DLC foils (1x0.6 m²) at CERN
Resistivity dispersion 0.3 – 0.7 $M\Omega$ provided by Be-Sputter (Japan) with help from A. Ochi

Mesh connection (silver paste) in the 4 corners

DLC & mesh connection
To HV PS via HV filter

Active area
1152 pads

Grounded mesh encapsulated in bulk-micromegas @ ~0.253 mm from pad plane

Not to scale

DLC HV ~+400 V
(2 contacts in corners)

Aluminum stiffener

Silver paste strip (1 mm width) connected to 2 mm width PCB copper strip

<1 µm DLC resistive layer
(≈0.4 Mohm after DLC pressing)

128 µm (Pyralux pillars)
50 µm (resistive Kapton)

75 µm (Glue)
35 µm (copper pad)
With epoxy filling inbetween

7 mm

Pad + DLC+ bulk (close-up)
Main goal of the testbench is to measure, verify and calibrate:
- Quality (find dead pads),
- Mapping for all MM modules of:
  - Signal amplitude/gain
  - Energy resolution
  - Assess spread of the signal—verify spatial resolution.
- Need to scan the active surface with a strong radioactive source or small X-ray lamp.
- Two identical chambers for supply and return gas
- Sequential measurement of drift velocity and gain

**Gain Measurement**
Detected charge from defined deposition

**Drift Velocity**
Time difference between ionization tracks of defined distance
### HA-TPC Timeline (2018-2019 R&D)

<table>
<thead>
<tr>
<th>Development / Prototypes</th>
<th>2018 Q3</th>
<th>2018 Q4</th>
<th>2019 Q1</th>
<th>2019 Q2</th>
<th>2019 Q3</th>
<th>2019 Q4</th>
</tr>
</thead>
<tbody>
<tr>
<td>MM0-DLC3 tests on Saclay TPC chamber</td>
<td></td>
<td></td>
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<tr>
<td>MM0-DLC3 beam test data analysis</td>
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<tr>
<td><strong>Field Cage Prototype for MM1 v2.7</strong></td>
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<tr>
<td>Mold production</td>
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<tr>
<td>Panels and Field cage production &amp; AIVT @ INFN</td>
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<tr>
<td>HA-TPC prototype MM1 Module Frame</td>
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<tr>
<td><strong>MM1 module v2.7 Prototype</strong></td>
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<tr>
<td>MM1 v2.7 stiffener &amp; mechanicals production</td>
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<tr>
<td>MM1 PCB Design</td>
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<tr>
<td>MM1-DLC1&amp;2 production</td>
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<tr>
<td>MM1 Saclay test chamber MF design &amp; production</td>
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<tr>
<td>MM1 &amp; detector test bench readout electronics</td>
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<tr>
<td>MM1 module mechanicals for test bench FEE</td>
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<tr>
<td>AIVT in Saclay TPC chamber</td>
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<tr>
<td><strong>HATPC-MM1 prototype beam test (Desy/CERN)</strong></td>
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<tr>
<td>AIVT Field cage + MM1 module (@ CERN)</td>
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<tr>
<td>beam tests</td>
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<tr>
<td>Beam test analysis</td>
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</tbody>
</table>

MM0 resistive bulk-micromegas on HARP TPC beam test @ CERN/PS-T9: sept 2018
HA-TPC prototype with MM1 resistive bulk-micromegas AIVT @ CERN: may 2019
Test beam in 0.2T magnet at DESY: 10-24 June 2019
**GOALS of the prototypes**

- Define the resistive layer technology (DLC or ink paste) & its specifications (resistivity & glue thickness)
- Define the most efficient PCB segmentation in accordance with the measured charge spreading

**USE of the prototypes**

- 2 prototypes produced in 2018: MM0-DLC1&2. A MM0-DLC3 with ~400 kOhm/Square was just produced
- Measure Pad Response Function in Saclay mini-TPC chamber with cosmics
- Beam test of prototype MM0-DLC1 on the HARP TPC at CERN August 22 – Sept 5 – on-going analysis
RESISTIVE MICROMEGAS MODULE MM0
TEST BEAM @ CERN/PS-T9 SETUP

HARP TPC + MM0
+ v-TPC FEE

MM0-DLC1 PCB

- 359.1 mm
- final cutting
- 200 µm glue
- + 50 µm APICAL with DLC foil
- ~2.5 MΩ/square

Pyralux border increased to 5 mm width: peripheral pads are partially covered

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Gas volume : HARP TPC
- 1.5 m drift distance / 25 kV (166 kV/cm)
- 25 l/h Argon(95%)/CF4(3%)/isobutane(2%)

Detector : MM0 module
- Micromegas module MM0 with 2.5 $\Omega$/DLC
- horiz. x vert. = 36 x 48 pads
- each pad 0.97 x 0.69 cm
- nominal MM voltage 340 V (up to 380 V)
- V-TPC FEE: Sampling time 80 ns (12.5 MHz)
- nominal peaking time 600 ns

Data taking
- Cosmic trigger with 2 plastic scintillators + MPPC
- Fe55 source for 5.9 kEV X-rays
- Beam : 0.5, ± 0.8, 1, 2 GeV/c momentum

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PRELIMINARY RESULTS : DE/DX RESOLUTION
MICROMEGAS GAIN

Gain uniformity ($Q_{pad}/Q_{pad \, average} \geq 0.93$)

known problematic pads (noise)

Border pads
Partially covered by insulator

\[ \text{Cluster charge} \]

\[ \text{Gain uniformity} \]

\[ \text{Entries} = 1547 \]
Mean $x = 17.54$
Mean $y = 23.29$
Std Dev $x = 9.659$
Std Dev $y = 13.17$

\[ \text{cluster charge} \]
Entries 12913
Mean 9630 ± 21.25
Std Dev 2414 ± 15.03

\[ \text{55Fe x-ray source} \]

\[ \text{dE/dx resolution vs. Drift distance using truncated mean method} \]

with 36 clusters

\[ \text{Resistive micromegas gain Vs DLC layer HV} \]

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PRELIMINARY RESULTS: SPATIAL RESOLUTION VS DRIFT DISTANCE

MM0-DLC resistive bulk-micromegas 6.9 x 9.7 mm² pads with 2.5 MΩ/ ■ DLC

These points still to understand Gas quality @ start of data taking? (expected $\sqrt{Z}$ behaviour)

~ 2 times better (~320 μm @ 30 cm) than non-resistive ν-TPC modules

Seems to have margin for going from MM0 6.9 x 9.7 mm² to MM1 10.09 x 11.18 mm² pads by decreasing the resistivity to ~0.4 MΩ/ ■ (trade-off btw charge spreading & spark protection)
Field cage + cathode (INFN)

MM1-DLC1 module + 4x ARCv1 cards (IRFU/CERN/LpnHe)

Module Frame + inner guard frame (IFJ PAN)

Supporting frame to mount in DESY/ILC-TPC magnet (operated @ 0.2 T)

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HA-TPC FULL-SIZE MM MODULE PROTOTYPE
READOUT ELECTRONICS FOR BEAM TESTS

MM1-DLC1
Glued on stiffener

4 ARCv2
(Lrfu)

2 FEC-interfARC
(Lpnhe)

TDCM
(Lrfu)

TDCM mechanics for insertion in a 6U crate

PC – MIDAS
Config. & DAQ
(IFAE)

Description

- Front-end: 4 x 288-channel ARCv2-AFTER (minor corrections compared to ARCv1)
- Back-end: TDCM (bare metal command interpreter) + PC running MIDAS for configuration and DAQ

Ref: D. Calvet (CEA-DRF-IRFU)
### HA-TPC Timeline (Production)

<table>
<thead>
<tr>
<th>HA-TPC Production &amp; AIVT @ CERN</th>
<th>MM Module final design &amp; Production</th>
<th>MM Module Readout Electronics</th>
<th>HA-TPC Field Cage</th>
<th>DAQ software</th>
<th>AIVT @ J-PARC &amp; Commissioning</th>
</tr>
</thead>
<tbody>
<tr>
<td>conceptual design</td>
<td>detailed design &amp; fabrication</td>
<td>AIVT</td>
<td>Final design</td>
<td>Pre-prod</td>
<td>Production</td>
</tr>
<tr>
<td>Front End Card (FEC Cards)</td>
<td>FEC components production</td>
<td>FEC production test bench</td>
<td>Front End Mezzanine card (FEM Cards)</td>
<td>FEC production test bench</td>
<td>FEC production test bench</td>
</tr>
<tr>
<td>HA-TPC Field Cage</td>
<td>Detailed design</td>
<td>Mold production</td>
<td>HA-TPC MOD1 Production</td>
<td>HA-TPC MOD1 MT production</td>
<td>HA-TPC MOD1 ANIV + test beam @ CERN</td>
</tr>
<tr>
<td>AIVT @ J-PARC &amp; Commissioning</td>
<td>POD removing &amp; Fission preparation</td>
<td>HA-TPC MOD1 ANIV @ J-PARC (surface)</td>
<td>HA-TPC MOD2 ANIV @ J-PARC (surface)</td>
<td>AIVT in J-PARC</td>
<td>Commissioning</td>
</tr>
</tbody>
</table>

PRRs for start of production: **June-October 2019**  
HA-TPC 1 ready: **March-June 2020**  
HA-TPC 2 ready: **January 2021**
The tests of a resistive bulk-micromegas module on CERN/PS-T9 beam showed a 2 times better spatial resolution while keeping the dE/dX capabilities in control (9-10% with only one module track length). Analysis is on-going to investigate the effects of the DLC resistivity non-uniformity and of lower shaping times.

A prototype of a HA-TPC field cage equipped with a full-size resistive bulk-micromegas module will be tested with beam at DESY in June 2019.

The T2K / ND280 near detector upgrade development is on-going. The 2 new HA-TPCs design will be soon fixed and production should start in October this year for a completion scheduled for March 2021.

Not covered in this talk but of great importance: HA-TPC gas system, HA-TPC FEE cooling, ND280 upgrade sub-detectors mechanical integration and cabling in basket (HV, LV, cooling, FEE datas, ...).

Thank you for your attention
Mean features
- Input current polarity: positive or negative
- 72 analog channels
- 4 charge ranges: 120 fC, 240 fC, 360 fC & 600 fC
- 16 peaking time values: 100 ns to 2 µs
- 511 analog memory cells / channel
- Fsampling: 1 MHz to 50 MHz; Fread: 20 MHz
- Slow Control (SPI protocol); Test inputs (calibration & test)

Main requirements
- MIP/Noise: 100
- Output Dynamic: 2V/10 MIPs
- I.N.L: 1% 0-3 MIPS; 5% 3/10 MIPs
- Minimum Ionizing Particle: MIP: 12 fC to 60 fC

Ref: P. Baron, IRFU MPGD workshop, CEA, Saclay 6-8 dec. 2011
## Development of resistive Micromegas TPCs for T2K, 15th Vienna Conference on Instrumentation, February 18th - 22nd 2019

**Ref:** P. Baron, IRFU MPGD workshop, CEA, Saclay 6-8 dec. 2011

### Table: Parameters and Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>AFTER</th>
<th>AGET</th>
<th>DREAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Polarity of detector signal</td>
<td>Negative or Positive</td>
<td>Negative or Positive</td>
<td>Negative or Positive</td>
</tr>
<tr>
<td>Number of channels</td>
<td>72</td>
<td>64</td>
<td>64</td>
</tr>
<tr>
<td>External Preamplifier</td>
<td>No</td>
<td>Yes; access to the filter or SCA inputs</td>
<td>Yes; access to the filter or SCA inputs</td>
</tr>
<tr>
<td>Charge measurement</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input dynamic range/gain</td>
<td>120 fC; 240 fC; 360 fC; 600 fC</td>
<td>120 fC; 240 fC; 1 pC; 10 pC /channel</td>
<td>50 fC; 100 fC; 200 fC; 1 pC /channel</td>
</tr>
<tr>
<td>Sampling</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Peaking time value</td>
<td>100 ns to 2 µs (16 values)</td>
<td>50 ns to 1 µs (16 values)</td>
<td>50 ns to 1 µs (16 values)</td>
</tr>
<tr>
<td>Number of SCA Time bins</td>
<td>511</td>
<td>512</td>
<td></td>
</tr>
<tr>
<td>Sampling Frequency (Wck)</td>
<td>1 MHz to 100 MHz</td>
<td>1 MHz to 100 MHz</td>
<td>1 MHz to 50 MHz</td>
</tr>
<tr>
<td>Triggering</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Discriminator solution</td>
<td>No</td>
<td>Leading edge</td>
<td>Leading edge</td>
</tr>
<tr>
<td>HIT signal</td>
<td></td>
<td>OR of the 64 discriminator outputs in LVDS level</td>
<td>OR of the 64 discriminator outputs in LVDS level</td>
</tr>
<tr>
<td>Threshold Range</td>
<td></td>
<td>5% of the dynamic range</td>
<td>5% of the dynamic range</td>
</tr>
<tr>
<td>Threshold value</td>
<td></td>
<td>(3-bit + polarity bit) common DAC + 4-bit DAC / channel</td>
<td>(7-bit + polarity bit) DAC common to all channels</td>
</tr>
<tr>
<td>Readout</td>
<td></td>
<td></td>
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<tr>
<td>Readout frequency</td>
<td>20 MHz</td>
<td>25 MHz</td>
<td>Up to 20 MHz</td>
</tr>
<tr>
<td>Channel Readout mode</td>
<td>all channels</td>
<td>All, hit or selected</td>
<td>all channels excepted those disabled</td>
</tr>
<tr>
<td>SCA cell Readout mode</td>
<td>all</td>
<td>1 to 512</td>
<td>Triggered columns only</td>
</tr>
<tr>
<td>Trigger rate</td>
<td>&lt; 0.3 Hz / channel</td>
<td>&lt; 1 kHz / channel</td>
<td>Up to 20kHz (4 samples read/trigger).</td>
</tr>
<tr>
<td>Power consumption</td>
<td>&lt; 8 mW / channel</td>
<td>&lt; 10 mW / channel</td>
<td>&lt; 50 kHz / channel</td>
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<tr>
<td>Functionality has been tested</td>
<td></td>
<td>Functionality has been tested successfully</td>
<td></td>
</tr>
<tr>
<td>Noise</td>
<td>370 e- + 14.6 e- / pF (measured)</td>
<td>550 e- + 14 e- / pF (measured)</td>
<td>685 e- + 2.3 e- / pF (simulated)</td>
</tr>
<tr>
<td>Power consumption</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
EXAMPLE OF DLC FOIL RESISTIVITY (FOIL 2)

Theoretical value **500 kΩ/□**

Real value: Min: **296 kΩ/□**  Max: **664.7 kΩ/□**

Foil size: 100x61 cm
Main components

- 8 AFTER chips
- No spark protection diodes, only one capacitor link per channel
- On-board small logic for signal distribution
- Octal-channel ADC 12 bit (e.g. AD9637), clocked at 12.5 MHz
- Calibration pulser, e.g. 16-bit DAC + analog switch + injection capacitor
- On-board voltage/current/temperature/serial number chip, e.g. Maxim DS2438
- 4.2 V to 5.5 V single power supply via FEM connector and/or cable connector
- Anticipated power consumption: ~2.5 A

Ref: D. Calvet (CEA-DRF-IRFU)  
J-M Parraud (In2P3/LpnHe)
Development of resistive Micromegas TPCs for T2K, 15th Vienna Conference on Instrumentation, February 18th - 22nd 2019 | alain.delbart@cea.fr
Look for clusters at the left and right side of the detector clusters are selected with relatively high threshold to suppress noise

Study all possible tracks from clusters combinations

Define the box in 3D space: X, Y, T

Take all the waveforms in pads inside this box

Select the “good” tracks:
  - Enough number of pads and columns

Main advantage:
  - Very simple!
  - Severe noise suppression
  - Possibility to select multiple tracks in the event

Display with charge:

Display with time:

Selected track:

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Reconstruction of the track position was done with the Pad Response Function (PRF).

Consider the PRF uniform for all the pads estimate it form:

PRF scatter plot:

\[
PRF(x_{\text{track}} - x_{\text{pad}}) = \frac{q_{\text{pad}}}{q_{\text{cluster}}}
\]

Based on the measured charge ratio we reconstruct the track position

with minimisation of

\[
\chi^2 = \sum_{\text{column}} \left( a - \frac{PRF(y_{\text{track}} - y_{\text{pad}})}{\sigma_a} \right)^2 \sigma_a = \sqrt{a}/q_{\text{total}}
\]

We perform several iterations of “estimation PRF → track position extraction” until the track fit quality stops improving.