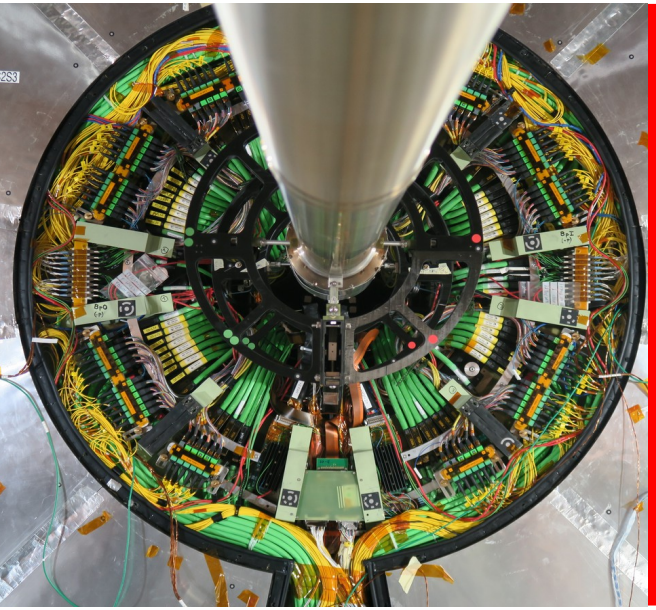


The CMS Phase-1 Pixel Detector

experience & lessons learned from 2 years of operation

Benedikt Vormwald
University of Hamburg
on behalf of the CMS collaboration

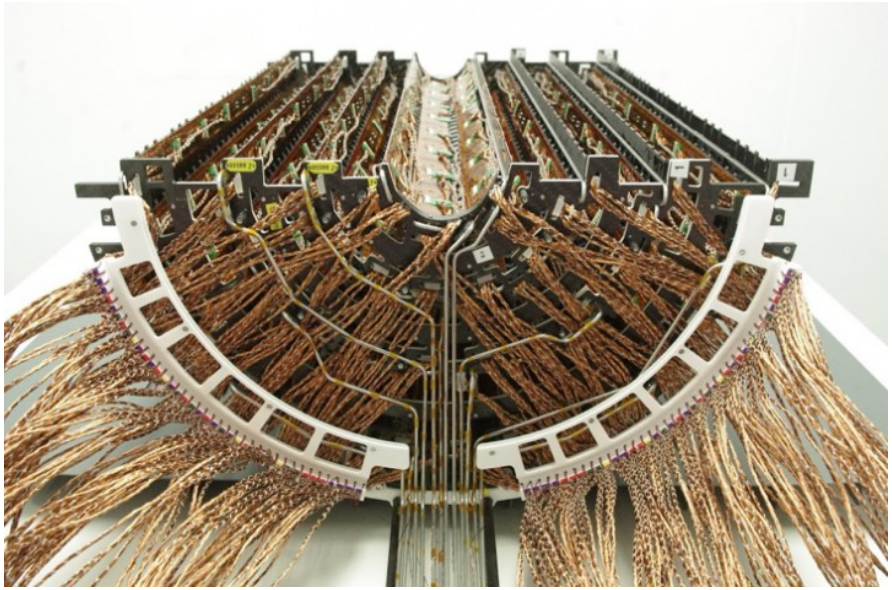
Bundesministerium für Bildung und Forschung

CMS Germany BMBF FSP-CMS

UHH

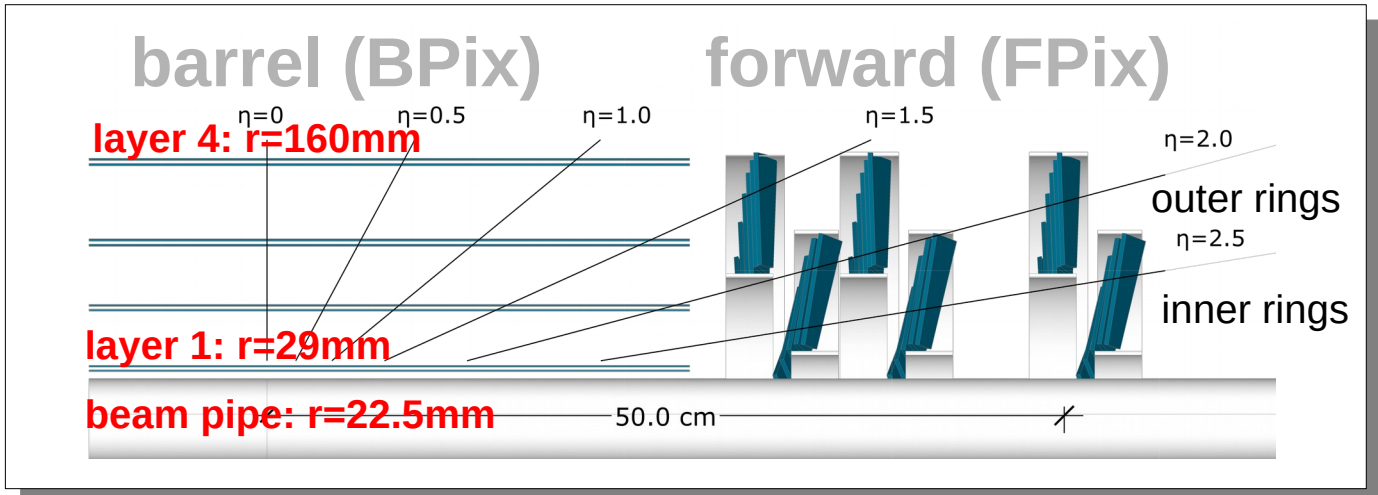
VCI 2019
Vienna, 18.-22.02.2019

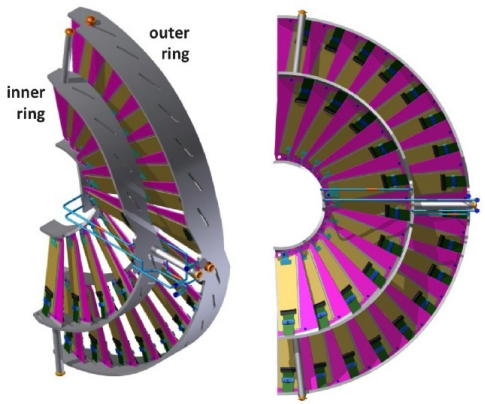
CMS Phase-1 Pixel Detector

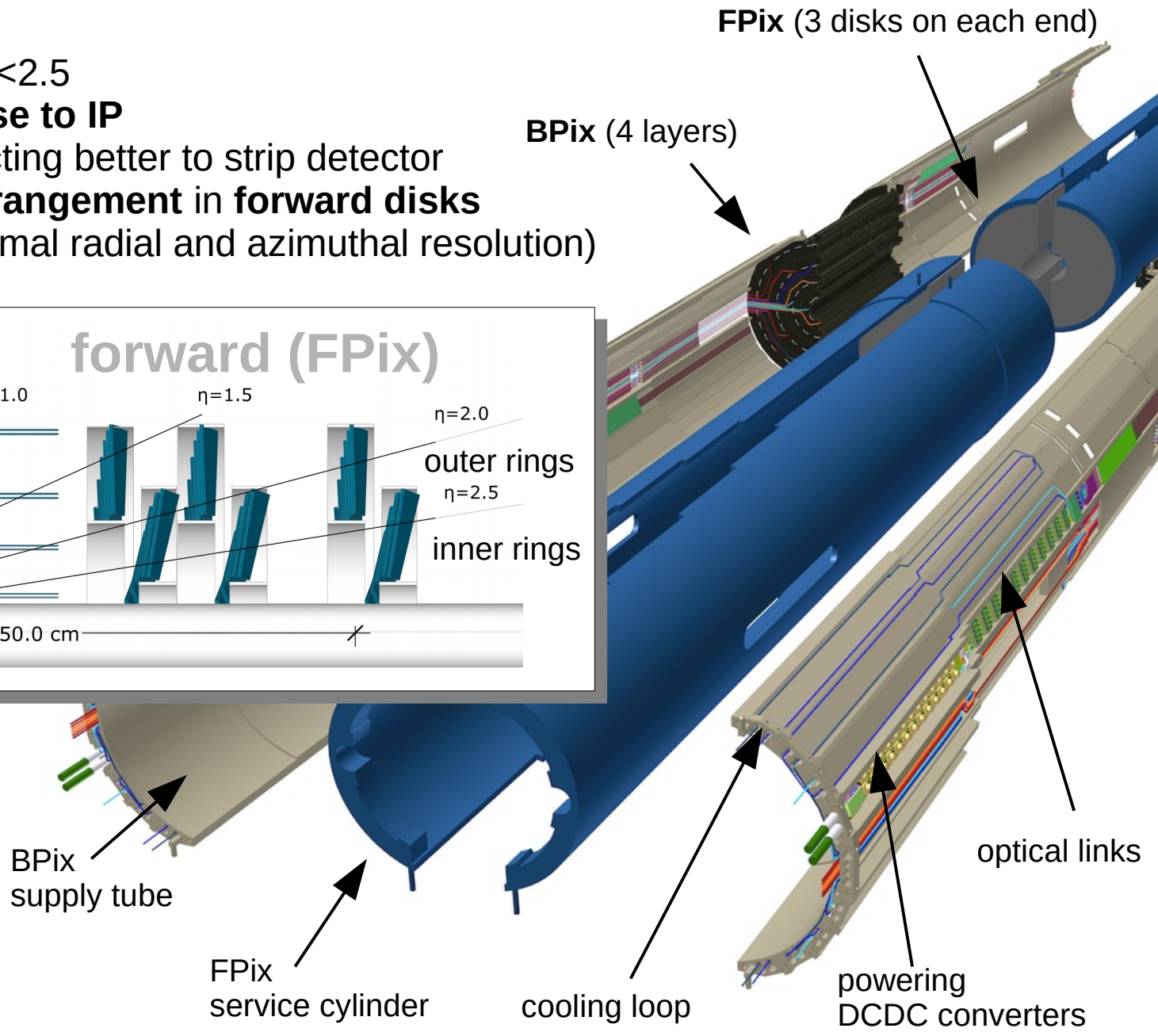


CMS Phase-1 Pixel Detector

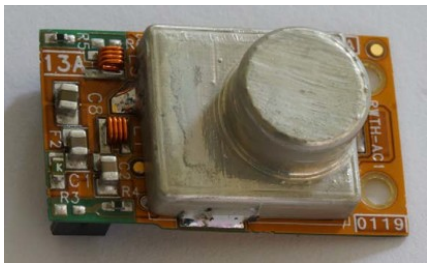
- **4-hit coverage** up to |η|<2.5
- first pixel layer **very close to IP**
- fourth pixel layer connecting better to strip detector
- **turbine-like module arrangement** in **forward disks**
  (inner rings tilted for optimal radial and azimuthal resolution)





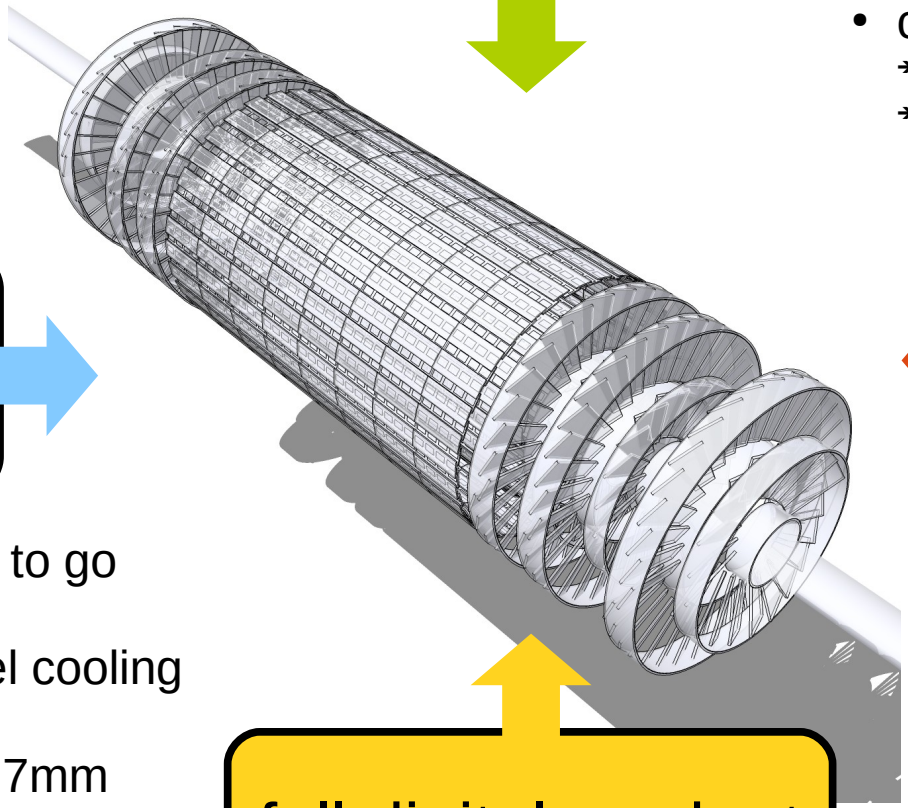


CMS Phase-1 Pixel Detector – Key Technologies



DCDC powering

- 1.9 times more channels
- same power cables
- DC-DC conversion near the detector 9-11.4V to 2.4V/3.0V
- core: FEAST 2 ASIC from CERN
  - magnetic field tolerant: 4T
  - radiation hard: >200 Mrad (Si), 5e14 n_{eq}/cm^2



CO_2 cooling

- -22°C, option to go lower
- stainless steel cooling loops:
  - diameter 1.7mm
  - wall thickness 50µm
- very lightweight

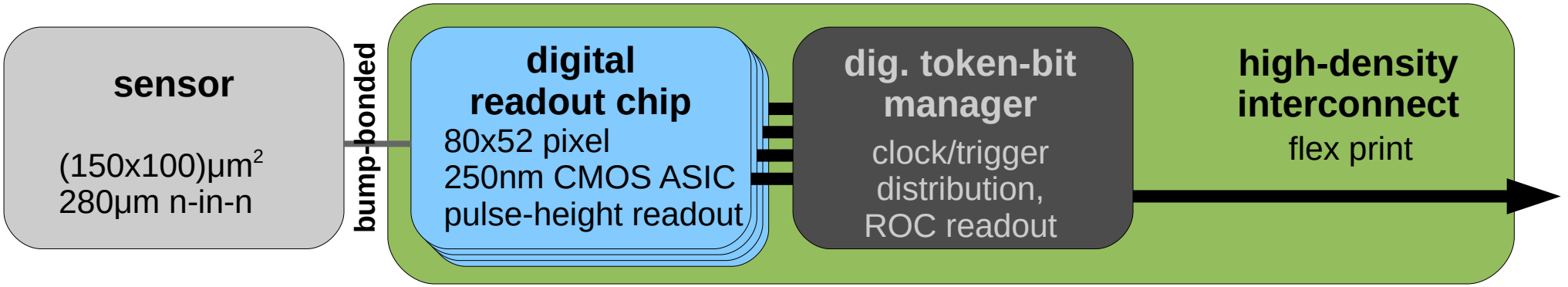
µTCA DAQ

- 108 **FrontEndDrivers** (FED)
- 16+3 **FrontEndController** (FEC)
- all based on **generic AMC card** (FC7) built around Kintech 7 FPGA and 4GB DDR3 RAM
- different flavors realized with **FPGA mezzanine cards** and **firmware**

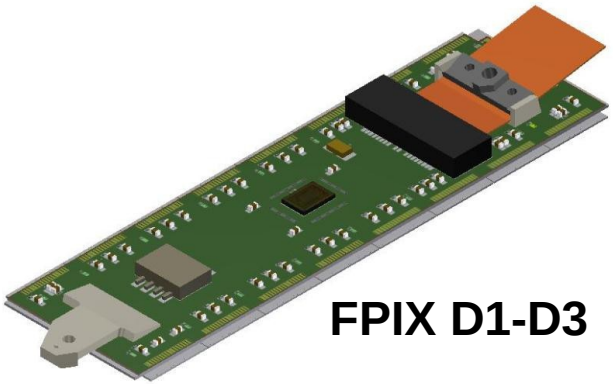
full digital readout

The Phase-1 Pixel Detector contains many key technologies used in the LHC phase-2 upgrade

CMS Phase-1 Pixel Detector – Modules

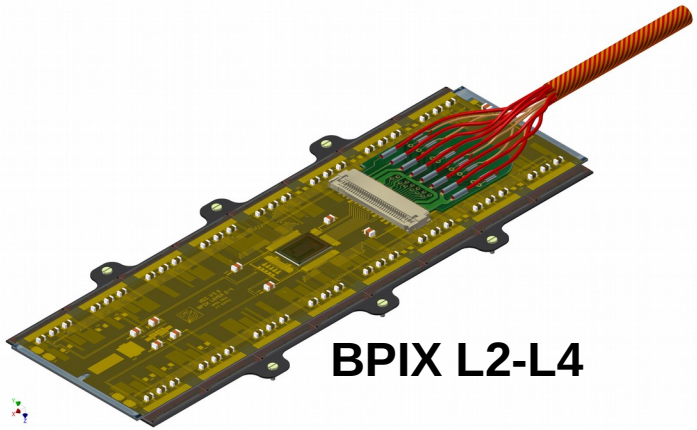


3 flavors of modules



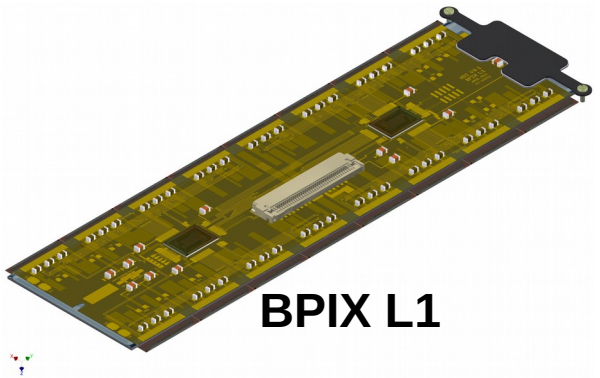
FPIX D1-D3

- 672 modules
- 40-100 MHz/cm²
- **PSI46dig** (column drain)
- 50 Mrad (Si)
- 672 fibers



BPIX L2-L4

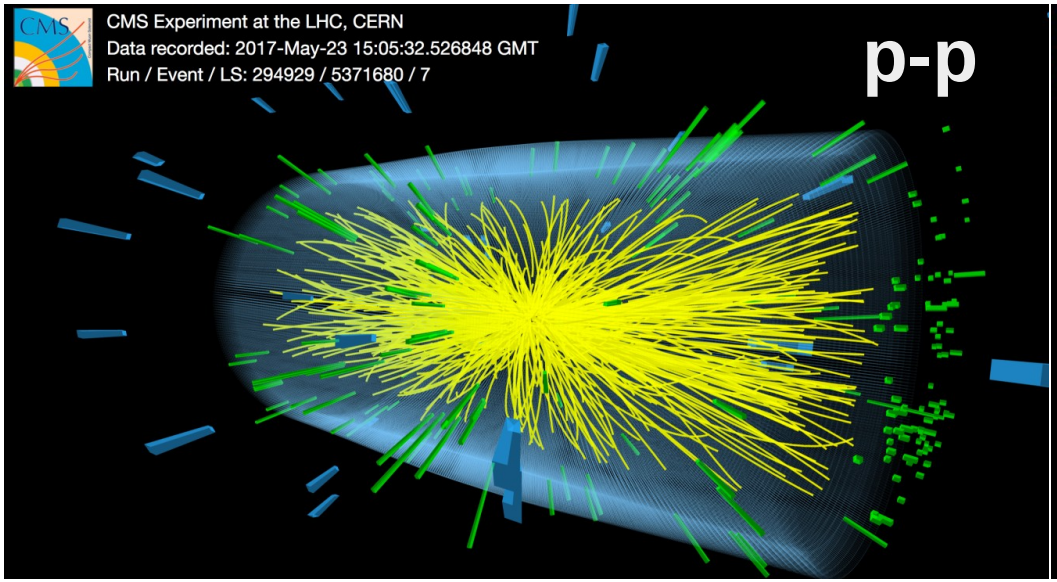
- 1088 modules
- 40-120 MHz/cm²
- **PSI46dig** (column drain)
- 50 Mrad (Si)
- 1312 fibers

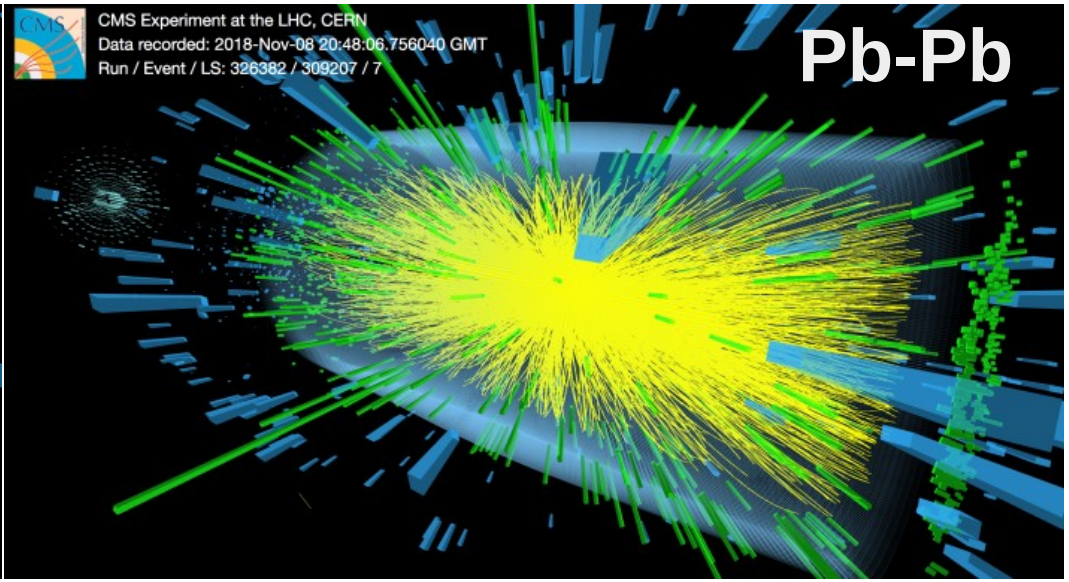


BPIX L1

- 96 modules
- 580 MHz/cm²
- **PROC600 (**dynamic cluster colmn drain)
- 480 Mrad (Si)
- 384 fibers

Operation Experience

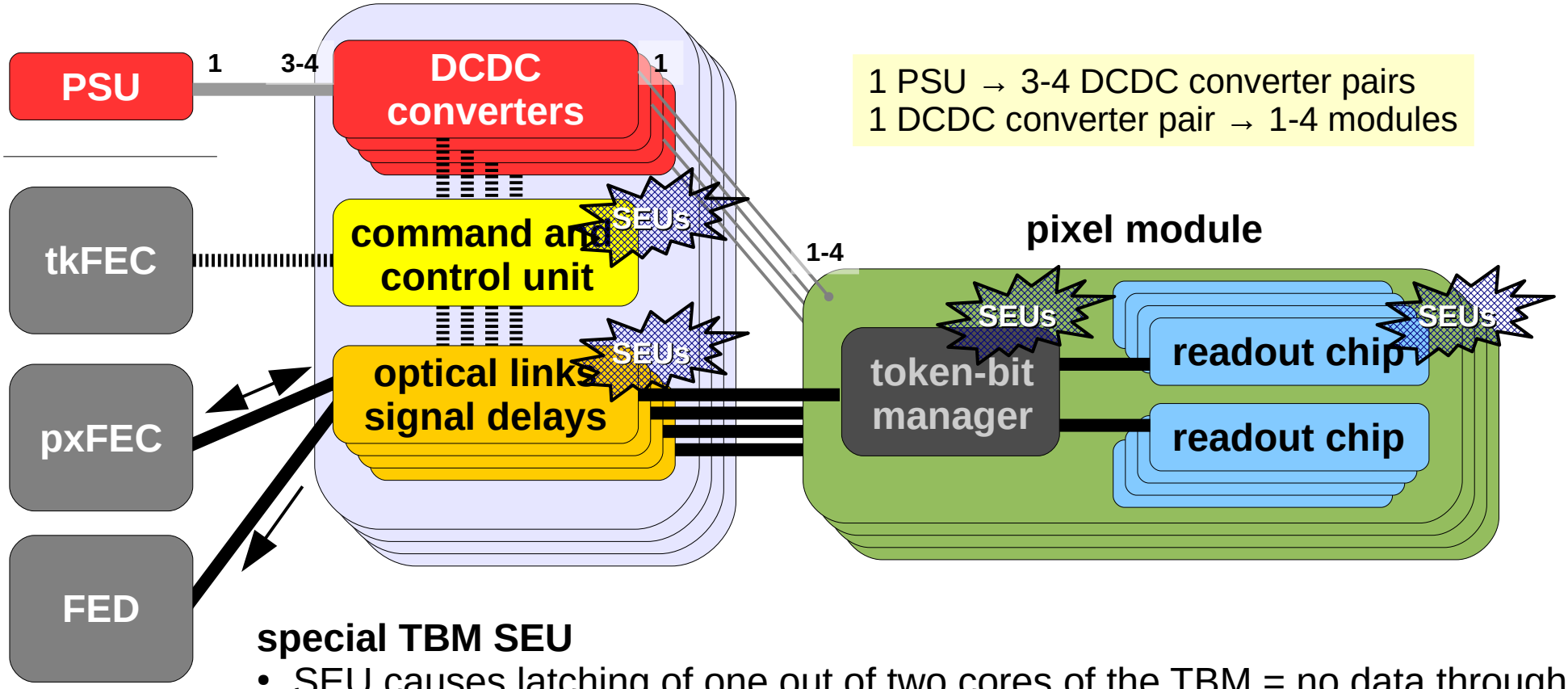




Single Event Upsets

status in 2017/2018

- single event upset expected in high radiation environment
- SEUs observed in many components in 2017/2018
- normal procedure: download configuration parameters to the front-end regularly



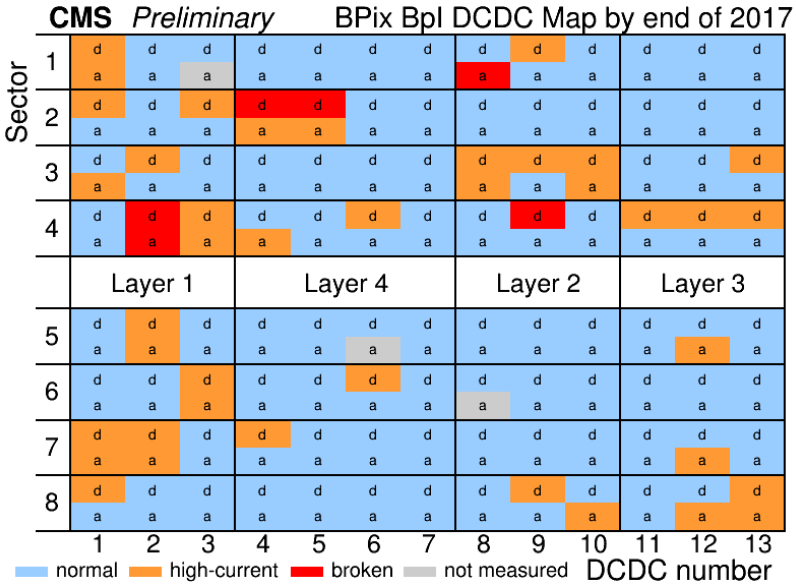
special TBM SEU

- SEU causes latching of one out of two cores of the TBM = no data throughput
- reprogramming the TBM does **not** resolve the problem
- only powercycle recovers the TBM core and thus the ROCs behind
- in 2017: command and control unit used to disable/enable DCDC converter

The DCDC Story

timeline

- October 5th 2017: first DCDC converter stopped working
- extrapolation of failure rate to 2018: no sufficient tracking by mid 2018
- extraction of the detector and replacement of ALL converters with similar version, but bigger fuse (allowing to operate the converters at a lower input voltage = higher input current)

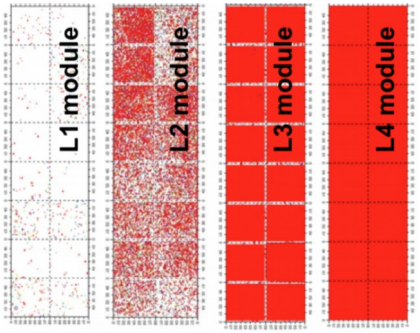


characterization of extracted converters

- I-V characterization of all extracted converters:
  - 65 not switching anymore
  - 333 higher currents in disabled state
  - rest (~1800) behaves normally

damage on modules

- sensor leakage currents cannot be drained efficiently if ROC is not powered
- damage on the pre-amplifier if HV on/ LV off
- damage proportional to time and sensor leakage current
- 6 (accessible) out of 8 damaged modules in L1 replaced



The DCDC Story

after months of investigation

- chip designers of the FEAST chip found a way to reproduce the breaking symptoms
- once a feedback loop was established, breaking mechanism could be identified quickly

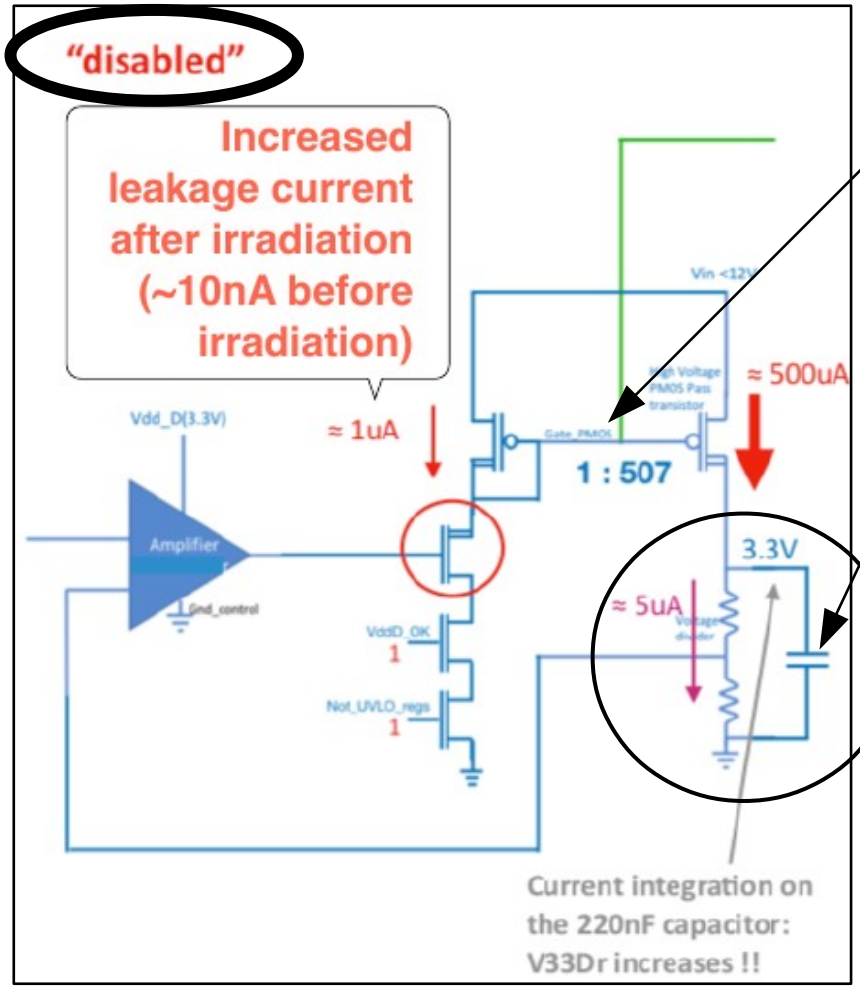


figure by Federico Faccio

amplifying current mirror

capacitor charging up in the disabled state causing voltage spikes well beyond 3.3V

part providing current to the drivers of the power transistors

two possible results

- high leakage current forms new ohmic path to ground (→ high current)
- converter breaks irreversibly (→ broken)

consequences for operation

- lower input voltage helps
- stop disabling the output
- what about latched TBM cores? → enable/disable output of the power supply (not DCDC)

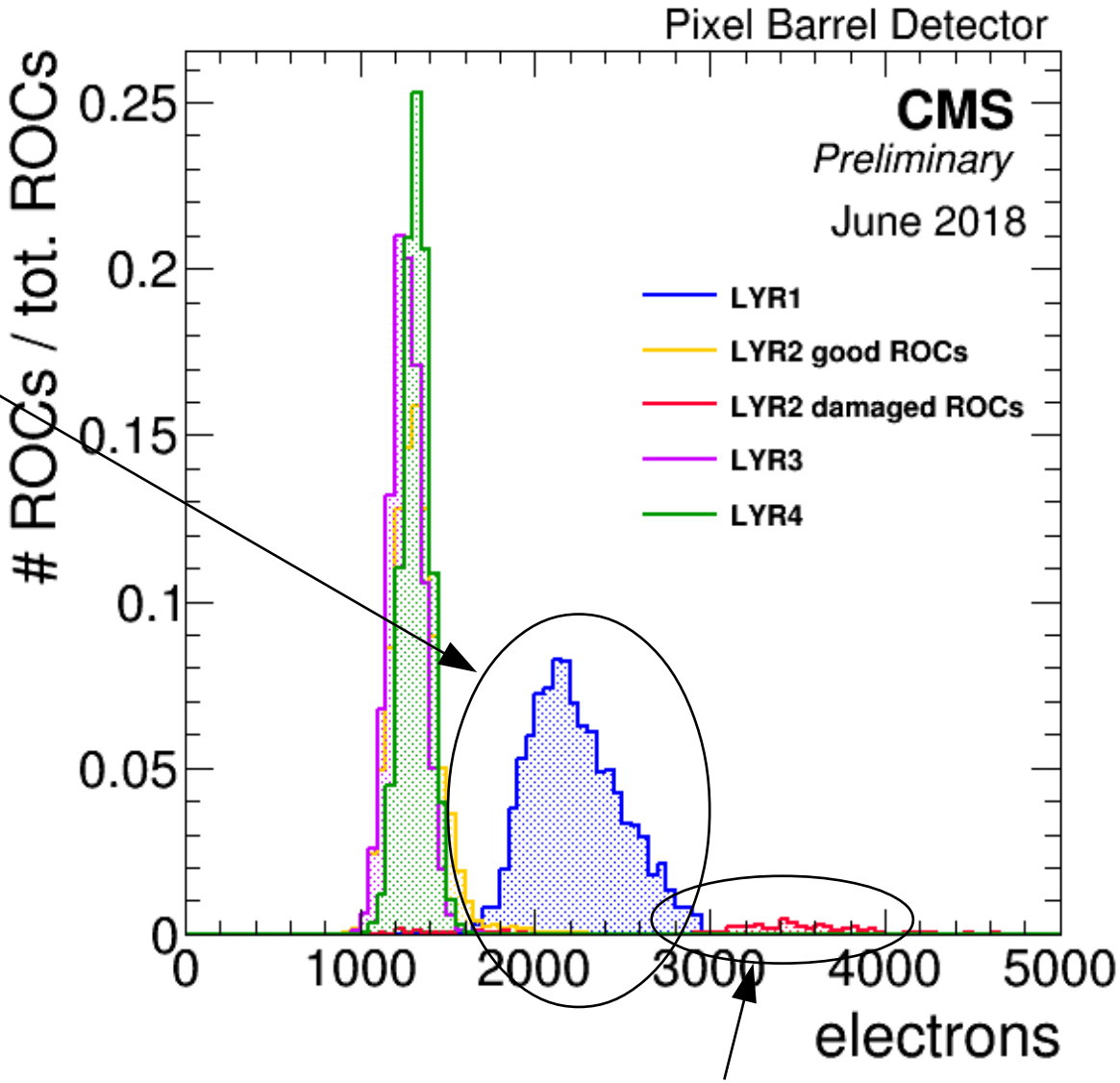
no DCDC converter broke in 2018!

Layer-1 Readout Chip Crosstalk

observation
- extra hits appear correlated with real hits
- effect is highly rate dependent

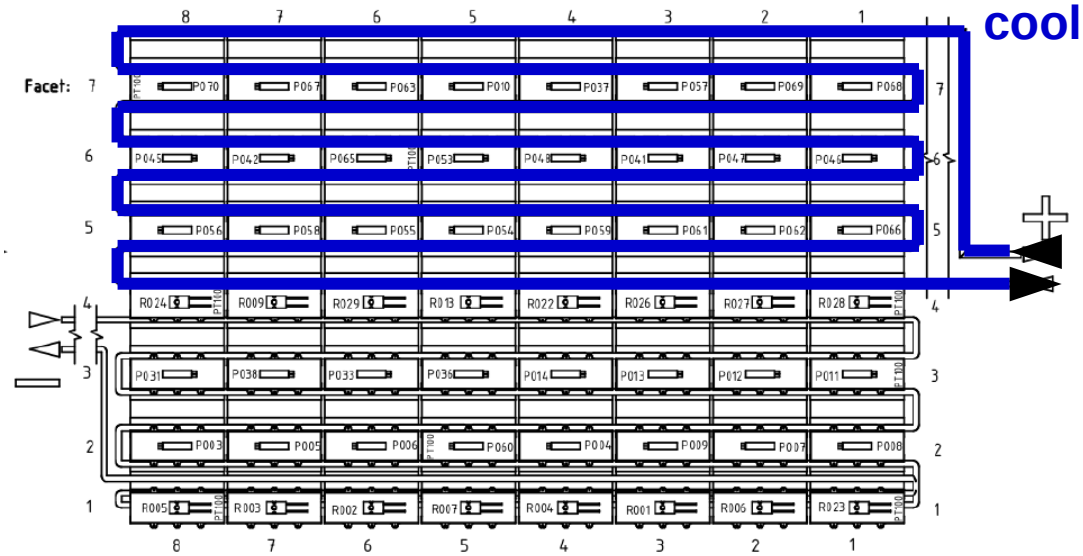
consequences for operation
- ➔ artificially higher thresholds in order to operate the chip efficiently with beam

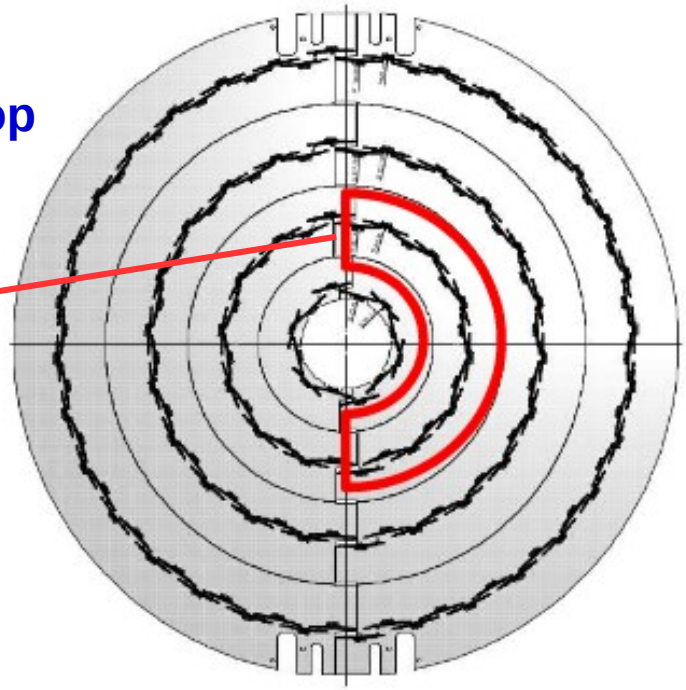
mitigation
- two main sources of the problem identified
  - ➔ dominant contribution can be mitigated by optimized programming sequence
  - ➔ better shielding in the ROC design will further improve the situation
- will be addressed in new version of PROC600

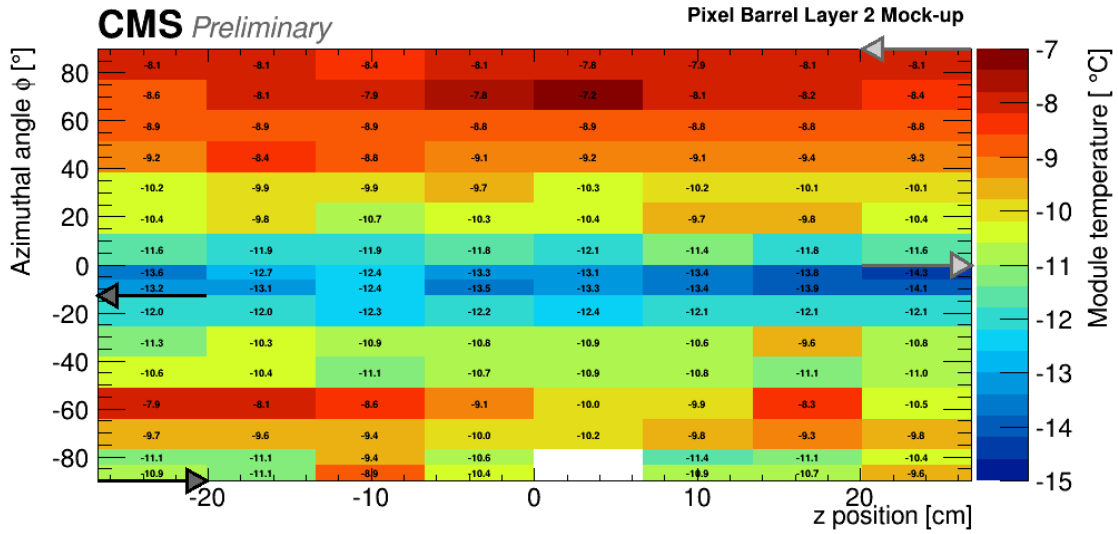


Experience with CO2 Cooling

thermal mock-up for CO2 cooling system







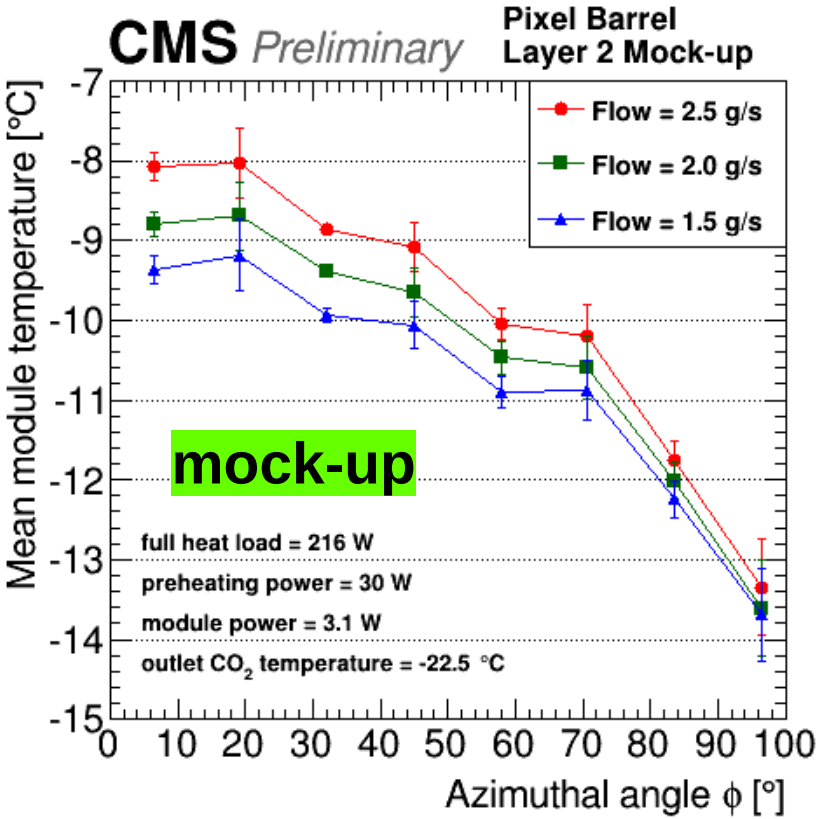
setup

- realistic layer-2 **half-shell rebuilt** (piping, mechanical structure, modules)
- **adjustable heat load** on pseudo modules
- small scale CO2 cooling plant in the lab
- temperature sensor on top of each module

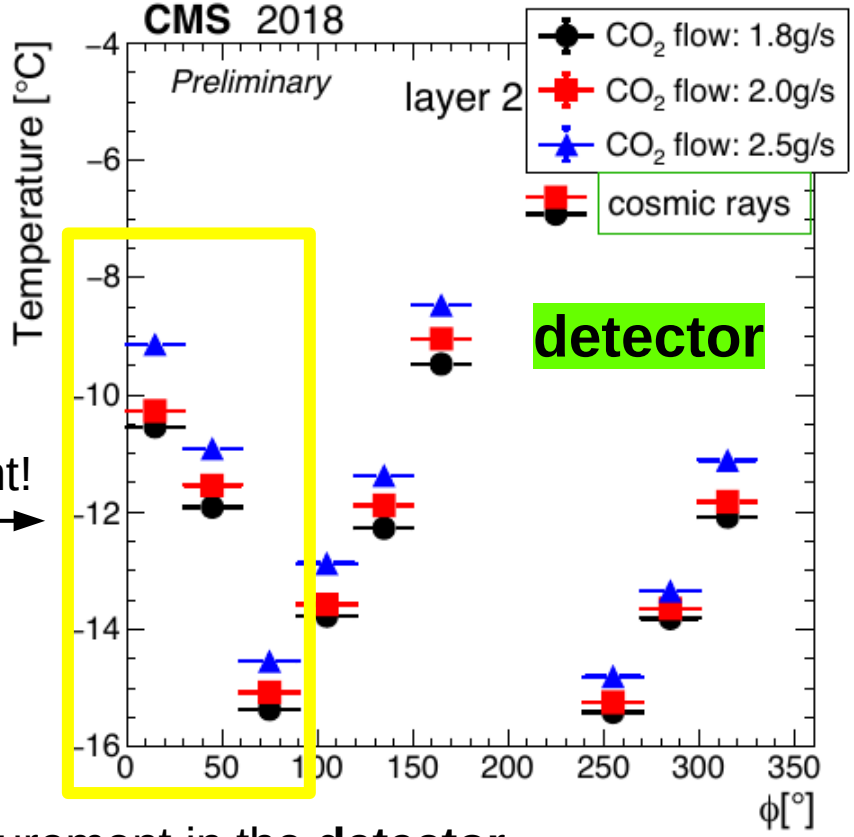
observation

- strong temperature gradient along pipe
- 4-5K along one cooling pipe

Experience with CO2 Cooling



good agreement!

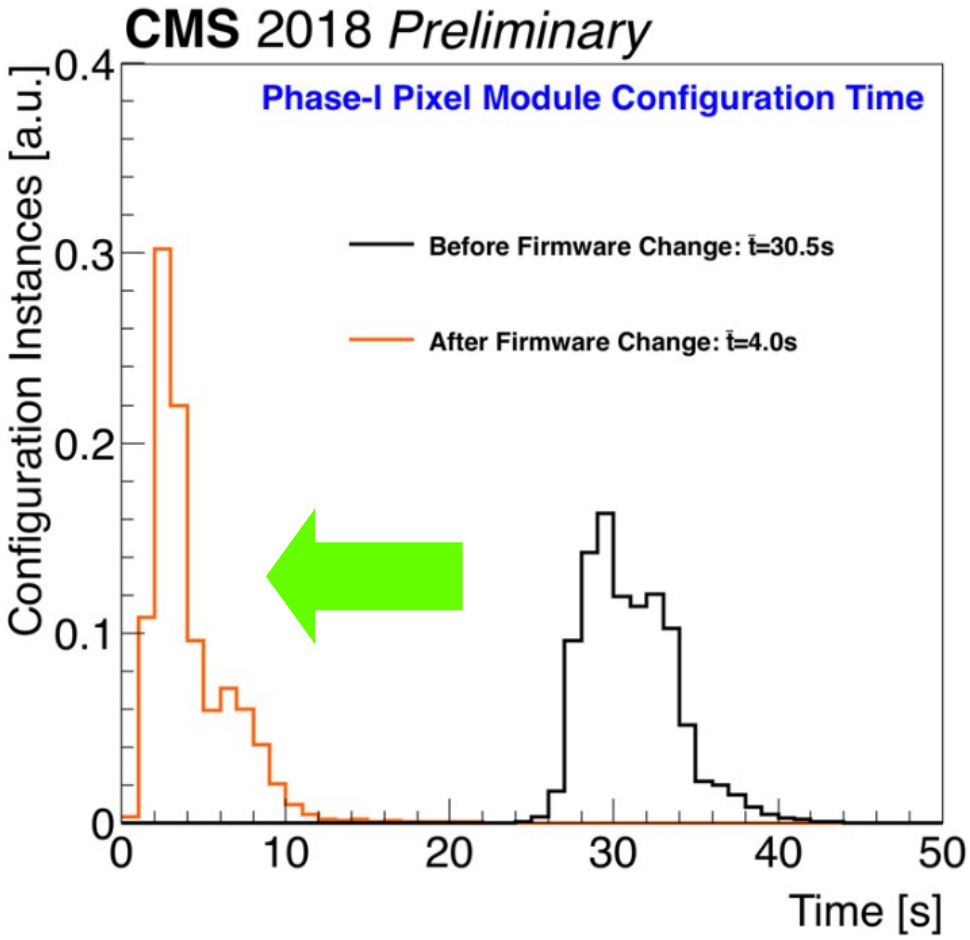


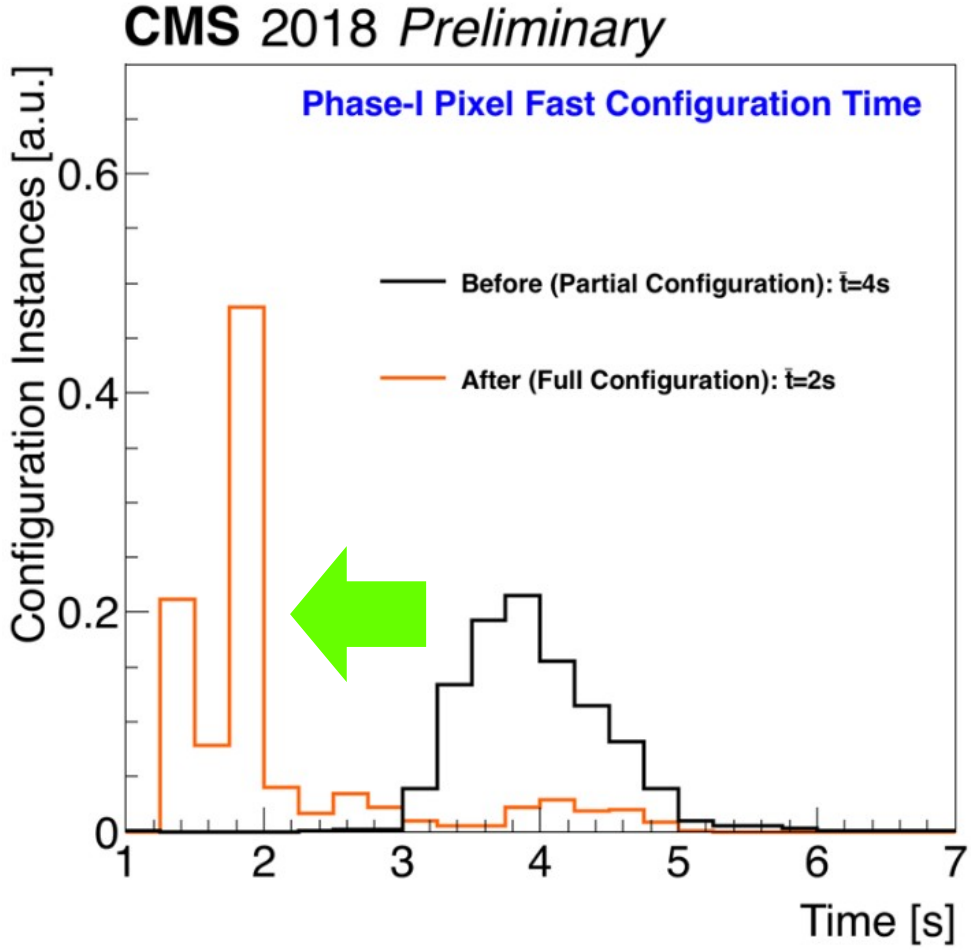
- observation in the **mock-up consistent** with measurement in the **detector**
- quite some **impact on the uniformity of the leakage currents** in same layers (factor 1.8)

lessons learned

- expect some temperature gradient with evaporative CO2 cooling
- characterize cooling performance in a mock-up
- 2-phase CO2 is a very efficient coolant, but it is not easy to warm up the detector if there is no heat dissipation from active components
- controlled annealing? safety?

Improvements in the Backend DAQ System

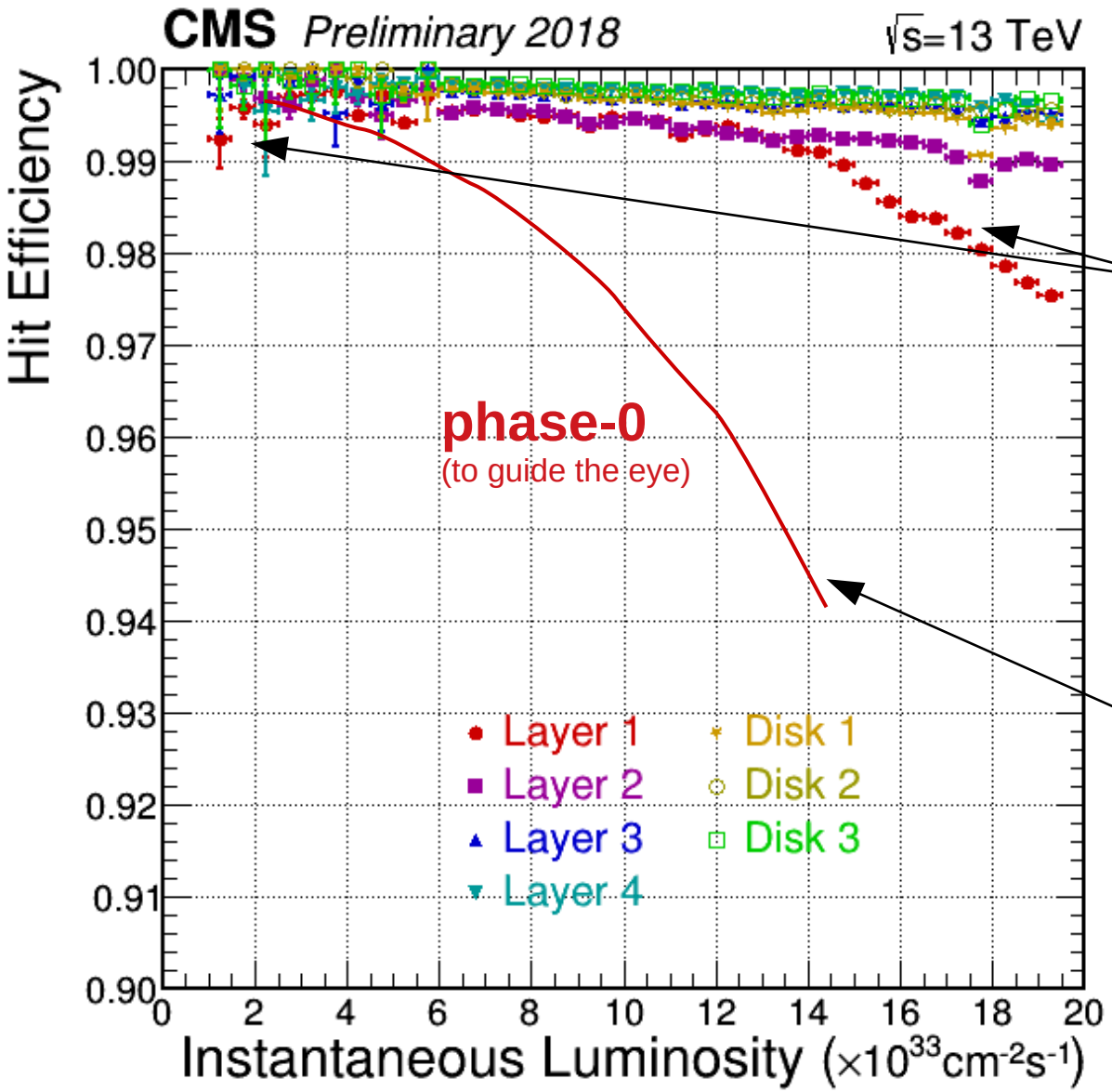




- very **reliable operation** of the µTCA backend electronics
- significant improvements during 2018 by fully **exploiting the DDR memory** capabilities on the FC7 cards
- **speed-up of front-end configuration** from 4s (only global ROC parameters) to 1.5-2s (also pixel level settings) by preloading the data into DDR

Detector Performance and Radiation Effects

Hit Efficiency

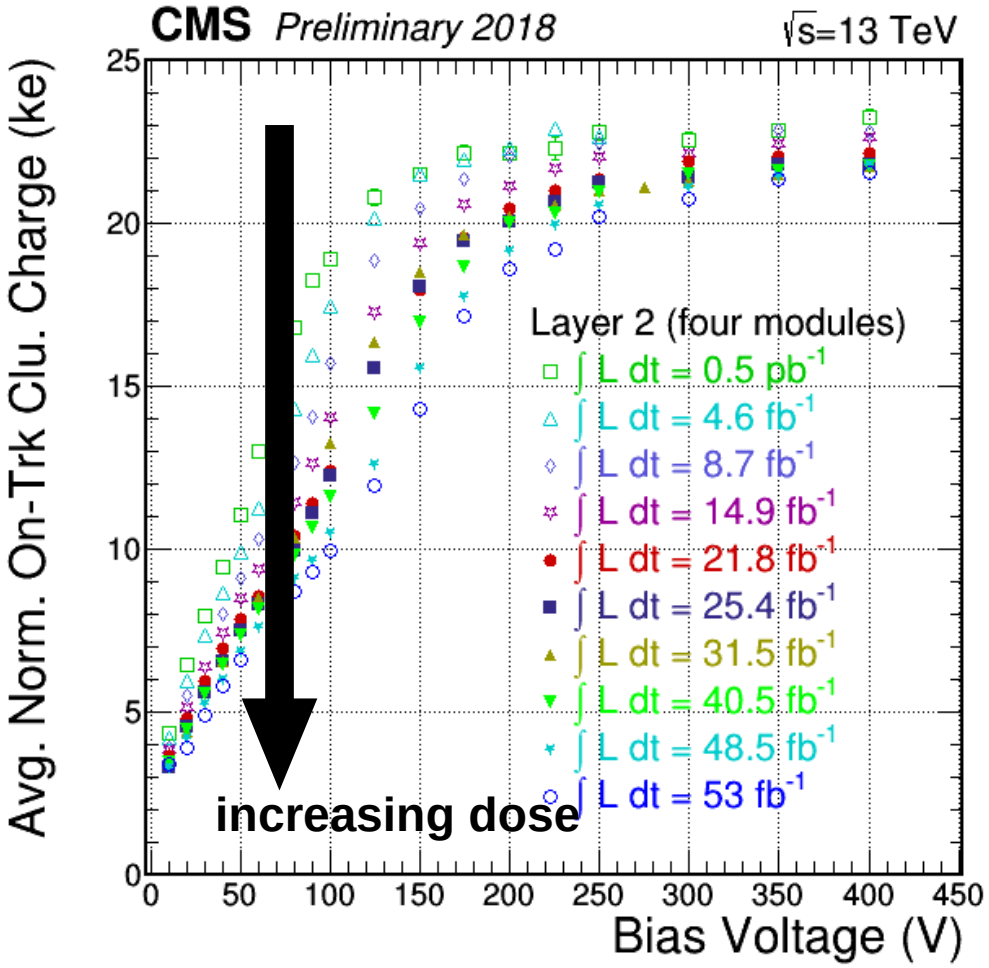


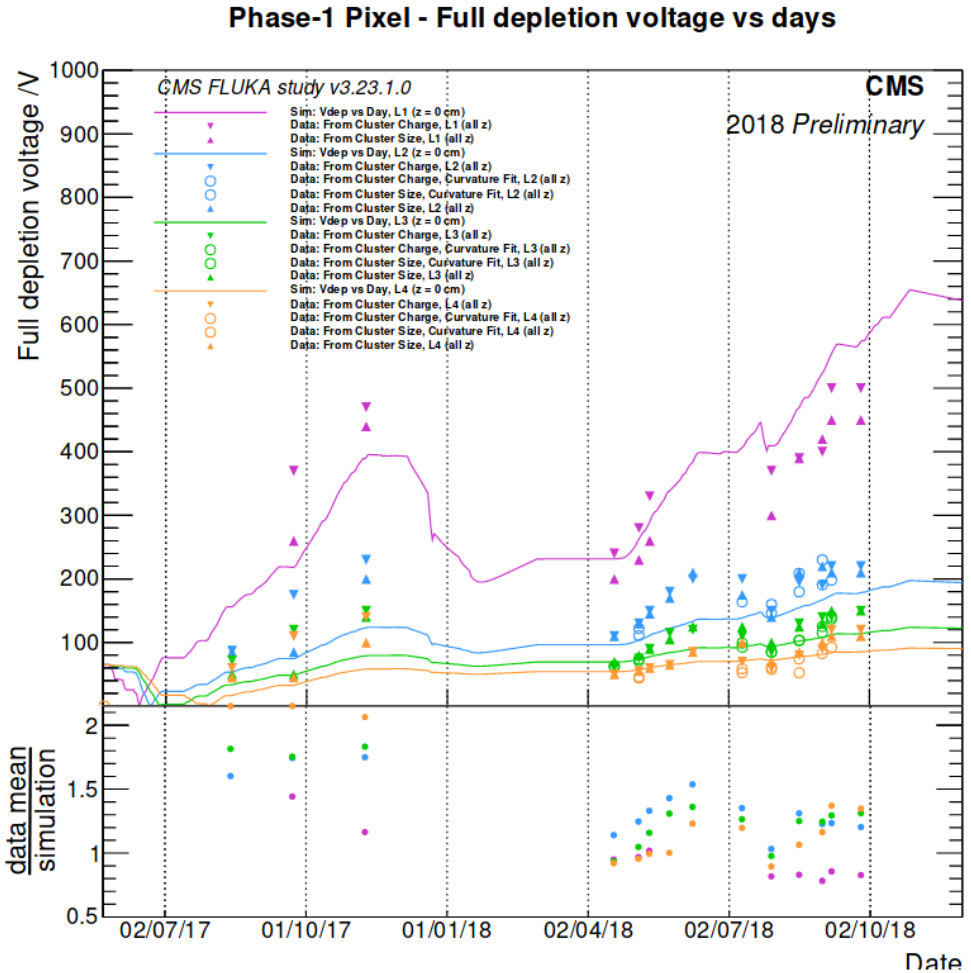
- overall **excellent hit efficiency**
- inefficiency in layer 1 for luminosities >1.4e34 $cm^{-2}s^{-1}$ and <1e33 $cm^{-2}s^{-1}$ understood
- will be addressed in new version of PROC600

note:
r_{L1}(phase-0)=43mm
r_{L1}(phase-1)=29mm

phase-1 ROCs exceed performance of phase-0 by far

Monitoring and Prediction of Depletion Voltage

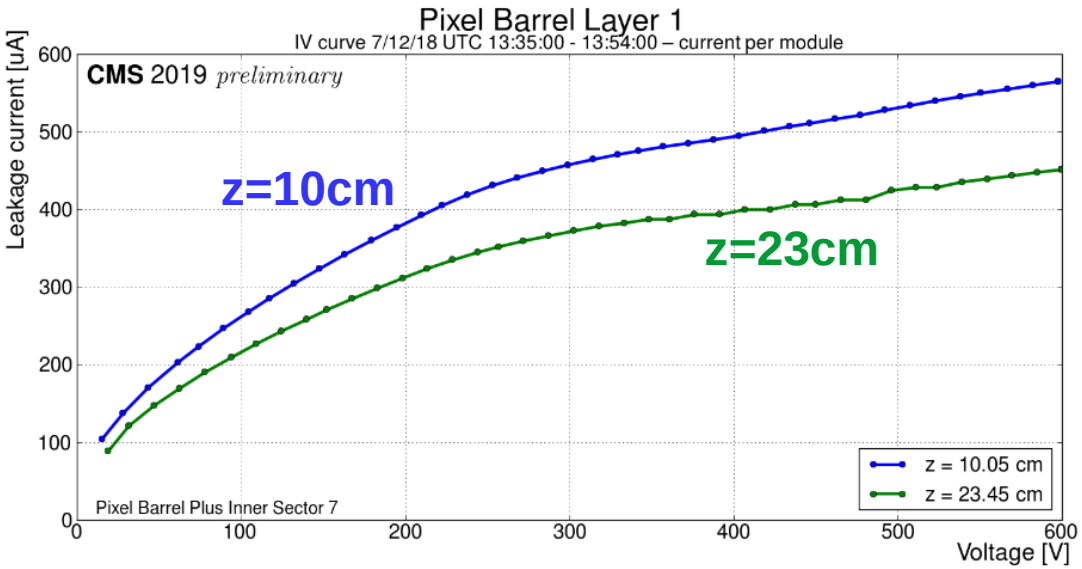


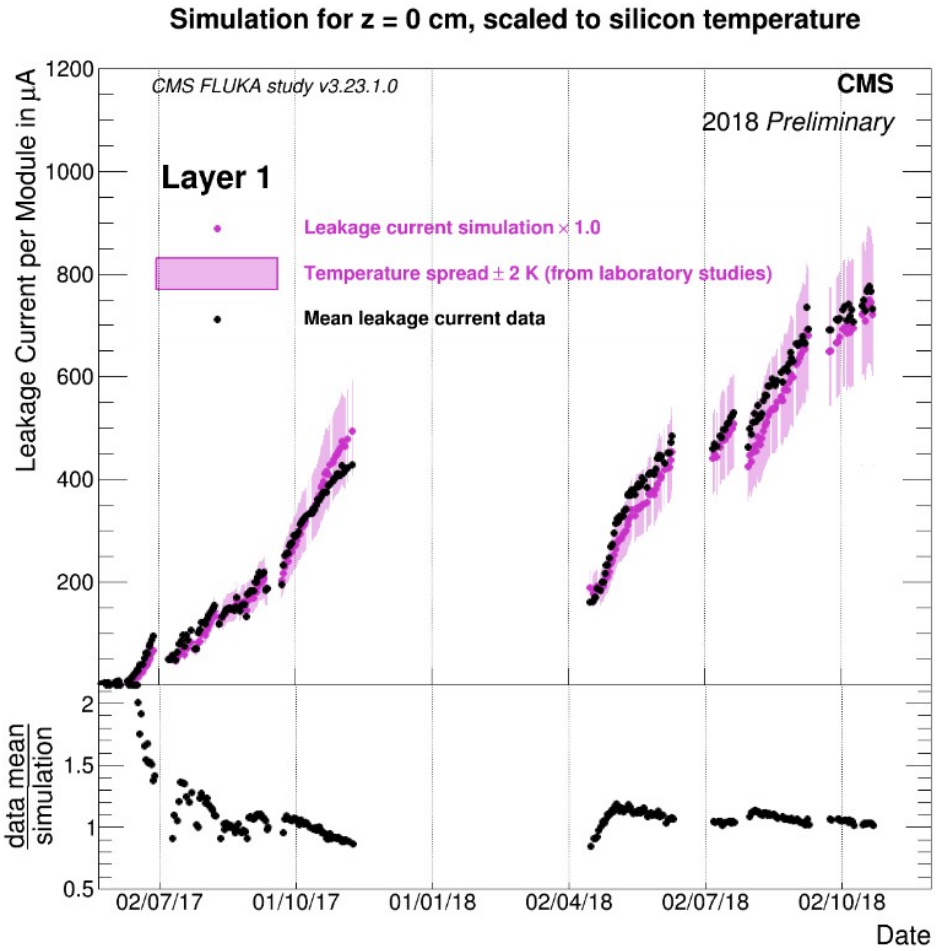


- **regular sensor bias scan** on representative subset of modules in order to monitor radiation effects on sensor
- simulation based on Hamburg-model (effective space charge) to predict evolution
- very valuable tool for detector operation → adjustment of bias voltage

Monitoring and Prediction of Leakage Current

- **excellent agreement** between predicted and measured leakage currents in layer 1
- different scale factors in other layers
- main uncertainties
  - FLUKA prediction
  - thermal model
- improvements on both aspects expected in the future
- first projections to end of run-3: **no limitations** from the power supplies wrt. **leakage currents**





- ATLAS measures **unexpected z-dependence** of **leakage currents** in the IBL
- similar effect **observed in layer 1** within CMS

Outlook & Summary

Plans for LHC Long Shutdown 2 (LS2)

general

- keep the detector dry and cold most of the time (~0 °C)
- replace all DCDCs with new version
- upgrade power supplies to be able to go to 800V (was 600V)
- general maintenance

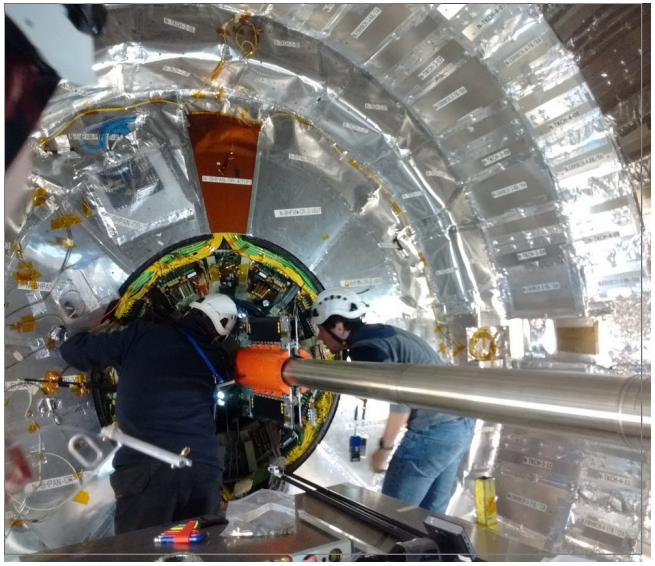
layer 1 replacement

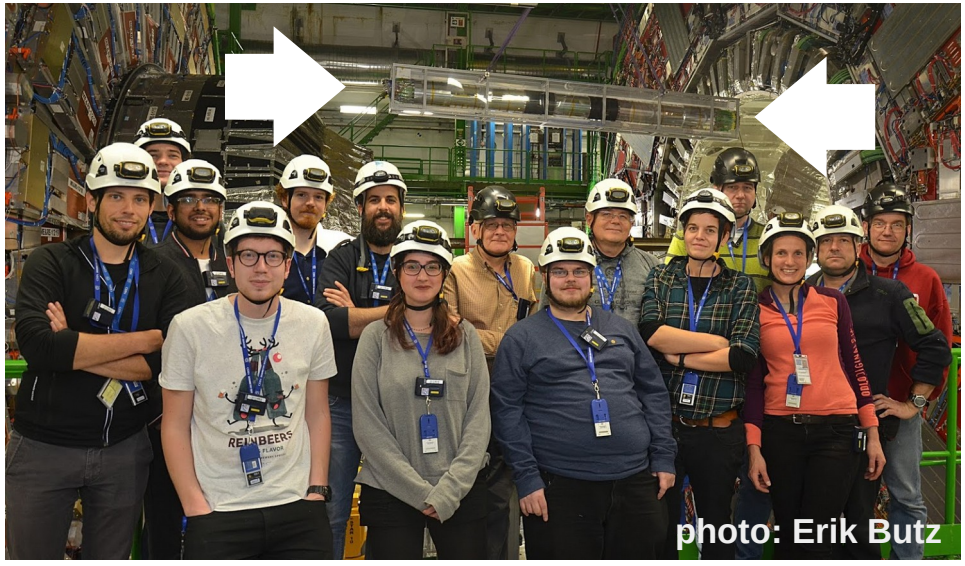
- new version of the TBM
  - protection against SEU (latching core)
  - additional timing adjustment (compensation for differences between PROC600/psi46dig)
- new version of PROC600
  - mitigate crosstalk → lower thresholds
  - mitigate further sources of inefficiencies

CMS Pixel detector will be in a significantly improved state at the beginning of LHC Run-3

Summary

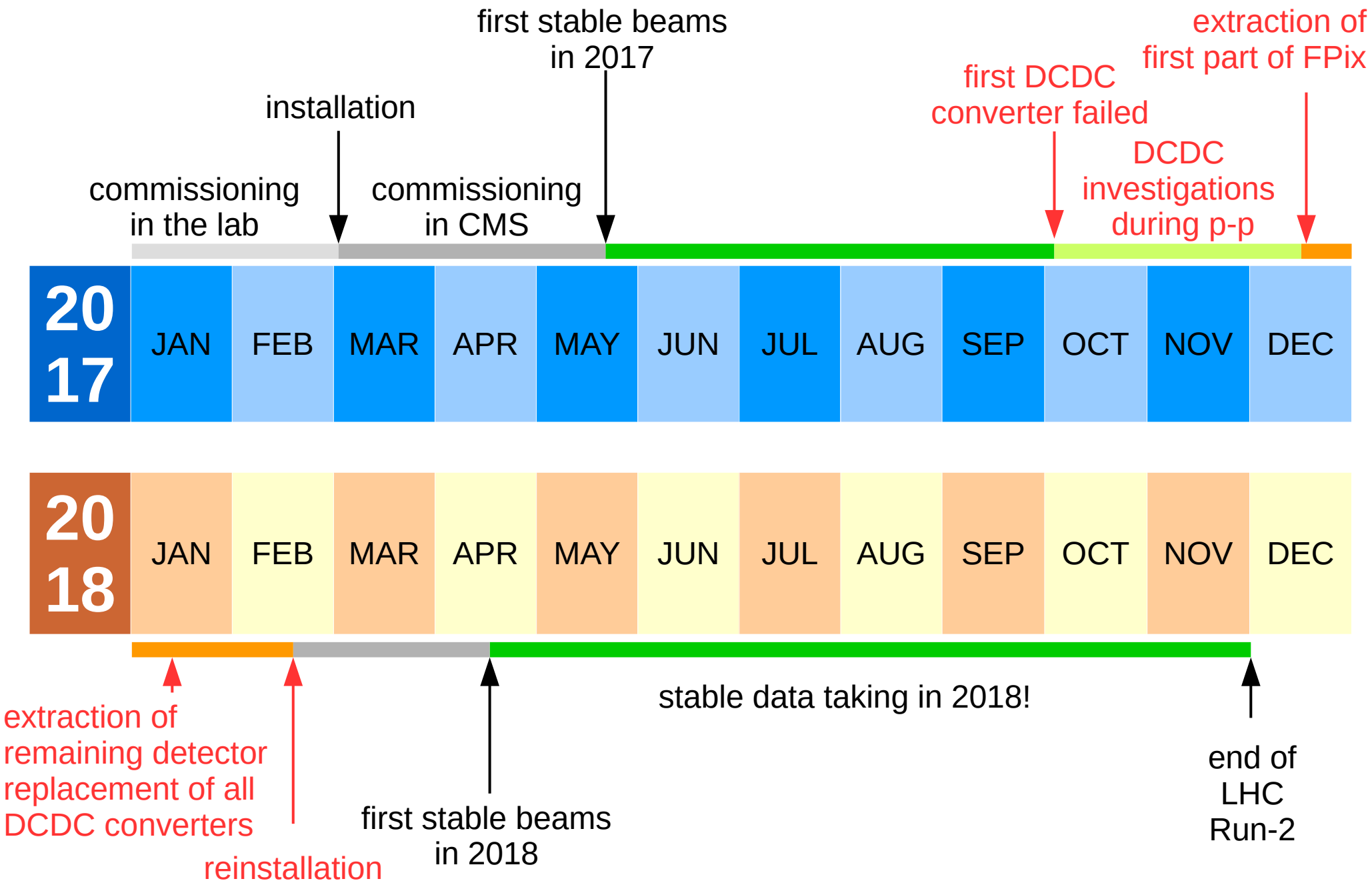
- successful commissioning and operation of the CMS phase-1 pixel detector since 2017
- unforeseen extraction at the end of 2017 due to massive DCDC failure
- very smooth running in 2018
- gathered very valuable experience with key technologies of modern silicon detectors
- significant improvements planned for LS2 to get the detector in the best possible shape for its remaining lifetime





Backup

Timeline of the last two years



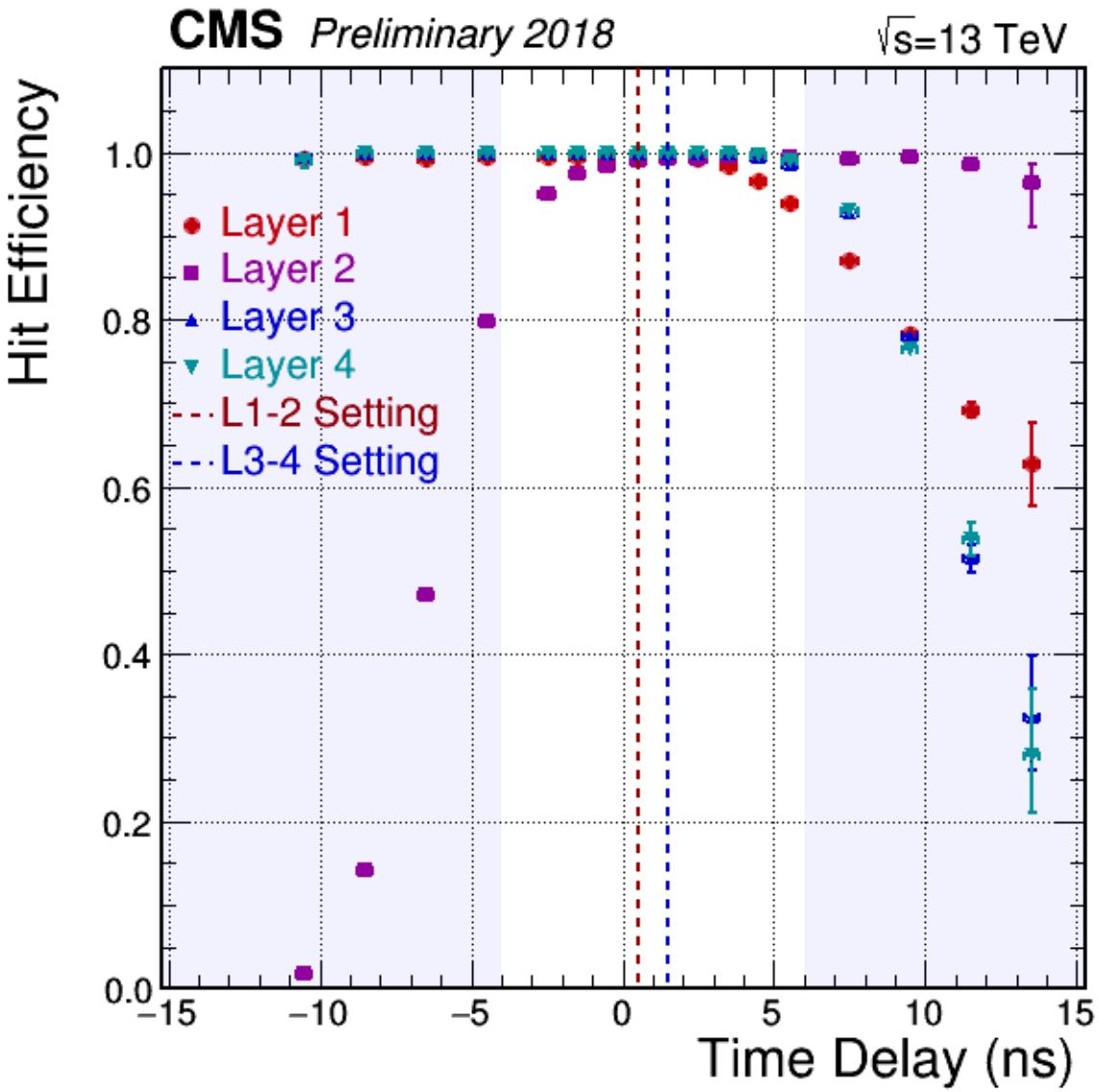
Timing between Layers

timing between layers

- read-out chip in layer 1 (PROC600) half a clock cycle (12.5ns) faster than the ROCs in layer 2-4 and FPix (psi46dig)
- shared clock/trigger distribution in layer 1/ layer 2 per φ-sector
- read-out of layer 2 too early, layer 1 too late
- very small overlap of efficiency plateau

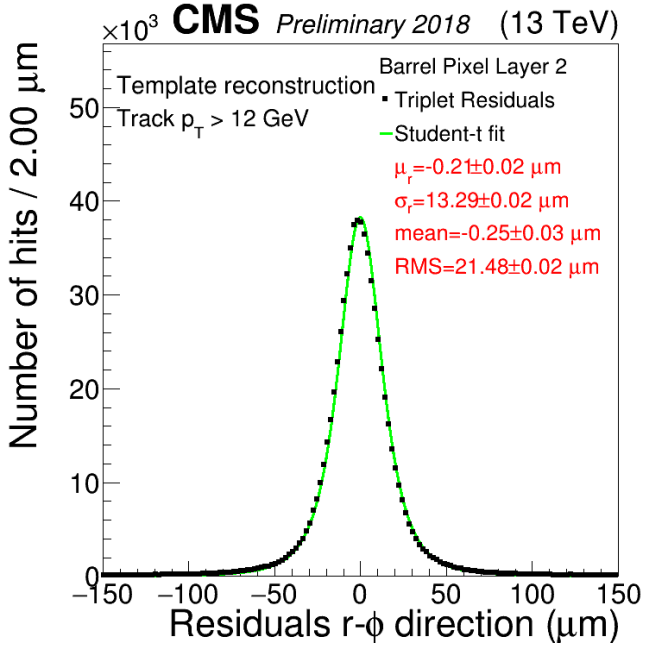
plans for the future

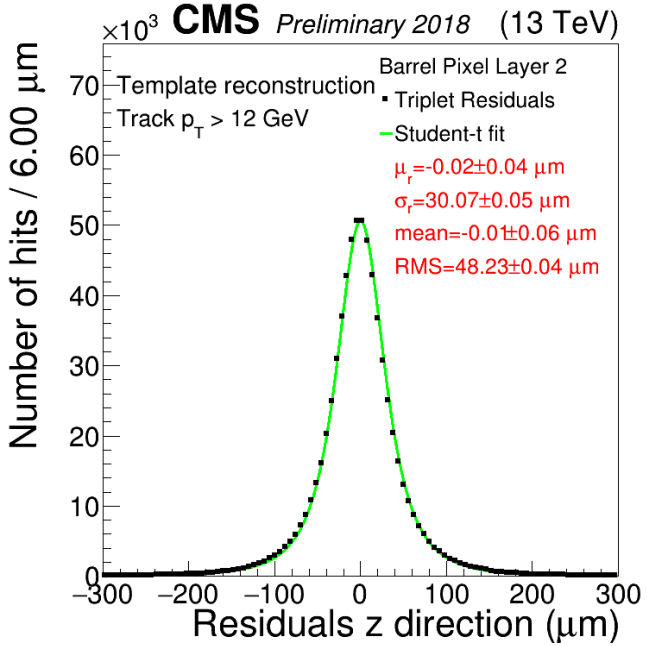
- current solution seems to work, though is not comfortable to operate so close to the efficiency edge
- TBM for layer 1 replacement includes adjustable delay (on the module level)



Residuals/ Resolution

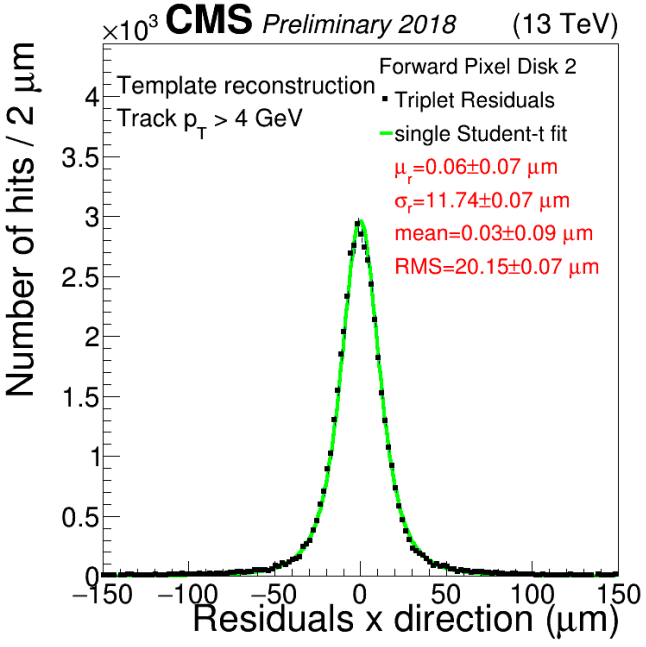
BPix L2

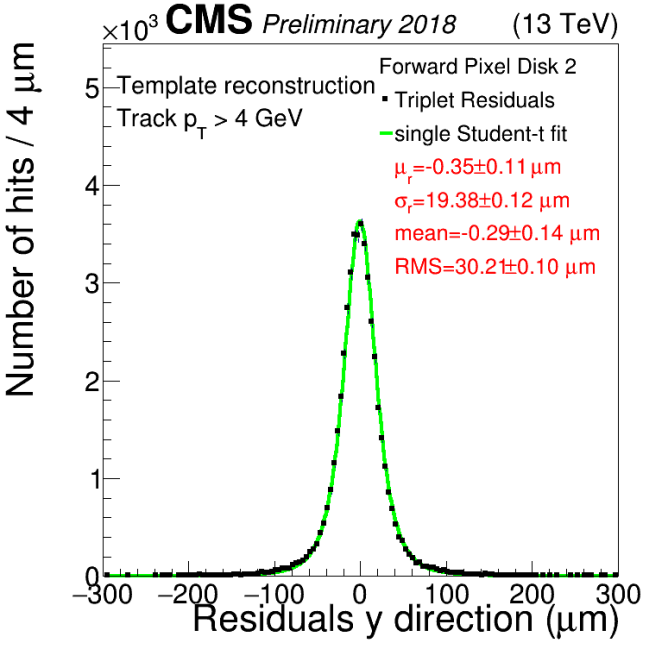




13 µm (r-φ)
30 µm (z)

FPix D2

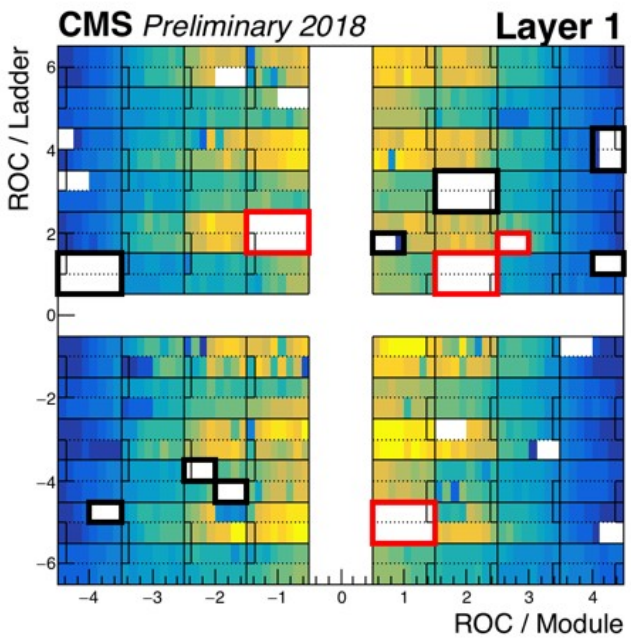


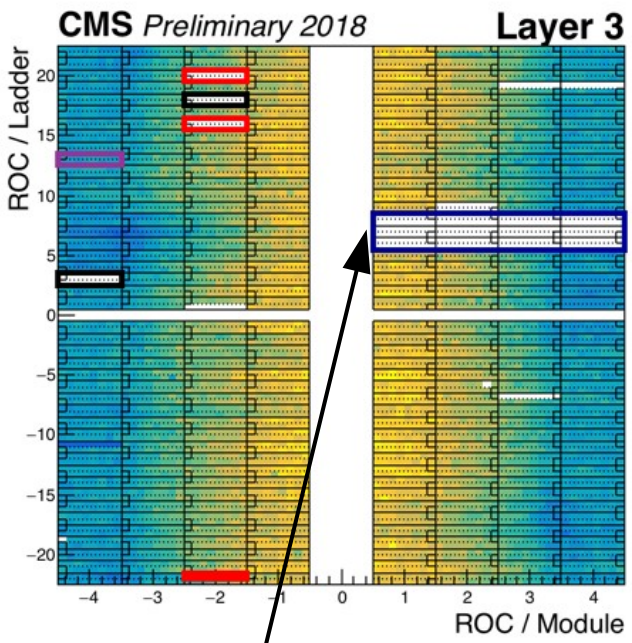


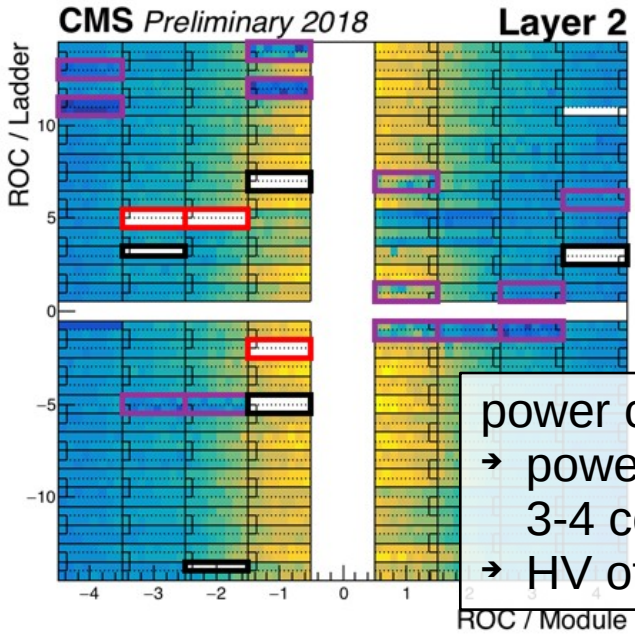
12 µm (x^{mod}),
19 µm (y^{mod})

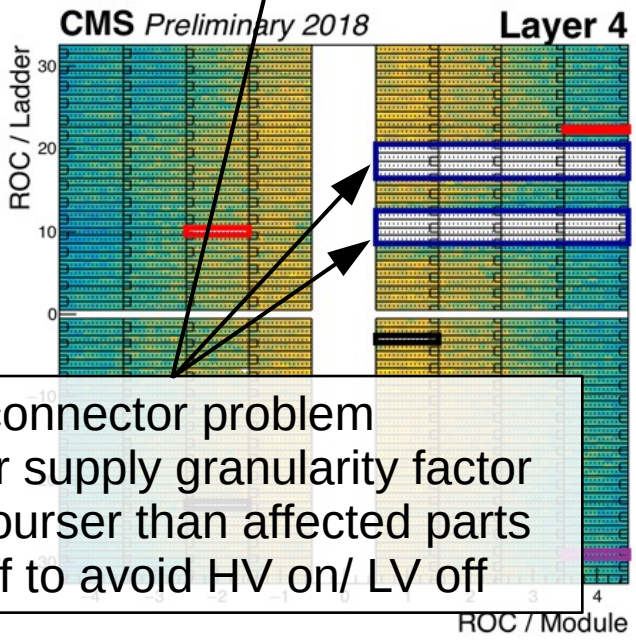
excellent hit resolution

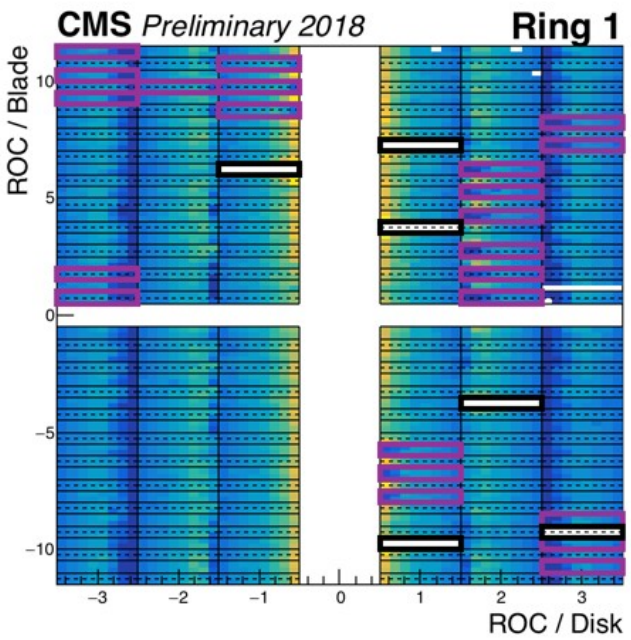
Detector Status

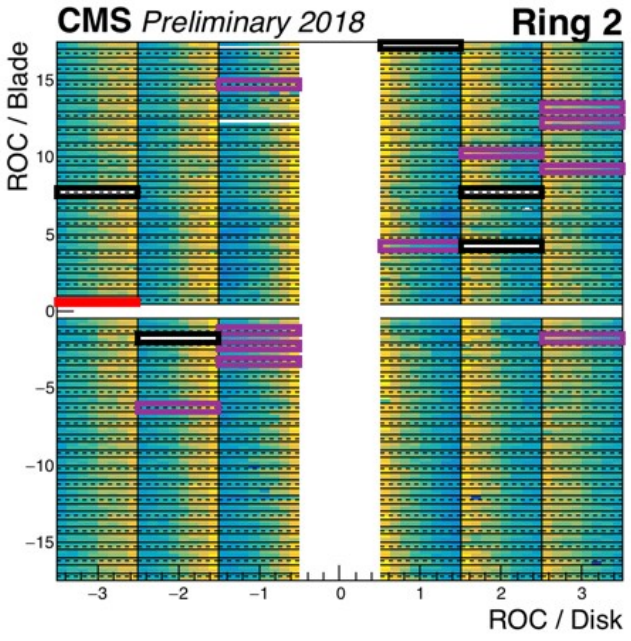






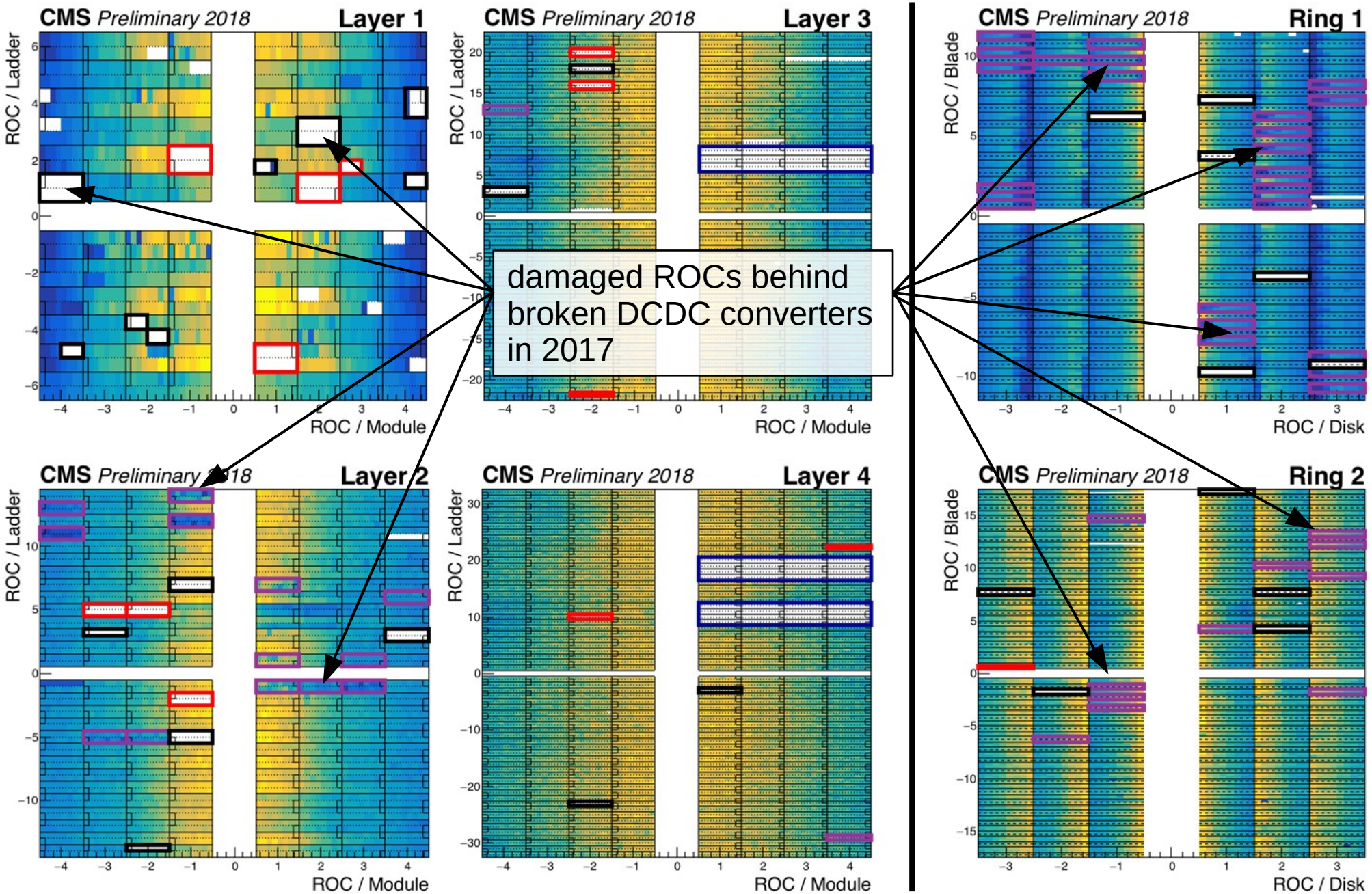




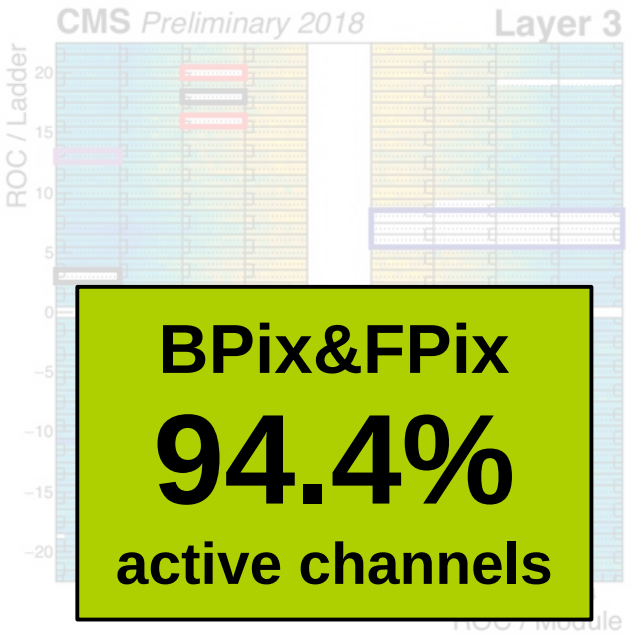


power connector problem
- ➔ power supply granularity factor 3-4 courser than affected parts
- ➔ HV off to avoid HV on/ LV off

Detector Status



Detector Status



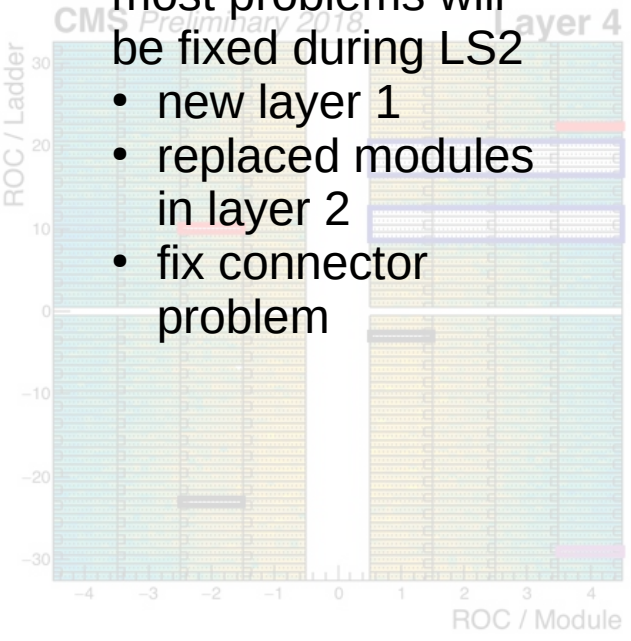
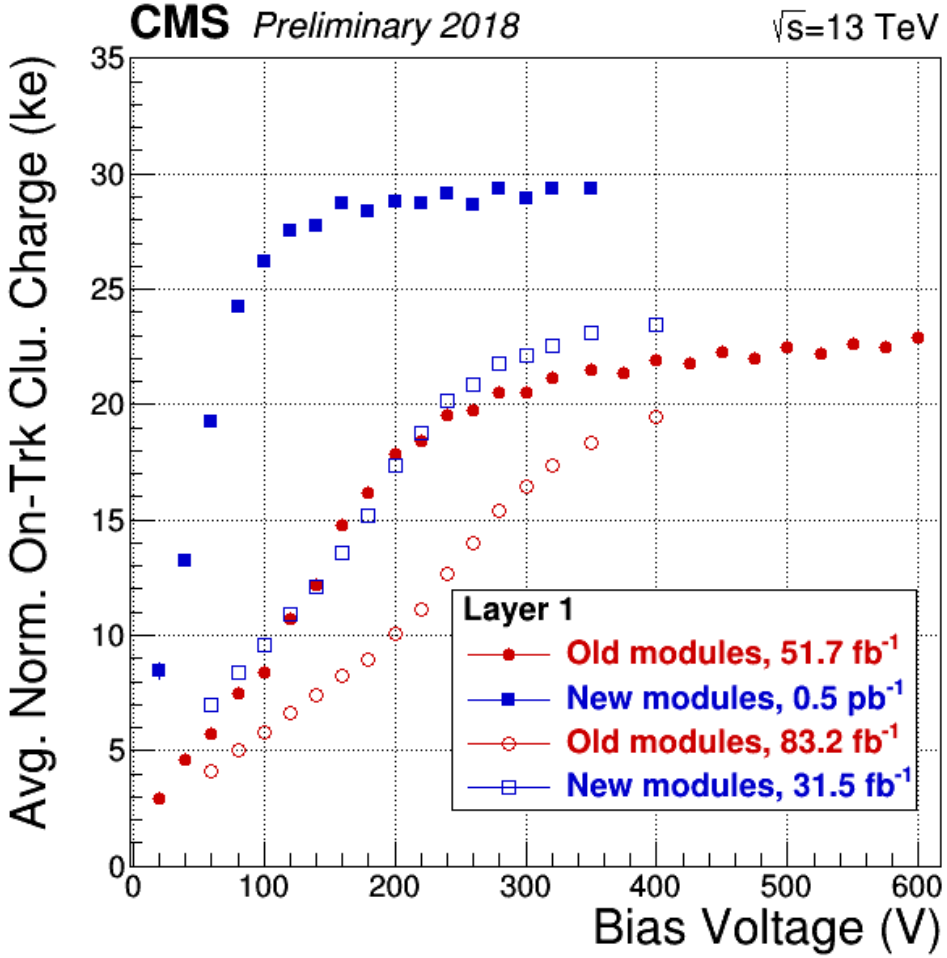
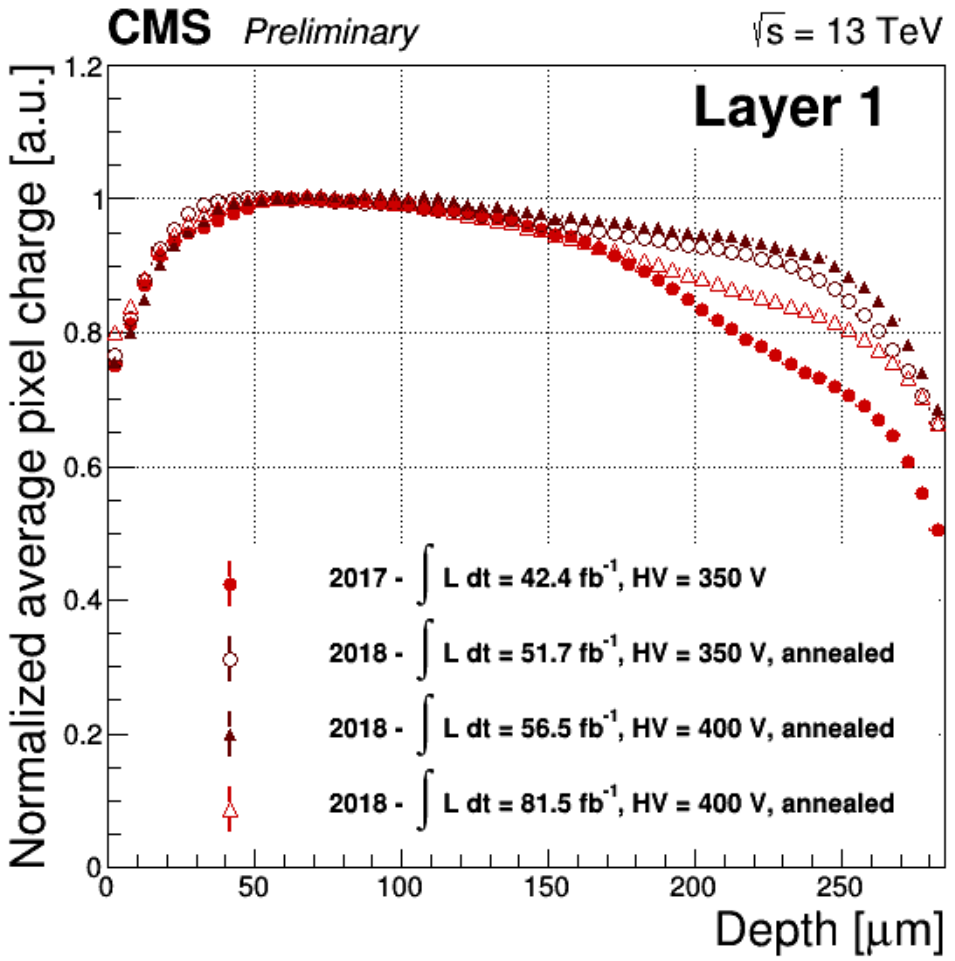
BPix&FPix

94.4%

active channels

most problems will be fixed during LS2

- new layer 1
- replaced modules in layer 2
- fix connector problem



Monitoring of Radiation Effects