Measurement results of the MALTA monolithic pixel detector

E. J. Schioppa

CMOS in the ATLAS Itk?

- 3 m² of pixel sensors (total Itk $10^2$)
- Ultimate low mass tracker
- Fast response
- Cost reduction:
  - Industrial CMOS process
  - No bump bonding

Radiation requirements:
- TID 80 Mrad
- NIEL $1.5 \times 10^{15}$ MeV neq/cm²
The TowerJazz 180 nm CMOS technology

- Small collection electrode (few um²)
- Small input capacitance
- High S/N for a **depletion depth of ~20um**
- To ensure full lateral depletion, **uniform n-implant** in the epi layer (modified process)*
- Successfully implemented for the ALICE ITS (modified process not sufficient for MALTA and Monopix)

* see https://doi.org/10.1016/j.nima.2017.07.046
The TowerJazz MALTA chip

- 22 x 20 mm² full size demonstrator
- 8 sectors with different pixel flavors
- Fully clock-less matrix architecture → low power
- Charge information from timewalk

- Pixel size 36.4 x 36.4 μm²
- 2-3 um collection electrode → small input capacitance
- 3.4 – 4 um separation between electrode and electronics → low cross talk
- 1 uW/pixel analog power (75 mW/cm²)
- 10 mW/cm² digital power @ layer4
MALTA architecture

- Groups of 2x8 pixels with pattern assignment to reduce data size from clusters
- Front-end discriminator output is processed by a double-column digital logic
- Pulse width adjustable between 0.5 ns and 2 ns
- Data are transmitted asynchronously over high speed bus to the end of column
- At the periphery, an arbitration and merging logic resolves timing conflicts of simultaneous signals
- Timing information is kept by dedicated bits
- Each hit is represented by a 40 bit word
- Output signals transmitted by 5Gbps LVDS drivers

I. Berdalovic et al 2018 JINST 13 C01023

E.J. Schioppa - VCI2019
Readout: asynchronous oversampling

- Implemented on a Xilinx Virtex707 evaluation board
- Signal speed is 1 GHz (pulse width ~1ns)
- Typical strategy is to sample with transceivers: recover clock from data and sample data
- But evaluation board does not have enough (40) transceivers to the FMC
- Alternative is to **oversample the signal** with 2 ISERDES shifted 45º and 2 clock phases shifted 90º (see Xilinx application note XAPP523)
MALTA first production: Jan. 2018

Very first image of a Fe$^{55}$ source

MALTA (asynchronous)

Monopix (synchronous)

raw, uncorrected
Timing properties

From analog measurements
(\(^{90}\)Sr source)

In-time threshold
130 mV = 300 e\(^-\)

Out of time hits (charge sharing) 5.3%

From digital measurements
(test beam)

98% in-time efficiency
@ 300 e\(^-\) threshold
(uncorrected for 7.5 ns propagation delay)
Threshold gain

- Fe-55 spectra from the analog pixels
- Threshold gain estimated from the distance between the K-alpha and K-beta peaks

<table>
<thead>
<tr>
<th>SUB (V)</th>
<th>gain ± 0.002 (mV/e)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-6</td>
<td>0.1464</td>
</tr>
<tr>
<td>-12</td>
<td>0.1480</td>
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<tr>
<td>-15</td>
<td>0.1371</td>
</tr>
<tr>
<td>-18</td>
<td>0.1364</td>
</tr>
</tbody>
</table>
Threshold dispersion

- Threshold dispersion $\sim x2$ larger than design
- Conclusion $\rightarrow$ **adjustment bits in next submissions**
Test beam campaign

- March and April → **ELSA, 3.2 GeV/c electrons**
- From April to October (ongoing) → **CERN SPS, 180 GeV/c pions**

- **CERN FEI4 telescope**, resolution ~8 um
- **MIMOSA telescope** (Kartel, Ljubljana), resolution <2 um
- Up to 2 DUTs can be tested simultaneously
- Irradiated samples are kept cold by a Si-oil system

- Chips we tested:
  - Unirradiated first production
  - Unirradiated MLVLC
  - Neutron irradiated $5 \times 10^{14} \text{n}_{eq}/\text{cm}^2$ first production
  - Neutron irradiated $5 \times 10^{14} \text{n}_{eq}/\text{cm}^2$ MLVLC
  - Neutron irradiated $1 \times 10^{15} \text{n}_{eq}/\text{cm}^2$ first production
  - X-ray irradiated 80 Mrad MLVLC (ongoing)

- Results shown here are on **SPS MIMOSA data**
- Reconstruction done with Proteus: [https://gitlab.cern.ch/unige-fei4tel/proteus](https://gitlab.cern.ch/unige-fei4tel/proteus)
In-pixel efficiency

Unirradiated
(MLVLC W6R6, S4)

Irradiated
$5 \times 10^{14} \text{n}_{\text{eq}} / \text{cm}^2$
(MLVLC W6R21, S4)

Could not reach lower threshold

Decreasing threshold, from $\sim 600 \text{ e}^-$ to $\sim 250 \text{(unirr)}/350 \text{(irr)} \text{ e}^-$
Effect of pwell extension

Difference between medium pwell and maximum pwell becomes visible on irradiated chips at high threshold

Sector 3
*Med deep pwell*

Sector 4
*Max deep pwell*
Improved pixel design

Modified process:

- **3D TCAD transient simulation** from M. Munker
- Constant potential at pixel border produces a field minimum (★)
- Additional implant and gap in n-layer provides a potential difference in the lateral direction
MiniMALTA

- Improved process design
- Matrix of 64x16 pixels
- 8 sector splits for analog FE design, reset mechanism and process
- Synchronization at the end of column
- Also, new version of MALTA available, with improved Slow Control
First results on MiniMALTA

miniMALTA Fe55 Spectrum

χ² / ndf 2.061 / 27
Constant 365.1 ± 110.8
Mean 1.069 ± 0.003
Sigma 0.008497 ± 0.002219

VDAC

IDAC
First results on MiniMALTA (ctd)

Threshold distribution, IDB 100

Noise distribution, IDB 100

Threshold distribution, IDB 20

Noise distribution, IDB 20
MALTA telescope

- 6+ MALTA planes
- 2 trigger schemes:
  - 2 scintillators
  - Coincidence on N MALTA planes
- Achieved 4um resolution on DUT at CERN SPS
- High portability
Outlook 2019

Chips
- MiniMALTA on desk
- New MALTA on desk
- New submission ~summer

Irradiation campaigns
- Neutrons at the Ljubljana TRIGA reactor
- Protons in Birmingham
- X-rays at CERN and Glasgow

Test beam campaigns
- 6 GeV electrons @ DESY, Hamburg
- 3 GeV electrons @ ELSA, Bonn
- Investigating ion and proton tests for SEE measurements
Conclusion

- MALTA is a full demonstrator monolithic CMOS sensor produced in 180nm TowerJazz technology
- First production came back in Jan 2018
- Tests performed on unirradiated and neutron irradiated chips ($5 \times 10^{14} \text{n}_{\text{eq}}/\text{cm}^2$ and $1 \times 10^{15} \text{n}_{\text{eq}}/\text{cm}^2$)
- Analog performance close to design expectations (will add threshold adjustment bits in next iteration)
- Test beam studies have shown efficiency loss at the corners after irradiation
- TCAD simulation have demonstrated the origin of such loss → new chips with improved process
- 2019 test campaign dedicated to
  - Validate the new process
  - Test synchronization logic
- First tests on MiniMALTA show promising results
- Ion tests for SEE studies are foreseen
Backup
MALTA MLVLC production, Jun. 2018

- **MLVLC = Metal Last Vias Last Change**
- Improve connections to **digital power in the slow control block**
- Improve **PWELL connections** in the matrix
- Modified top metal and top via

*Example:*
Cluster size

Unirradiated
(MLVLC W6R6, S4)

Irradiated
$5 \times 10^{14}$ \( n_{eq} \)/cm\(^2\)
(MLVLC W6R21, S4)

Decreasing threshold, from $\sim 600$ e\(^-\) to $\sim 250$ (unirr)/350 (irr) e\(^-\)

Couldn’t reach lower threshold
Substrate bias sweep on first production unirradiated (W4R7)