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EDET DH80k – Characterization of a DePFET based sensors for TEM Direct Electron Imaging

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Motivation and Introduction

DePFET Structure and Measurement Setup

Optimization of Operation Parameters and Response Function

Summary and Outlook

Motivation
for the project

Stroboscopic imaging provides insights to the dynamics of processes:

- short, discrete illumination periods with high intensity
- decouples exposure time, image contrast and motion blur
- pulse intensity defines the image contrast
- frequency of illumination defines time resolution
- pulse duration defines impact of motion blur

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Challenges of stroboscopic imaging in TEM world:

- real space imaging → high granularity
- high intensity → high dynamic range
- direct electron detection → thin substrate
- high pulse frequency → high framerate
- “grey scale” image → no data reduction possible

Introduction

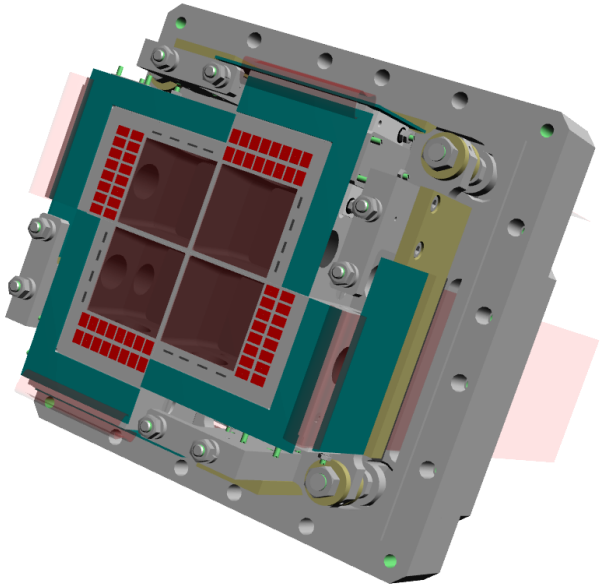
to the camera system and its challenges

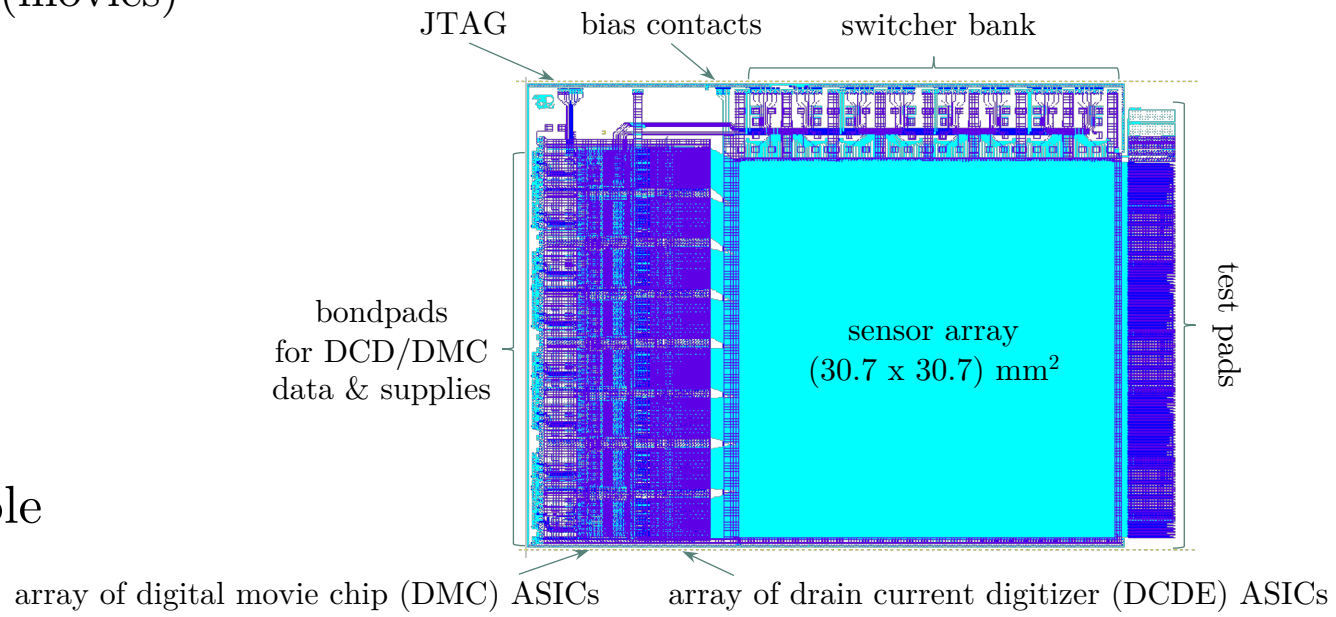
Camera system:

- focal plane area (FPA) consists of 4 individual and independent modules ("tiles"), each capable of stand-alone operation
- small sensitivity gap between tiles (1.2 mm)
- All Silicon Module (ASM)
- readout in rolling shutter mode, 100 ns/row, 4 rows in parallel
- maximum framerate of 80 kHz or 12.8 µs/frame
- front end electronics (FEE) buffers bursts (movies) with 100 frames
- maximum burst rate 100 Hz

Data rate:

- 8 bit digitization resolution:
  - tile module data rate of ~3 GB/s
  - total data rate of ~12 GB/s
- data reduction difficult if not impossible





Introduction

to the camera system and its challenges

Sensor array

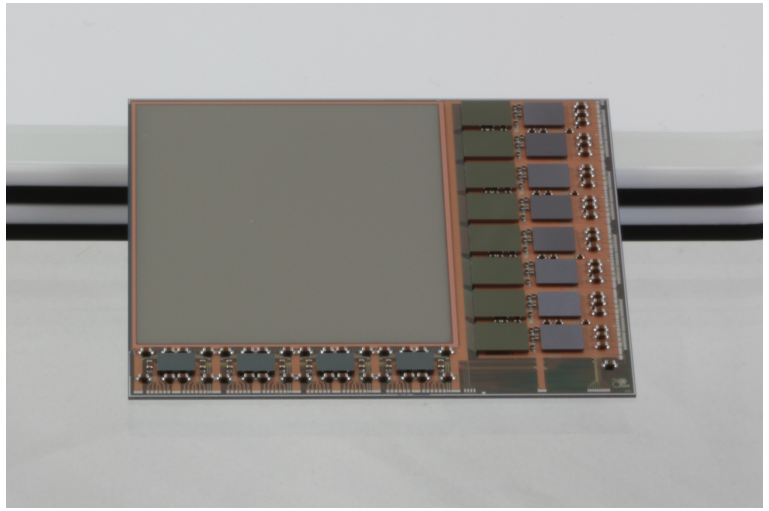
- 1 MPixel for the complete FPA
- 512 x 512 pixels per tile
- (60 x 60) μm^2 pixel size

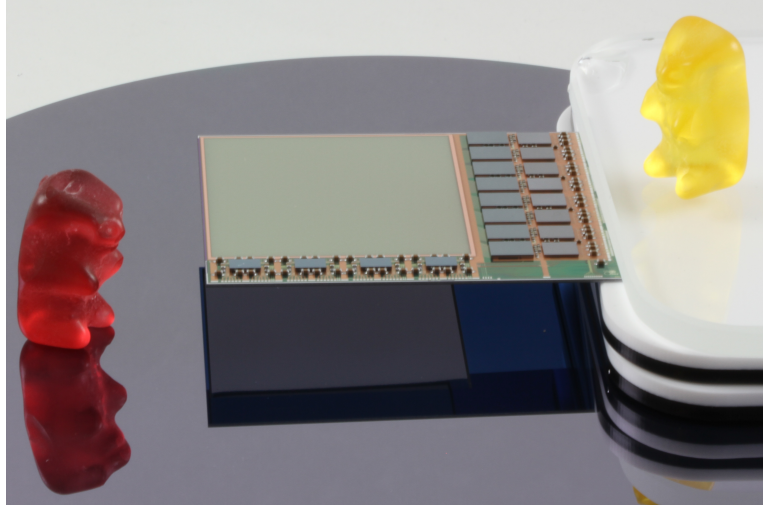
Dynamic range of pixels:

- single primary e^- sensitivity
- capable of storing the signal from 100 primary e^- at 300 keV (~800k signal e^-)

Spatial resolution improvements:

- reduce e^- multiple scattering
  - thin sensitive detector substrate (50 µm and 30 µm)
- reduce e^- back scattering
  - no support layer
  - highly effective beam dump





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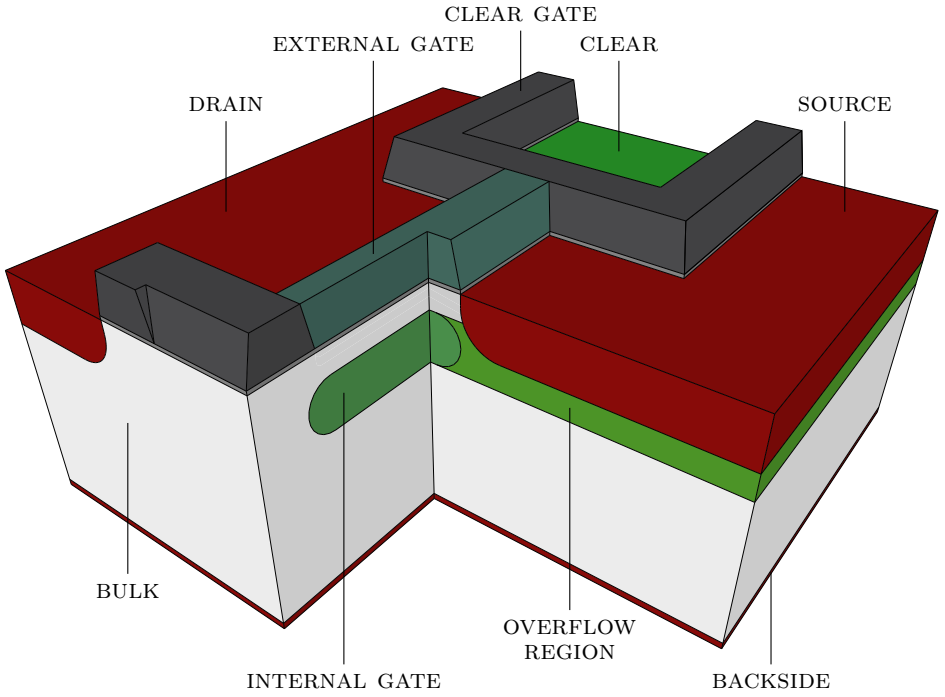
The DePFET structure

and its positive sides

Depleted p-channel Field Efect Transistor on high resistive n-doped bulk

- integrated 1st stage amplification (g_q)
- charge storage capability
  - readout on demand
  - rolling shutter mode
- small capacitance and low noise
- high quantum efficiency and fill factor
- fully depleted bulk
  - optionally thinned
- front- or back-side illumination possible
- easily scalable
- adjustable dynamic range
- signal compression
  - achieved by overflow charge storage regions with different g_q

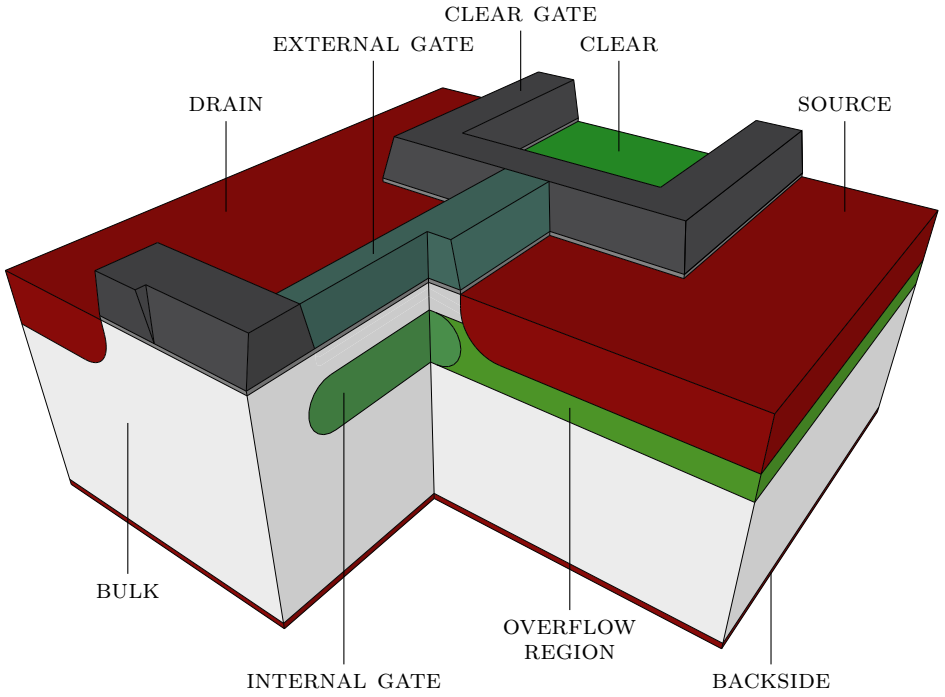


The DePFET structure

and its operation principle

Two states of operation:

- OFF state:
  - idle state, no power dissipation, but collecting signal charge
- ON state:
  - transistor current depending on signal charge in internal gate



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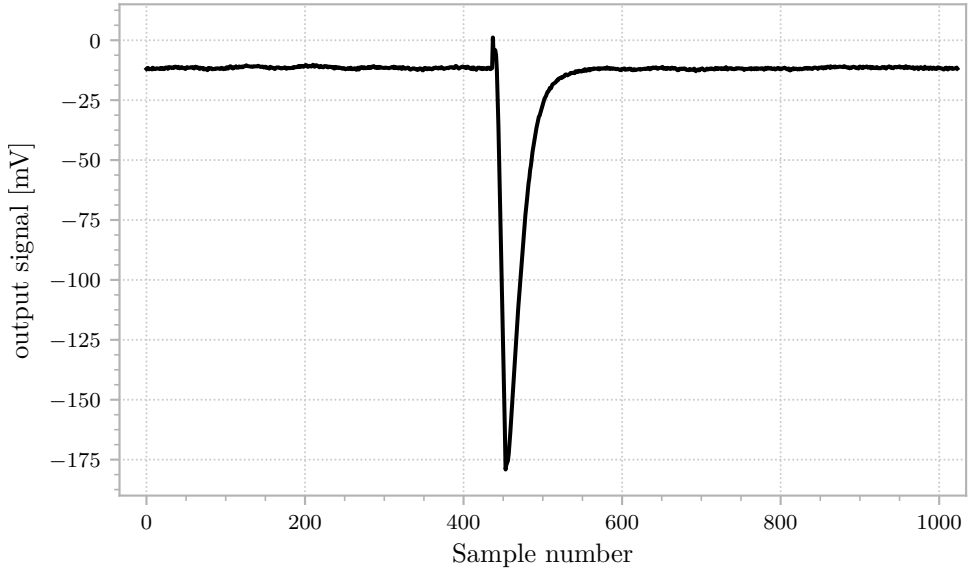

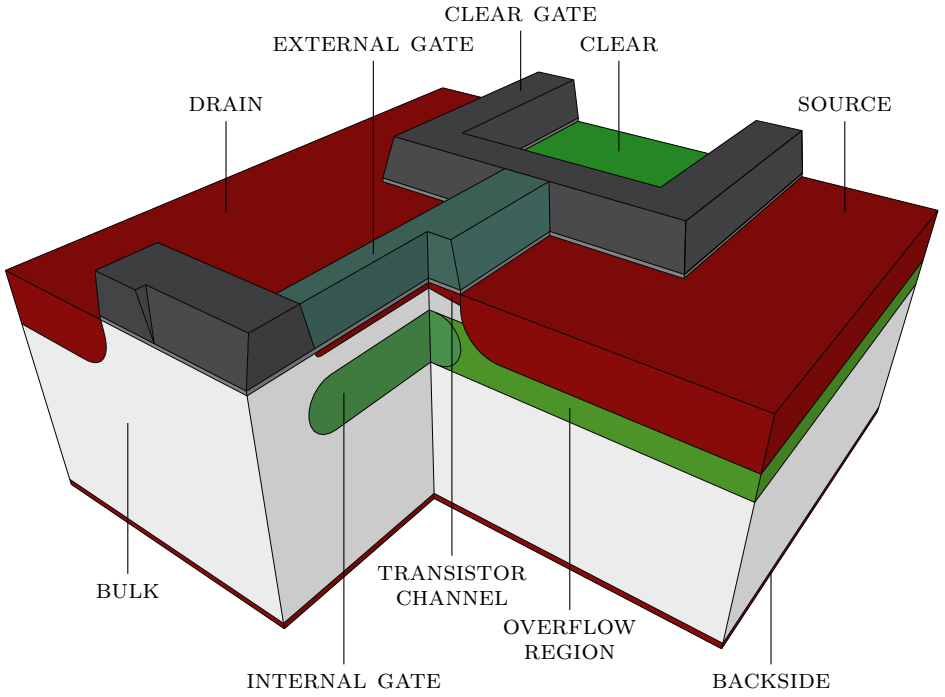

EMPTY ON STATE

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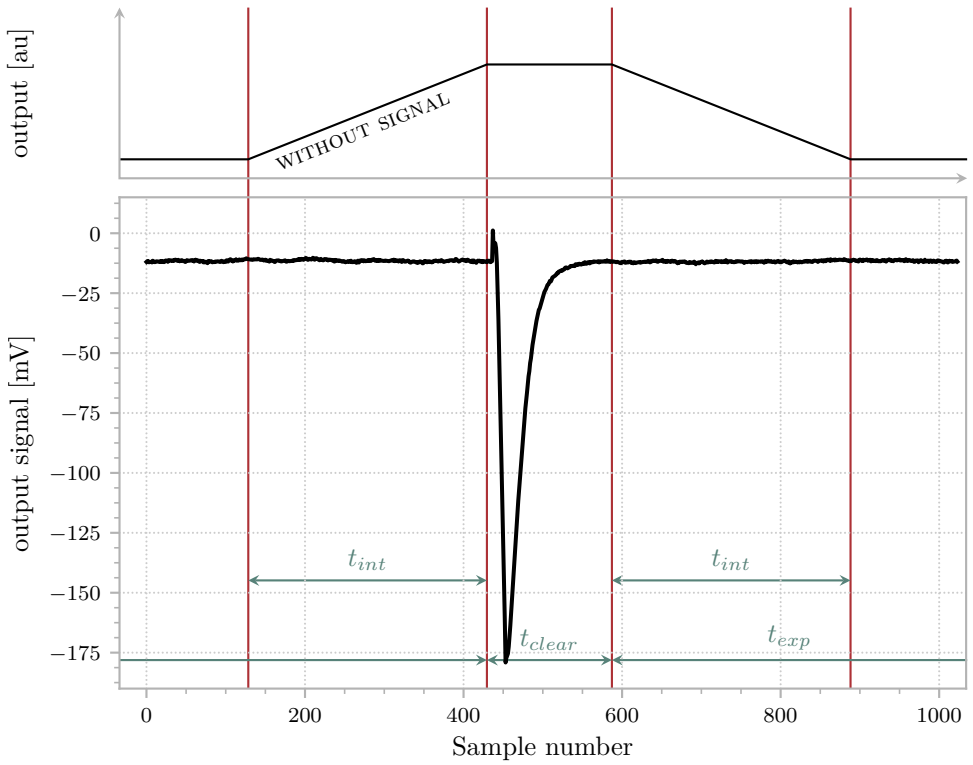

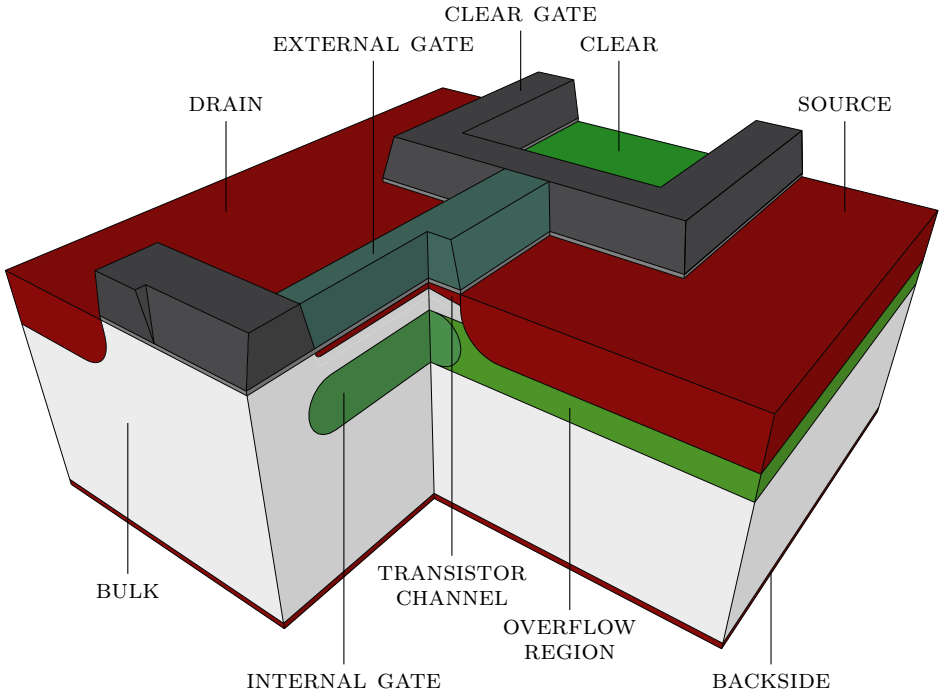

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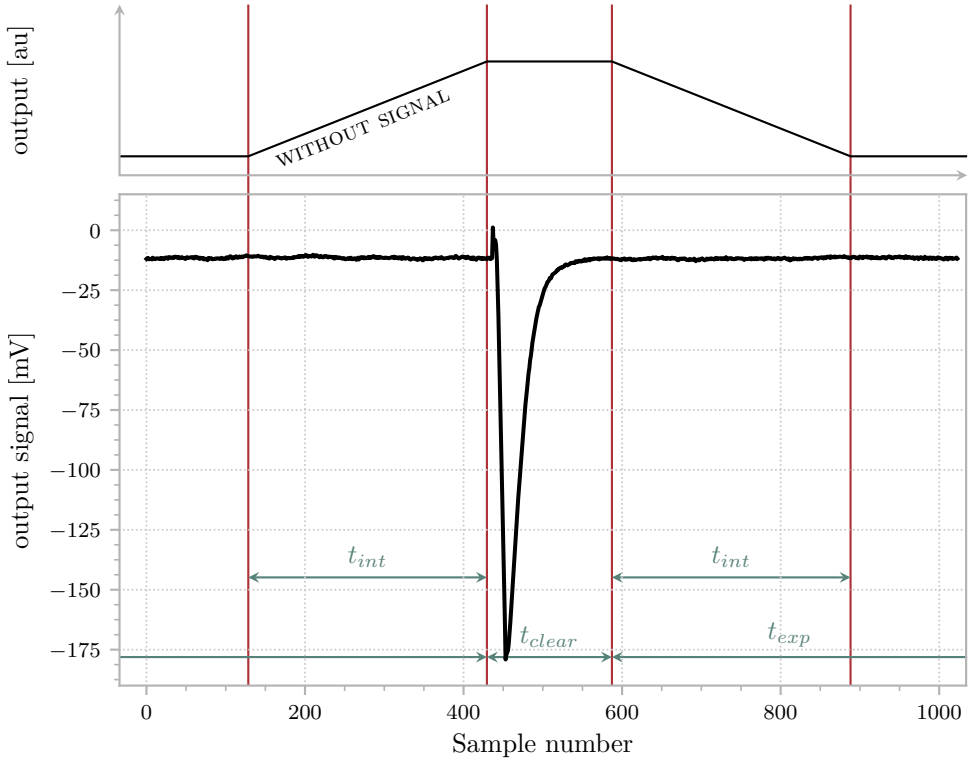

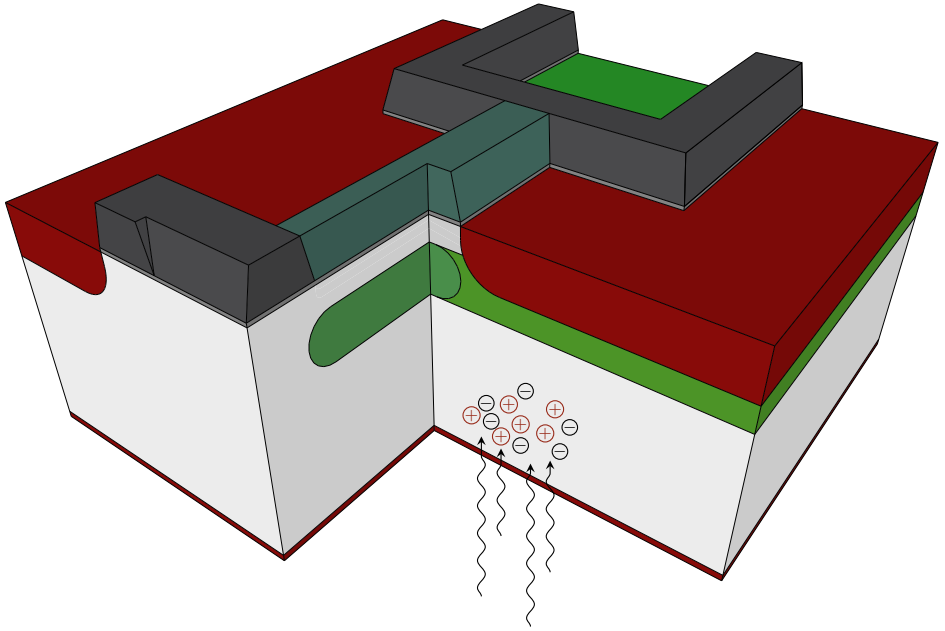

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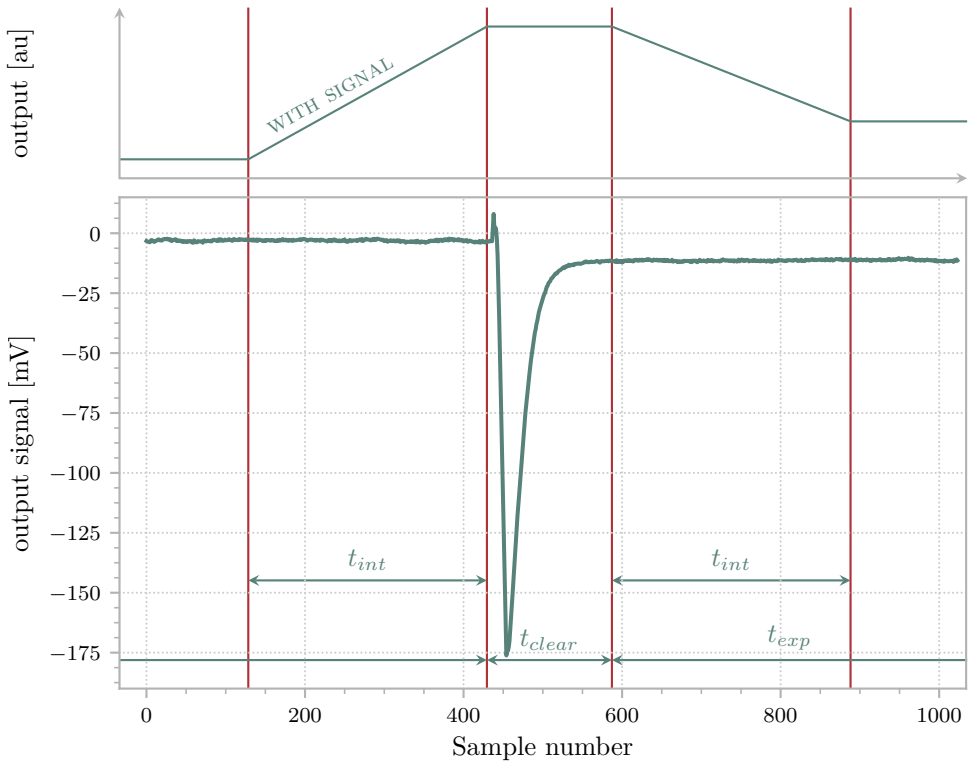
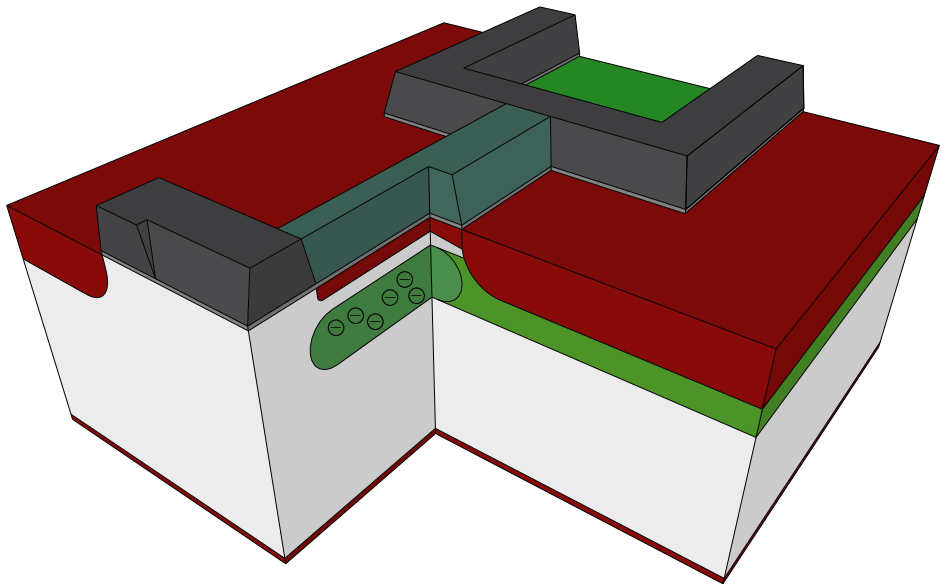


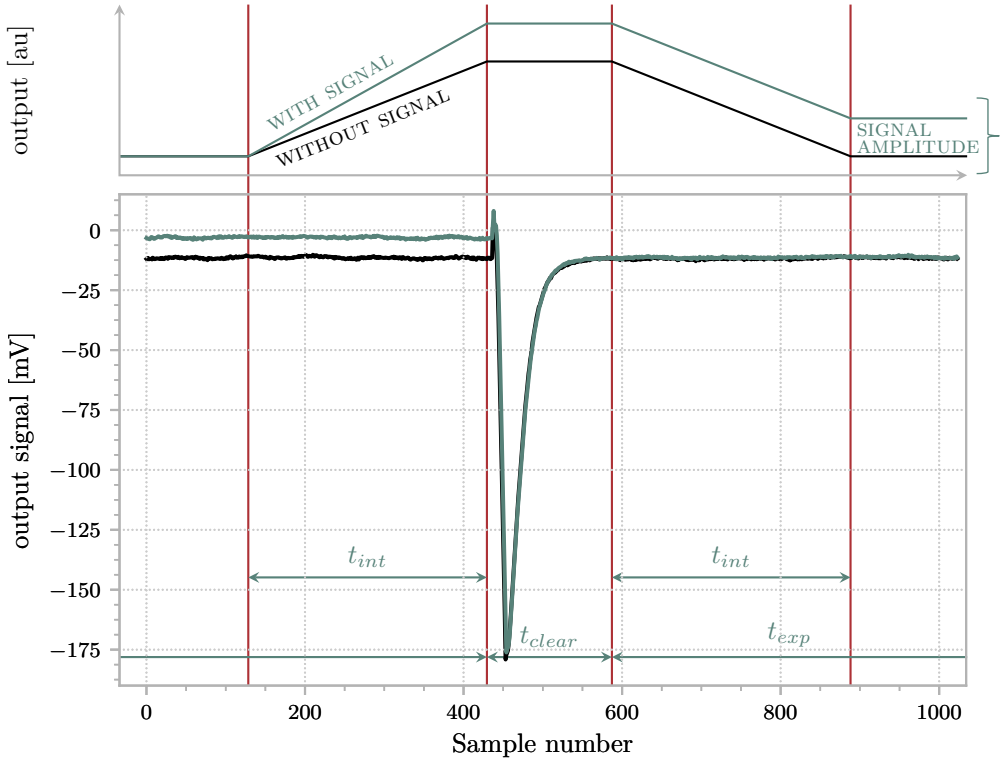


FILLED ON STATE

The DePFET structure

and its operation principle

INITIAL STATE VS. FILLED STATE

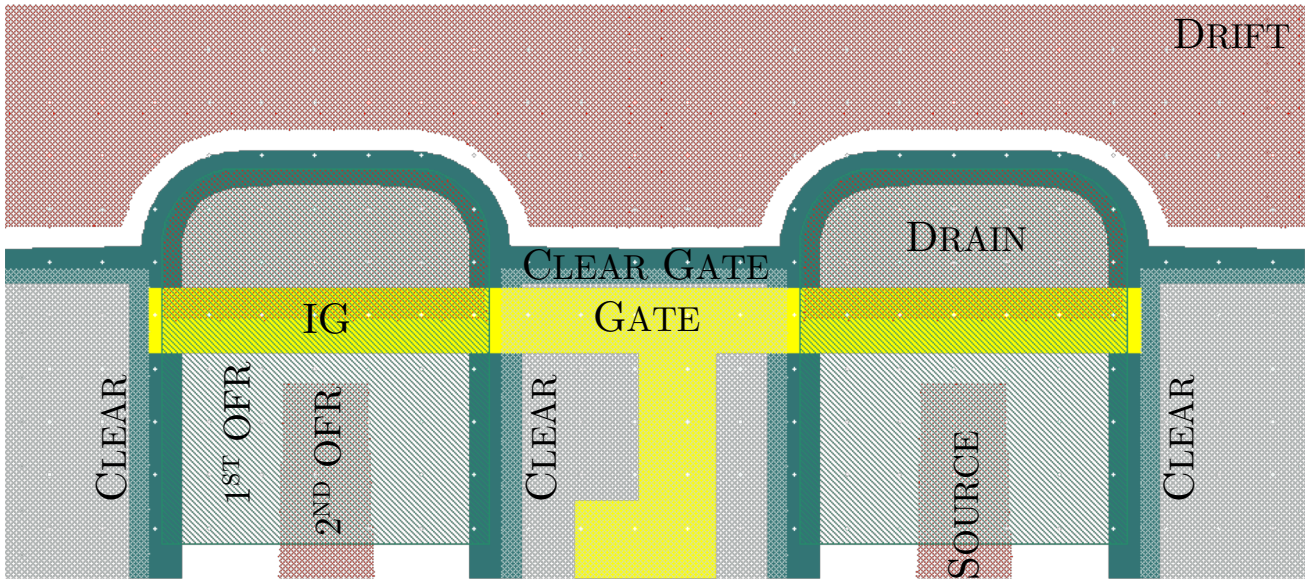


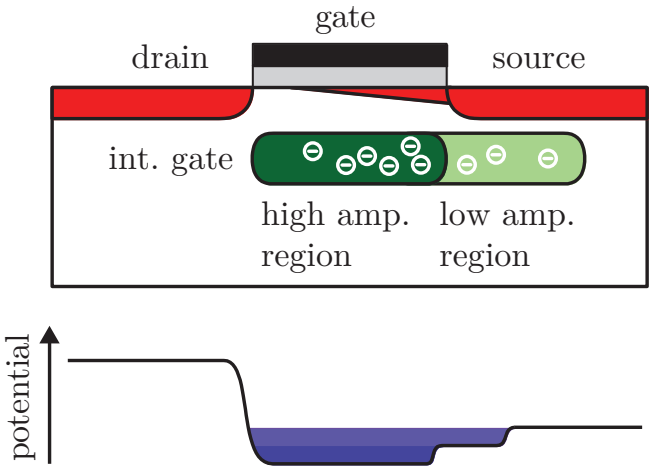
INITIAL DEPFET RESPONSE IS LINEAR

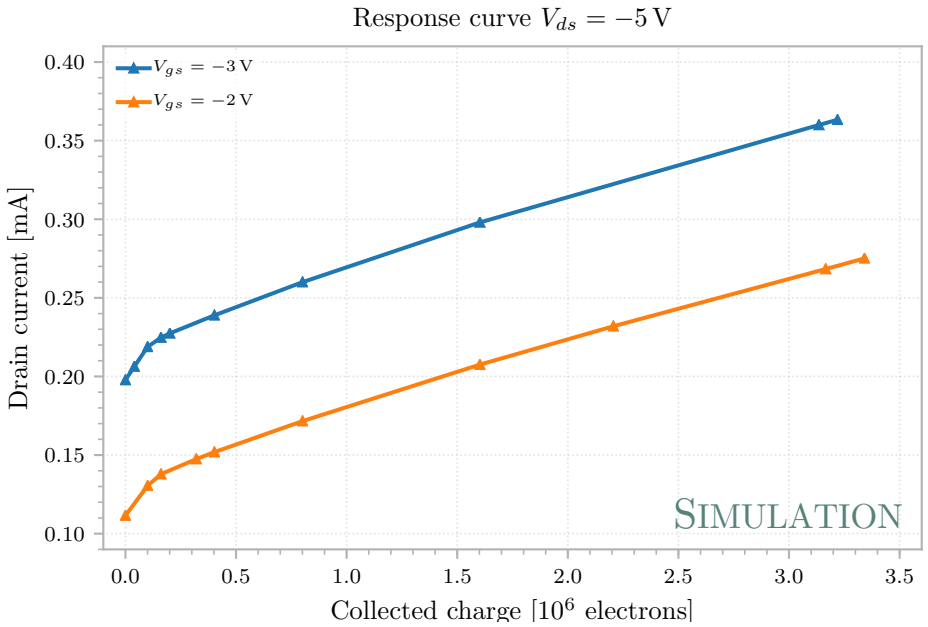
CALIBRATION WITH A KNOWN RADIOACTIVE SOURCE

The EDET DePFET structure

and its operation principle







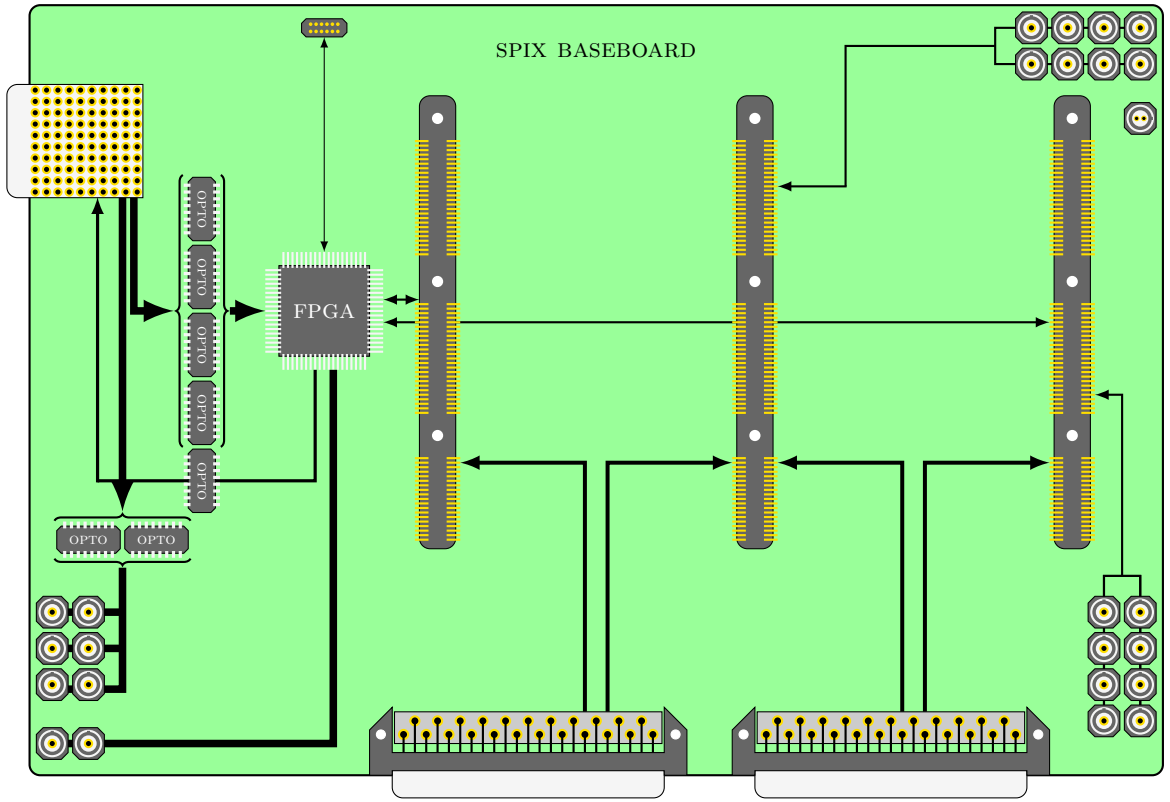
Internal Gate is under the Gate
1st OverFlow Region is around the Source
2nd OverFlow Region is under the Source

Measurement setup

operating principle

Design concept:

MODULARITY



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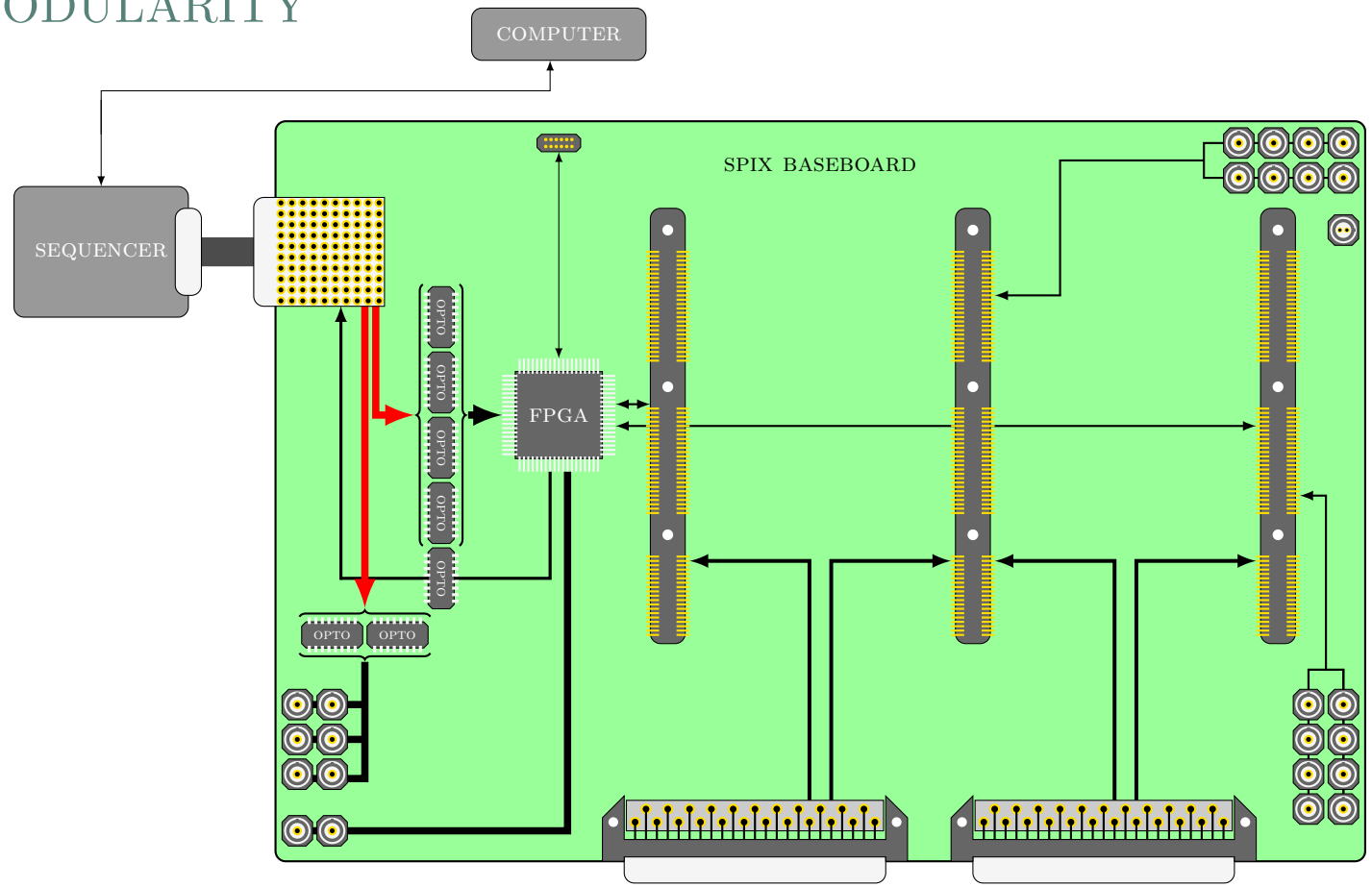

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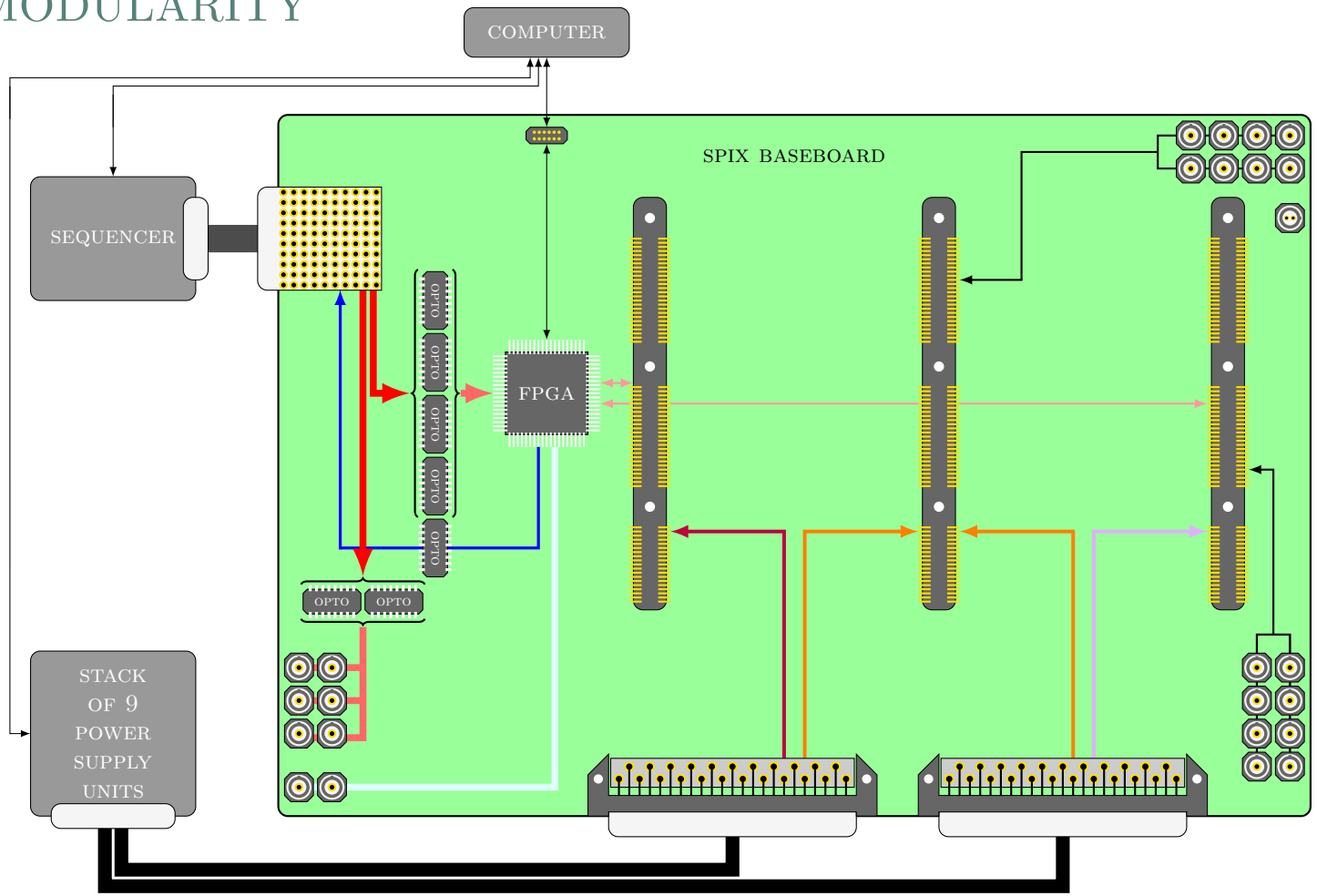

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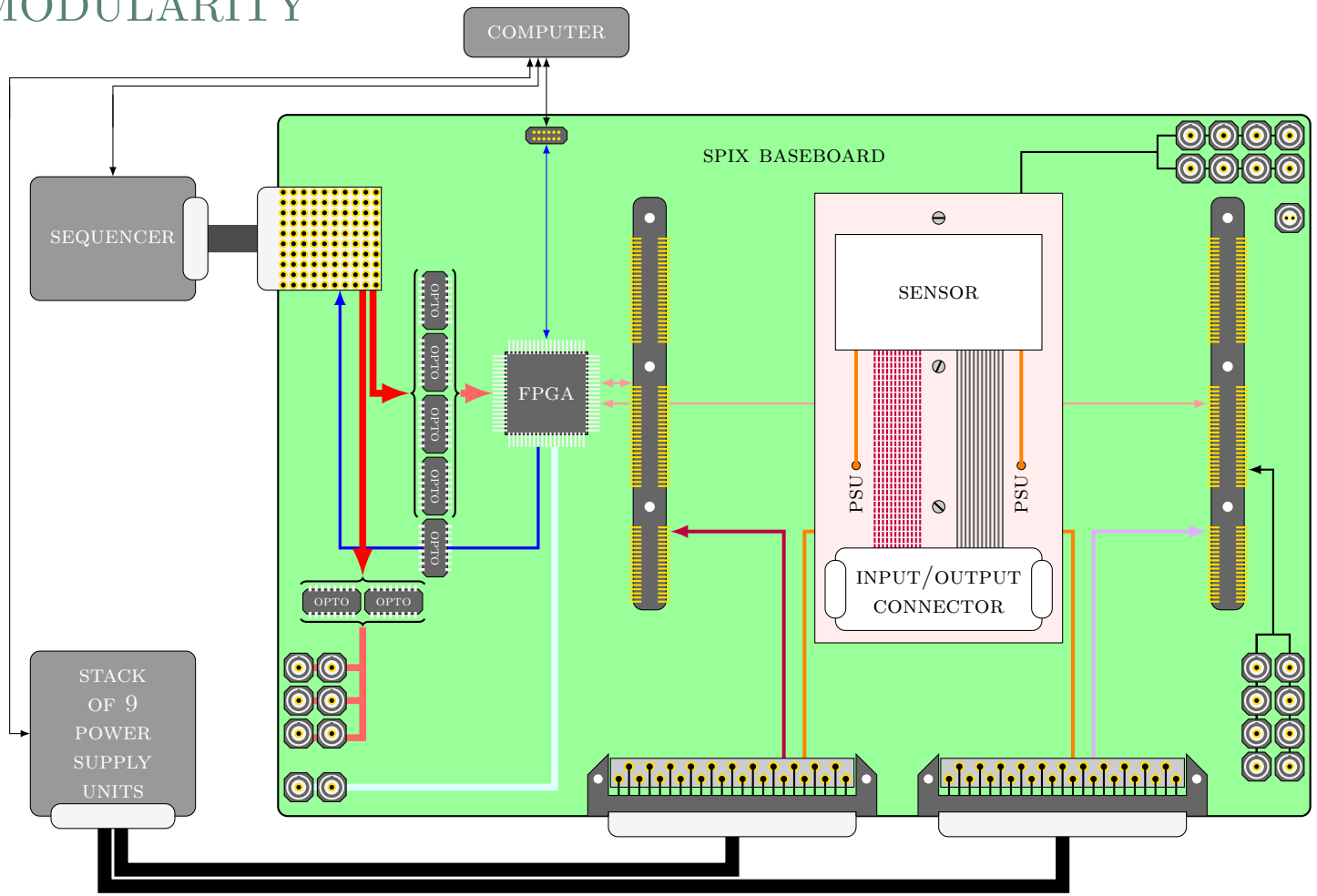

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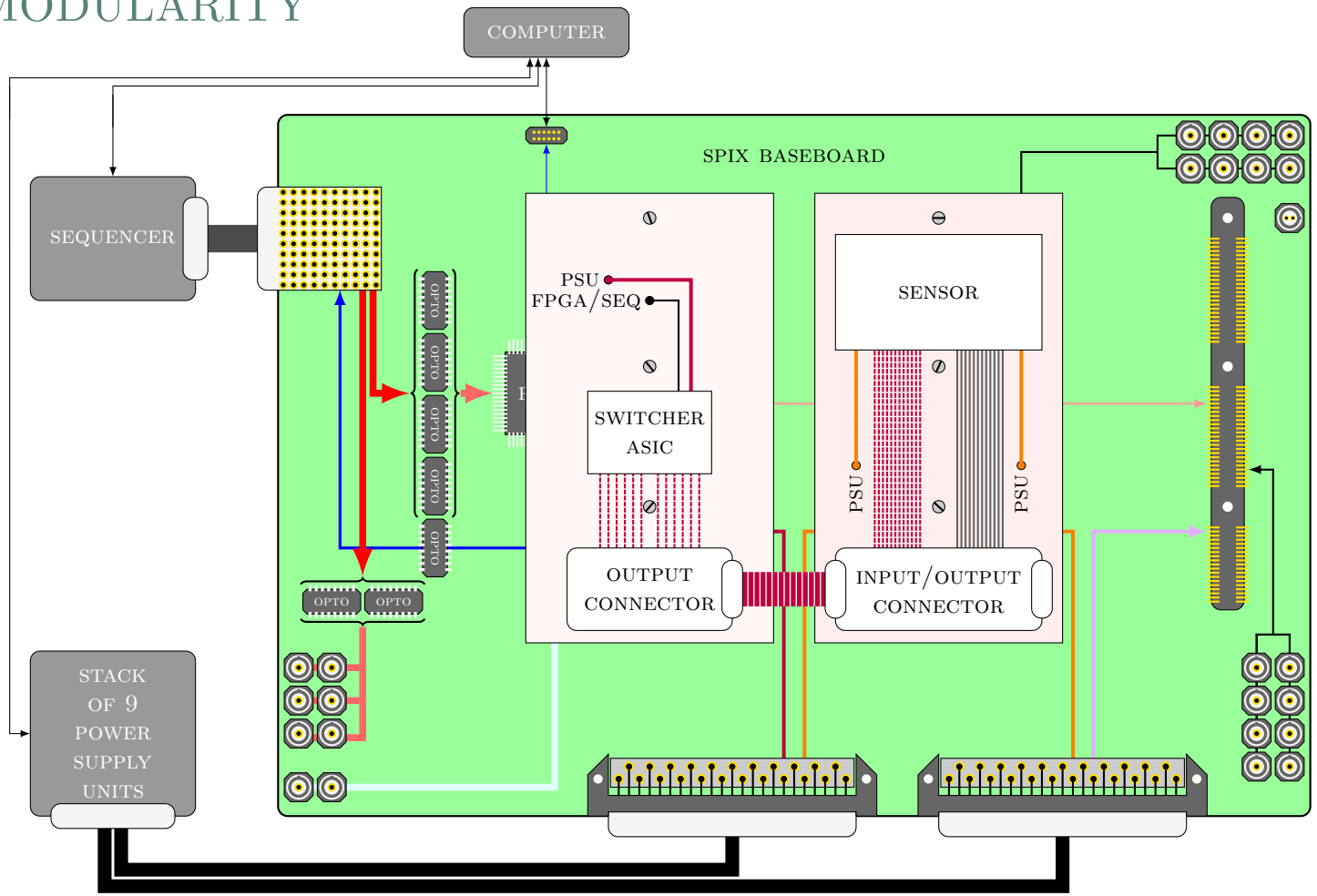

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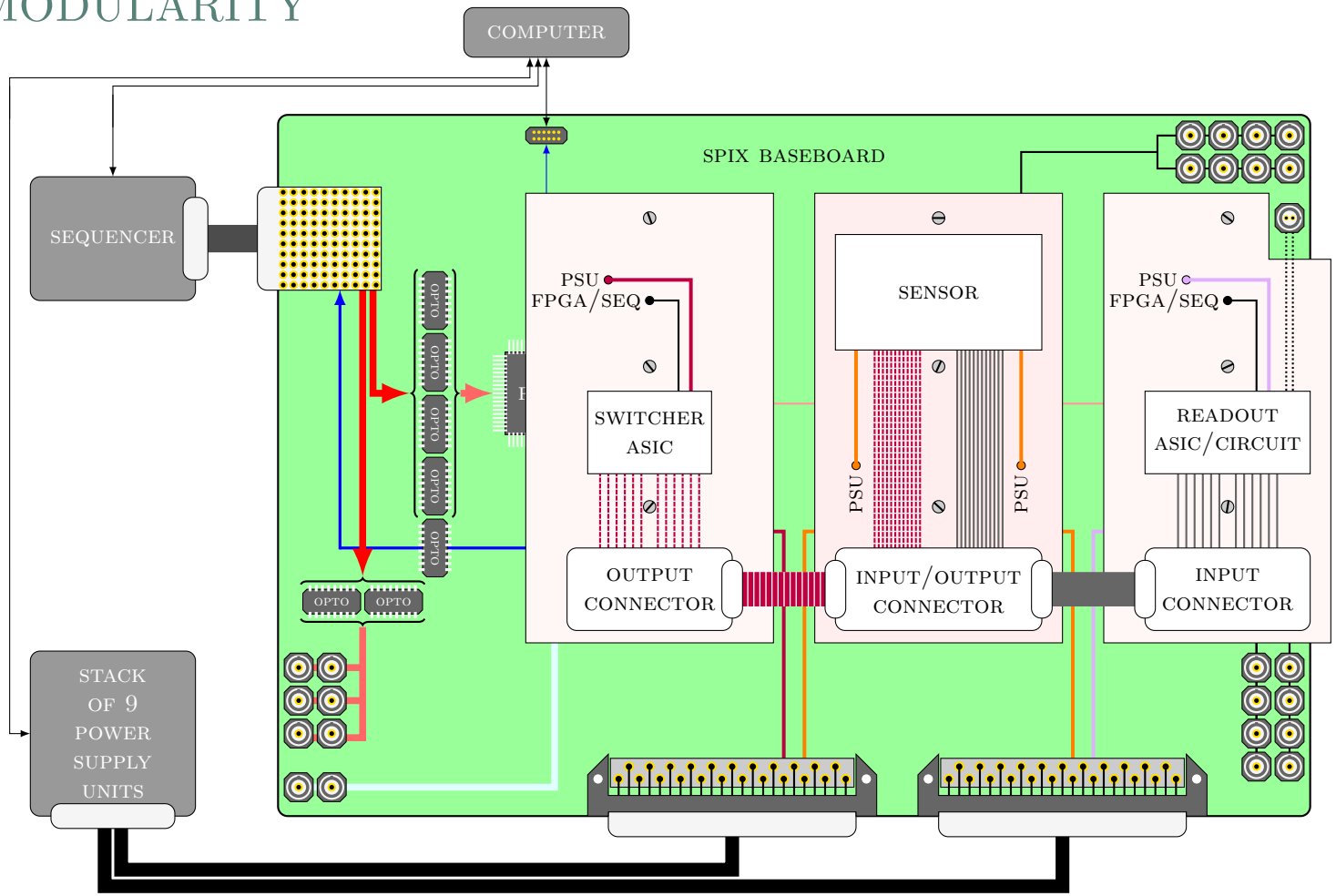

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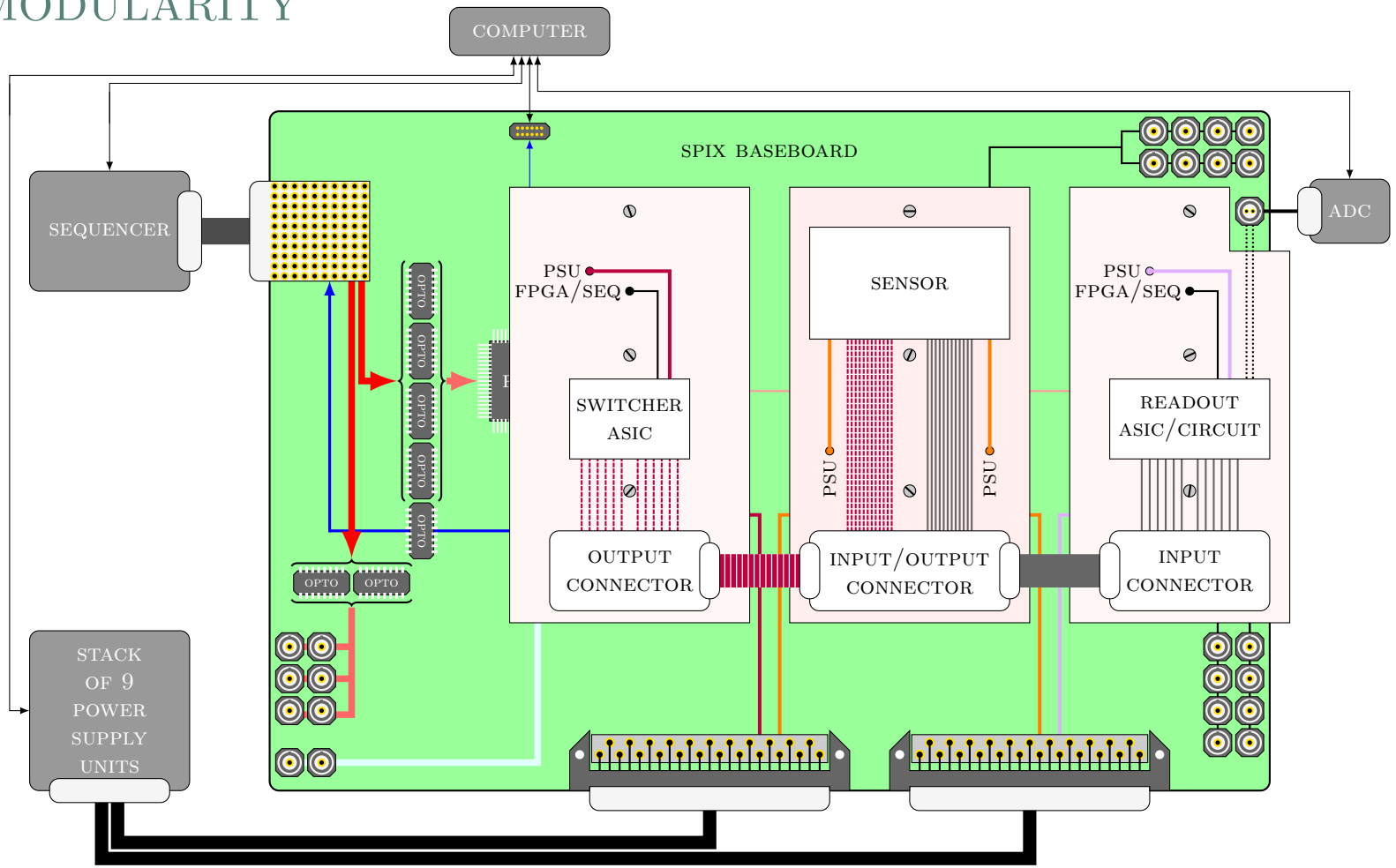

Single PIXle setup

actual setup

Design concept:

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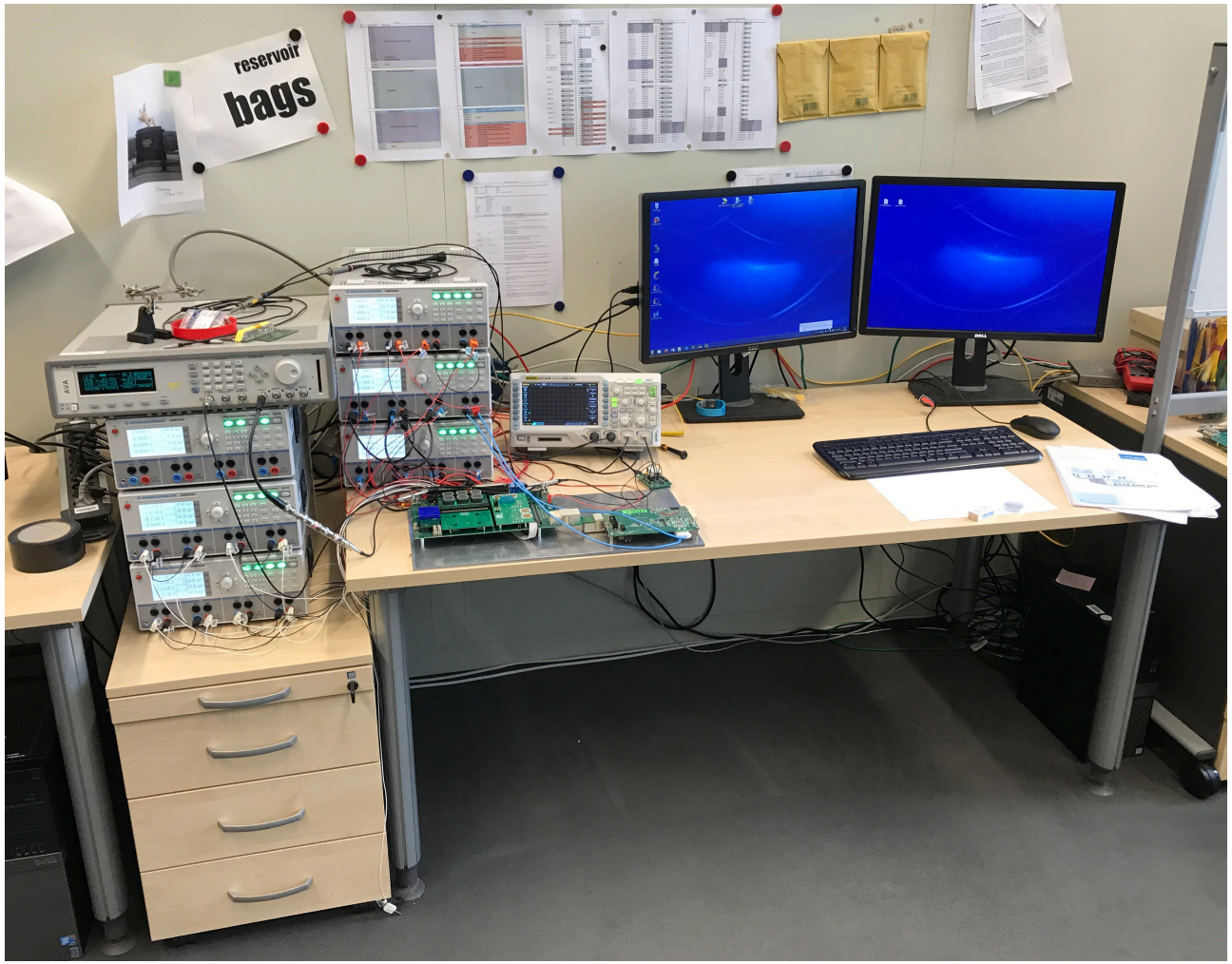

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on depleted 50 µm thick EDET structures

Clear Gate and Clear low voltage influence

- back-emission of e^- from clear contact,
- inversion (parasitic channel under the Clear Gate), and
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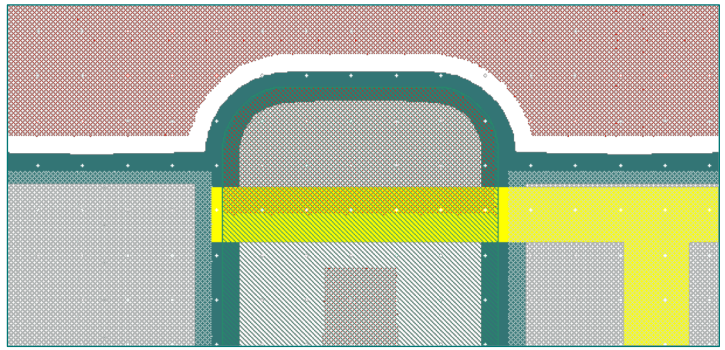

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Thickness	50 µm
Gate L	5.0 µm
Gate W	27.2 µm
Drain	-5.0 V
Source	0.0 V
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Clear low	sweep
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Depletion	-35.0 V
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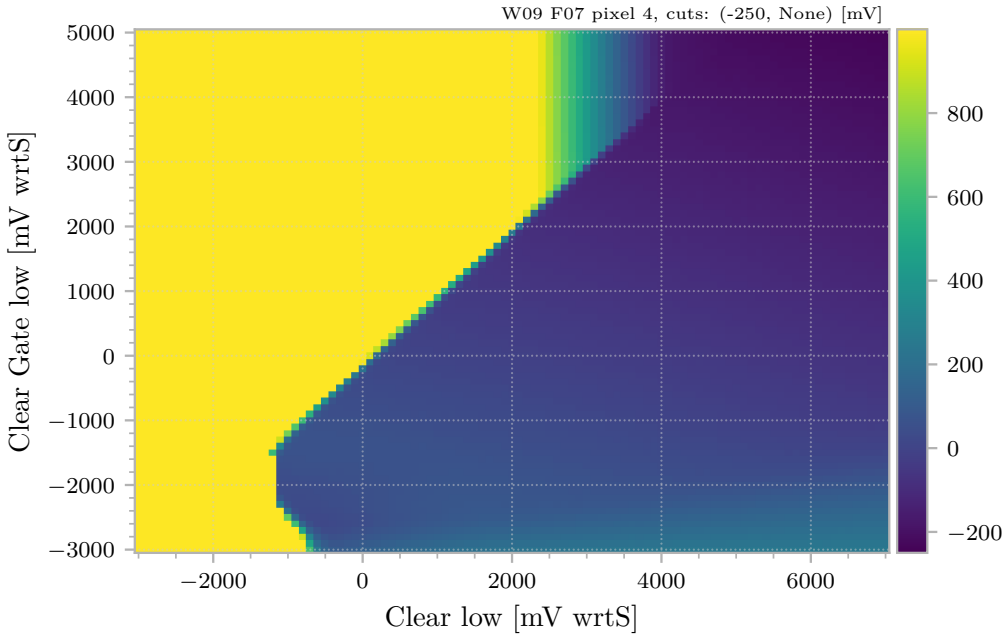
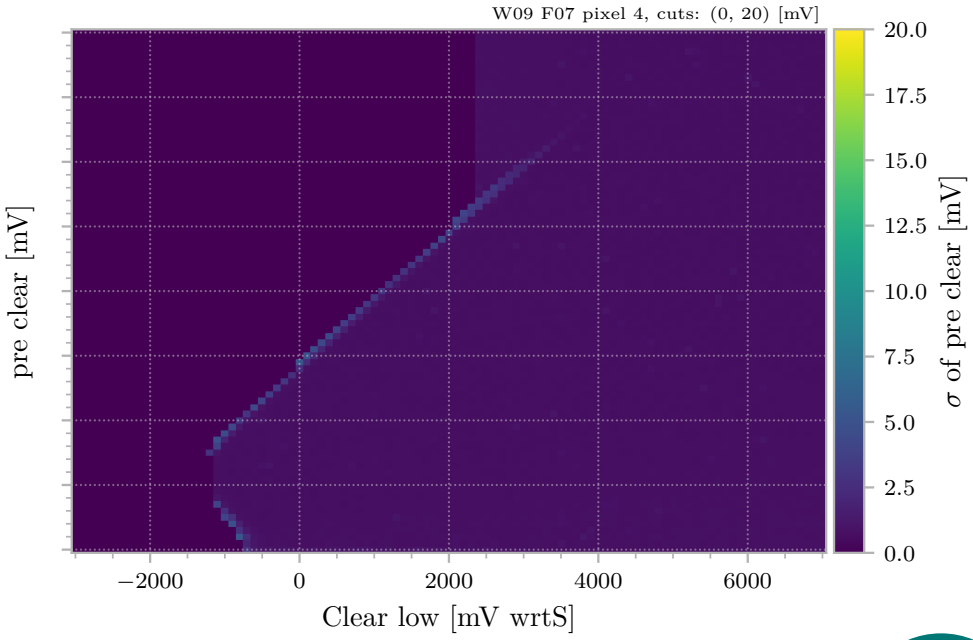
No external illumination; Observing only the initial state





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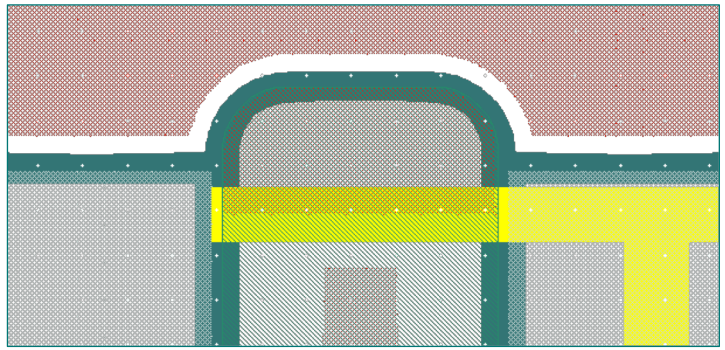

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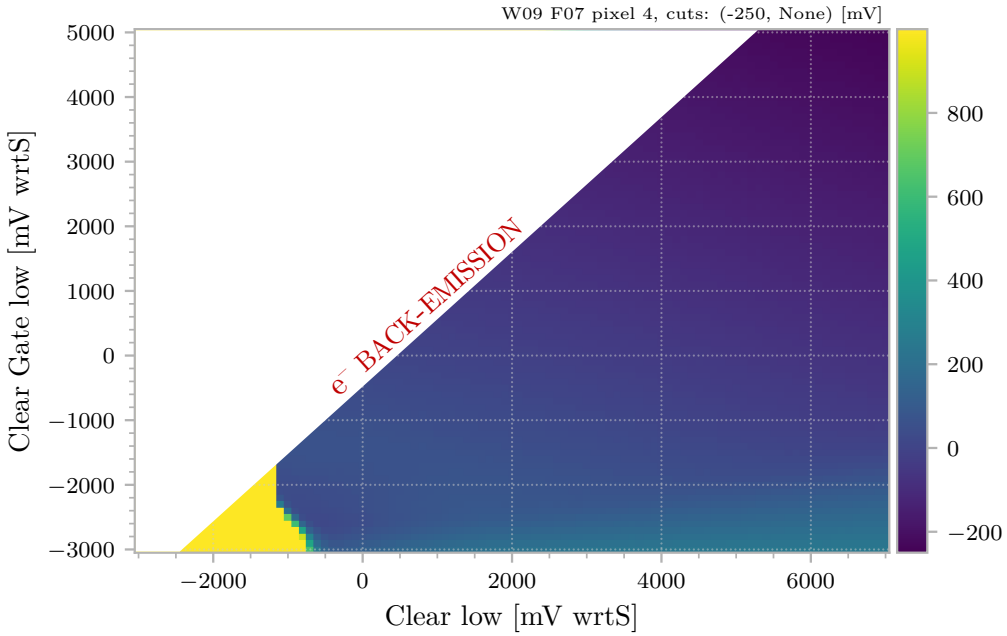

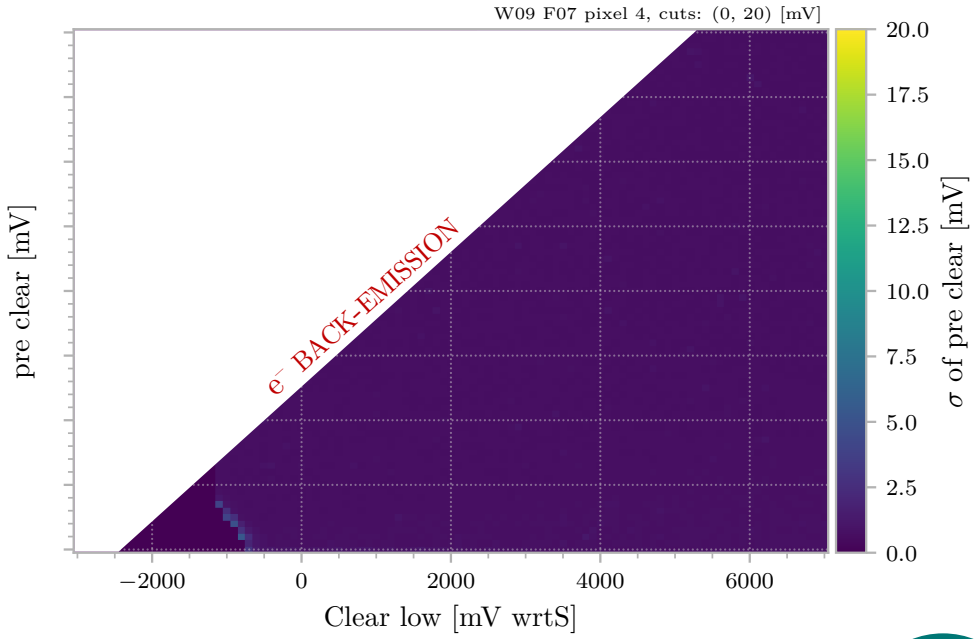

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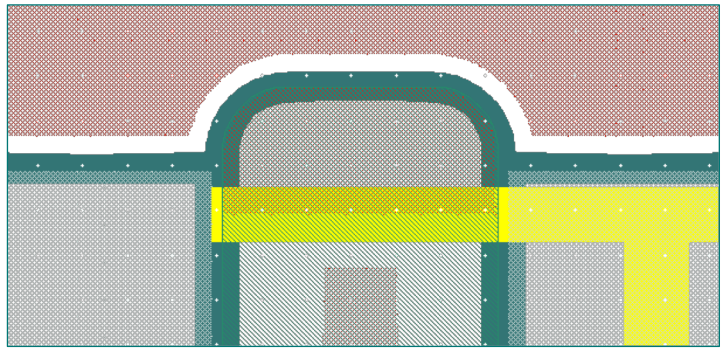

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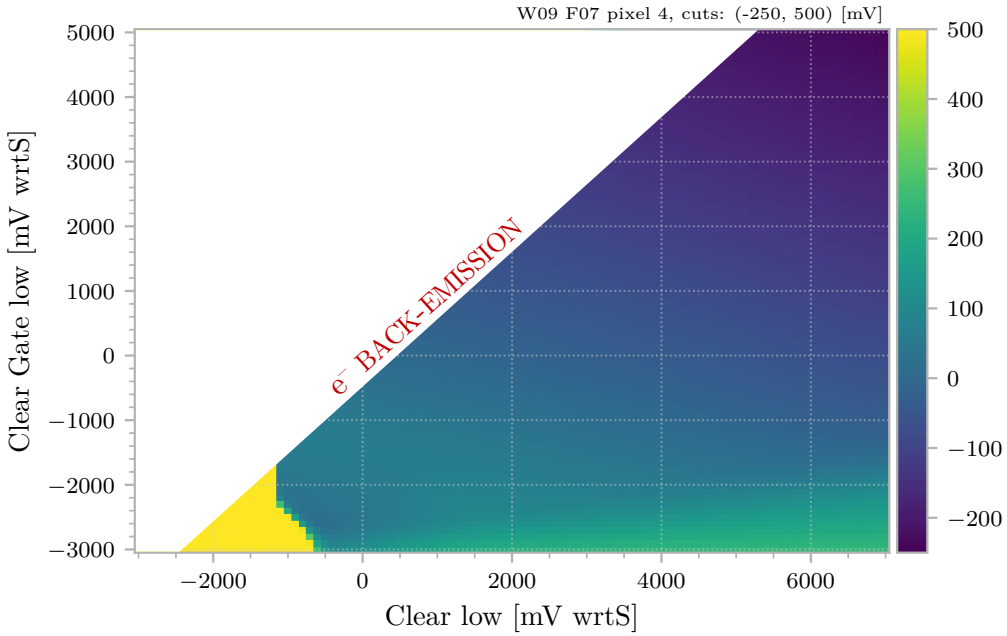

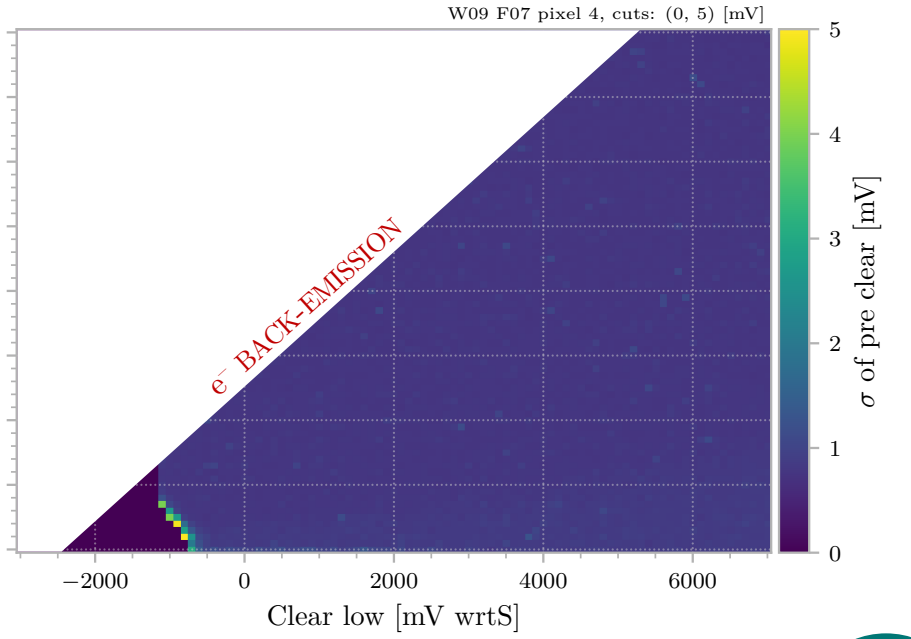

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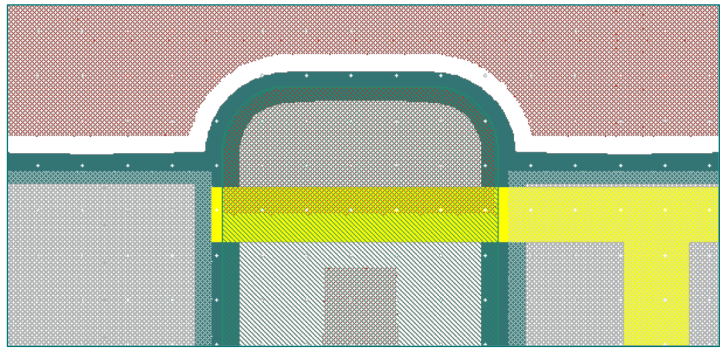

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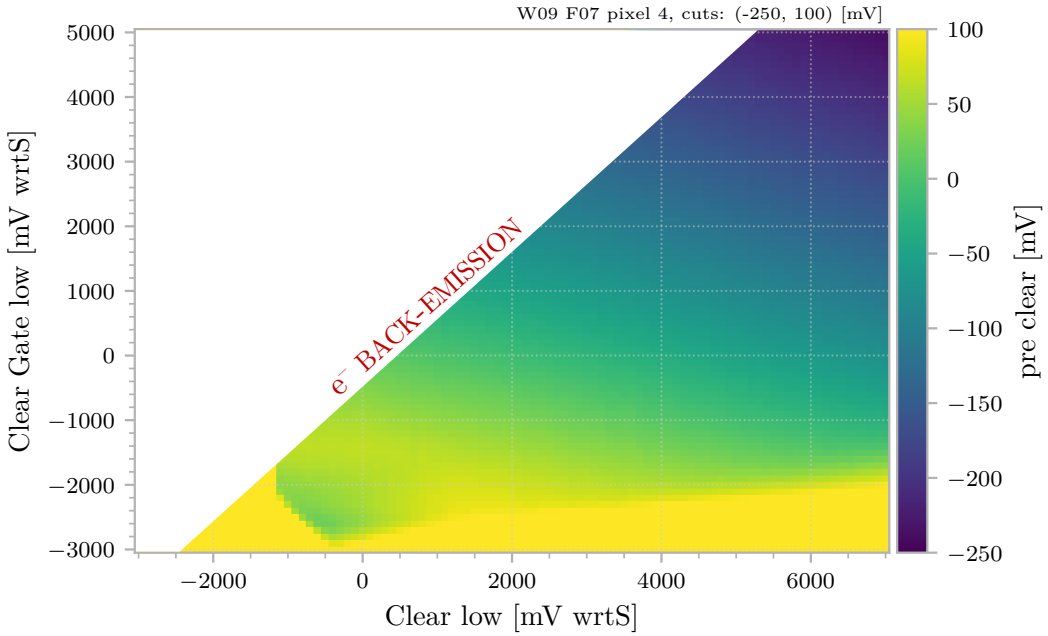

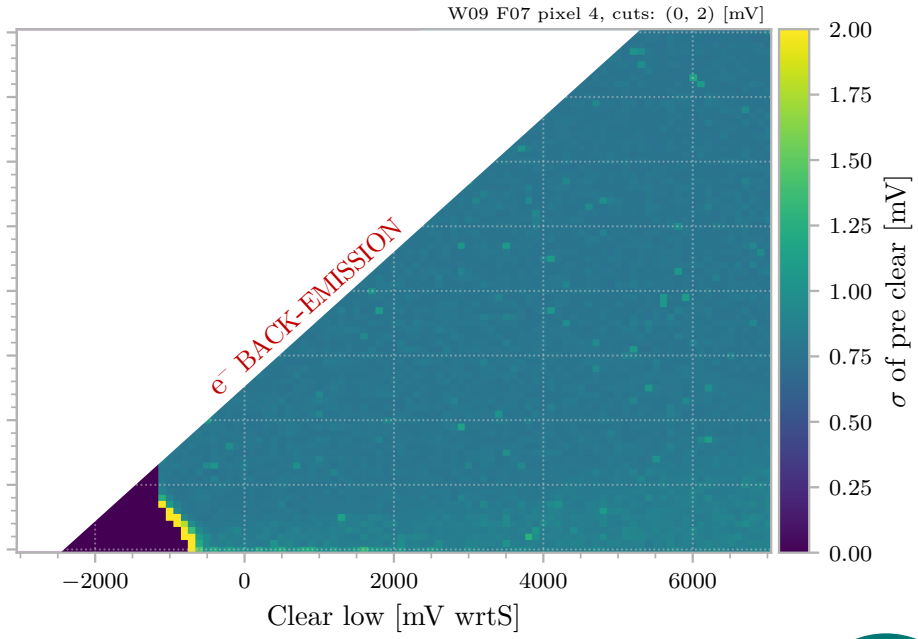

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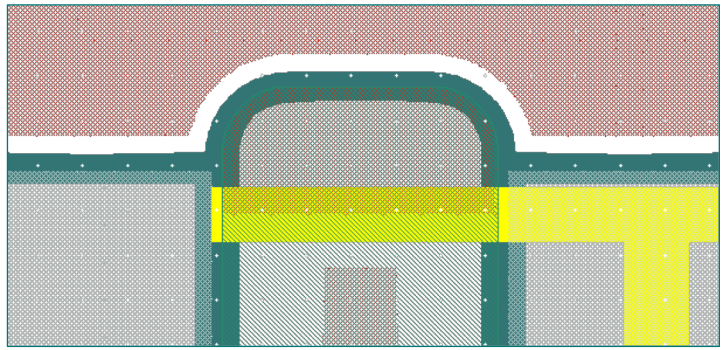

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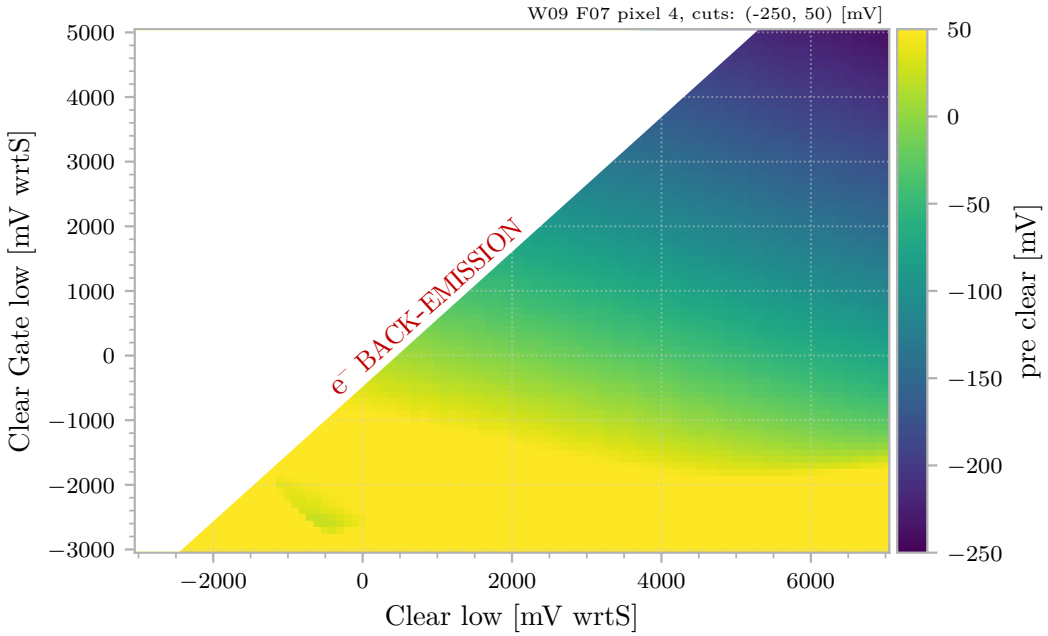

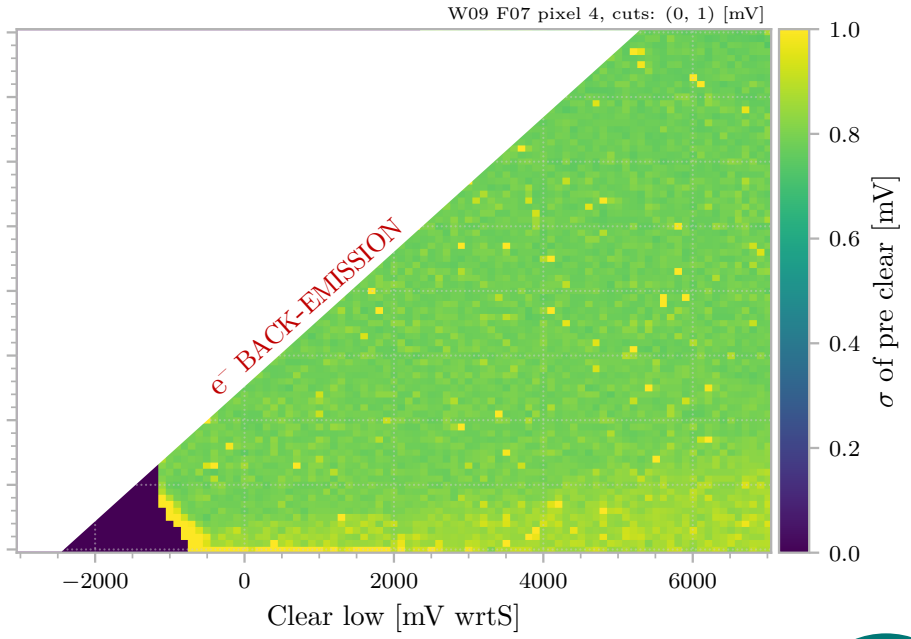

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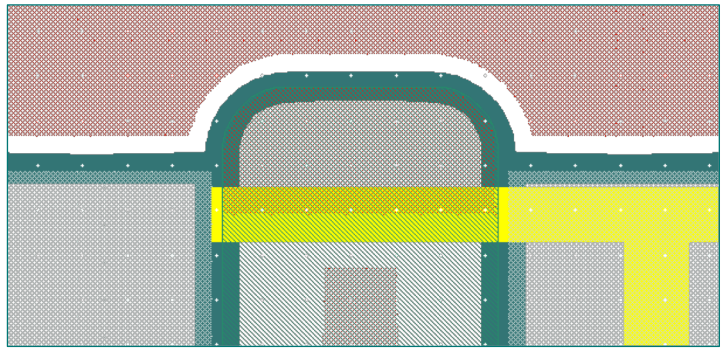

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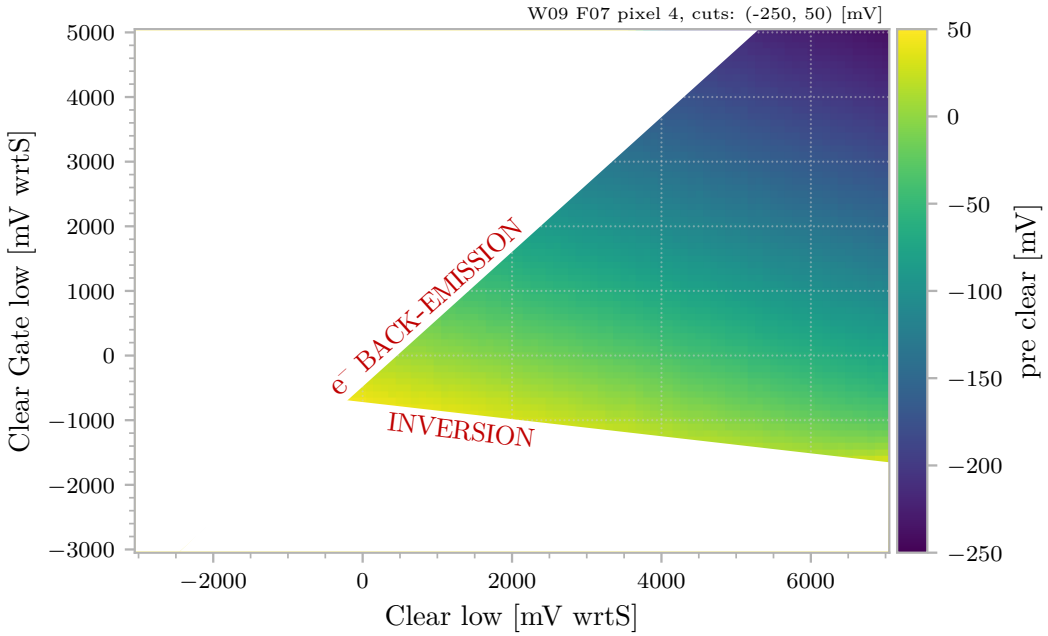
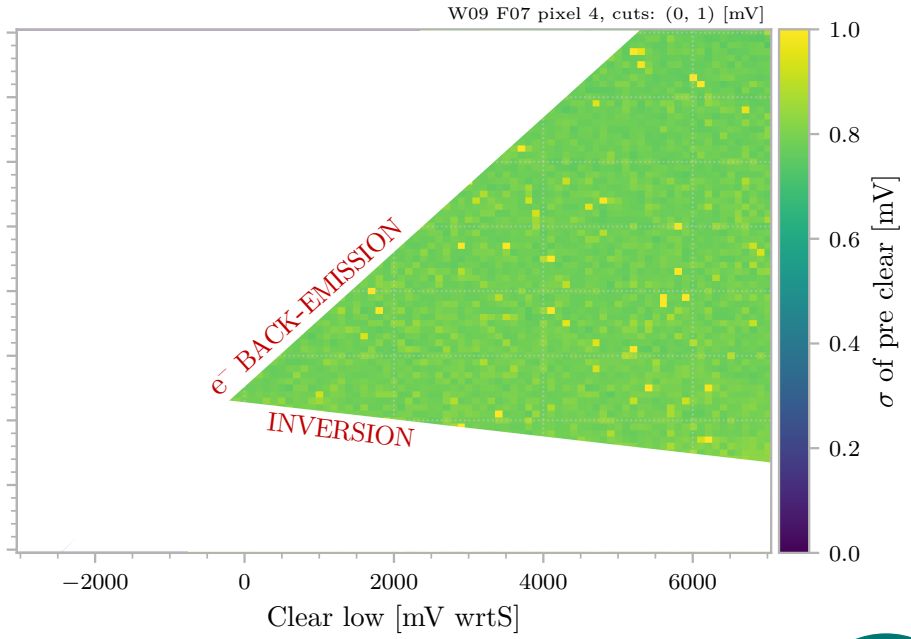




Measurements – operation window

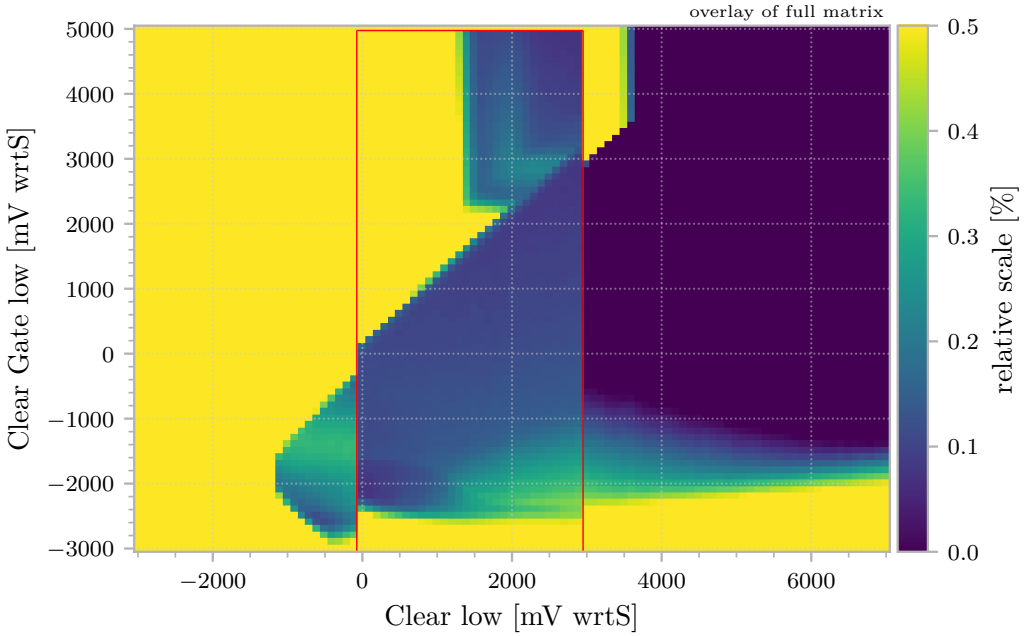
on depleted 50 µm thick EDET structures

Clear Gate and Clear low voltage influence

- back-emission of e^- from clear contact,
- inversion (parasitic channel under the Clear Gate), and
- charge loss to clear contact.

W09 F07	
Thickness	50 µm
Gate L	5.0 µm
Gate W	27.2 µm
Drain	-5.0 V
Source	0.0 V
Gate Off	5.0 V
Gate On	-2.17 V
Clear low	sweep
Clear high	17.0 V
Clear Gate	sweep
Depletion	-35.0 V
Bulk	10.0 V
Drift	-5.0 V
Guard	-5.0 V

NO EXTERNAL ILLUMINATION; OBSERVING ONLY THE INITIAL STATE



OVERLAY (RED BOX) OF AN IDENTICAL MEASUREMENT DONE WITH THE SMALLER VERSION OF THE FINAL CAMERA SETUP.

Measurements – operation window

on depleted 50 µm thick EDET structures

Clear Gate and Clear low voltage influence

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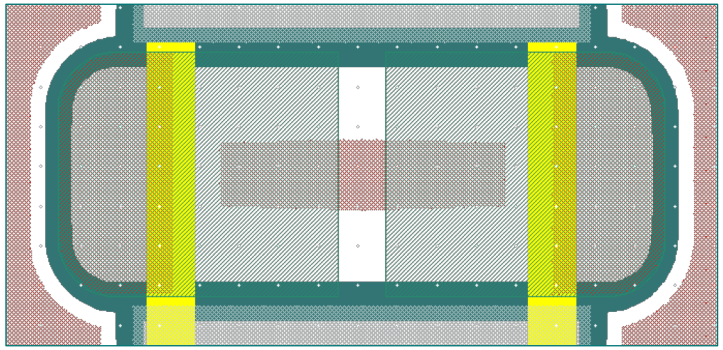
- inversion (parasitic channel under the Clear Gate), and
- charge loss to clear contact.



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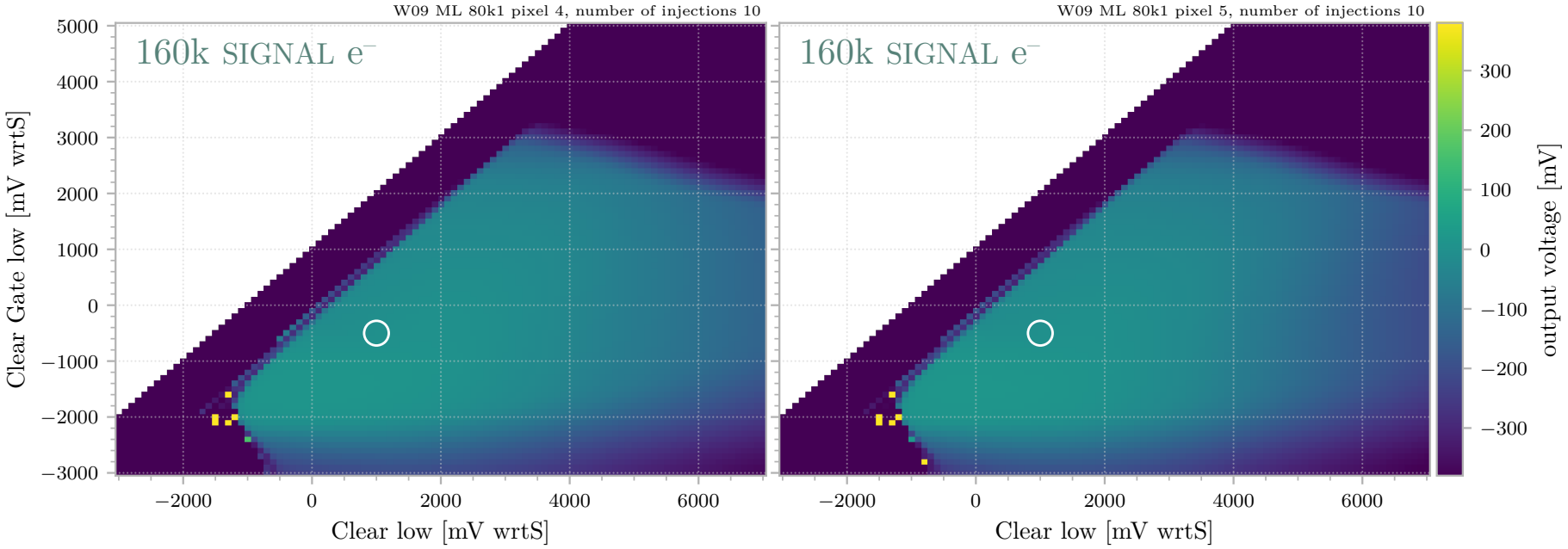
Clear low	sweep
Clear high	17.0 V
Clear Gate	sweep
Depletion	-35.0 V
Bulk	10.0 V
Drift	-5.0 V
Guard	-5.0 V

LED FLATFIELD ILLUMINATION (FFIL); 1 INJECTION CORRESPONDS TO ~10X ^{55}Fe K_α



Measurements – operation window

on depleted 50 µm thick EDET structures

Clear Gate and Clear low voltage influence

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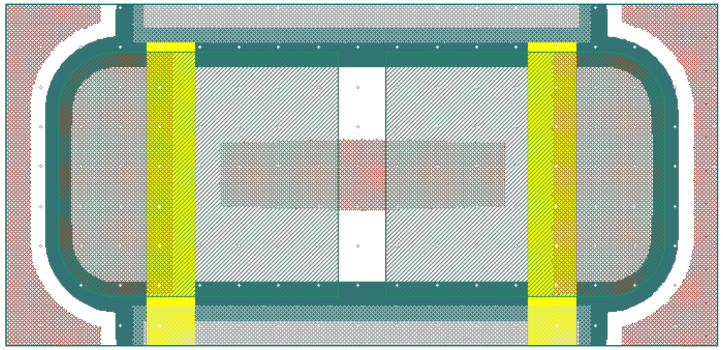

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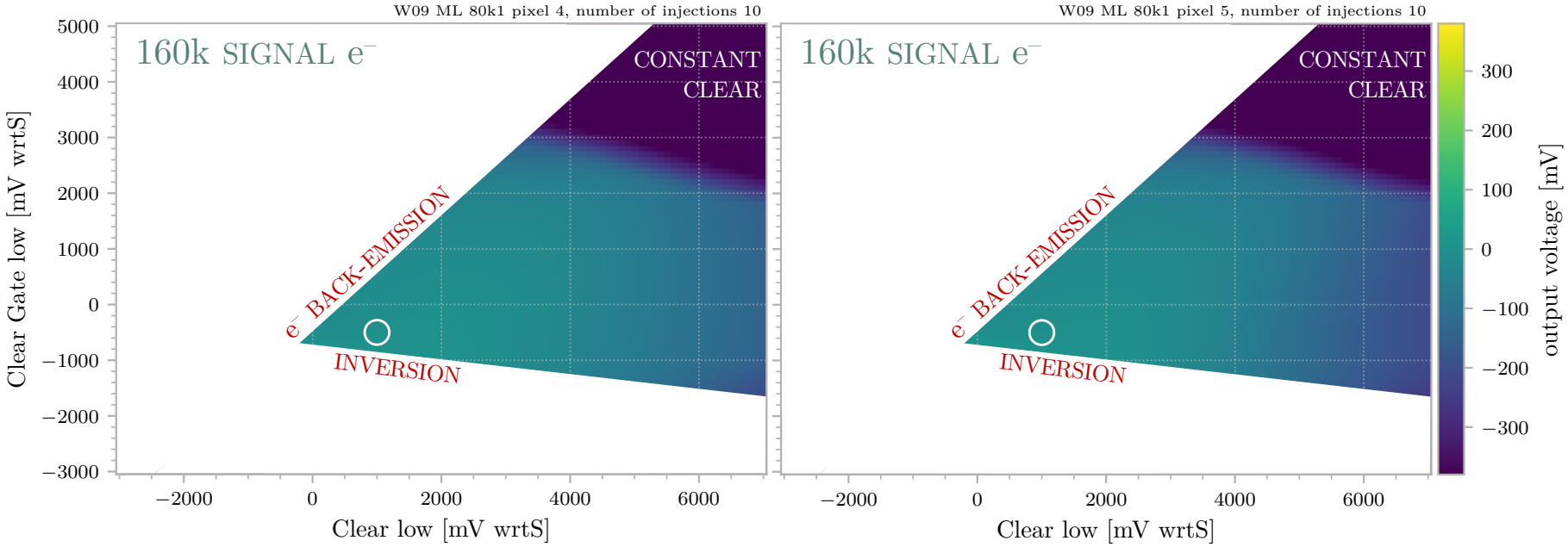

Measurements – operation window

on depleted 50 µm thick EDET structures

Clear Gate and Clear low voltage influence

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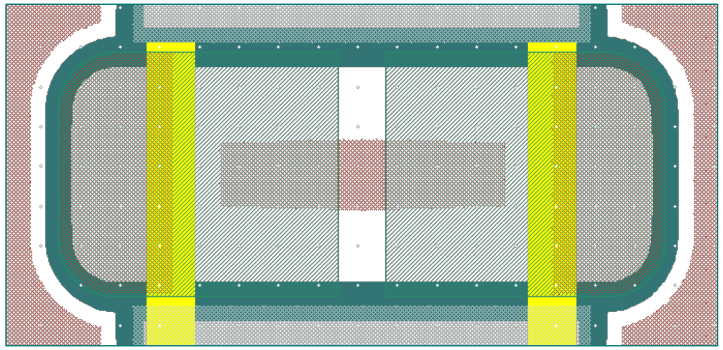

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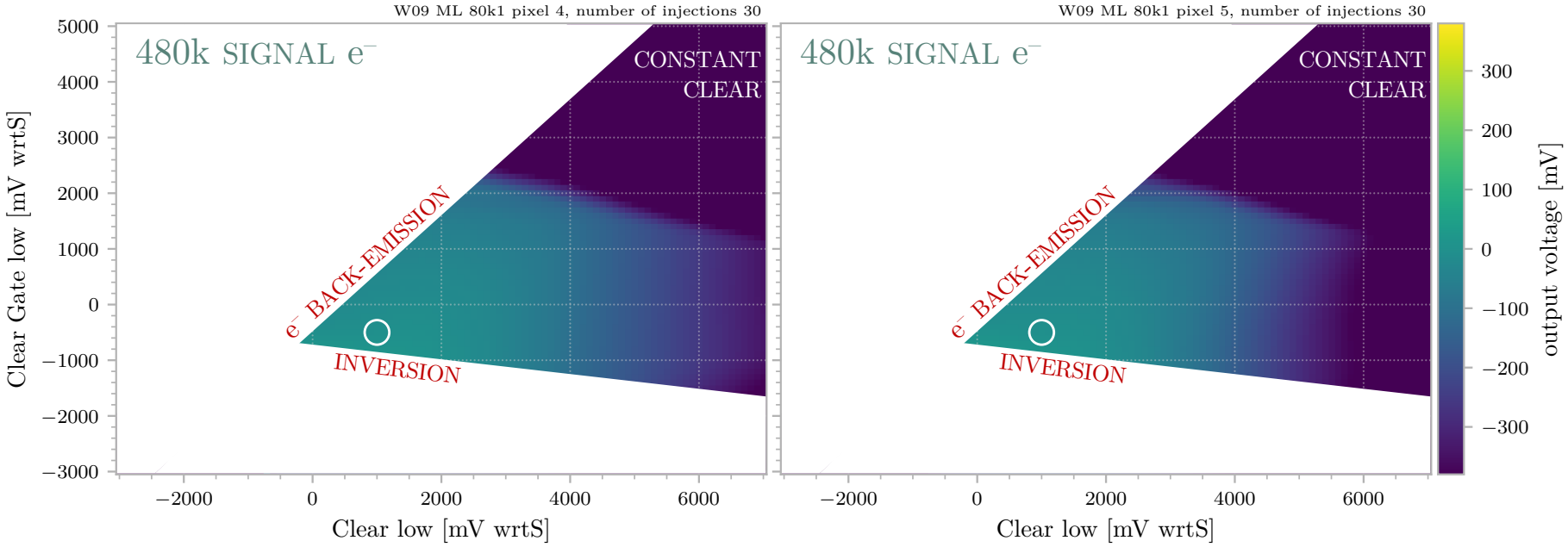

Measurements – operation window

on depleted 50 µm thick EDET structures

Clear Gate and Clear low voltage influence

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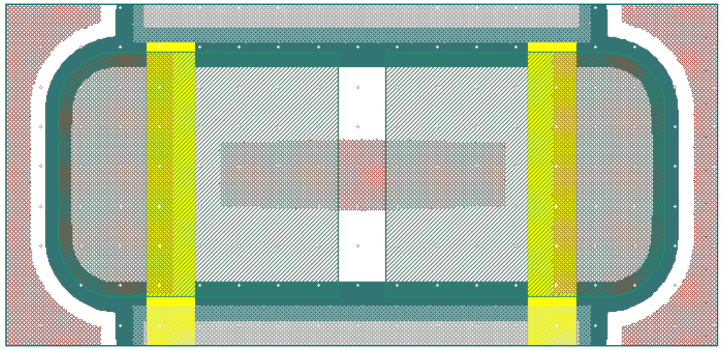

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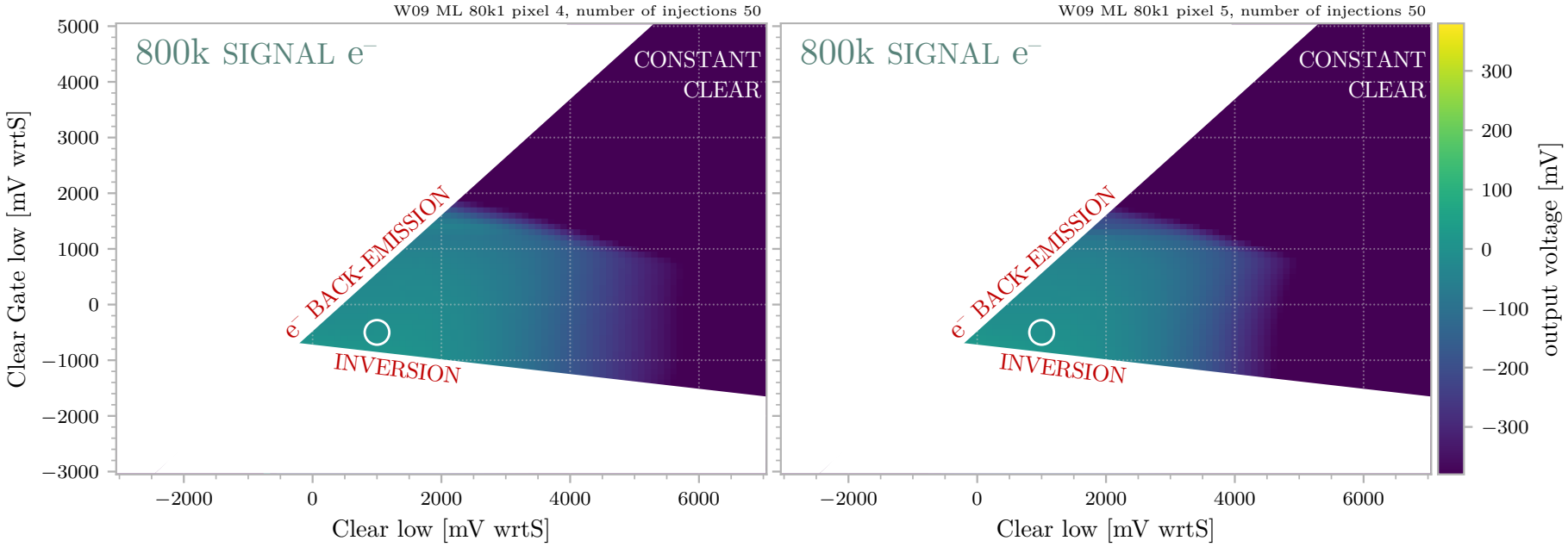

Measurements – operation window

on depleted 50 µm thick EDET structures

Clear Gate and Clear low voltage influence

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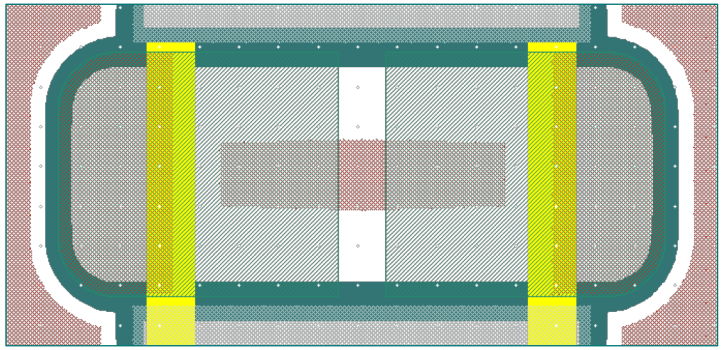

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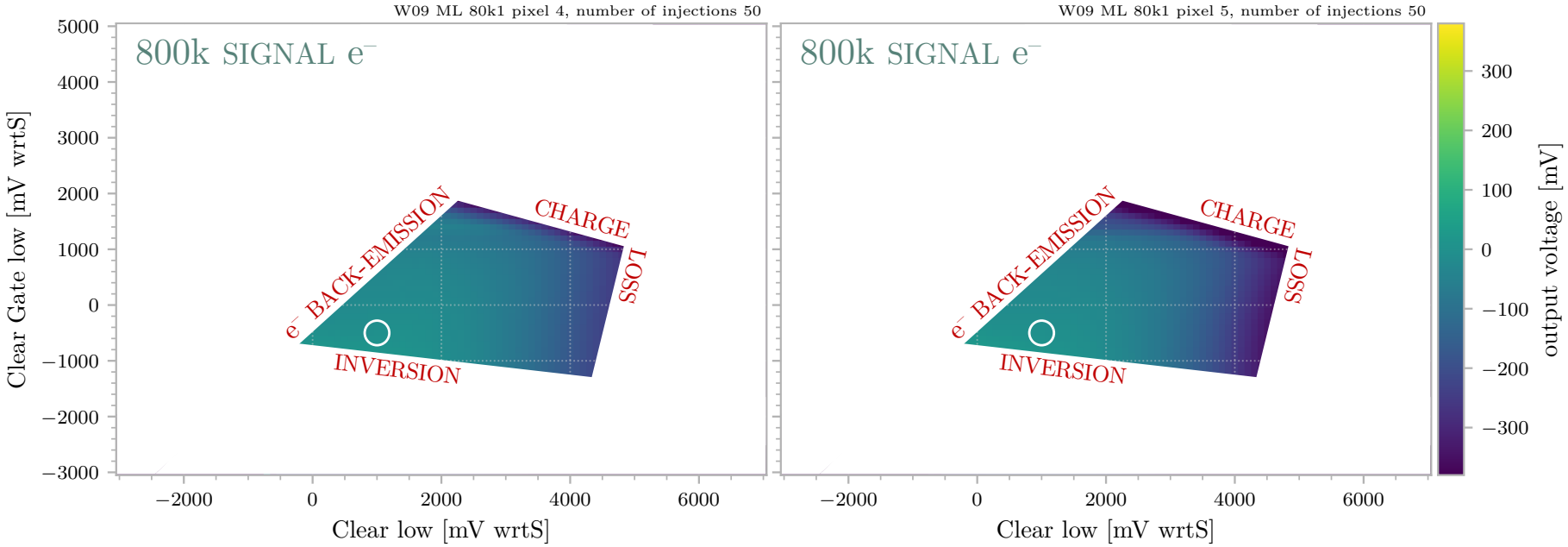

Measurements – operation window

on depleted 50 µm thick EDET structures

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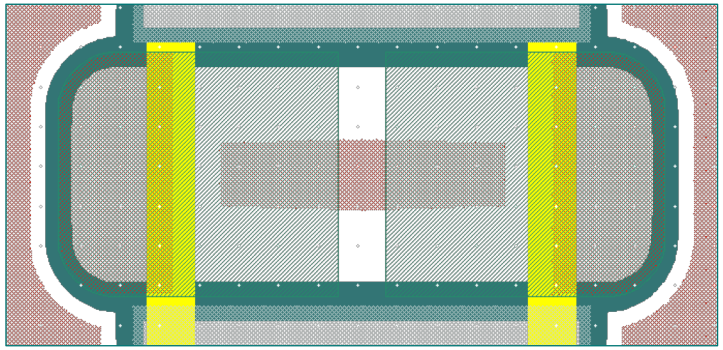

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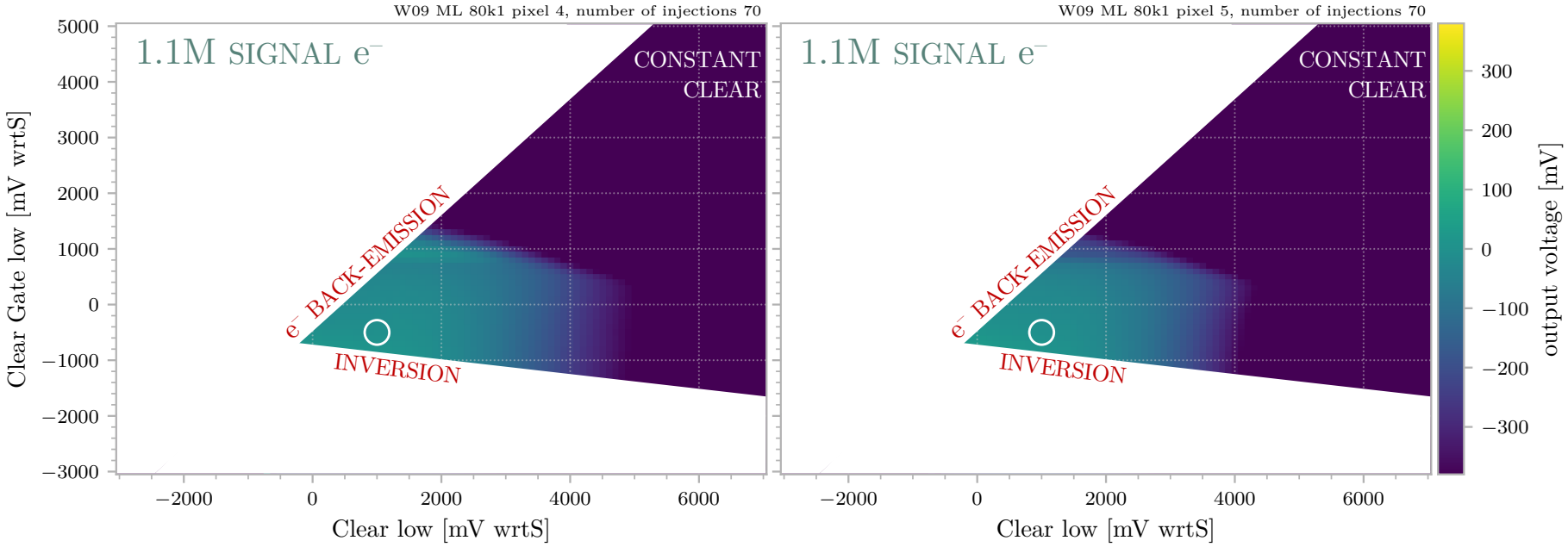

Measurements – operation window

on depleted 50 µm thick EDET structures

Clear Gate and Clear low voltage influence

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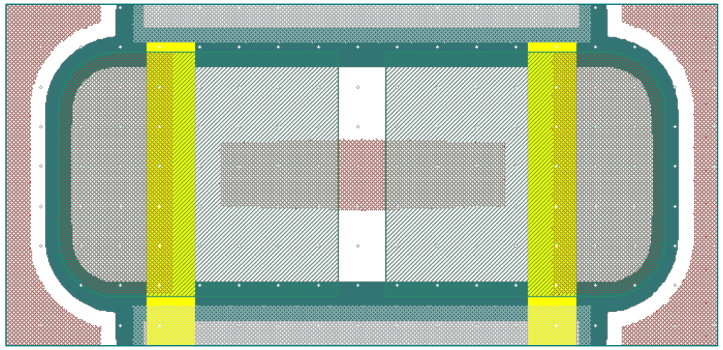

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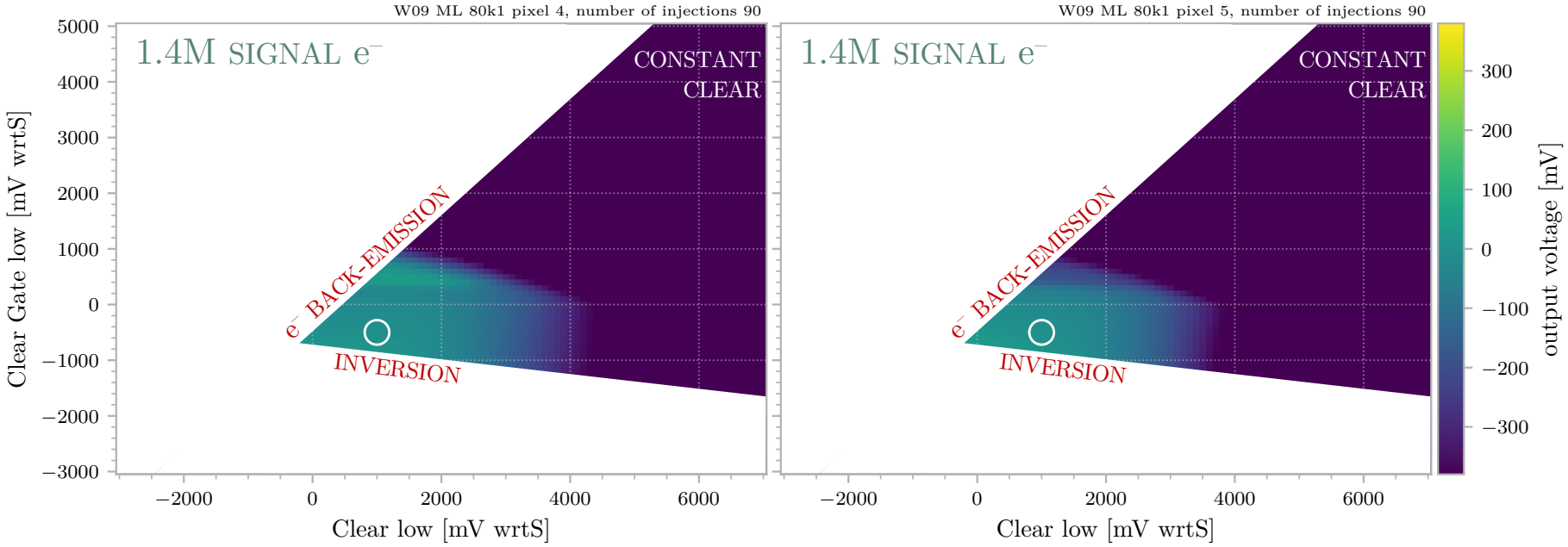

Measurements – operation window

on depleted 50 µm thick EDET structures

Clear Gate and Clear low voltage influence

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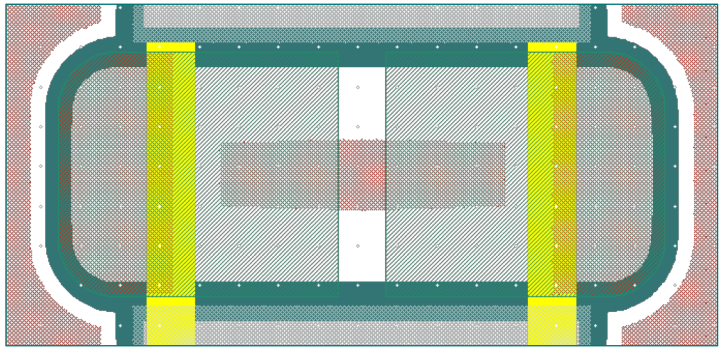

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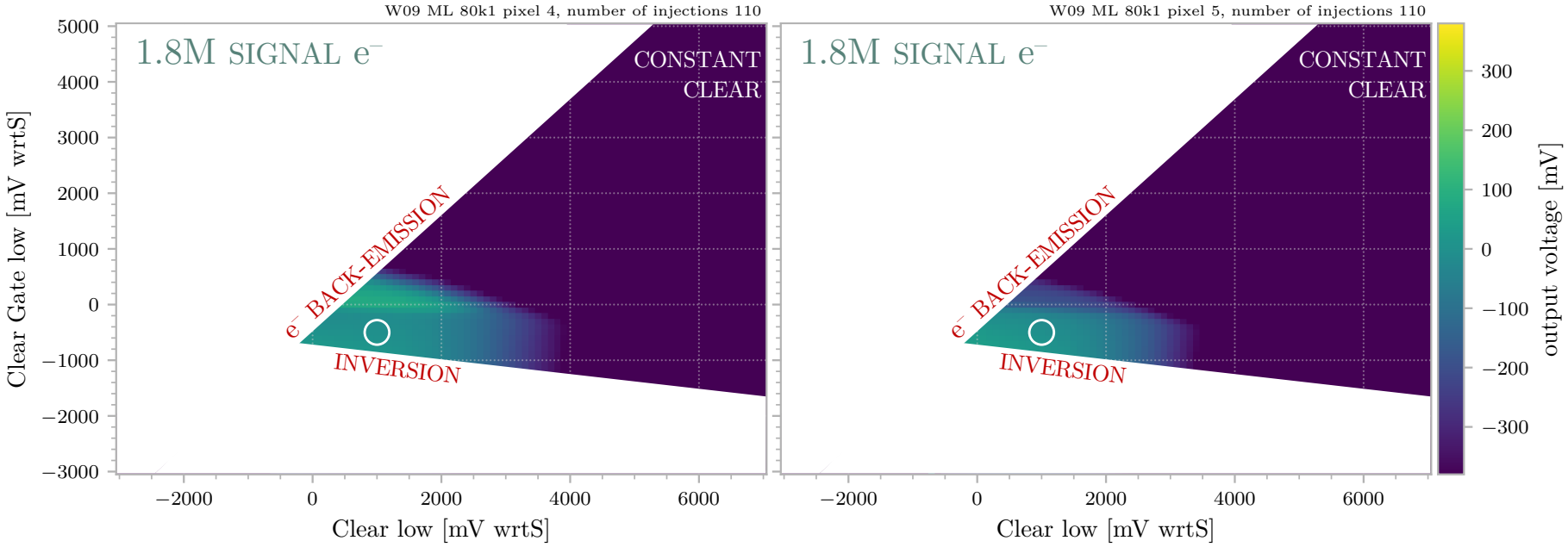
Guard	-5.0 V

LED FLATFIELD ILLUMINATION (FFIL); 1 INJECTION CORRESPONDS TO ~10X ^{55}Fe K_α



Measurements – incomplete clear

on depleted 50 µm thick EDET structures

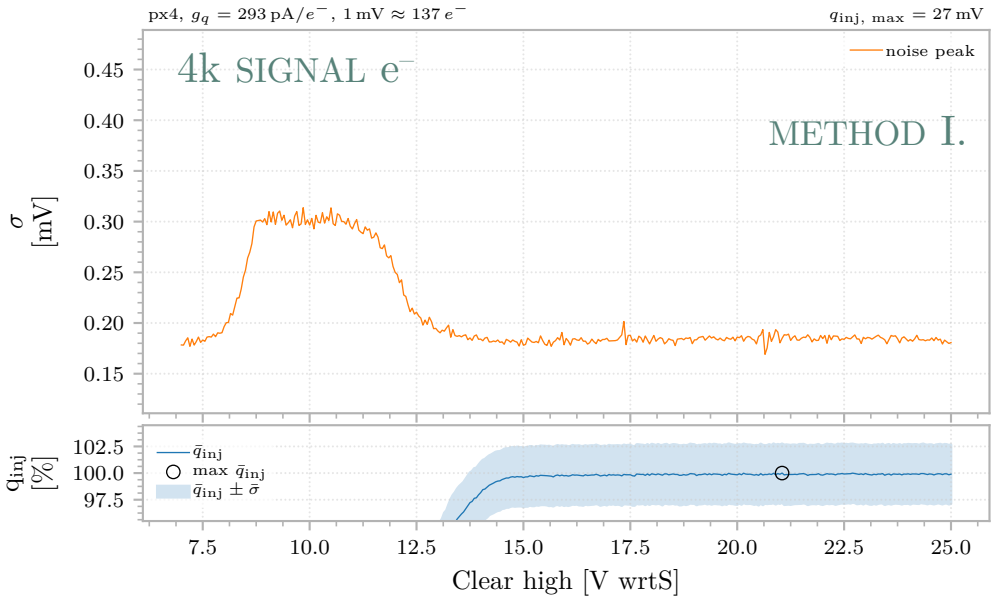
Clear high voltage and clear pulse length (t_c) influence

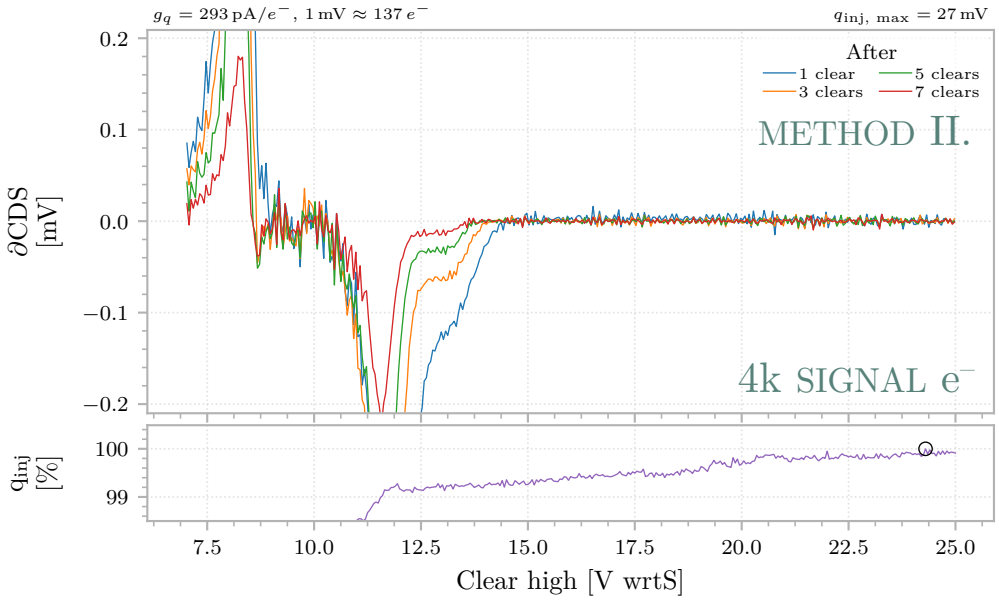
- efficiency of complete charge removal from internal gate and overflow regions.

Slow switching stage of SwitcherS ASIC limits $t_c > 70$ ns. Final camera setup $t_c \sim 20$ ns achieved with SwitcherB ASIC.

W09 F07	
Thickness	50 µm
Gate L	5.0 µm
Gate W	27.2 µm
Drain	-5.0 V
Source	0.0 V
Gate Off	5.0 V
Gate On	-2.17 V
Clear low	1.0 V
Clear high	sweep
Clear Gate	-0.5 V
Depletion	-35.0 V
Bulk	10.0 V
Drift	-5.0 V
Guard	-5.0 V

FFIL; SMALL SIGNAL CHARGE ~2.5x ^{55}Fe K_α; HARDEST TO REMOVE





Measurements – incomplete clear

on depleted 50 µm thick EDET structures

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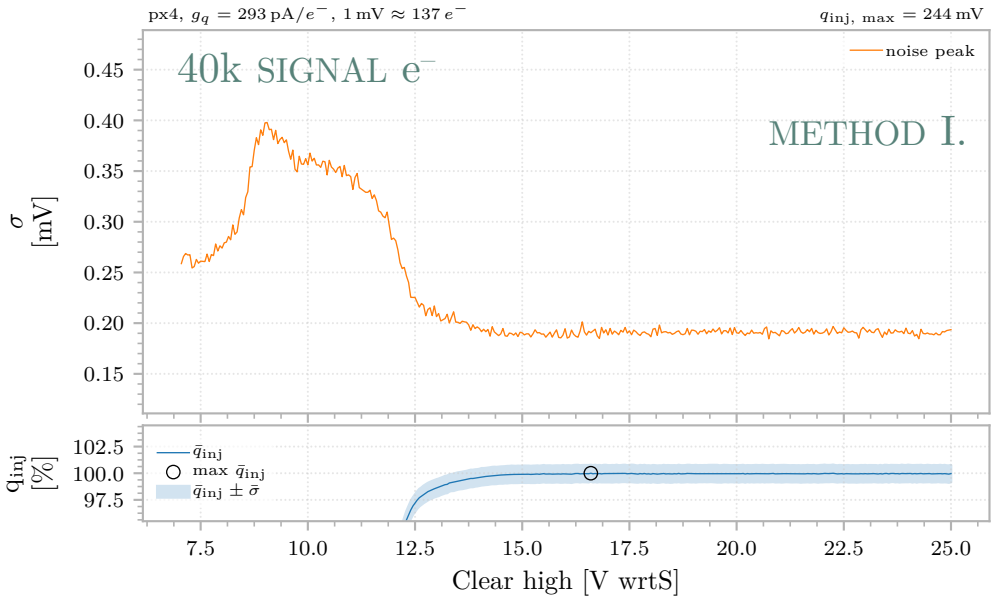
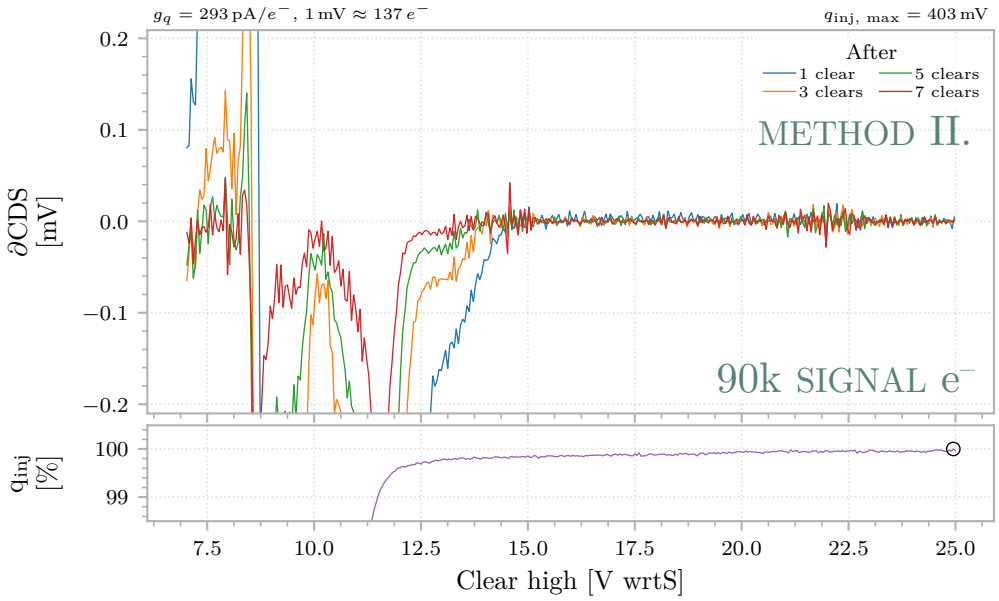
Source	0.0 V
Gate Off	5.0 V
Gate On	-2.17 V
Clear low	1.0 V
Clear high	sweep
Clear Gate	-0.5 V
Depletion	-35.0 V
Bulk	10.0 V
Drift	-5.0 V
Guard	-5.0 V

FFIL; ALMOST FULL INTERNAL GATE



FFIL; FILLING THE OVERFLOW REGIONS



Measurements – incomplete clear

on depleted 50 µm thick EDET structures

Clear high voltage and clear pulse length (t_c) influence

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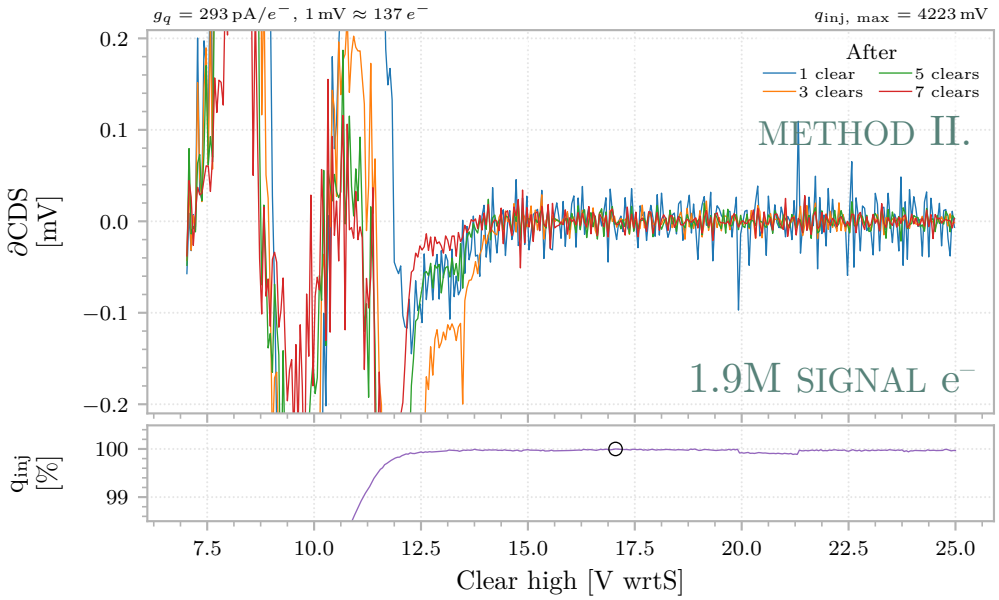
Clear low	1.0 V
Clear high	sweep
Clear Gate	-0.5 V
Depletion	-35.0 V
Bulk	10.0 V
Drift	-5.0 V
Guard	-5.0 V

FFIL; COMPLETELY FILLED STATE

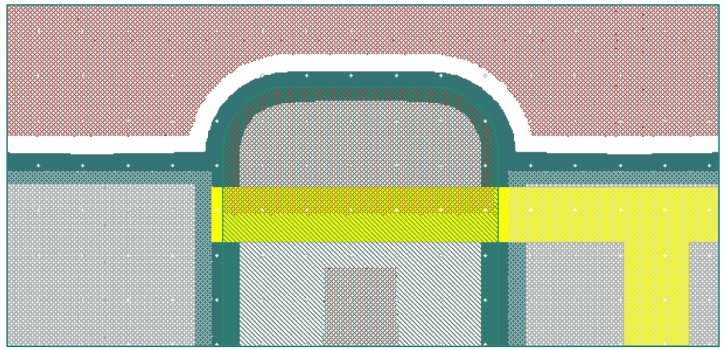


Measurements – charge collection

on depleted 50 µm thick EDET structures

Depletion and Drift voltage influence

- integrated 1st stage amplification (g_q),
- charge loss to Clear, and
- charge loss to Drift region.



W09 F07	
Thickness	50 µm
Gate L	5.0 µm
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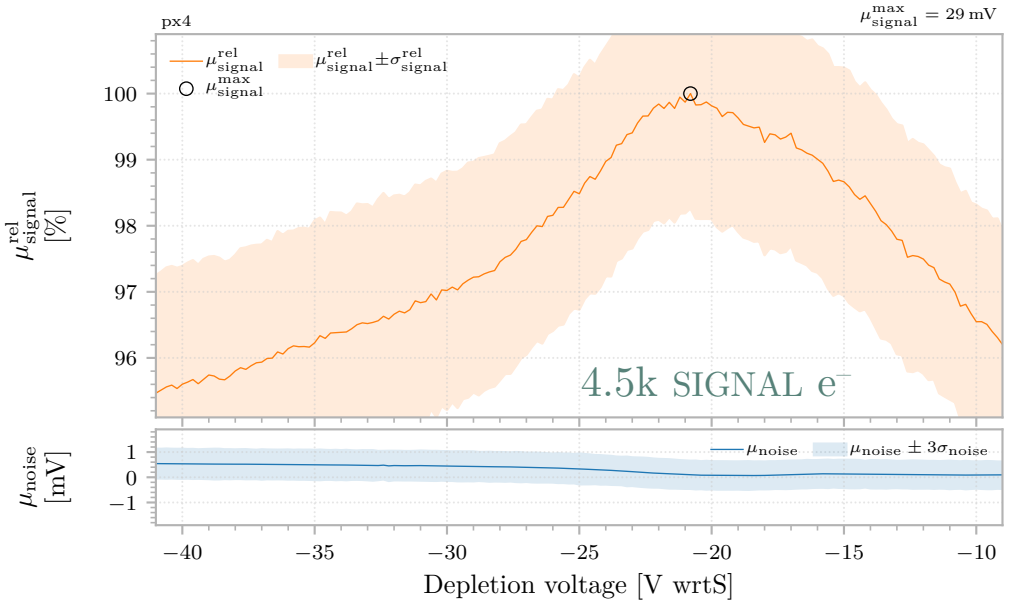
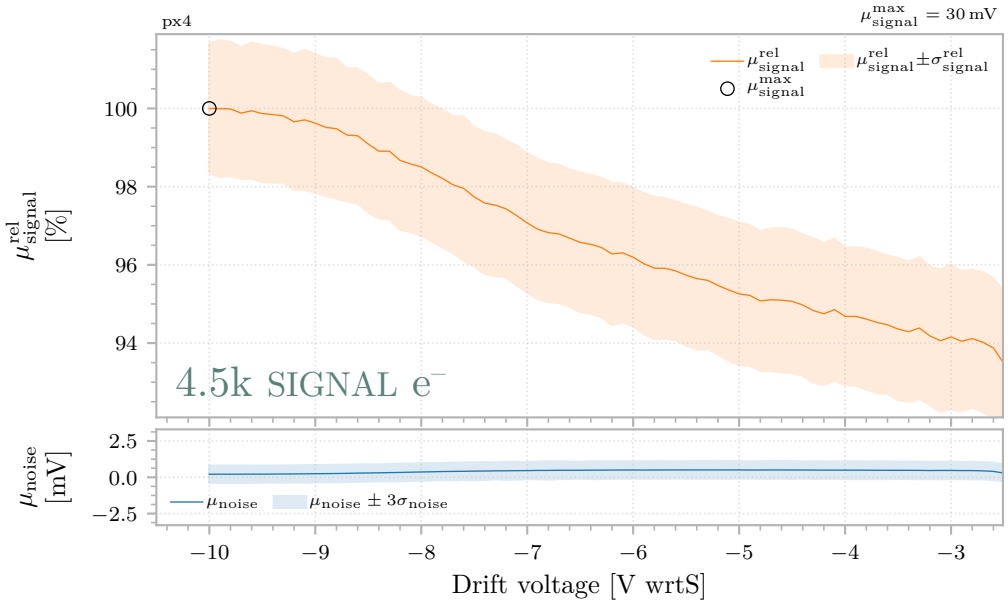
Drain	-5.0 V
Source	0.0 V
Gate Off	5.0 V
Gate On	-2.17 V
Clear low	1.0 V
Clear high	18.0 V
Clear Gate	-0.5 V
Depletion	sweep
Bulk	10.0 V
Drift	sweep
Guard	-5.0 V

FFIL; SMALL SIGNAL CHARGE ~2.8X ^{55}Fe K_α





Measurements – charge collection

on depleted 50 µm thick EDET structures

Depletion and Drift voltage influence

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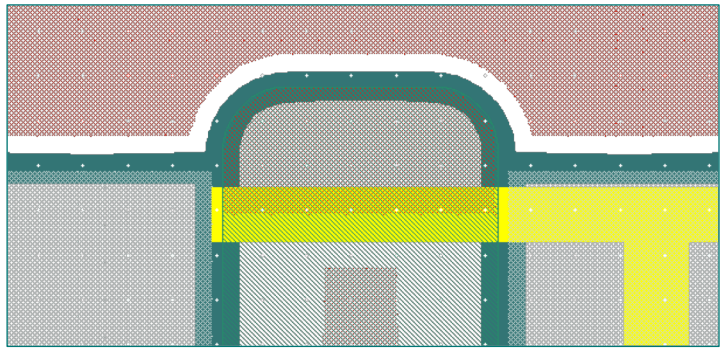

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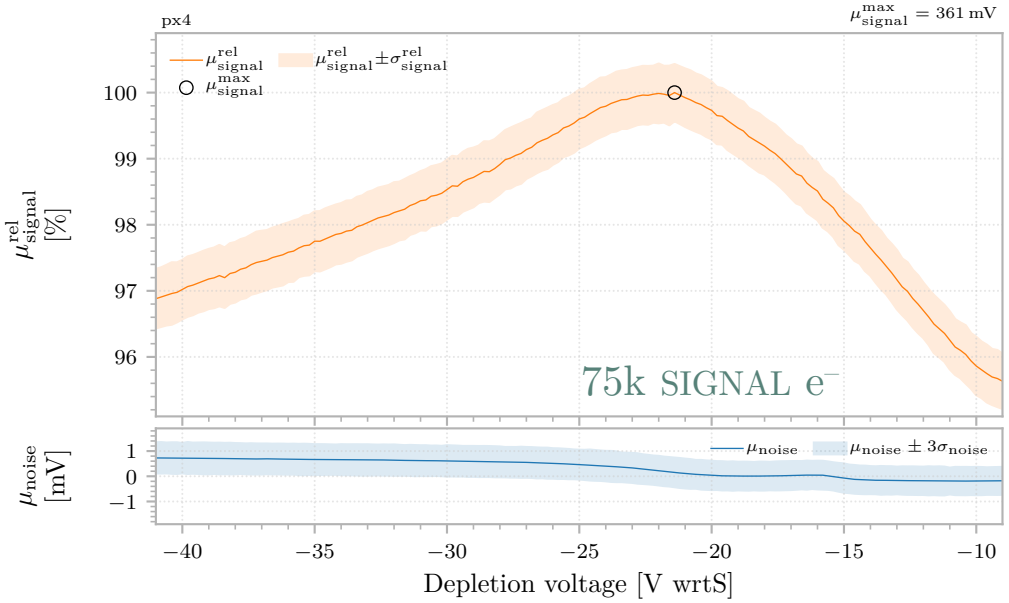
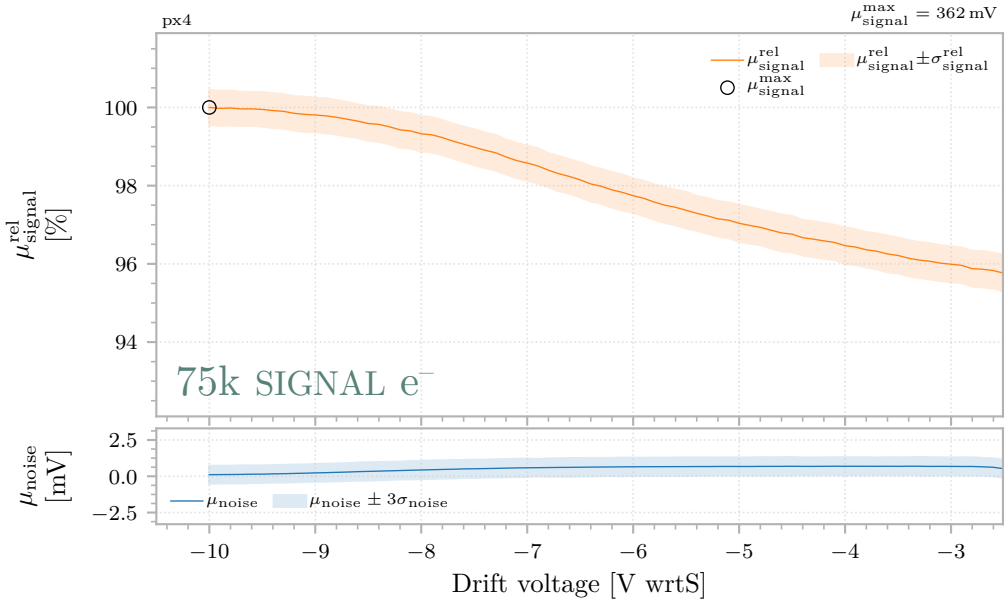
Gate On	-2.17 V
Clear low	1.0 V
Clear high	18.0 V
Clear Gate	-0.5 V
Depletion	sweep
Bulk	10.0 V
Drift	sweep
Guard	-5.0 V

FFIL; FILLING THE OVERFLOW REGIONS; LESS LOSSES – FILLED POTENTIAL POCKET UNDER DRIFT





Measurements – charge collection

on depleted 50 µm thick EDET structures

Depletion and Drift voltage influence

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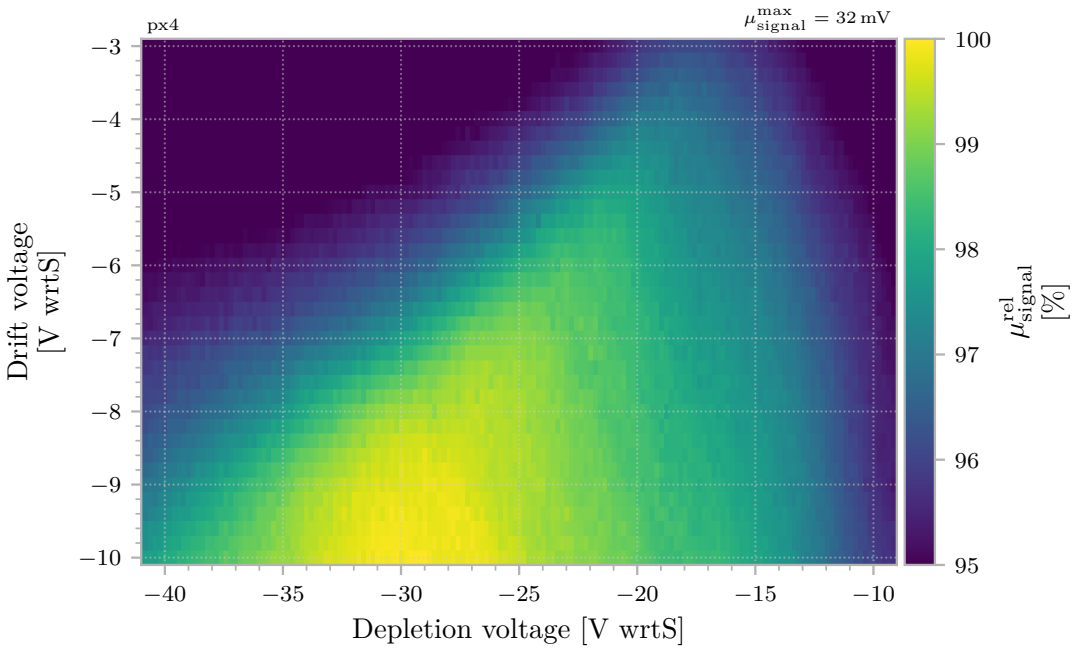
Clear low	1.0 V
Clear high	18.0 V
Clear Gate	-0.5 V
Depletion	sweep
Bulk	10.0 V
Drift	sweep
Guard	-5.0 V

FFIL; SMALL SIGNAL CHARGE ~2.8X ^{55}Fe K_α



OPERATIONAL POINT ALSO DEPENDS ON THE DRIFT AND THE DEPLETION CURRENT DUE TO PROBLEMATIC HEAT DISSIPATION IN THIN DEVICES.

Measurements – charge collection

on depleted 50 µm thick EDET structures

Depletion and Drift voltage influence

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Bulk	10.0 V
Drift	sweep
Guard	-5.0 V

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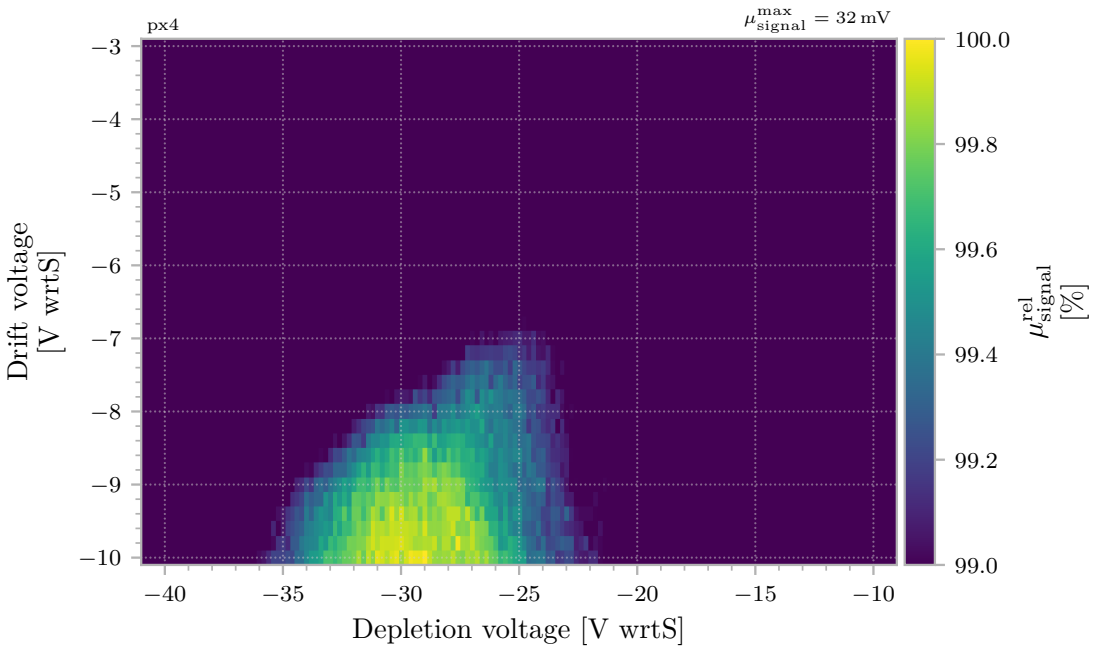


OPERATIONAL POINT ALSO DEPENDS ON THE DRIFT AND THE DEPLETION CURRENT DUE TO PROBLEMATIC HEAT DISSIPATION IN THIN DEVICES.

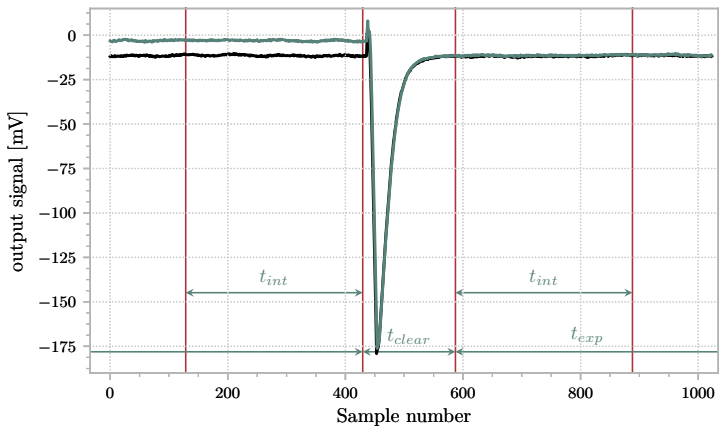
Measurements – noise v integration time

on depleted 50 µm thick EDET structures

Integration time (t_{int}) influences

- the overall noise performance of the system.

Noise dominated by Leakage Current and Common Mode Noise.



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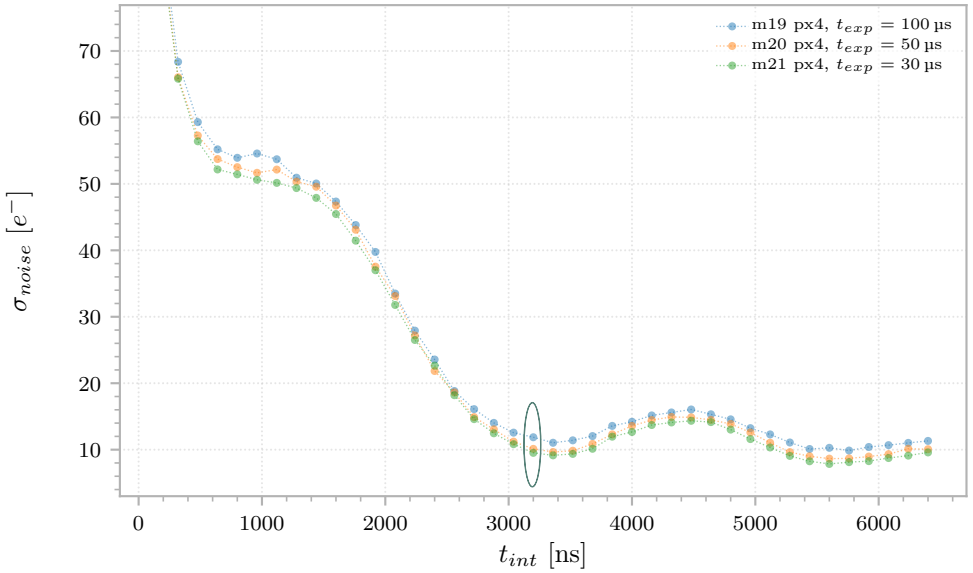
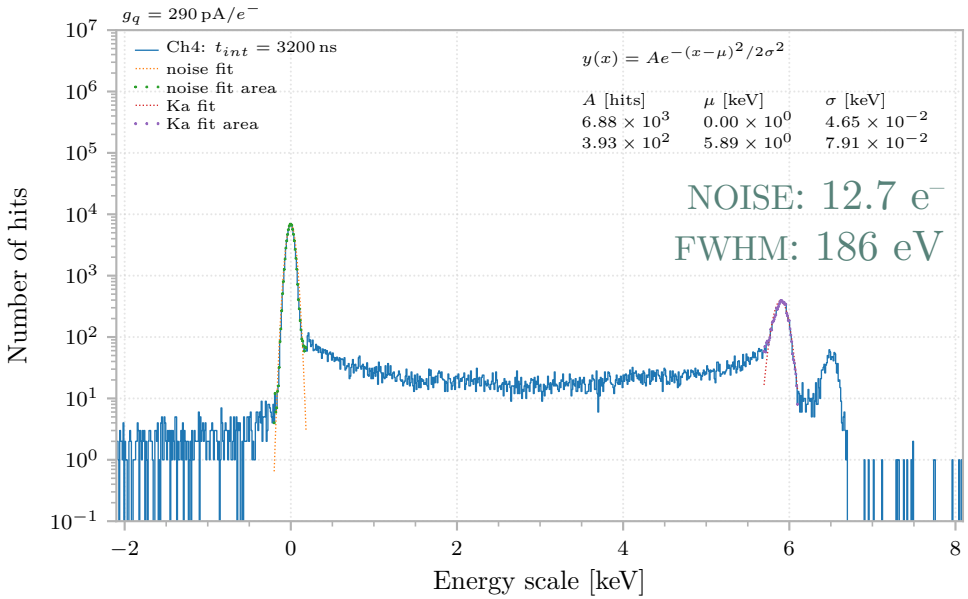
Source	0.0 V
Gate Off	5.0 V
Gate On	-2.17 V
Clear low	1.0 V
Clear high	18.0 V
Clear Gate	-0.5 V
Depletion	-21.0 V
Bulk	10.0 V
Drift	-5.0 V
Guard	-5.0 V

^{55}Fe RADIOACTIVE SOURCE ILLUMINATION





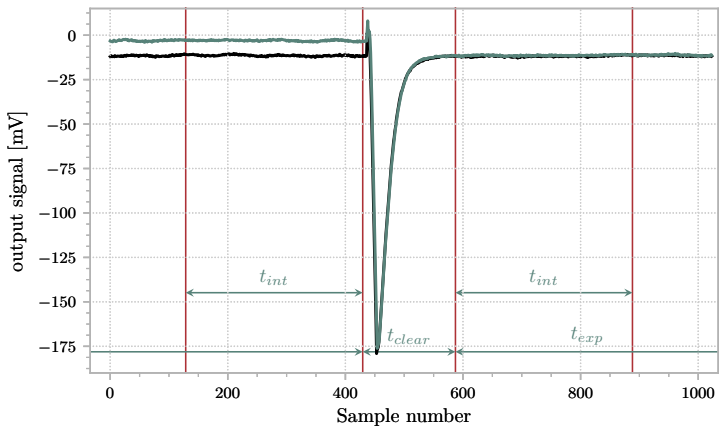
Measurements – noise v integration time

on depleted 50 µm thick EDET structures

Integration time (t_{int}) influences

- the overall noise performance of the system.

Noise dominated by Leakage Current and Common Mode Noise.



W09 F07	
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Source	0.0 V
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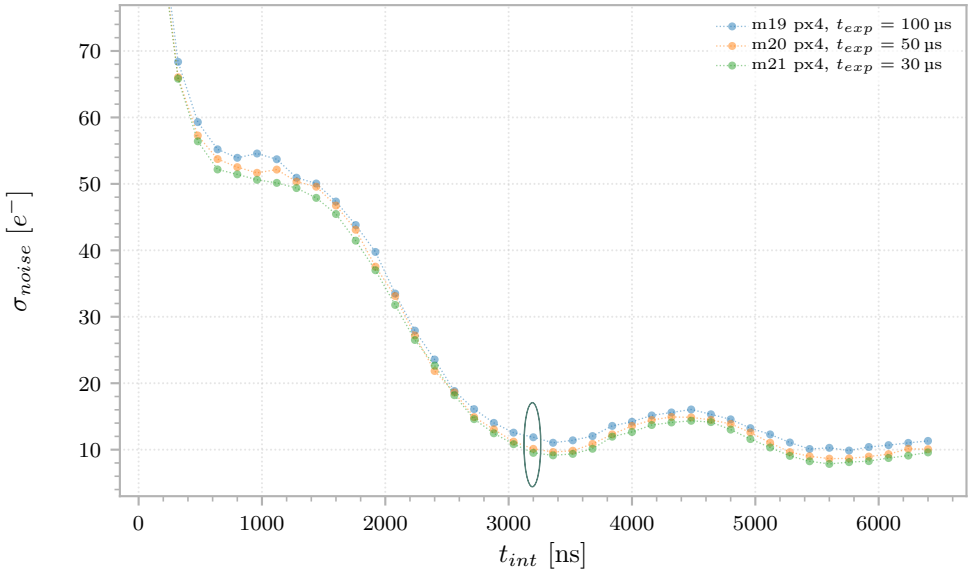

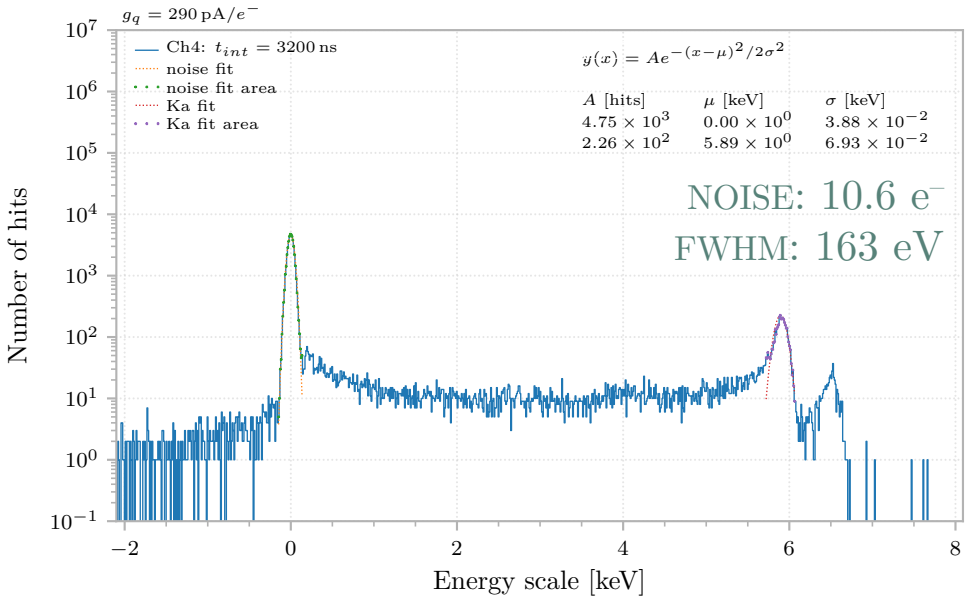

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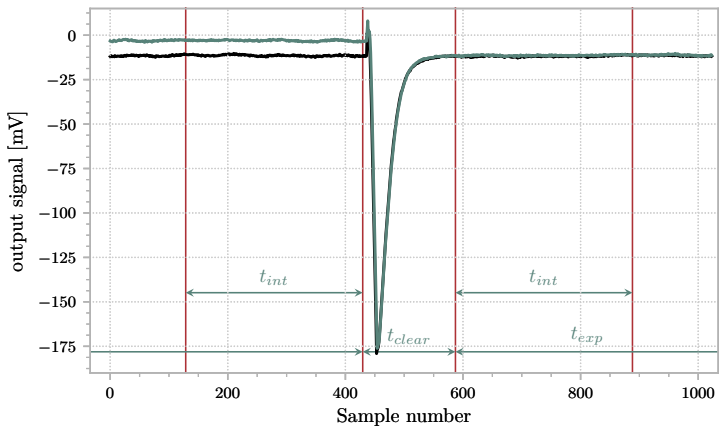

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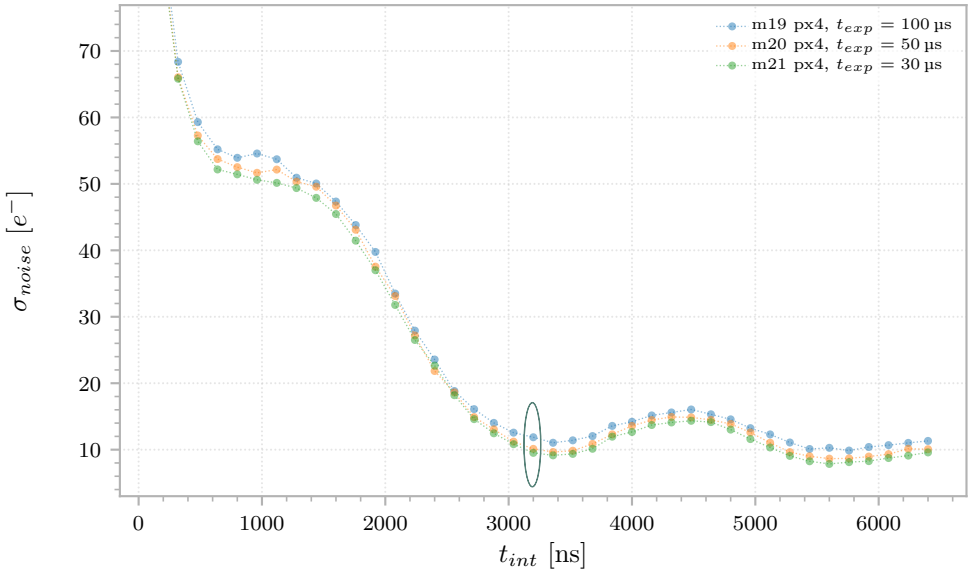

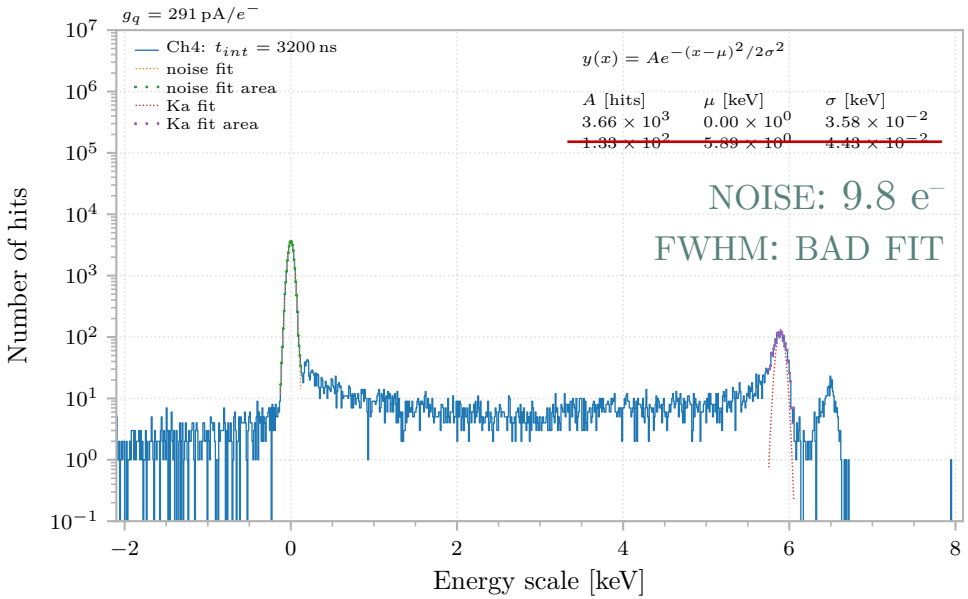

Response function – Calibration

of depleted 50 µm thick EDET structures

Procedure:

- insertion of fixed amount of charge by ^{55}Fe radioactive source at optimized operation voltages
- extraction of the primary g_q
- explore the full dynamic range with calibrated LED pulses and leakage current

PRIMARY $g_q = 291\ \mathrm{pA/e^-}\ (1 \pm 0.014)$

W09 F07	
Thickness	50 µm
Gate L	5.0 µm
Gate W	27.2 µm
Drain	-5.0 V
Source	0.0 V
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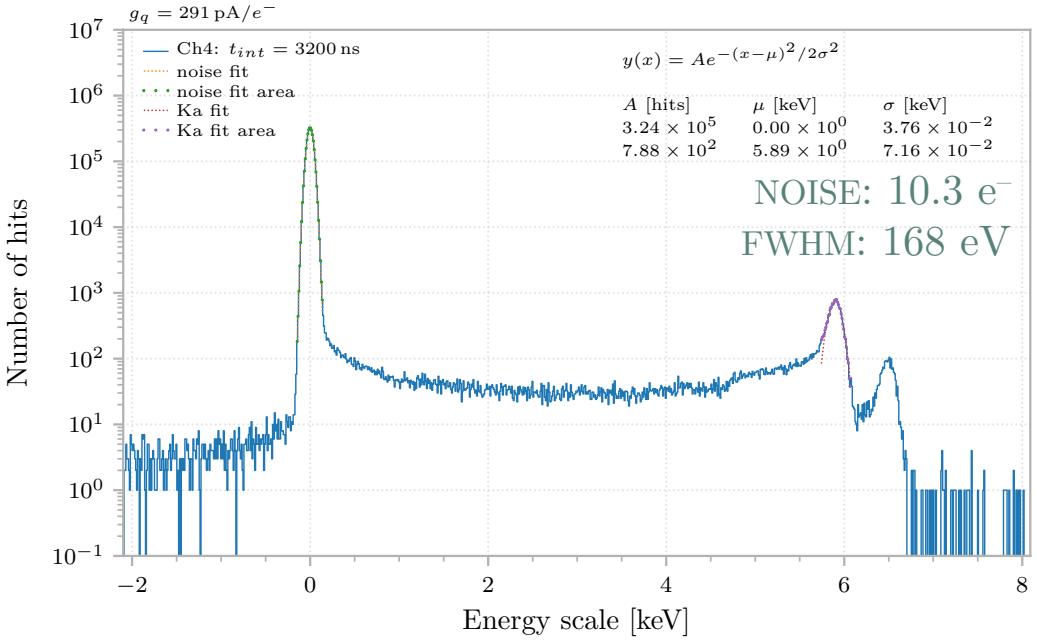
^{55}Fe RADIOACTIVE SOURCE ILLUMINATION



Response function – Dynamic range

of depleted 50 µm thick EDET structures

Procedure:

- insertion of fixed amount of charge by ^{55}Fe radioactive source at optimized operation voltages
- extraction of the primary g_q
- explore the full dynamic range with calibrated LED pulses and leakage current

PRIMARY $g_q = 291\ \mathrm{pA/e^-}\ (1 \pm 0.003)$

SECONDARY $g_q = 70\ \mathrm{pA/e^-}\ (1 \pm 0.10)$

LEAKAGE $I_L = 0.57\ \mathrm{e^-/\mu s}(1 \pm 0.05)$

W09 F07	
Thickness	50 µm
Gate L	5.0 µm
Gate W	27.2 µm
Drain	-5.0 V
Source	0.0 V
Gate Off	5.0 V
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Clear low	1.0 V
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Clear Gate	-0.5 V
Depletion	-21.0 V
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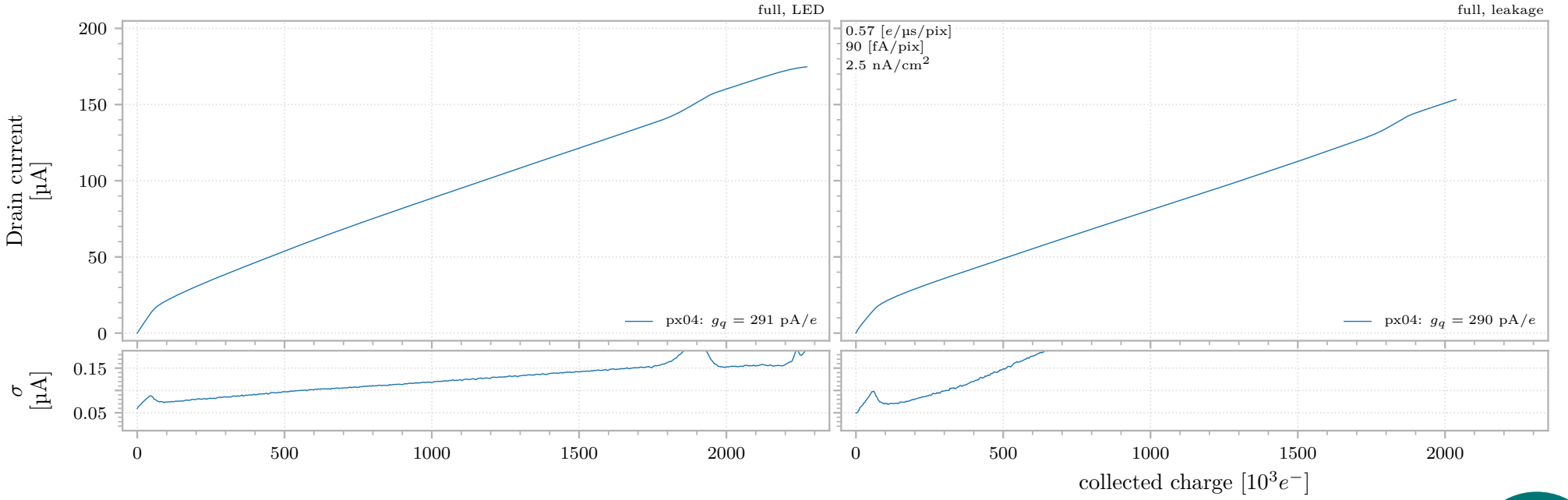
Guard	-5.0 V

FFIL; $t_{exp} = 3.1$ ms; 601 PULSES

LEAKAGE CURRENT; $t_{exp} = 3.6$ s;



Motivation and Introduction

DePFET Structure and Measurement Setup

Optimization of Operation Parameters and Response Function

Summary and Outlook

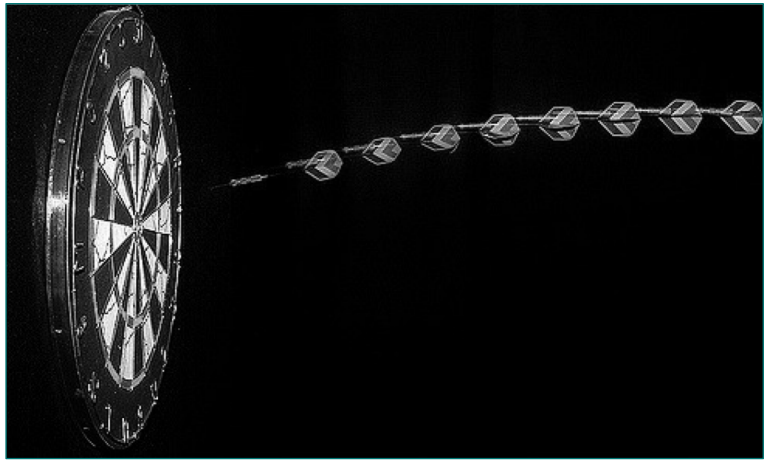
Summary and outlook
for the project

DePFETs

- extremely versatile detectors
- established in spectroscopy
- paving their way in the tracking applications

EDET project

- pilot production successfully finished, fabrication of the main batch has been resumed
- pilot devices showing expected results
  - signal compression
  - dynamic range of >800k signal e^-
  - operation window big enough to operate the large area devices
- commissioning of the first tile modules with FEE without movie storage (Belle II DHP ASICs) in 2Q2019
- FEE with movie storage (DMC ASIC) currently under evaluation at MPG HLL
- commissioning of the first fully EDET tiles in late 4Q2019



Thank You for Your attention!

Backup slides

Common mode noise

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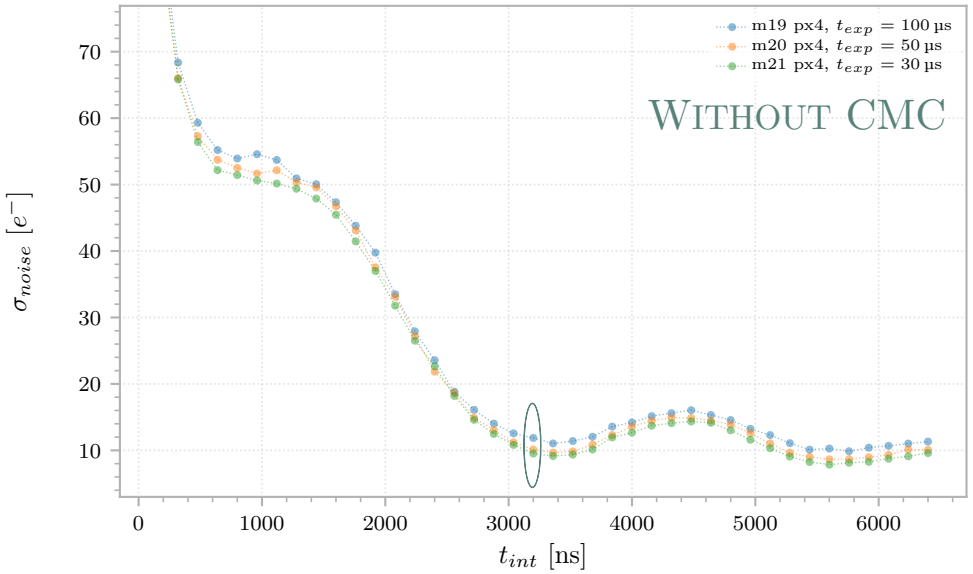
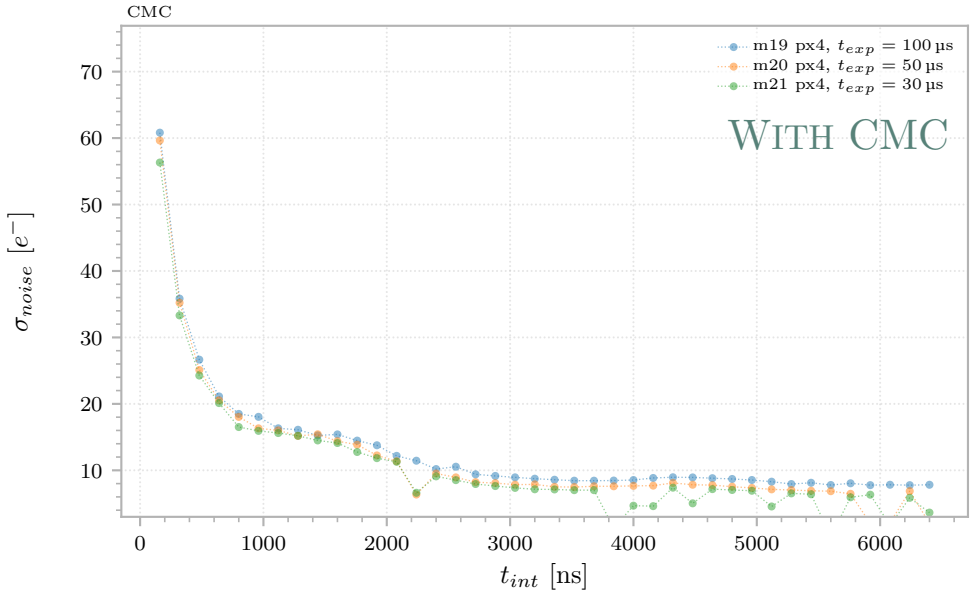
^{55}Fe RADIOACTIVE SOURCE ILLUMINATION





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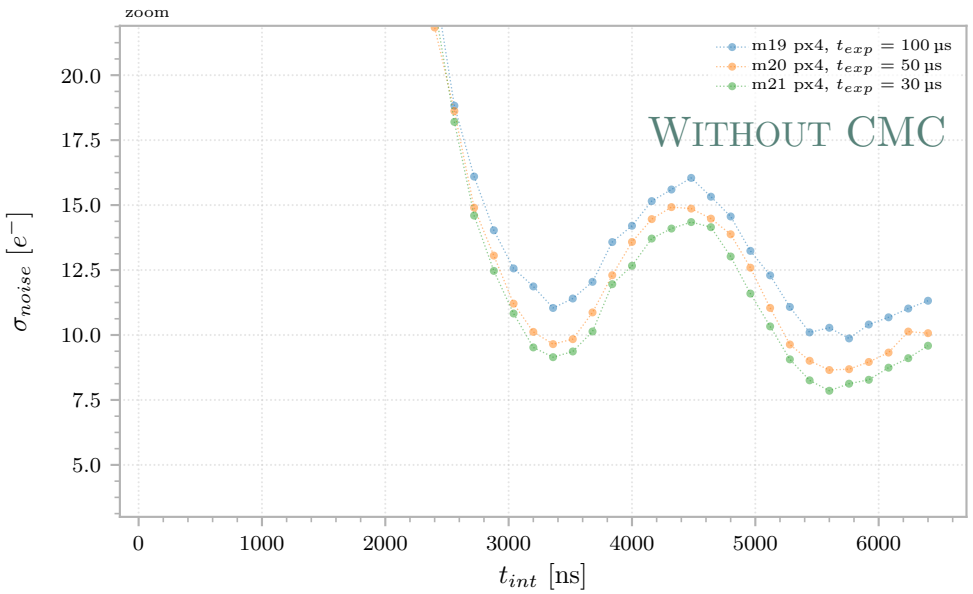

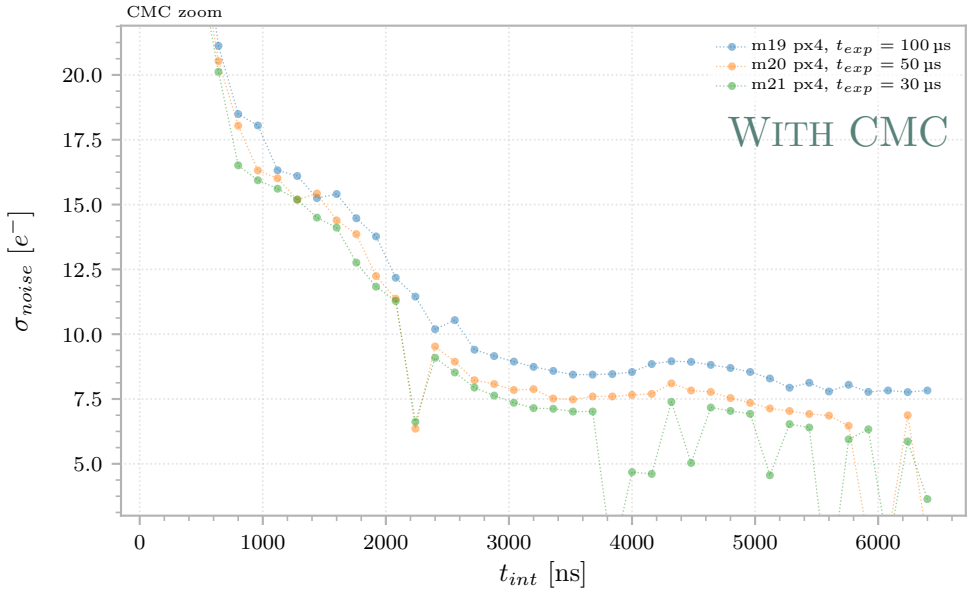

20 % CHANGE IN $\boldsymbol{\sigma}_{\text{noise}}$

Radiation hardness

Radiation causes positive charge buildup in Oxide:

- homogeneous radiation – compensated by gate voltage shifts
- inhomogeneous radiation – could cause problems