Radiation hard active pixel sensor with 25µm x 50µm pixel size designed for capacitive readout with RD53 ASIC

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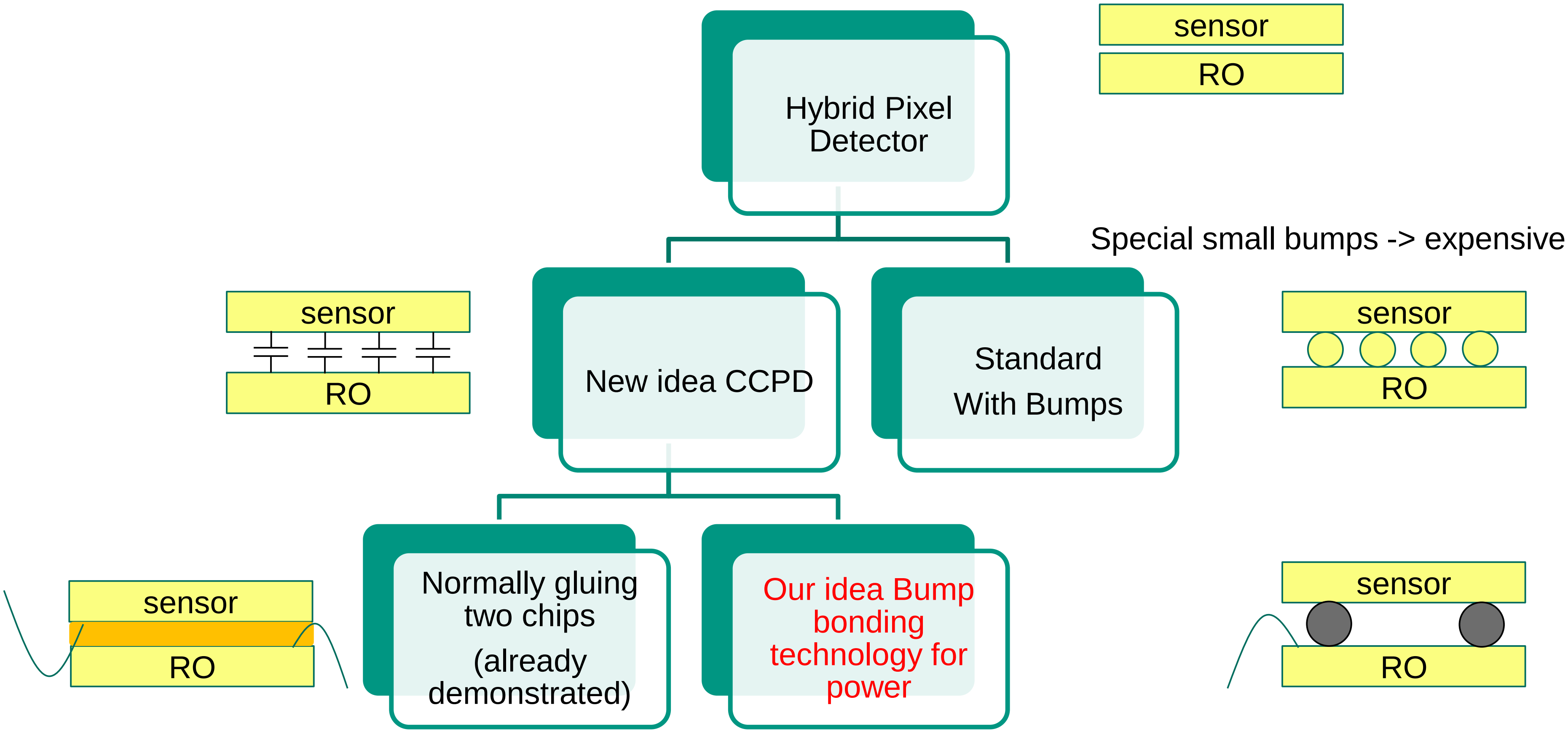
- Summary

CCPD - Introduction

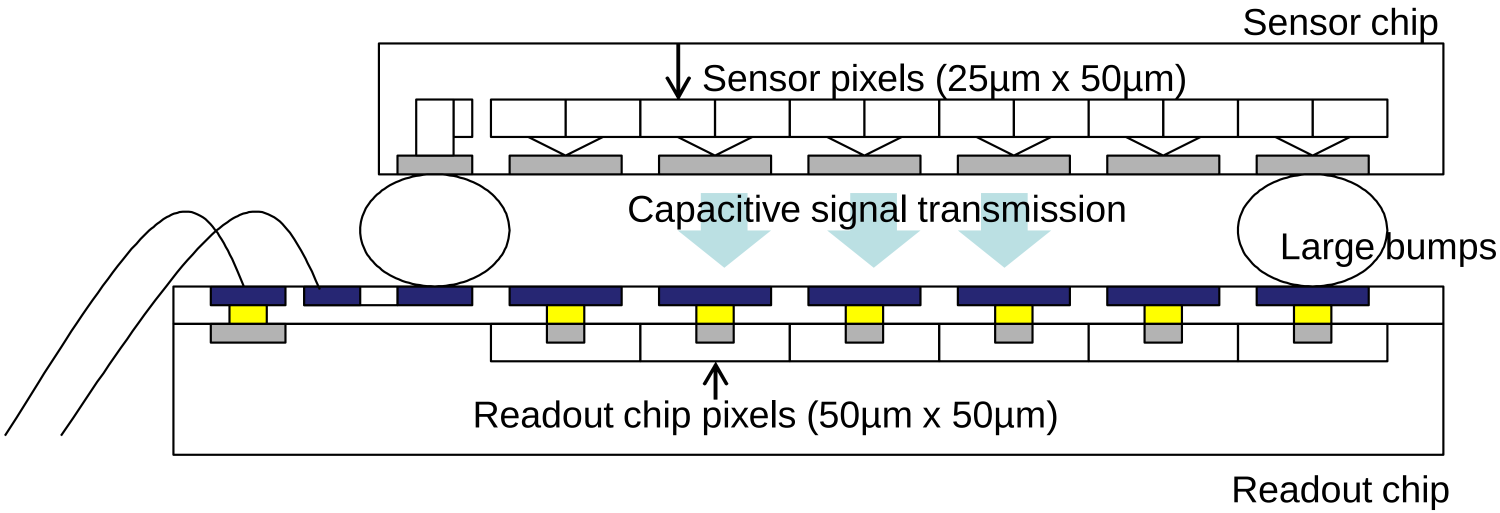
- CCPD (capacitively coupling pixel detector) is a type of hybrid pixel detector, that means the sensor chip and electronic parts are separate



A conventional flip chip technique can be used to build the detector
Since the bumps can be large, an industrial bumping process can be used which assure low cost.
Allow signal transmission through big gap (about 32µm)

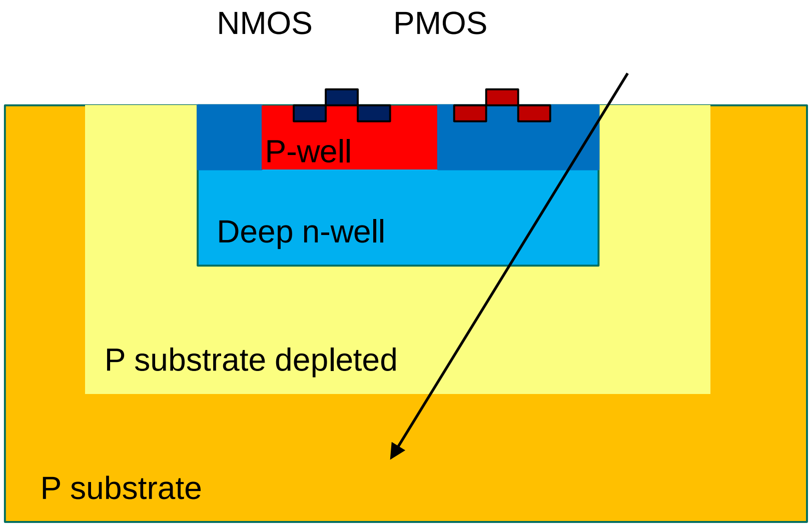
The benefit of the new concept

- Application: inner layer of ATLAS pixel detector
- The idea that I present here is to transmit large amplitude digital signals rather the analogue signals
- For the readout RD53 would be used. The goal is a pixel size of 25µm x 25µm (in our design in 25µm x 50µm). Since RD53 has 50µm x 50µm, pixels multiplexing would be used



Implementation of the sensor

- Implemented in 180nm HVCMOS technology
- The pixel sensor structure is a deep n-well in p-substrate
  - P-substrate is biased with negative high voltage ~-50V
  - The active region below the deep n-well is depleted (high voltage used)
  - N-well acts as the charge collecting electrode, charge collection by drift
  - The pixel electronics has been implemented inside the n-well, this means inside the charge collecting electrode. Such a structure assure that the sensor has 100% fill factor and that the electronics is shielded from the high voltage



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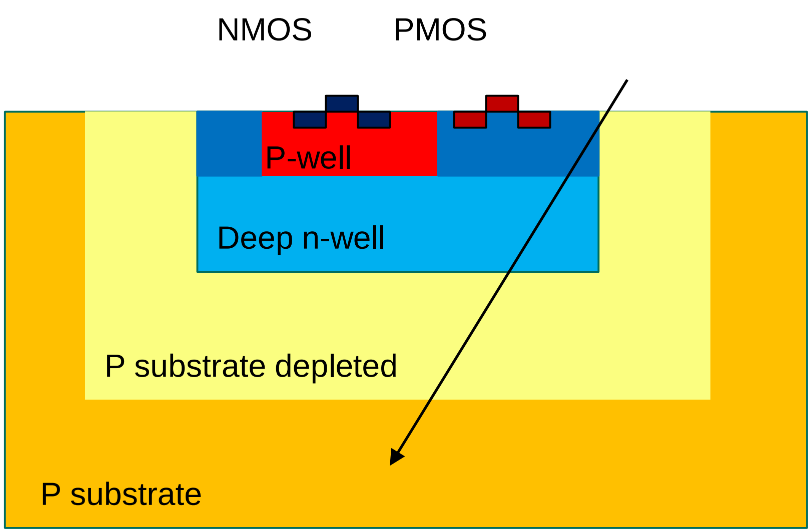
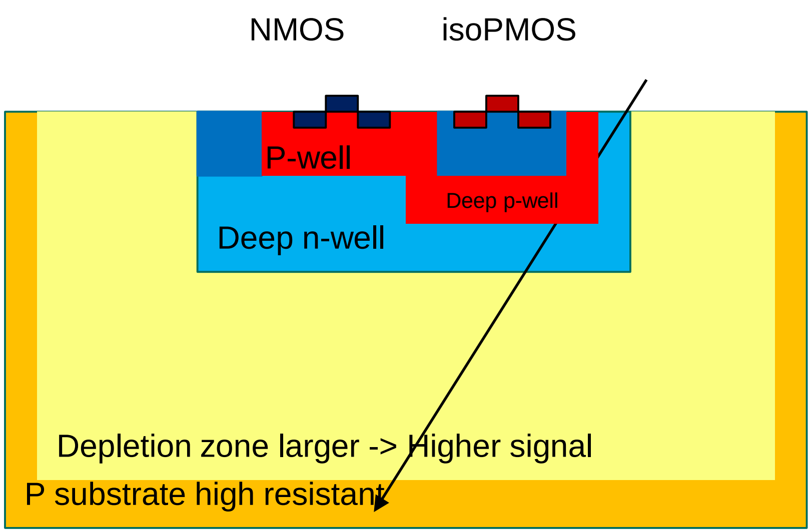
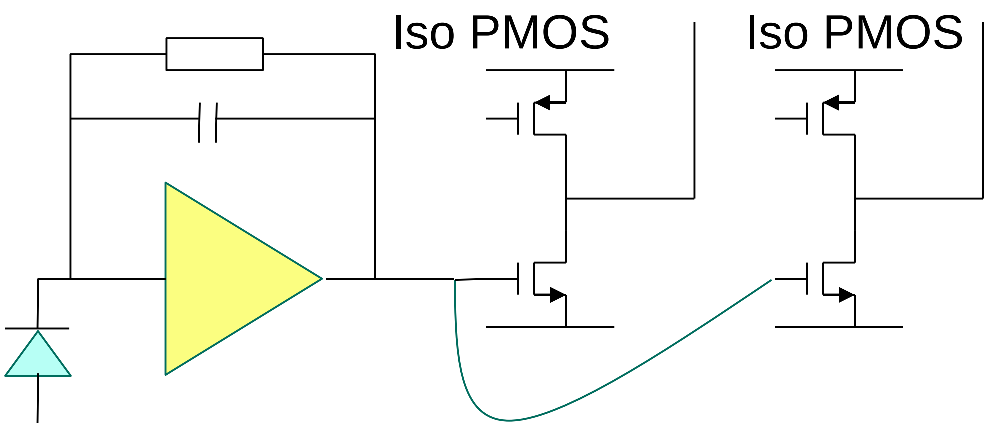
- The used HVCMOS process have been modified in two methods:
  - A deep p-well implant has been added
  - A high resistivity substrate of 200 Ohm has been used



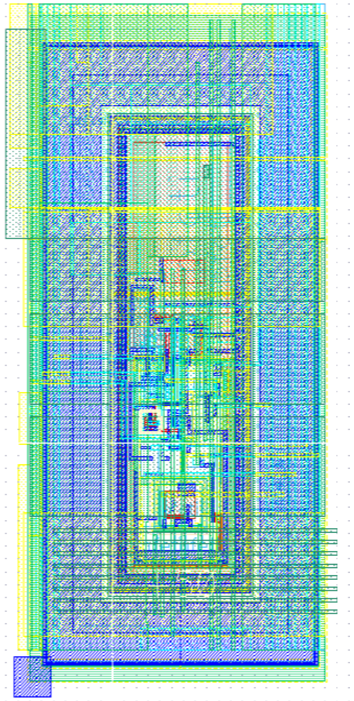


Pixel Design

- The pixel electronics contains a charge sensitive amplifier (CSA), a RC feedback circuit and two CMOS bias comparators.
- The simple comparator contains one input transistor (NMOS) and one pull up transistor (isoPMOS).
- The pull up transistor is isolated by a deep p-well
- If several comparator outputs of different pixels are shorted it corresponds to OR function



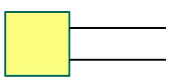
Schmetic of Pixel

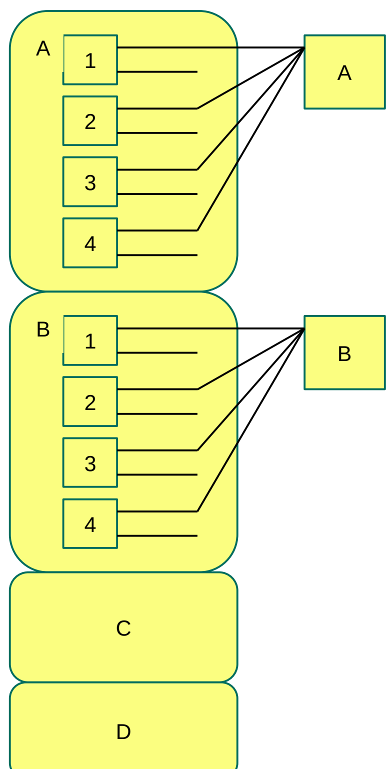


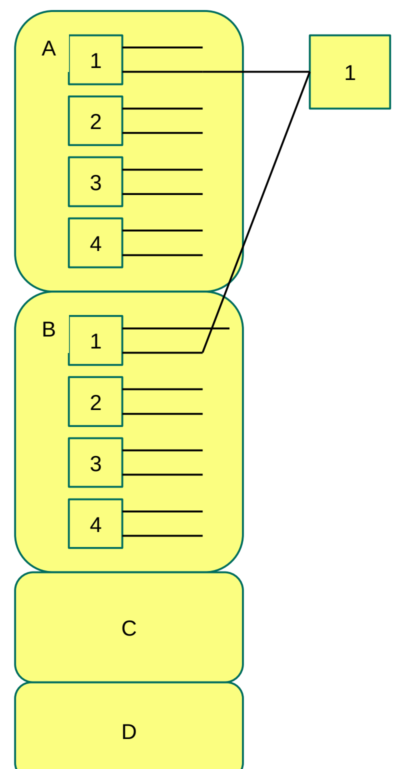
Layout of Pixel

Pixel position encoding

- The pixel size is 50µm x 25µm. The sensor is designed to be readout with RD53 ASIC
- 16 pixels connected to 8 transmitting electrodes
  - 16 pixels are arranged into 4 groups (a b c d) and each with 4 pixels, every pixel has index (1 2 3 4)
  - 8 pads are labeled as 1,2,3,4 and A,B,C,D
- Each pixel has two outputs 1 and 2
- Group A – every output 1 connected to pad A
- Pixels with index 1 – every output 2 connected to pad 1

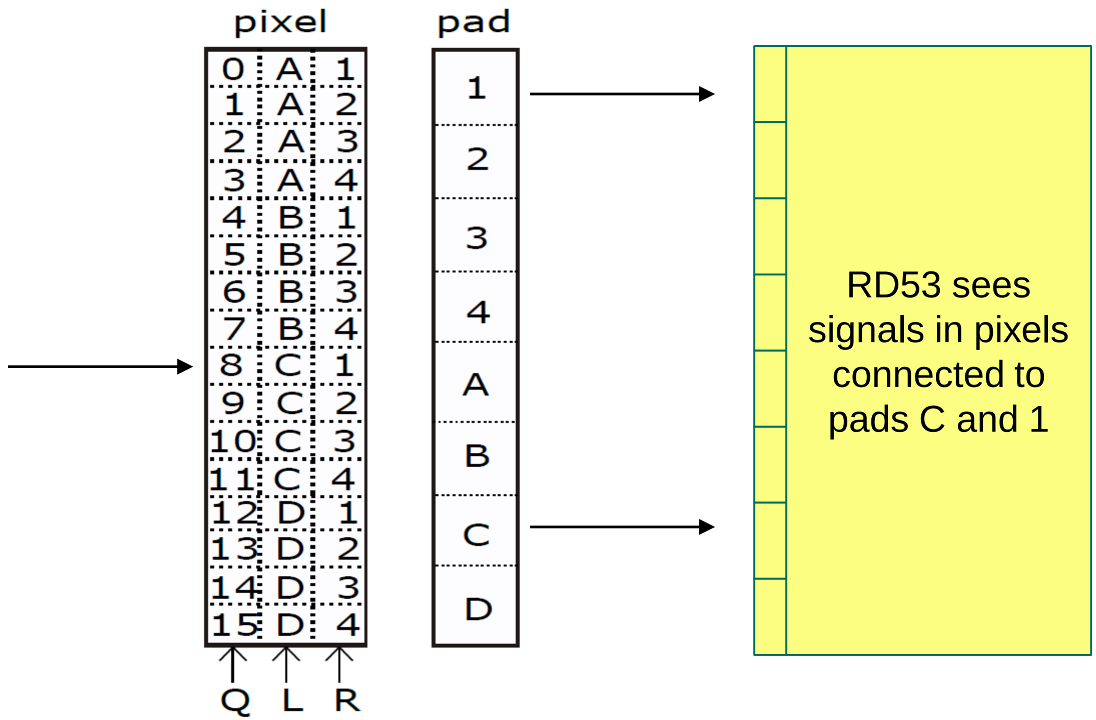




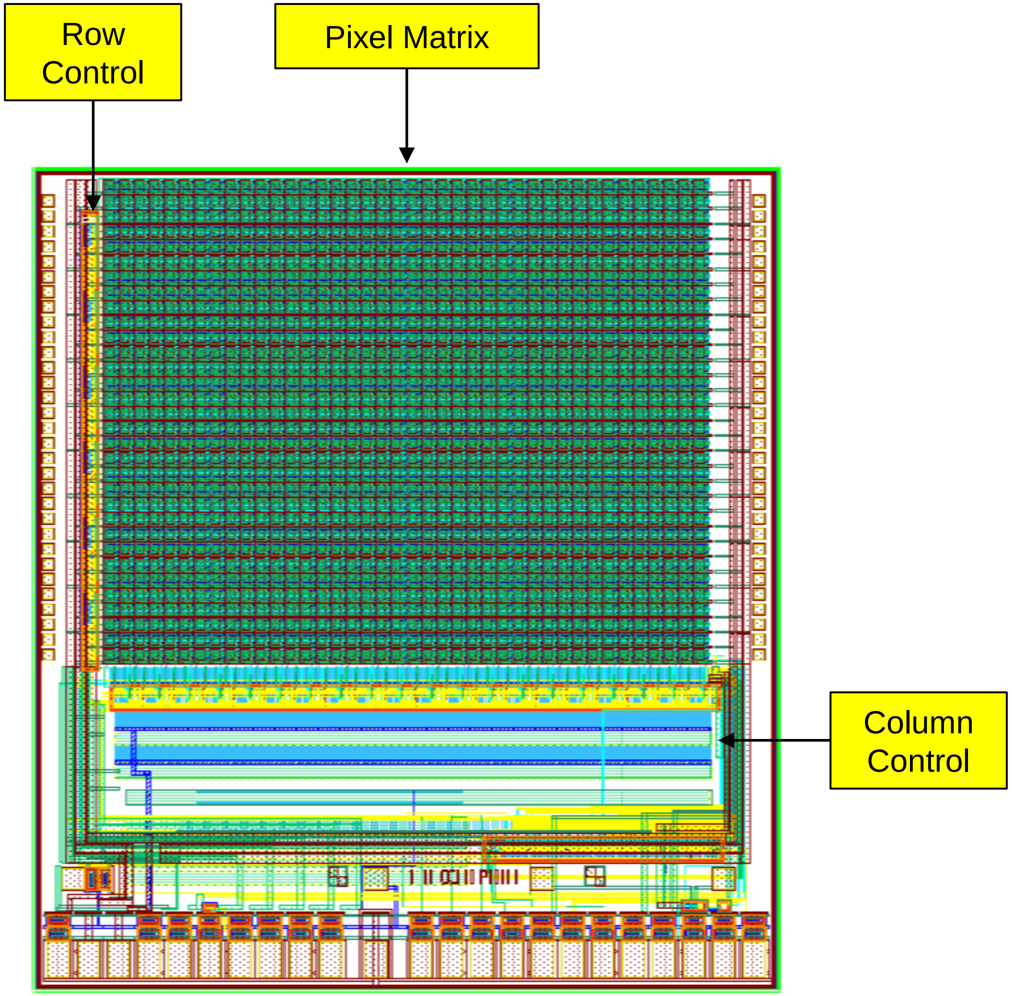


Pixel position encoding

- Assume a particle hit in pixel C 1, there will be a signal at the pad C and pad 1
- The signals have full swing of 1.8V and are easy to transmit over larger gaps between chips
- By recording two signals in the readout chip, the exact hit position can be reconstructed



The whole structure of sensor chip



Layout of sensor chip

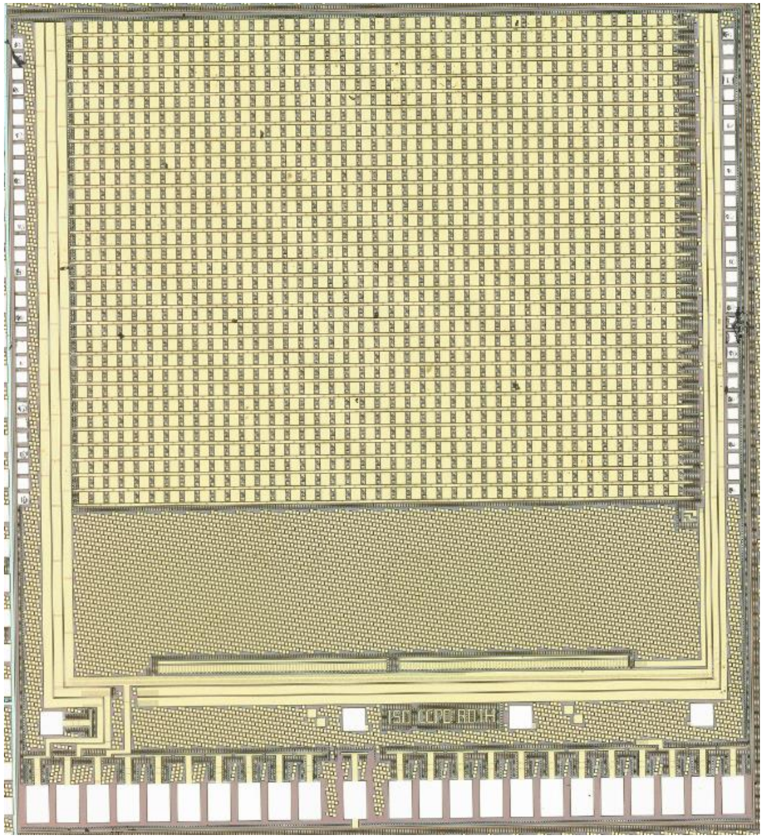
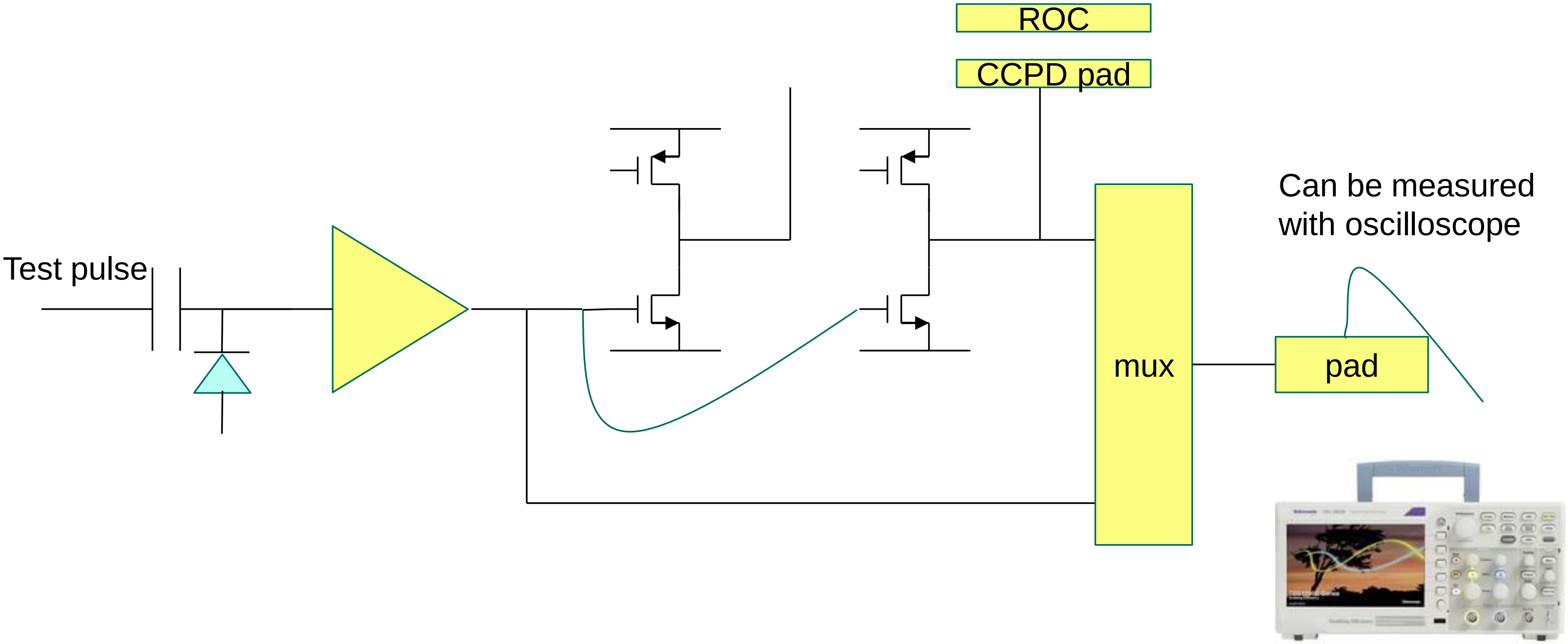


Photo of sensor chip

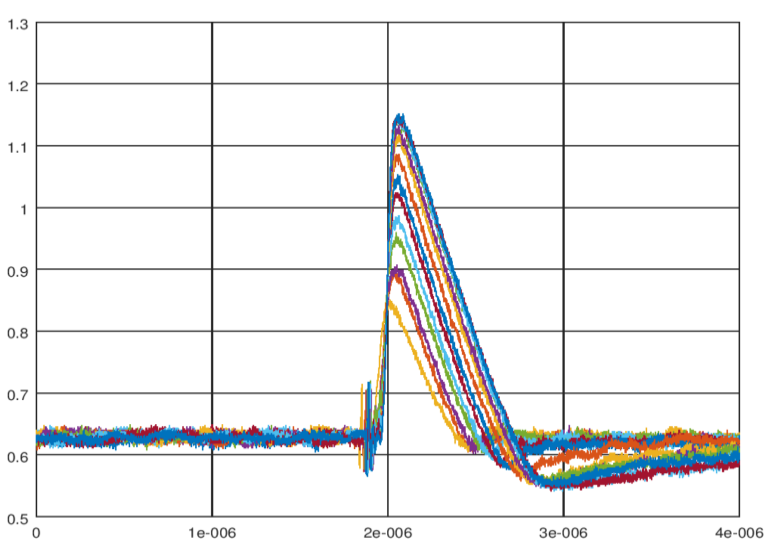
Test possibilities

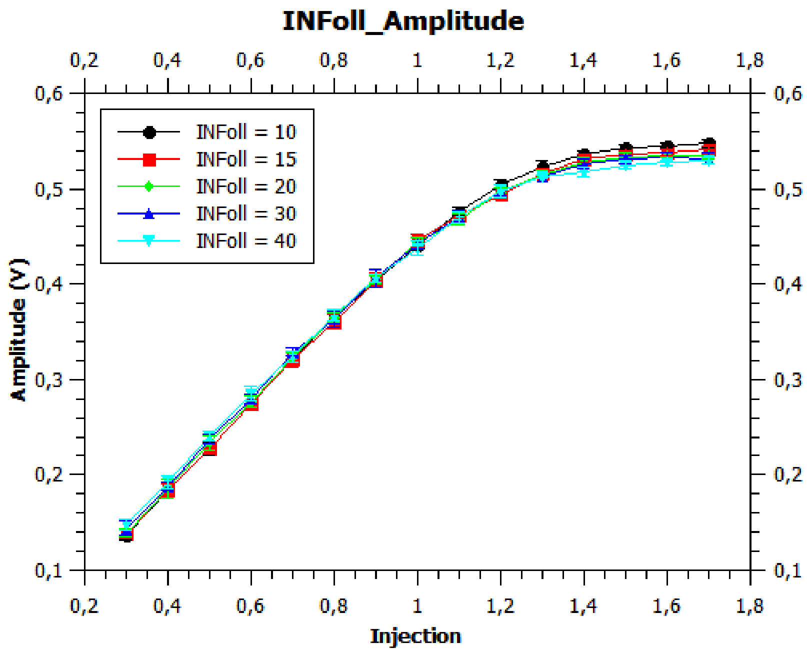
- It is possible to inject charge into a single pixel using a capacitive injection circuit. In this way the sensor can be tested using only electrical input signals
- It is also possible to measure the amplifier and pad output through a test multiplexer
- These two features allow standalone chip tests without a readout chip



- Stand alone tests (without readout chip), injection used
- Injection voltage changed from 0.3V to 1.7V
- Measured amplifier signal vs injection
- The amplitude depends on the input signal in linear way

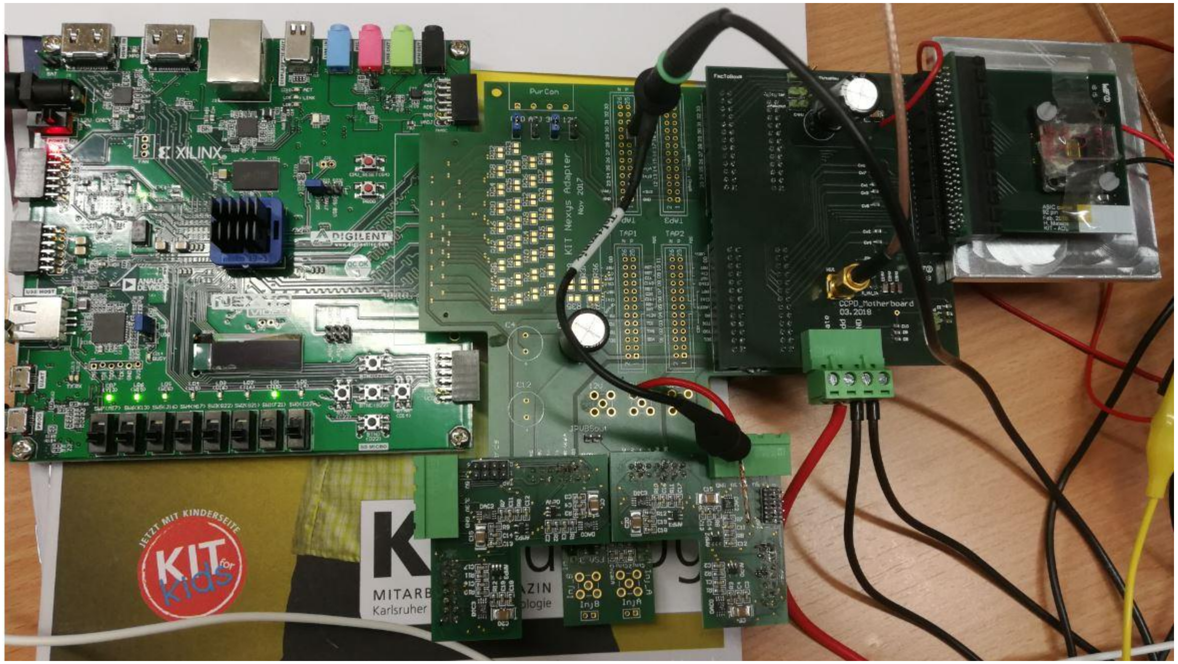
- The amplitude of the pad signal is nearly constant 1.8V. The pulse width of the comparator signal depends on the sensor input
- ToT, SNR, rise time



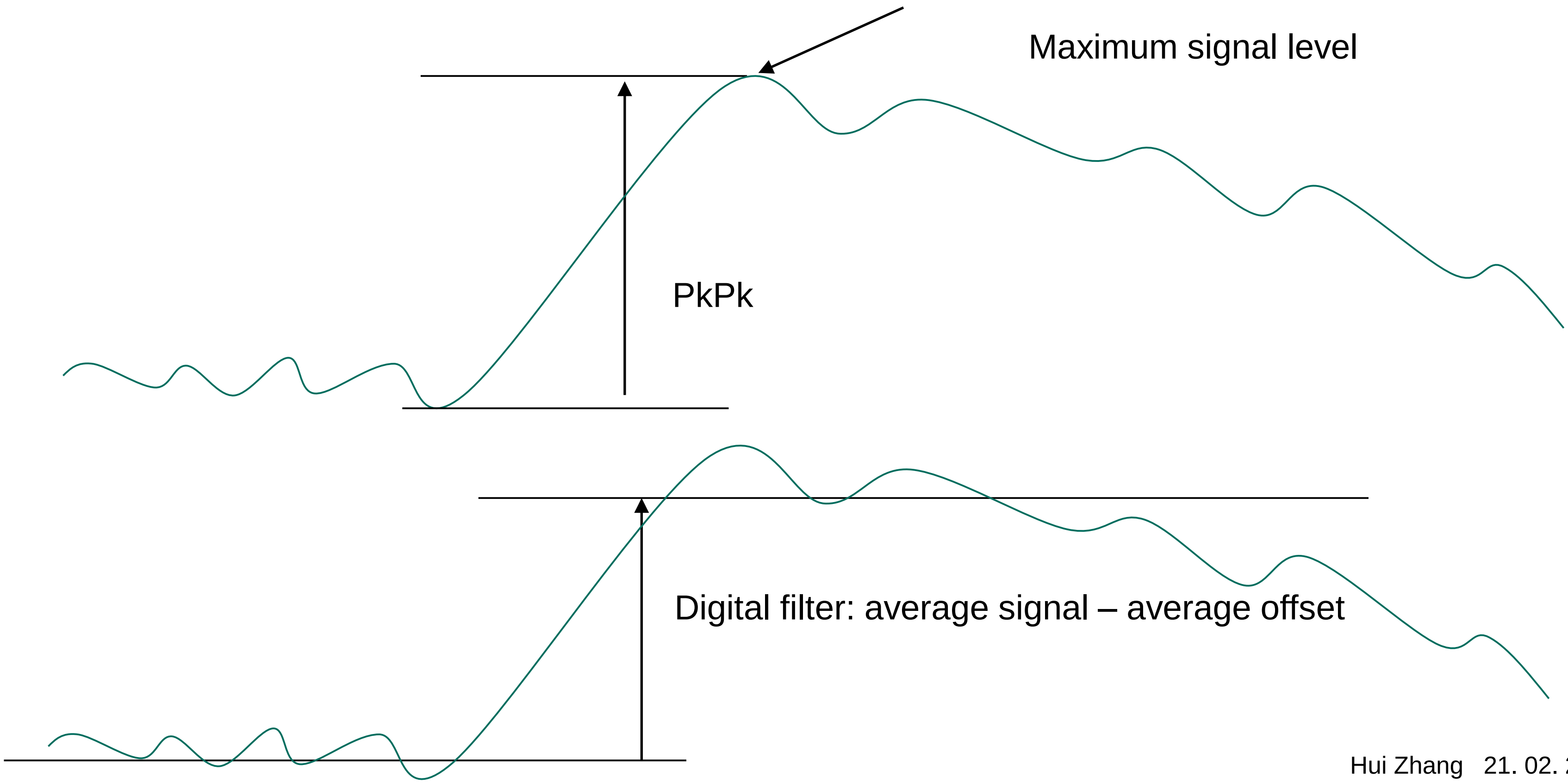


Source measurements

- We have irradiated the senor with Fe55 radioactive source to calibrate amplitude, injection circuits and determine noise
- Fe55 makes photons two energies 5.9keV and 6.5keV
- Amplifier signals have been measured via the output multiplexer and recorded by scope

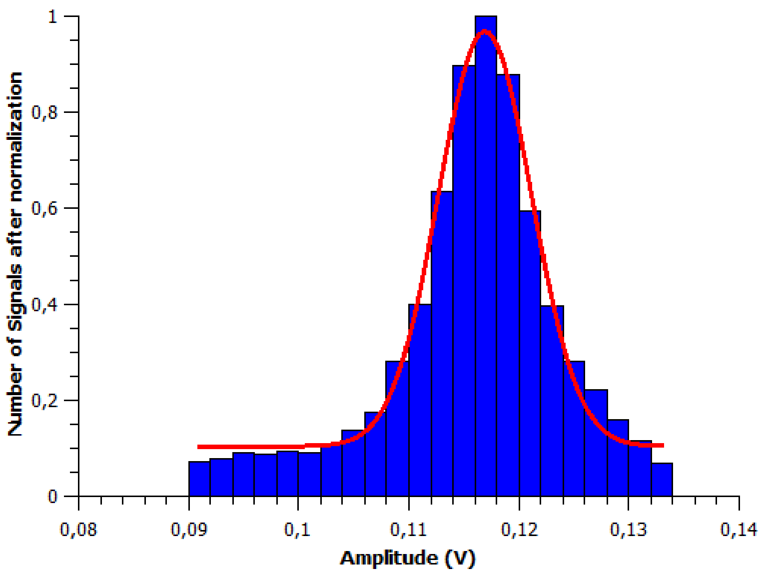


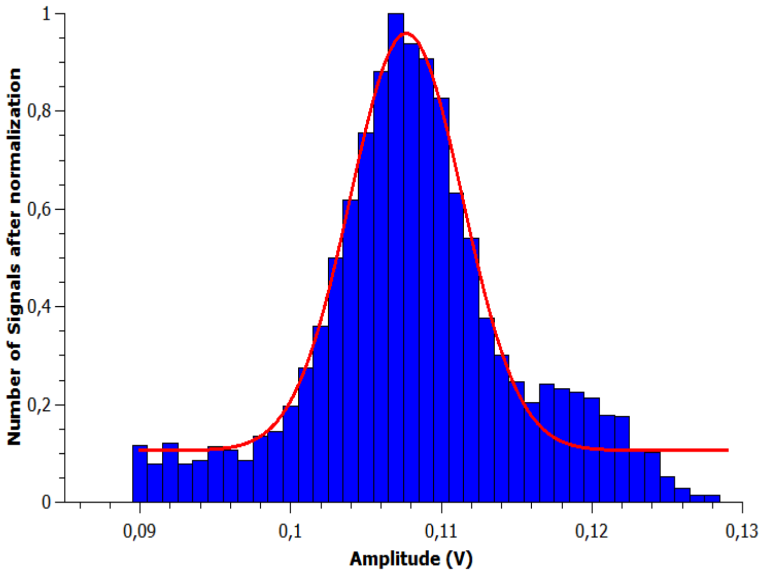
- Three methods to measure spectrum
- 1. from the maximal signal level
- 2. from peak to peak amplitude
- 3. The whole waveforms have been recorded and a Software based filter has been used to calculate the mean value of the waveform before the signal and the mean value of the waveform after the signal



Source measurements

- The third method (Software based filter) leads to the best signal to noise values
- Different methods:
  - Obtained from waveforms
  - Obtained from peak to peak method

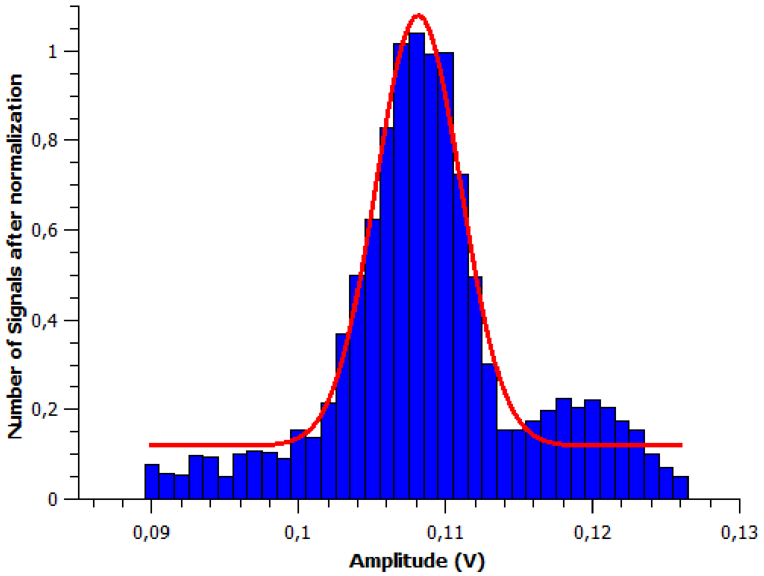




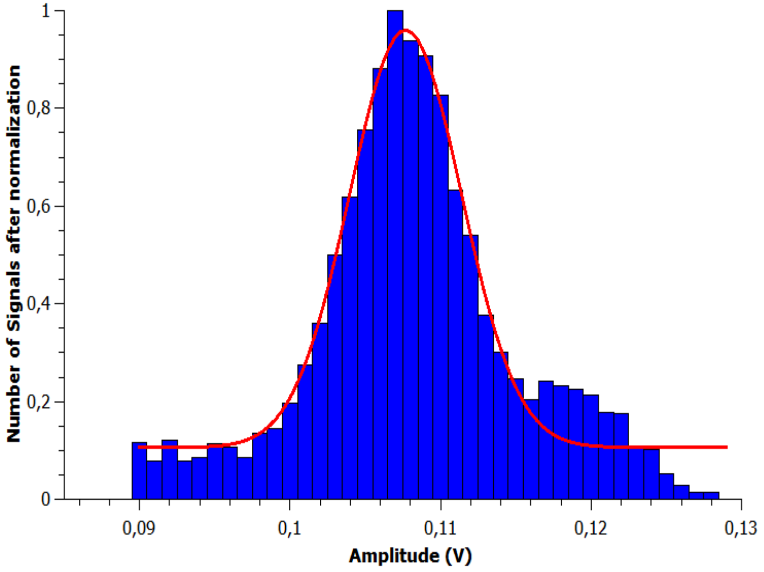
Measurement with room temperature- Fe55 spectrum
Obtained from peak to peak method
Mean value: 117mV
Sigma: 4.66mV (71e).

Measurement with room temperature - Fe55 spectrum
Obtained from waveforms - mean signal vs mean offset
Mean value: 107mV
Sigma: 3.69mV (57e)

- The noise of 43e has been measured from the Fe55 at the sensor temperature of about -10 °C
- Under different temperatures
  - Room temperature
  - Peltier cooler



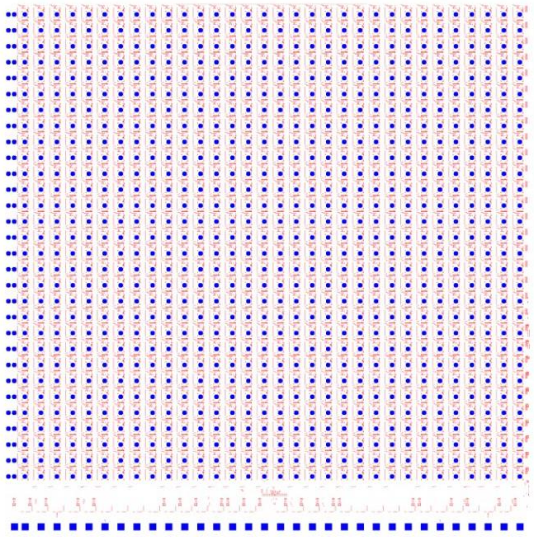
Measurement with Peltier cooler- Fe55 spectrum
Obtained from waveforms - mean signal vs mean offset
Mean value: 107mV
Sigma: 2.8mV (43e)



Measurement with room temperature - Fe55 spectrum
Obtained from waveforms - mean signal vs mean offset
Mean value: 107mV
Sigma: 3.69mV (57e)

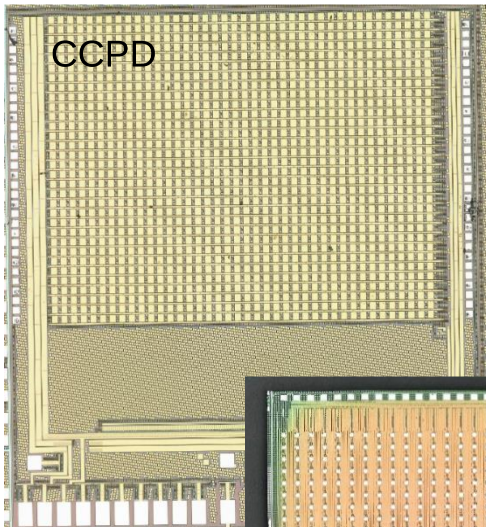
CCPD with a readout chip

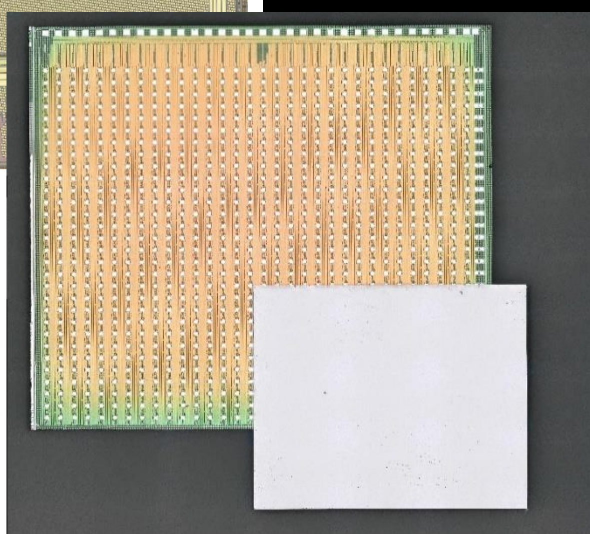
- Finally we have made a CCPD sensor bonded onto a readout chip. Since no RD53 ASICs were available we have used the readout chip PHOTON developed in our group. This chip has pixel pitch of 150µm so that only every third pixel pad can be readout
- PHOTON chip can count the signals and integrate the charge. Counting mode has been used
- The pad size for photonV2 chip is 40µm and for CCPD is 38µm*32µm.



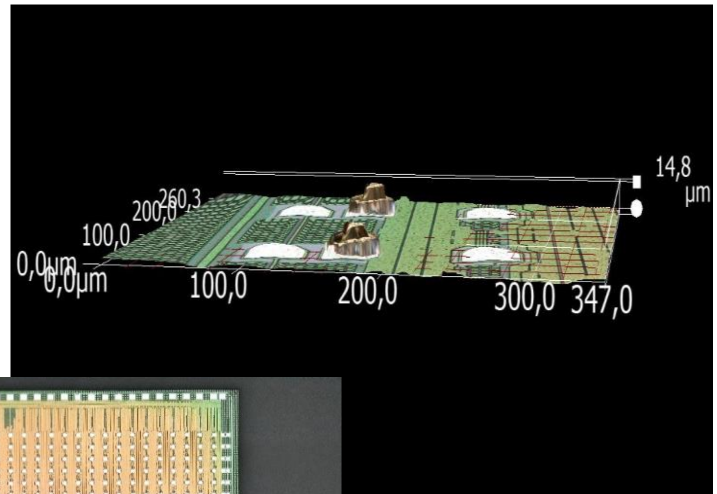
CCPD with a readout chip

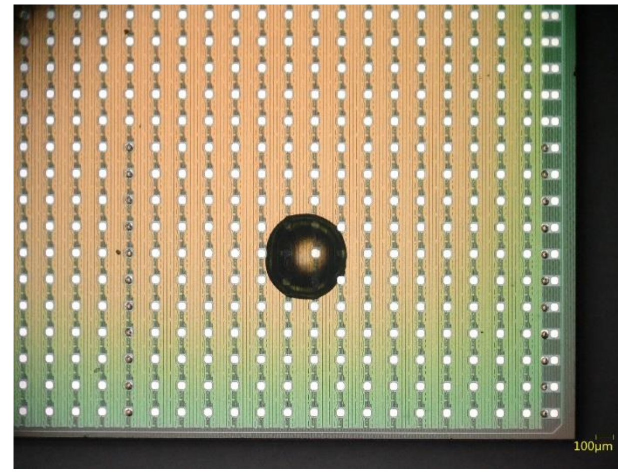
- The chips have been bonded in the following way: first gold stud bumps have been made on the PHOTON chip. Then the CCPD chips without bumps have been placed onto PHOTON chips and bonded using flip chip machine. Glue has been used
- After this procedure the gap between chips is 15µm.



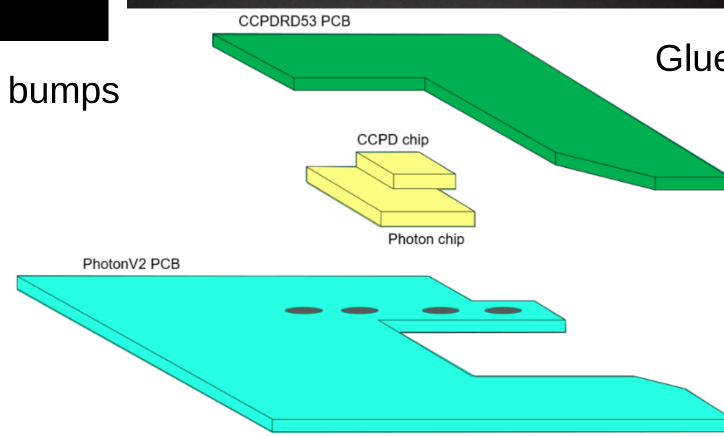


After flip chip



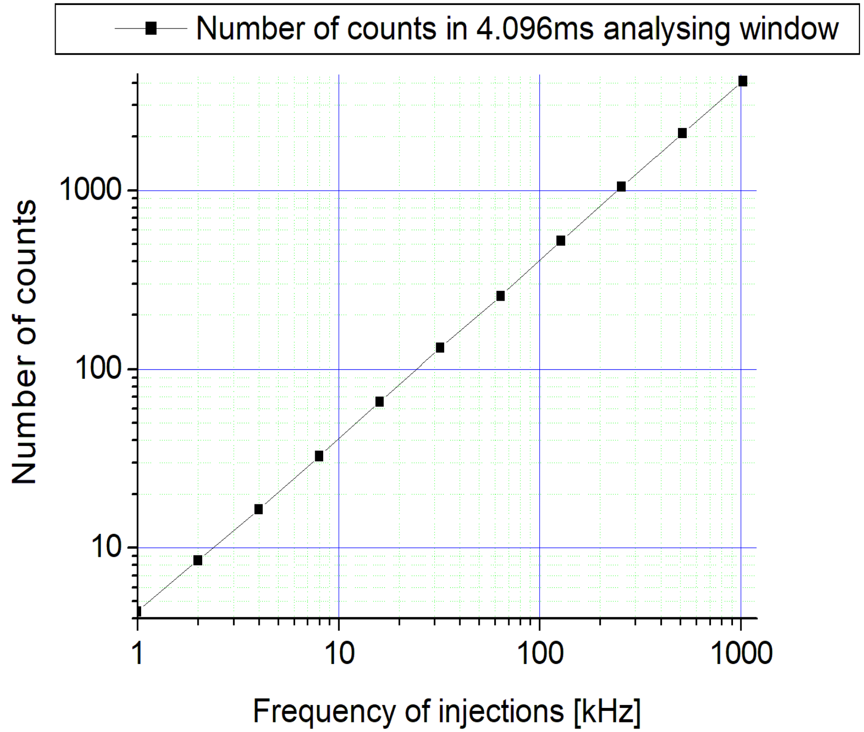


PhotonV2 with bumps



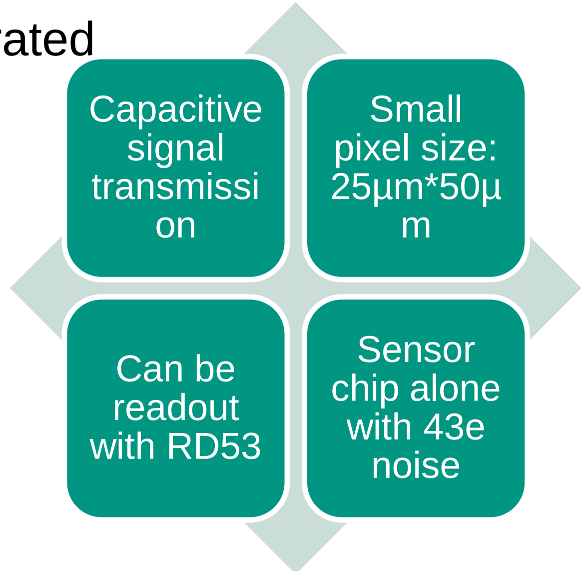
CCPD with a readout chip

- PHOTON chip is counting/integrating ASIC, it can count the signals with 13 bit pixel-counters and simultaneously measure the total signal charge. Counting mode has been used in the measurements.
- We have injected charge signals of about 6000e into CCPD with different frequencies between 1kHz to 1MHz and read out the pixel counters of PHOTON chip. The counting time was 4ms per measurements. PHOTON chip could correctly count the signals in this frequency range with small error.



Summary

- We have designed a pixel sensor chip with 25µm x 50µm pixels
- Pixel signals are multiplexed to pads of 50µm x 50µm size
- The sensor can be readout with standard ASIC for ATLAS and CMS upgrade RD53
- The sensor chip has been implemented in a HVCMOS technology on a high resistivity wafer and with deep p-well option
- Digital signals of large amplitudes (1.8) are transmitted over larger gaps and use of bumps for power transmission
- The sensor is functional, has low noise
- Readout with a PHOTON chip has been demonstrated



- Thank all that contributed to this project, especially Felix Ehrler and Rudolf Schimassek

- Radiation hard: ionizing 1GRad, and noionizing damage is more than $5*10^{15}$ neq/cm^2