The ATLAS Pixel Detector at the Large Hadron Collider: Operational Experience and Performance

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universitätbonn

Overview

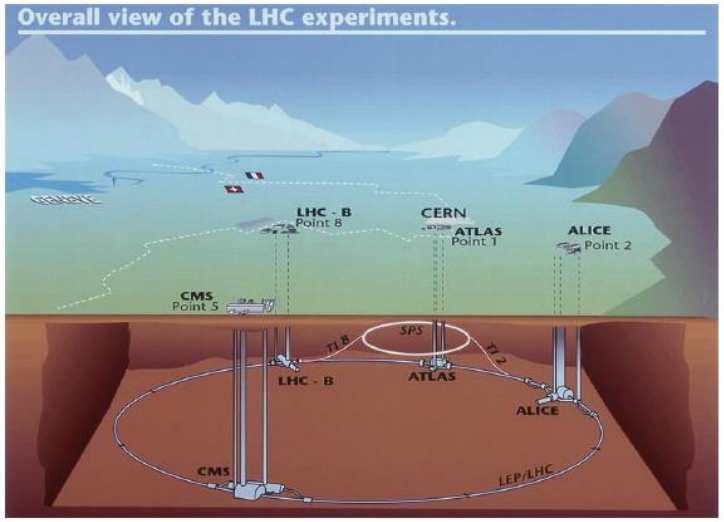
- Introduction
  - *LHC and ATLAS*
  - *Pixel and IBL*
- Operations and Performance
  - *End of Run 2 + Considerations for Run 3*
- Summary and Outlook

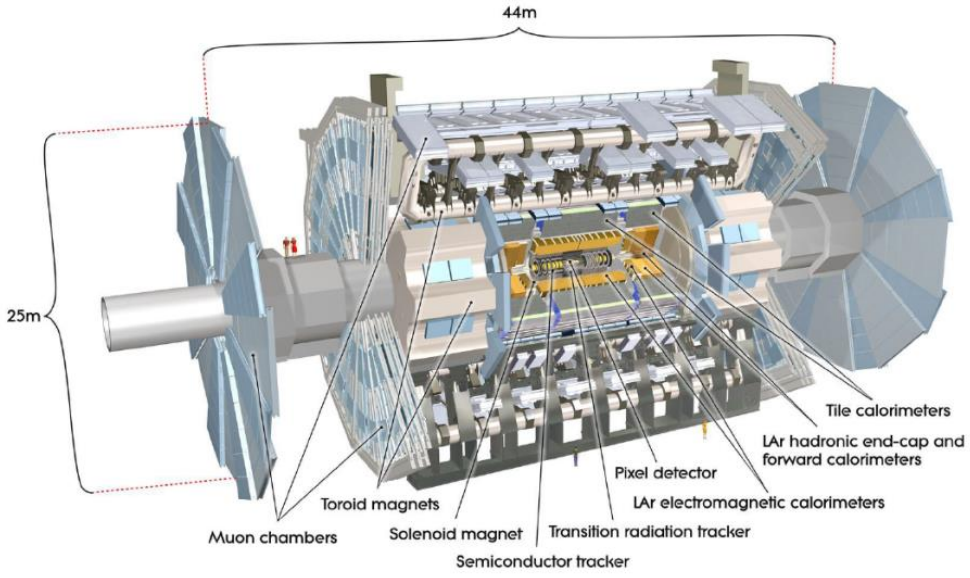
LHC – Large Hadron Collider

design vs. 2018 conditions

- 7 TeV nominal beam energy (6.5 TeV)
- 1 x 10^{34} cm^{-2} s^{-1} nominal luminosity (> 2 x 10^{34} cm^{-2} s^{-1})
- 2808 proton bunches per beam (2544b)
- 25 ns bunch spacing/40 Mhz

- First Long Shutdown (LS1) 2013/14 with repairs and upgrades to the accelerator and the experiments
- Second Long Shutdown has just started…





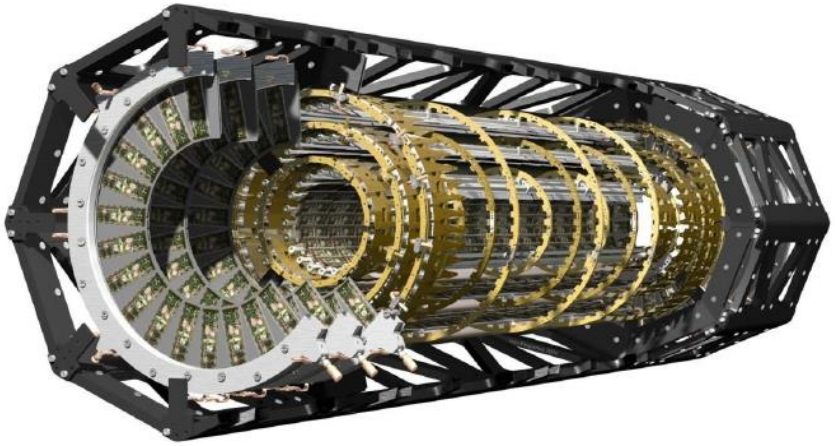
ATLAS

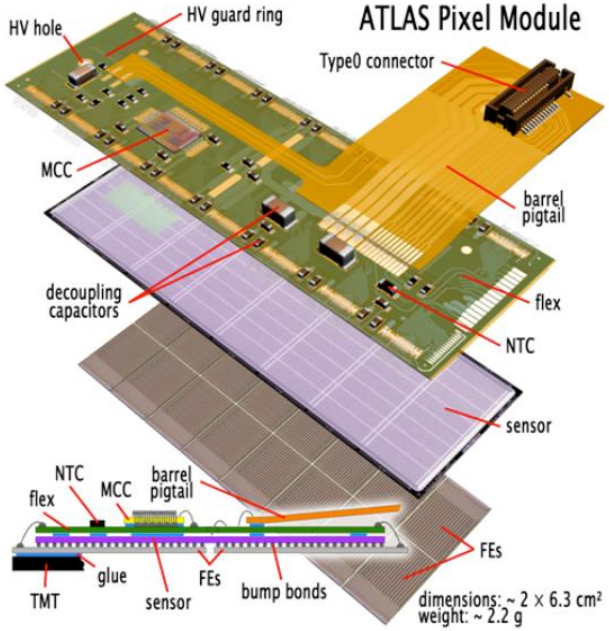
Multi-purpose detector designed to

- Investigate the TeV scale
- Search for the Higgs boson
- Search beyond the standard model
- Make precision measurements of the Standard Model

The ATLAS Pixel Detector – before LS1

- 3 hit-system for $|\eta| < 2.5$
  - 3 barrel layers
  - 3 disks per end-cap
- Resolution in r-ϕ < 15 µm
- 1744 modules, 80M readout channels
- Innermost barrel layer at 50.5 mm
- Radiation tolerance 500 kGy / 10^{15} 1MeV neq cm^{-2}
- Evaporative C_3F_8 cooling





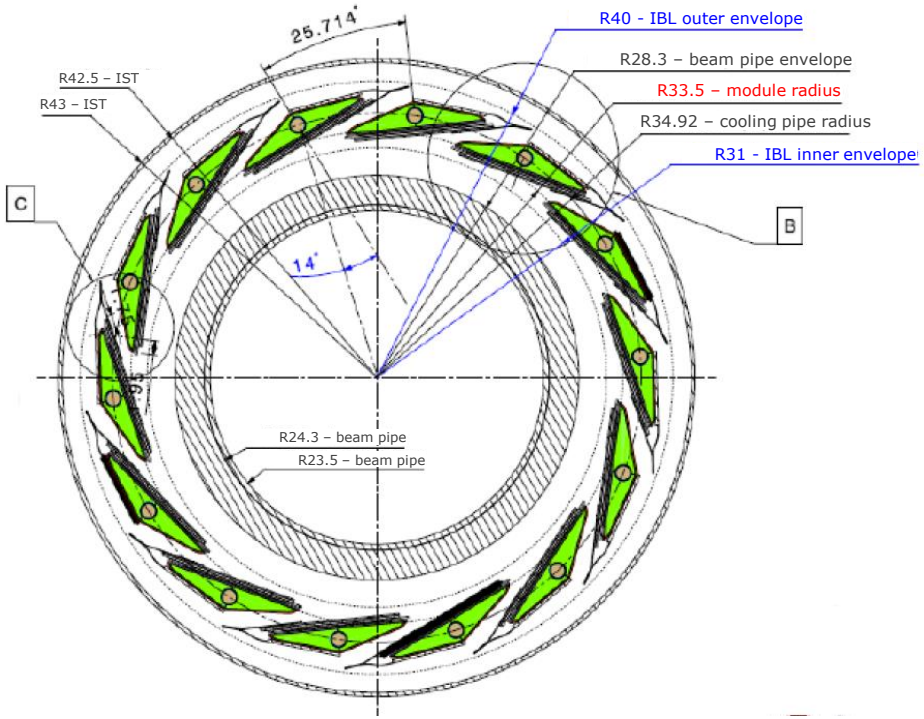
Sensor

- 250 µm thick n-on-n sensor
- 47,232 (328 x 144) pixels
- Typical pixel size 50 x 400 μm^2

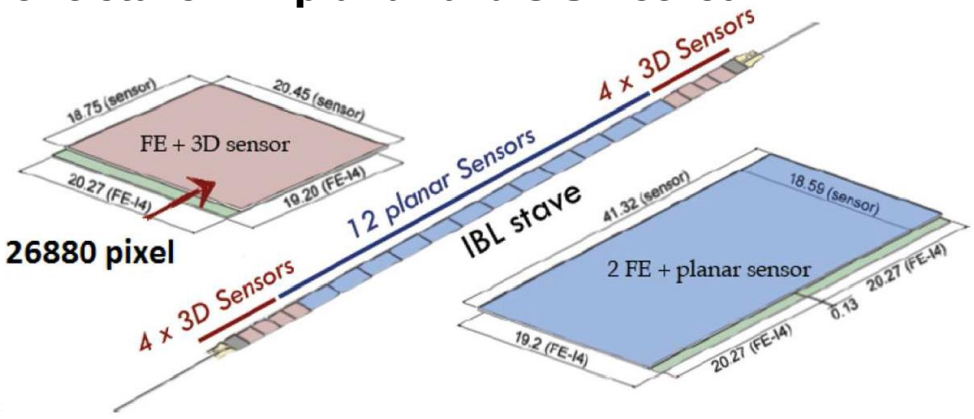
Readout

- 16 FE chips in 250 nm CMOS technology (FEI3)
- 8 bit time-over-threshold, zero suppression in the FE chip, MCC builds module event
- Data transfer 40 – 160 Mb/s depending on layer

IBL: Insertable B-Layer



One stave: **12 planar** and **8 3D** sensor



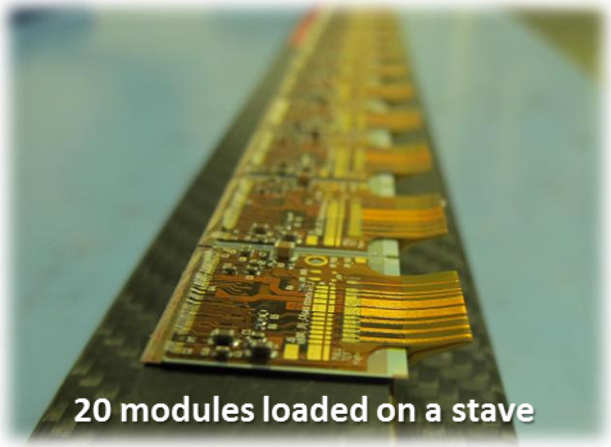
IBL a new innermost layer installed in LS1:

- With a new reduced beam pipe radius
- 14 staves inside a ***10mm*** radius envelope
- New detector: sensor, FE, readout, cooling

Why?

- B-layer aging was anticipated
- Improvement of the tracking performance with a unique 4-Layer Pixel Detector

IBL



20 modules per stave

Sensors:

Planar:

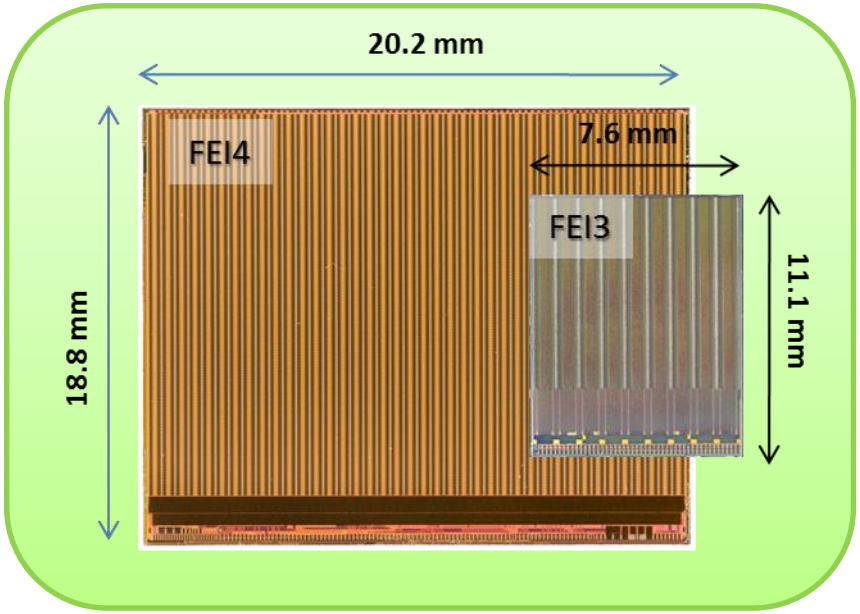
- Used in the central part of IBL
- n-on-n, 200 µm thickness.
- Slim edge technology.
- 2 frontends per sensor.

3D:

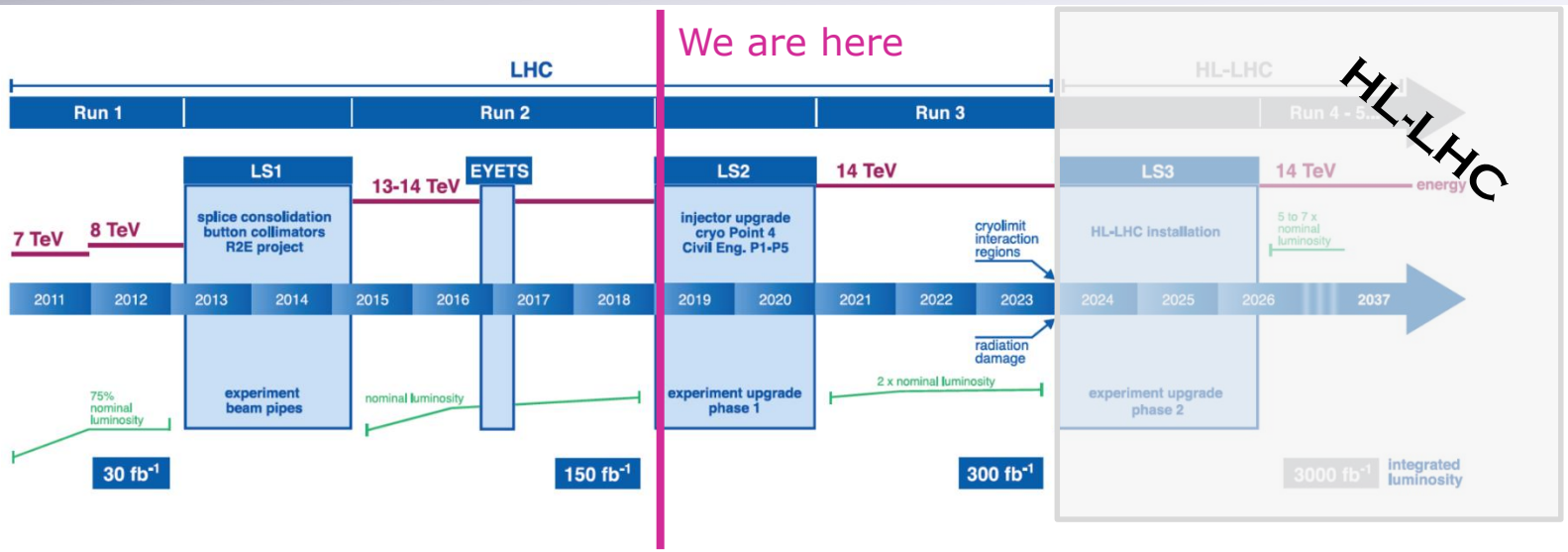
- Used in the outer parts of IBL
- 230 µm thickness.
- 2 columns per pixel.
- 1 frontend per sensor.

- CO_2 evaporative cooling.
- Radiation hard up to 5 x 10^{15} n_{eq}/cm^2

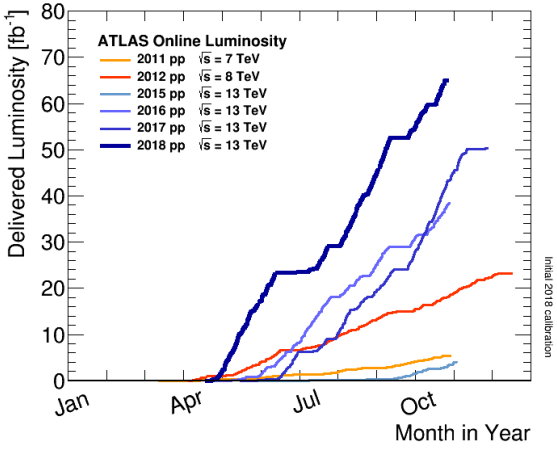
- 448 frontend chips (FEI4)
- 130 nm CMOS
- 26,880 pixels per frontend
- 336 rows (phi) and 80 columns (z)
- 2 cm x 1.9 cm in size
- 4-bit time-over-threshold information



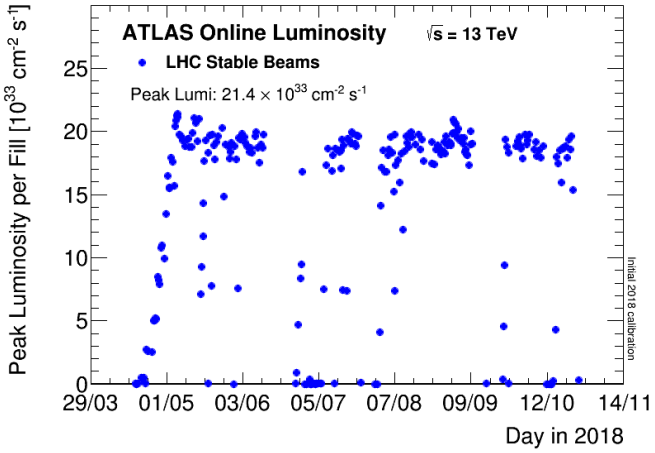
LHC Run 2



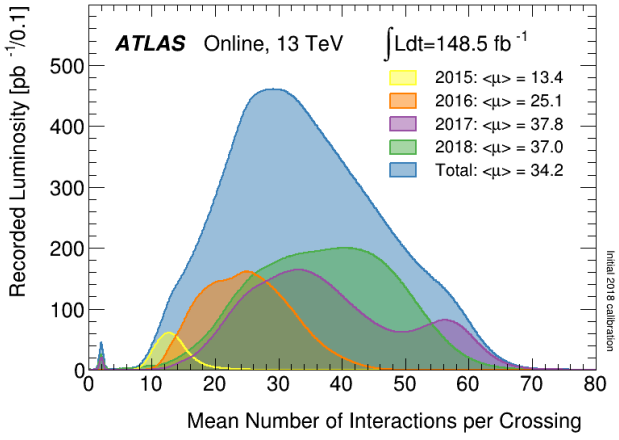
158 fb^{-1} in Run 2,
65 fb^{-1} in 2018



Peak Lumi 2018:
~2 x 10^{34} $cm^{-2}s^{-1}$



Peak Pile-up ~ 60
Average (Run 2) ~ 34



Operations Overview 2018

- More than 10 years after its first installation in ATLAS and at twice the LHC design luminosity, the Pixel Detector is still operating exceptionally well.
- The ATLAS deadtime caused by each Pixel and IBL has been reduced to less than 0.2% during 2018.
- The DQ efficiency has been 99.8% for 2018 p-p data taking.
- 4.3% of the modules were not operated in 2018. Some of those can be recovered.

ATLAS pp data: April 25-October 24 2018

Inner Tracker			Calorimeters		Muon Spectrometer				Magnets	
Pixel	SCT	TRT	LAr	Tile	MDT	RPC	CSC	TGC	Solenoid	Toroid
99.8	99.8	100	99.7	100	99.8	99.7	100	100	100	99.6

Good for physics: 97.5% (60.1 fb^{-1})

Luminosity weighted relative detector uptime and good data quality efficiencies (in %) during stable beam in pp collisions at $\sqrt{s}$=13 TeV between April 25 – October 24 2018, corresponding to a delivered integrated luminosity of 63.8 fb^{-1} and a recorded integrated luminosity of 61.7 fb^{-1}. Dedicated luminosity calibration activities during LHC fills used 0.7% of recorded data and are included in the inefficiency. The luminosity includes 193 pb^{-1} of good data taken at an average pileup of μ=2.

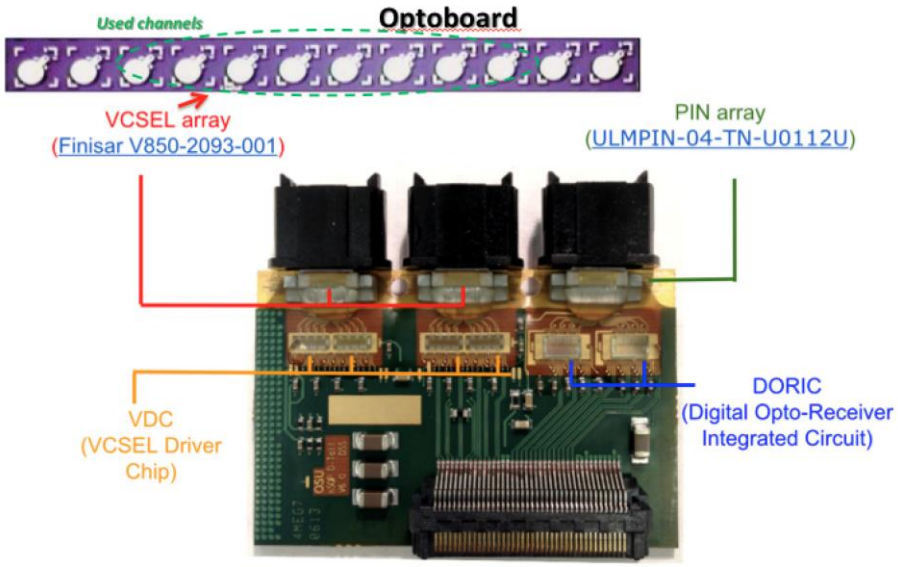
Disabled Modules

Layer	Failures/Total	Percentage
Disks	15/288	5.2
B-Layer	17/286	5.9
Layer 1	28/494	5.7
Layer 2	31/676	4.6
Total (Pixel)	91/1744	5.2
IBL	3/448	0.7
Total	**94/2192**	**4.3**

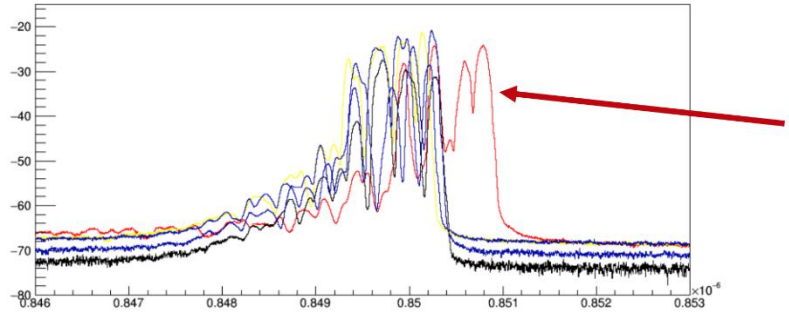
Run 2 commissioning Report: VCI 2016

Optoboard Failures

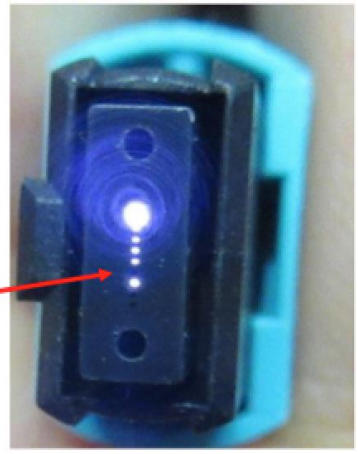
- Dominant hardware issue in Run 2 is a high failure rate of the VCSELs used for data transmission on the detector.
- The failure rate increased dramatically about 2 years after installation of the optoboards.
- The cause of the failures is not known.
  - possibly humidity or thermal cycling of VCSELs during operation due to non-DC-balanced data transmission.
- ~30 boards were replaced before the start of 2018 data taking.
- 19 new channels died in 2018.



ALL 272 Optoboards will be replaced in 2020 before the start of Run 3

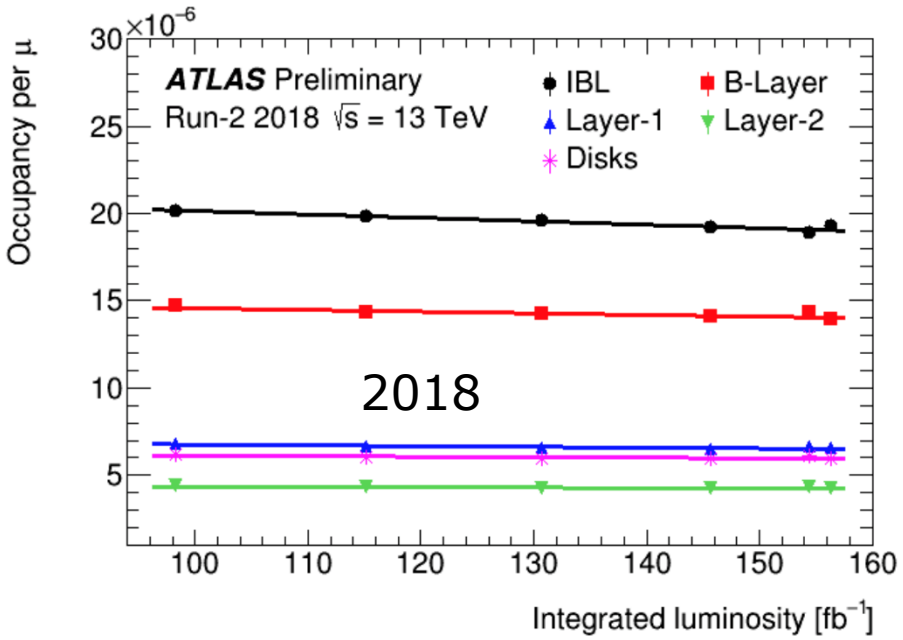


Shifted spectrum is a predictor for death long before failure.



VCSEL light from data fiber

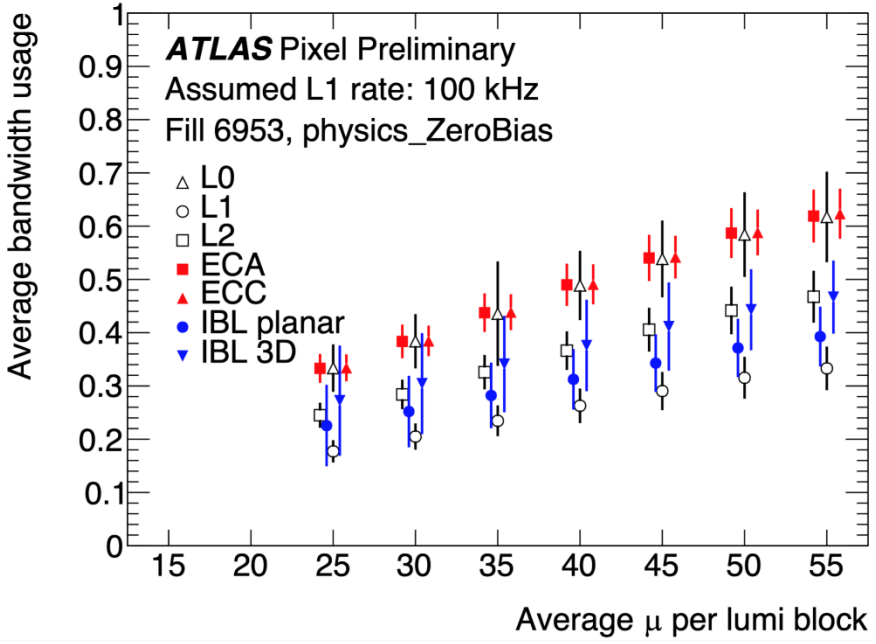
Thresholds and Bandwidth



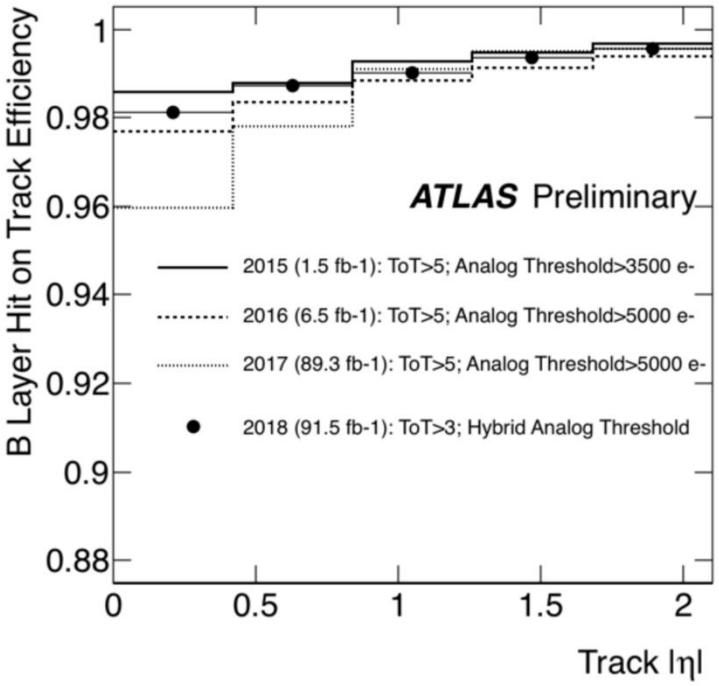
Threshold	2017	2018
IBL	2500e, ToT>0	**2000e**, ToT>0
B-layer	5000e, ToT>5	**4300e(*), ToT>3**
Layer-1	3500e, ToT>5	3500e, ToT>5
Layer-2	3500e, ToT>5	3500e, ToT>5
Endcap	4500e, ToT>5	**3500e**, ToT>5

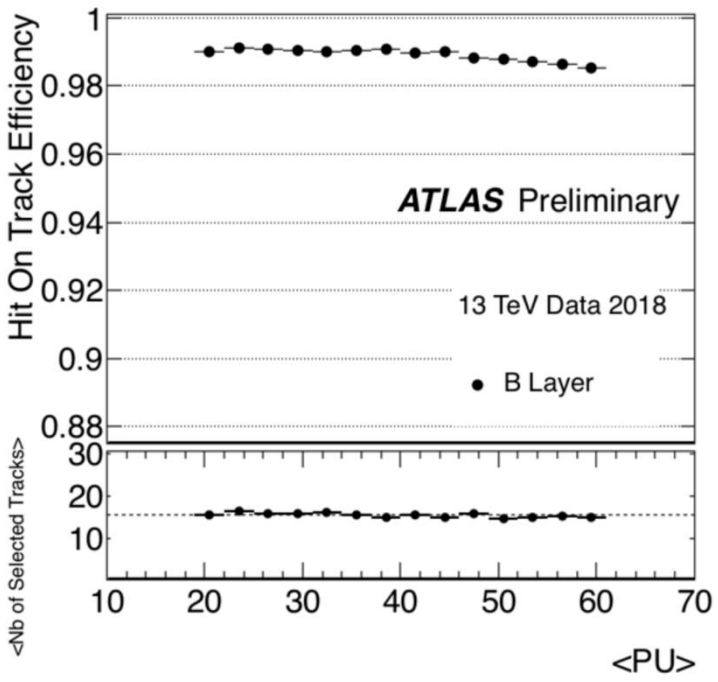
(*) M1A/M0/M1C : 4300e, otherwise : 5000e

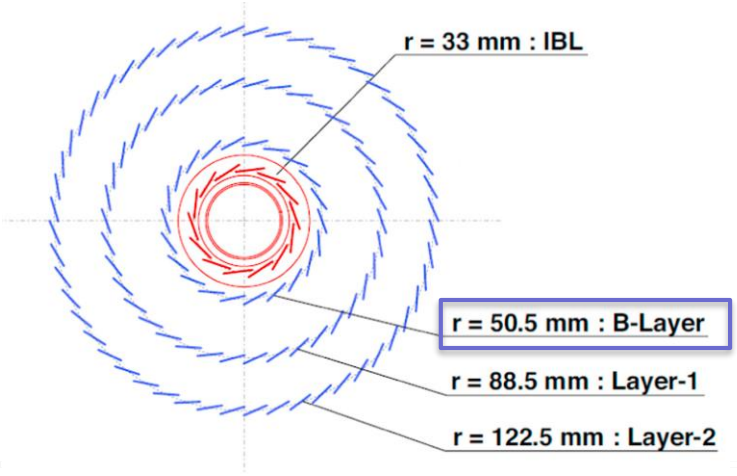
- To ensure a stable readout, bandwidth usage is required to stay below 80 % at 100 kHz trigger rate and a pile-up of 60. B-Layer and Disk thresholds had to be increased in 2016 and 17 respectively.
- Occupancy decreases due to radiation damage.
- To optimize efficiency, the thresholds were lowered again at the beginning of 2018.
- Typical values at the start of run in 2018 were a pile-up of 55 and a trigger rate of 83 kHz.



Efficiency



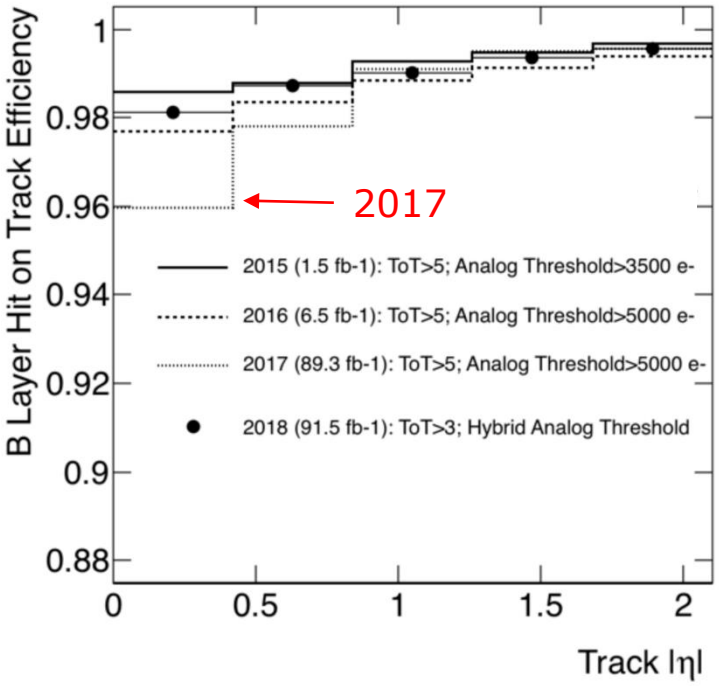


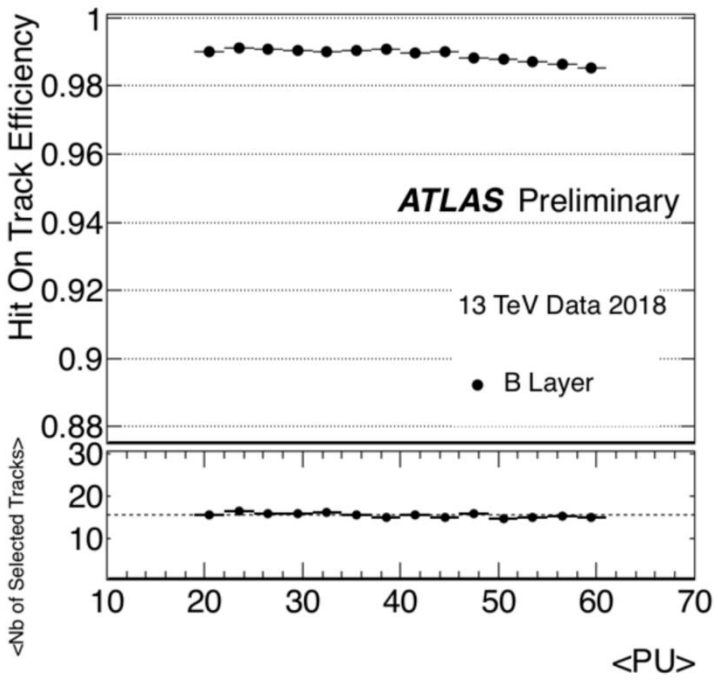


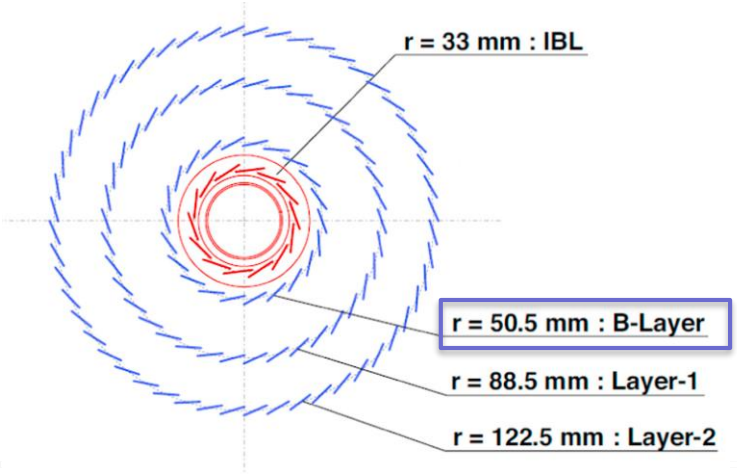
- The B-layer has the highest threshold because of bandwidth considerations.
- More radiation damage than other (old) Pixel layers → decreasing occupancy
- z dependent threshold adjustment: most margin in terms of bandwidth at low |η|, most affected in terms of fluence.

- Almost full efficiency recovery after lowering thresholds!
- Good stability of efficiency at high pile-up.

Efficiency







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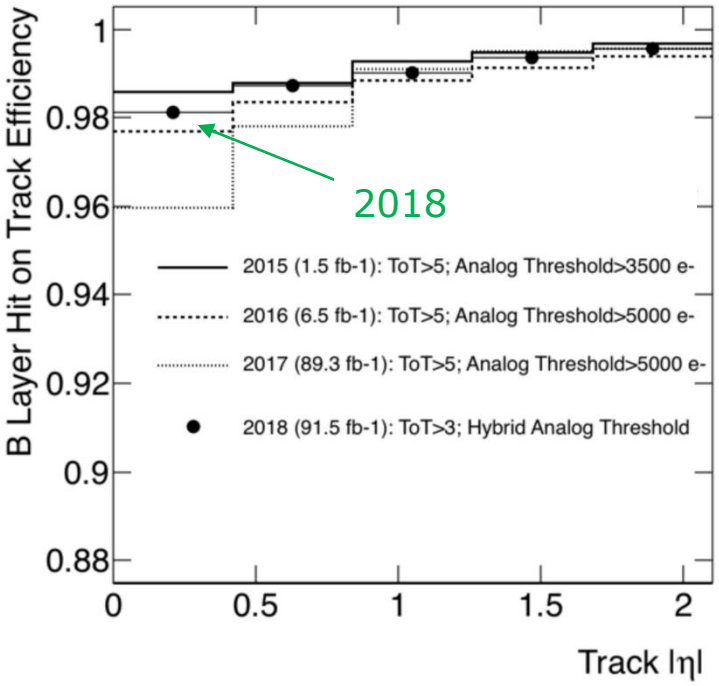

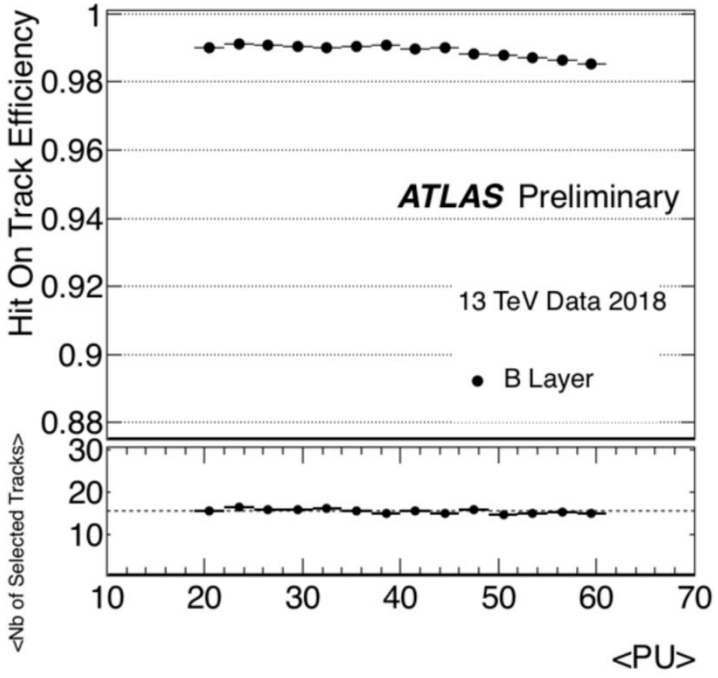

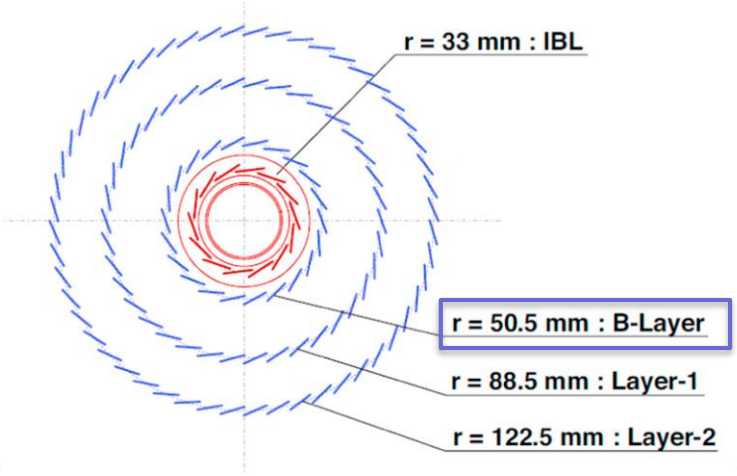

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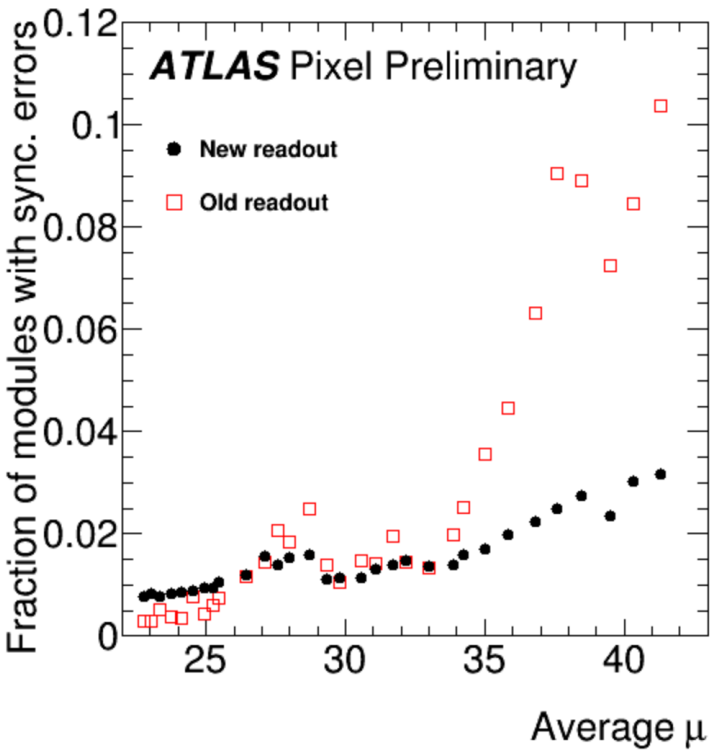
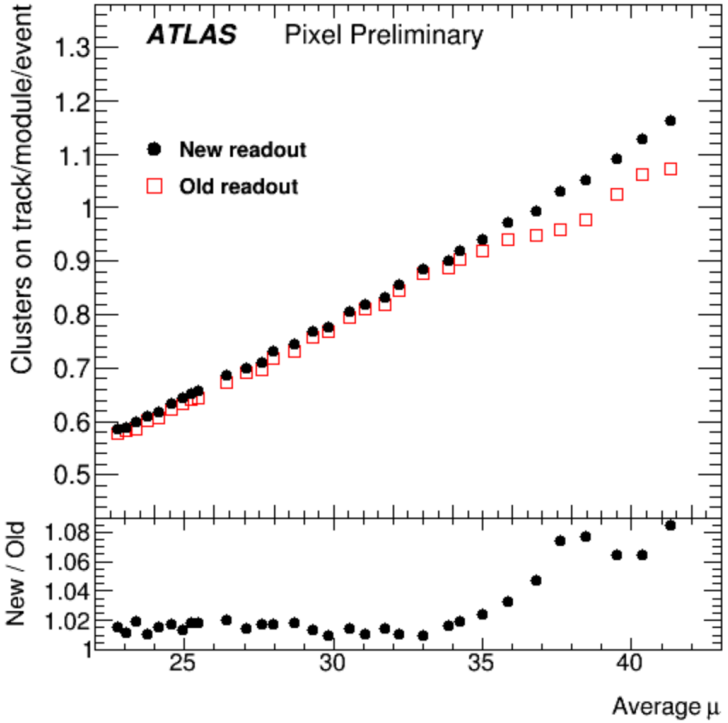
Desynchronisation





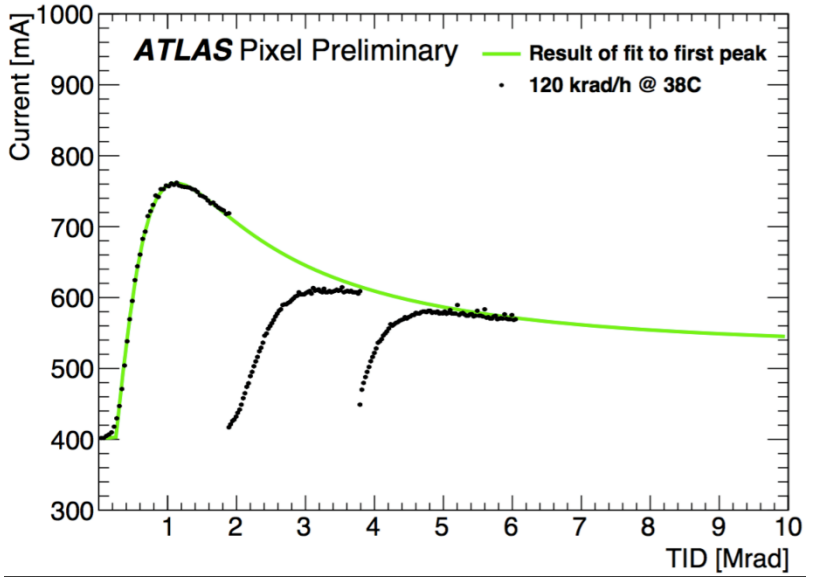
- Luminosity and pile-up are much larger than originally anticipated.
- High occupancy can lead to buffer overflows resulting in event fragments being associated with the wrong event ("desynchronization").
- Hardware upgrades in each winter shutdown from 2015 to 2017 to increase the bandwidth in Layer 2 (*) (2015), Layer 1 (2016) and Disk Layer 2 (2017). The B-Layer and remaining Disks were also upgraded in 2017 for uniformity of the readout system.
- Firmware upgrades to introduce a periodic reset of the frontend ASICs and of the backend every 5 seconds to resynchronize all data sources.

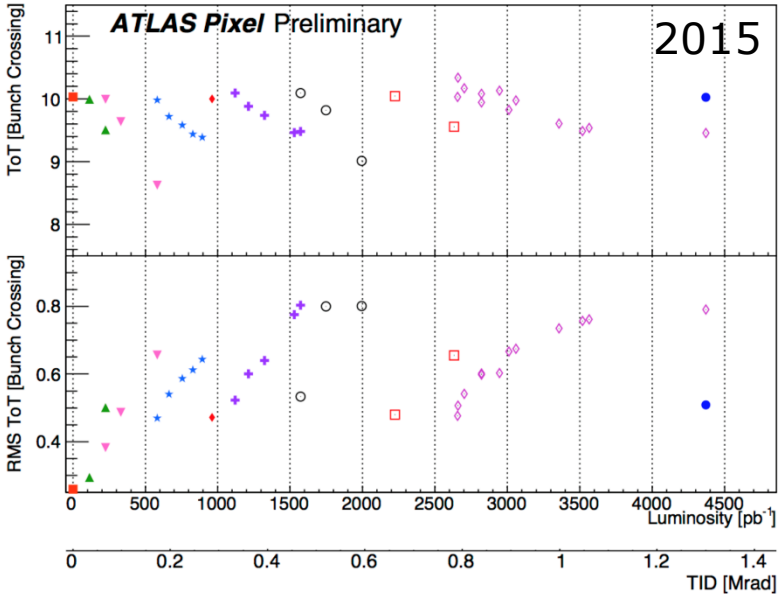
Significant improvement in Data Quality

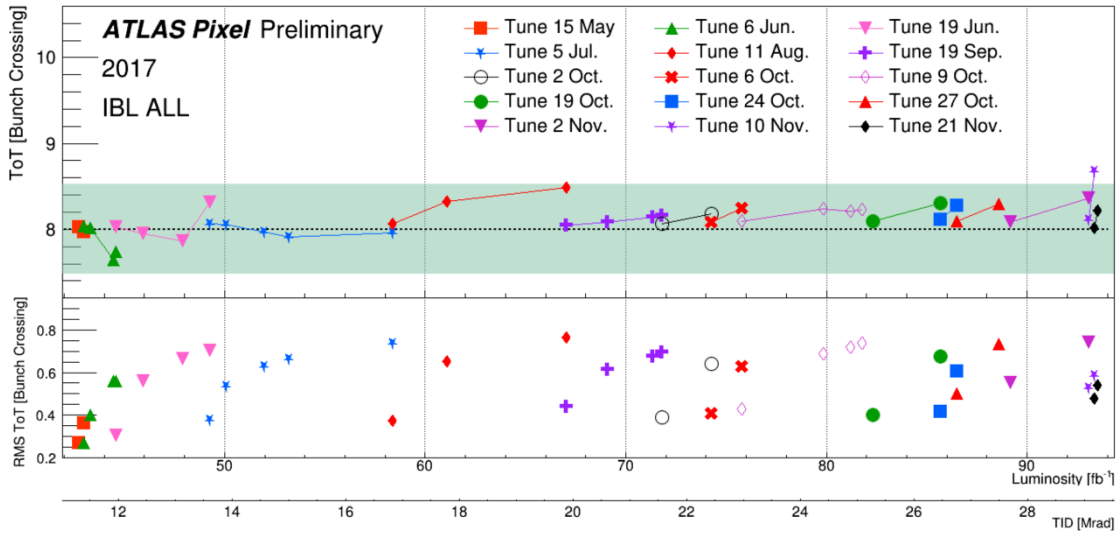
(*) A small fraction of Layer 1 was already upgraded in 2015

Calibration Drift

- The leakage currents inside the transistors of the FEI4 readout chip (130 nm IBM process) show a strong dependence on TID with a peak at 1 Mrad.
- The leakage currents have a direct impact on the tuning of feedback currents and thresholds.
- In 2015 we were on the rising edge of the TID peak. Now we are on the falling edge.
- Regular retuning of the detector (ToT and Threshold) necessary to compensate!



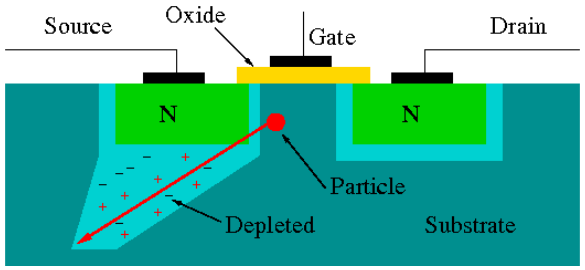


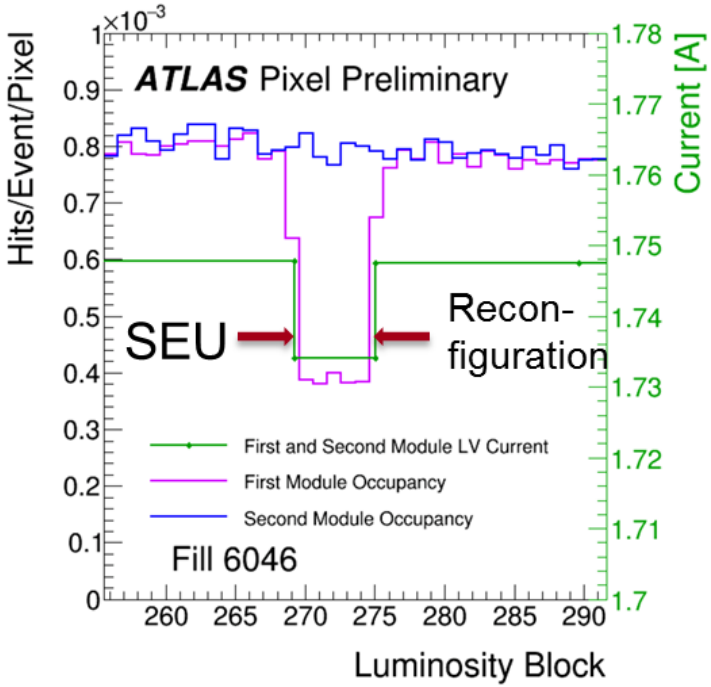


Tuning target was lowered to 8 in 2016 and 2017

Single Event Upsets

- Particles crossing the frontend chip can cause register settings to be corrupted.
- The dominant mechanism in IBL is SET (Single Event Transient): A glitch caused by single event effect travels through combinational logic and is captured into a storage element.
- The consequence of a global register being upset was first observed as a drop in occupancy with a change in current consumption. In data quality the corruption of local registers was seen as increase in noisy Pixels during a run. The observed effects are depending on the type of register affected (e.g. global FE GDAC or local Pixel TDAC register for threshold, or enable bit, …)
- As a countermeasure the *global* registers in IBL are reloaded during a 2 ms gap that is provided by ATLAS every 5 s without incurring any deadtime.
- Mitigating measures for corrupted local pixel registers are being prepared for deployment in Run 3





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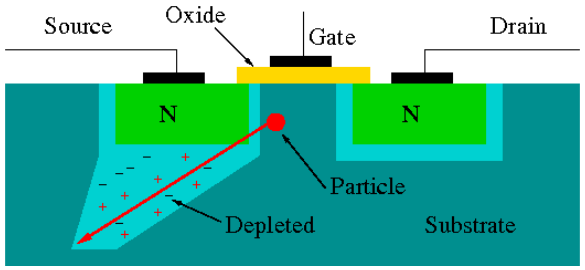
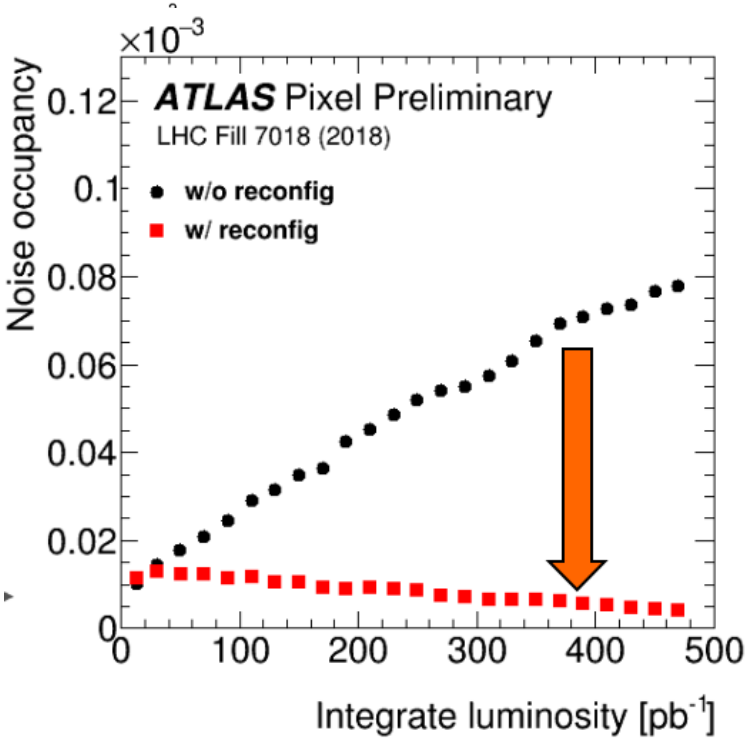
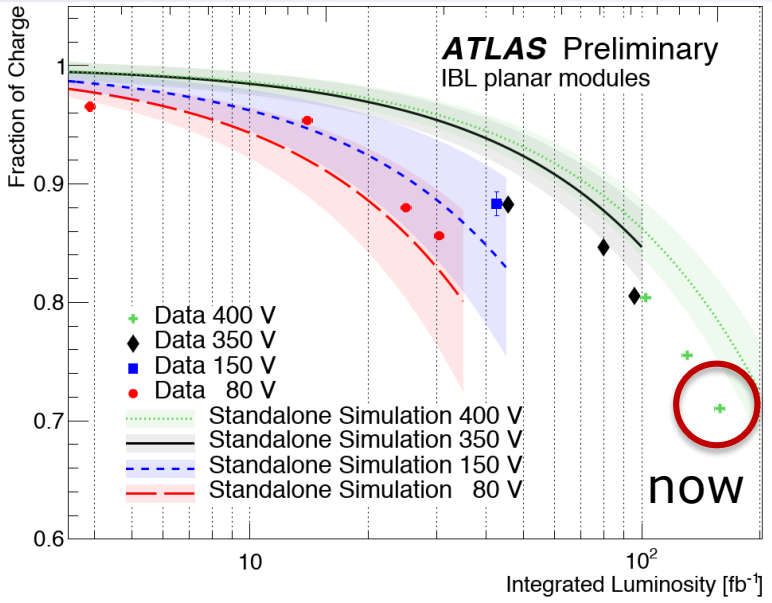
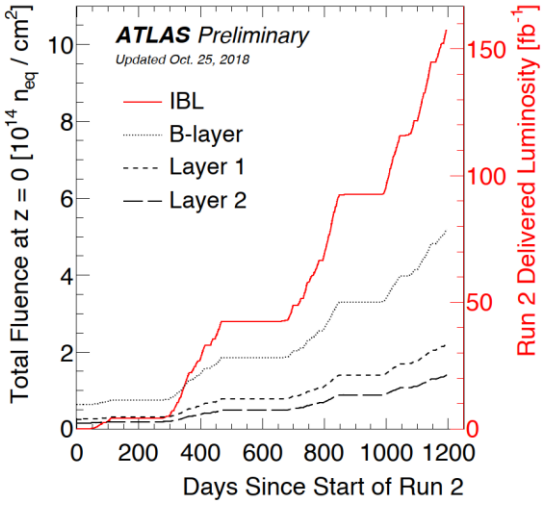




Radiation Damage

- *Radiation damage effects are getting to be significant for the performance of the detector.*
- For B-Layer, we are now around 50 % of the max. fluence. Depending on the luminosity we will see in run 3, we are at 40-50% of the total expected fluence.
- Models are used to understand and predict radiation damage effects.
- The ATLAS ***Monte Carlo*** now includes radiation damage effects.
- The operational parameters (HV, thresholds, temperature) can be adjusted to counteract the effects.



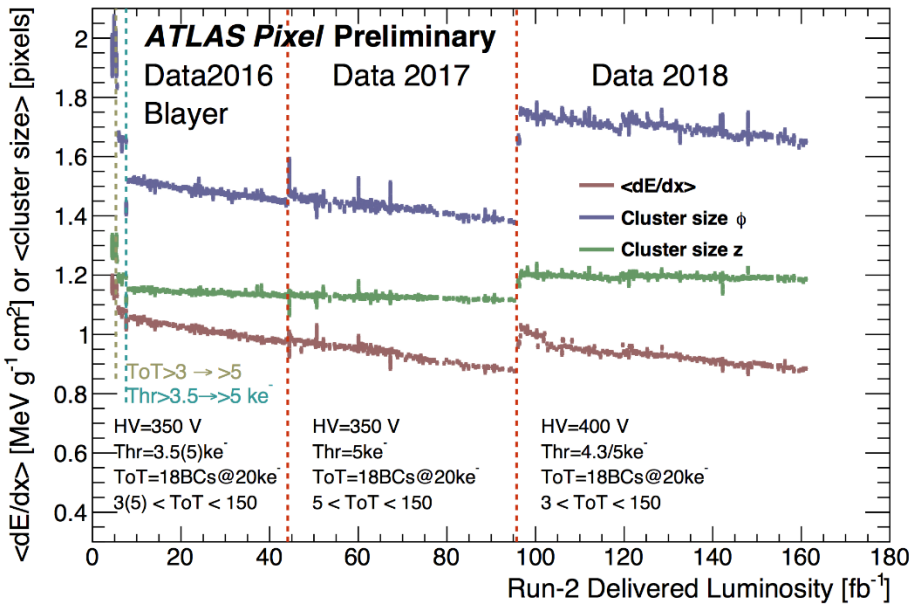


Layer	Fluence End of Run 2 [n_{eq} cm^{-2}]	max. Fluence [n_{eq} cm^{-2}]
IBL	1 x 10^{15} (at z=0)	5 x 10^{15}
B-Layer	0.5 x 10^{15} (at z=0)	1 x 10^{15}

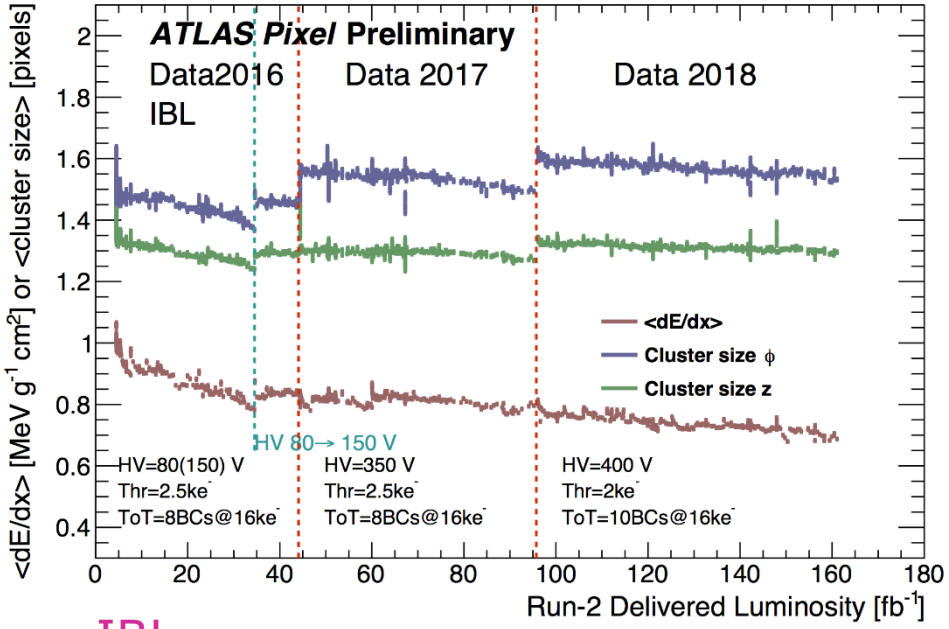
Fluence based on prediction (Pythia 8 + FLUKA). Value extracted from data higher for B-Layer.

With the DAQ consolidated during Run 2, we expect the aging of the detector to be now the main focus of Run 3.

dE/dx



B-Layer

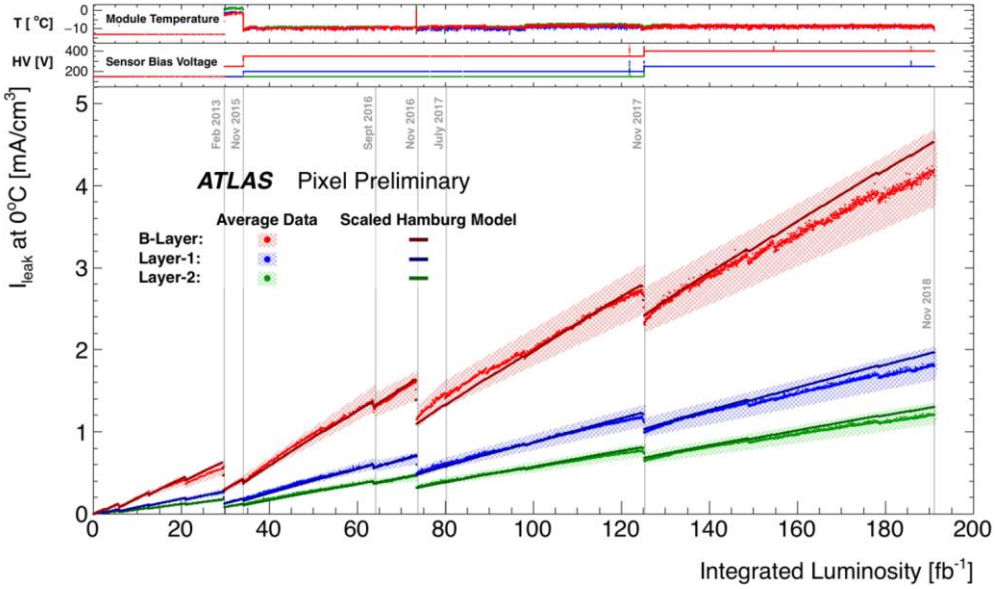


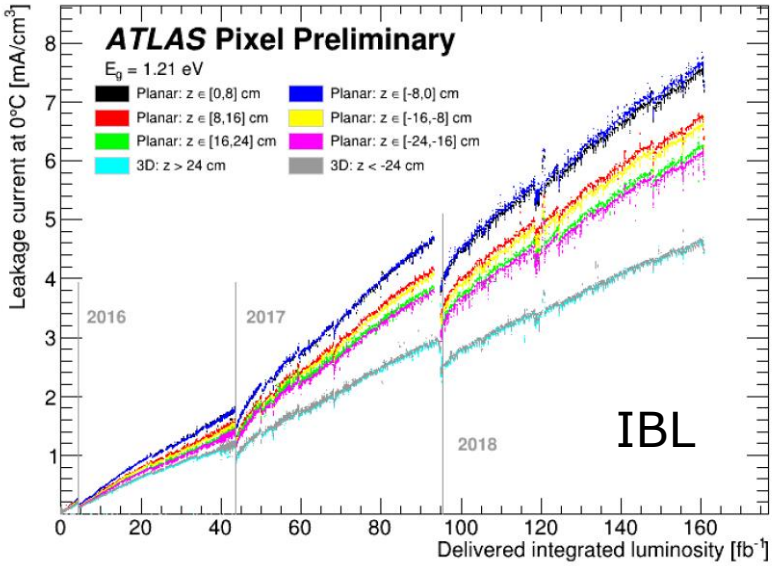
IBL

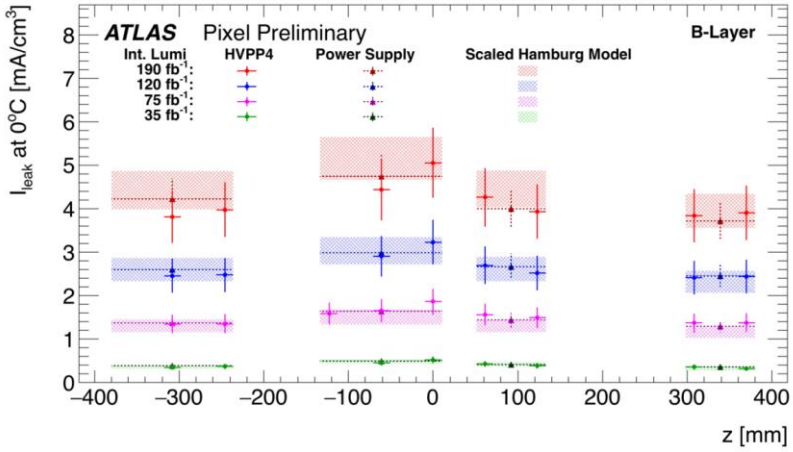
- The measured dE/dx decreases due to the decreasing charge collection efficiency.
  - Threshold changes show up as steps in dE/dx (hits below threshold do not get recorded).
  - The high voltage can have an influence if the detector is not fully depleted.

Leakage Current

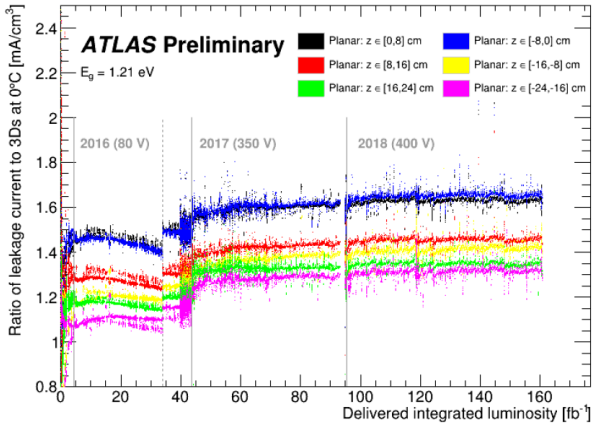
Average measured leakage current data match scaled Hamburg Model predictions







z-dependence (fluence) of Leakage Current.



Current Ratio between planar and 3D (assumed fully depleted) sensors

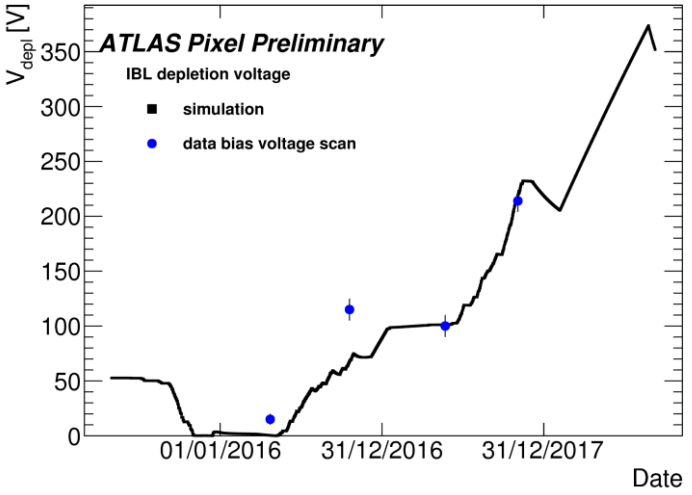
Depletion Voltage Evolution

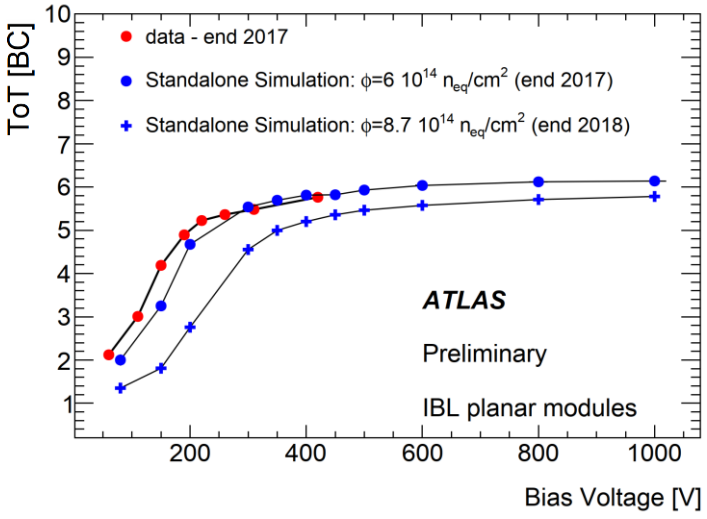
RUN-2 HV

HV	2015	2016	2017	2018
IBL	80V ⇨	150V ⇨	350V ⇨	400V
B-layer	250V	350V	350V	400V
Layer-1	150V	200V	200V	250V
Layer-2	150V	150V	150V	250V
Endcap	150V	150V	150V	250V

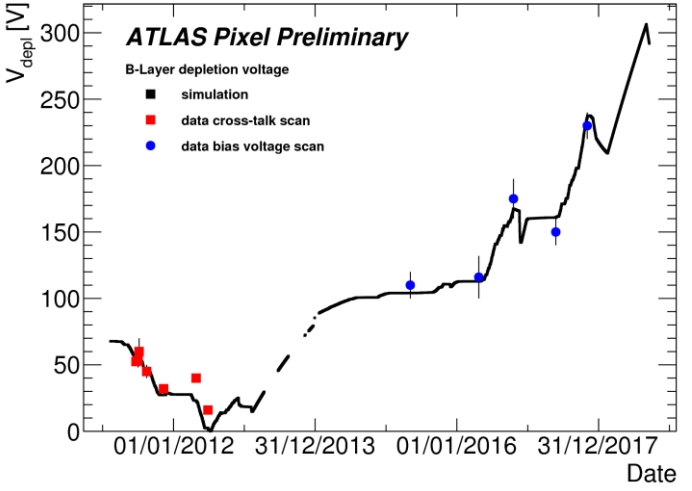
- The High Voltage settings are increased at the beginning of each year according to the predictions of the simulation in order to keep the sensors fully depleted for the entire year.

Simulation based on Hamburg model





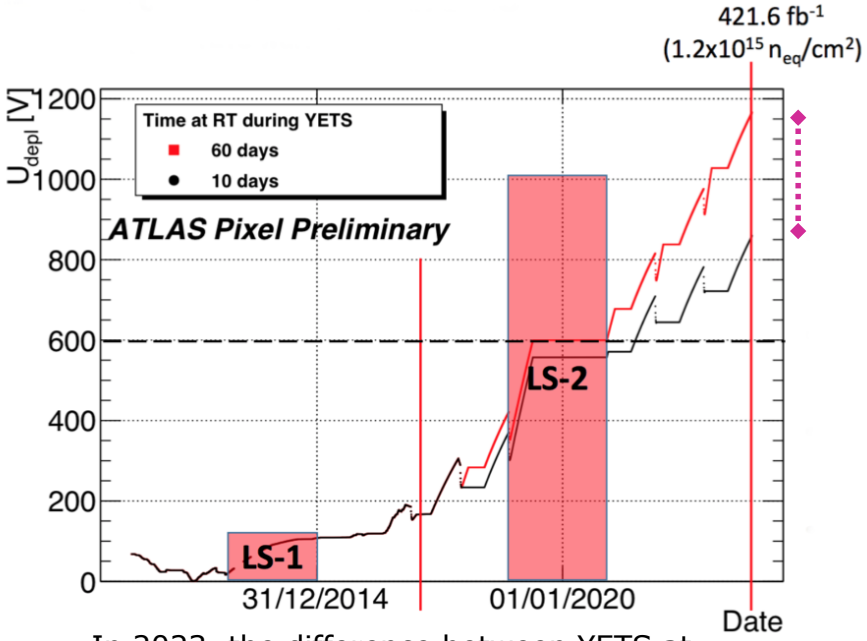
- The depletion voltage is monitored in special high voltage scans during collisions by monitoring collected charge (ToT) for a given HV setting.



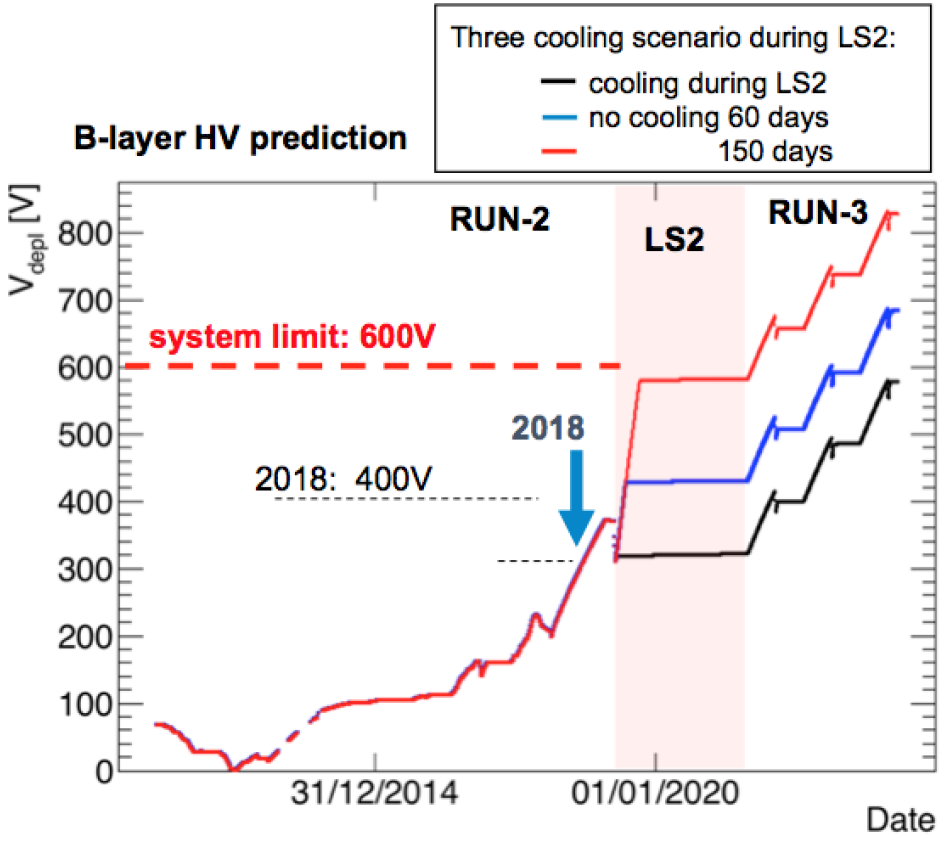
- The operational limit for IBL is 1000 V, for B-layer 600 V.

Reverse Annealing

- Different cooling scenarios for Year-End-Shutdown Periods up to Run 3 and for LS 2 have been simulated.
- Keeping the detector cold during shutdown periods is critical to prevent reverse annealing, in particular in B-layer and IBL.



In 2023, the difference between YETS at room temperature and minimal warm-up can amount to ~300 V higher depletion Voltage.



- Unfortunately warming up the detector can not be fully avoided due to requests of other systems as well as needed maintenance periods.

Keep Pixel cold whenever possible

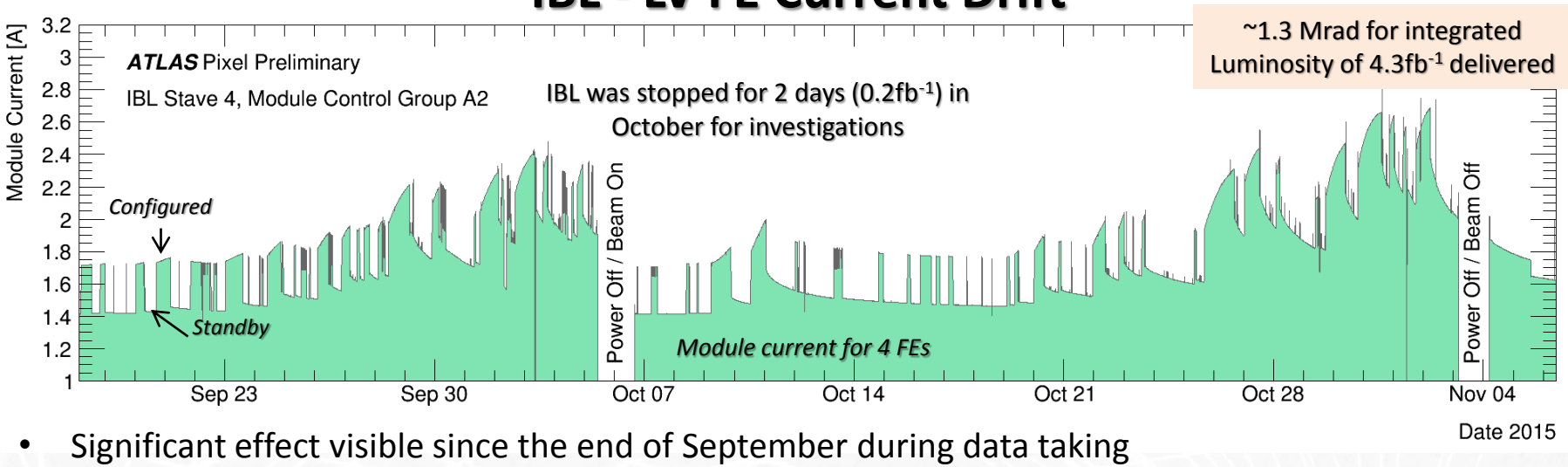
Summary and Conclusion

- The ATLAS Pixel Detector has delivered an *excellent performance* in the last year of Run 2.
- Main problem on the hardware side are dying *on-detector VCSELs* for optical data transmission. A full exchange will happen during the shutdown, as well as further analysis of the failed components to understand the failure mode.
- The *Readout System is largely consolidated*, and the remaining issues will be addressed during the long shutdown.
- With the projected LHC running scenarios in Run-3, the main focus is expected to shift towards the aging of the detector due to *radiation damage*.
  - Handles to mitigate the effects are present in the tweaking of operational parameters. Major progress has been made in furthering the description and its introduction into MC simulation. B-Layer performance will have to be closely monitored.

We hope for another three years of excellent data taking with the Pixel Detector during Run 3, before it will be replaced by the ITk for HL-LHC.

BACKUP

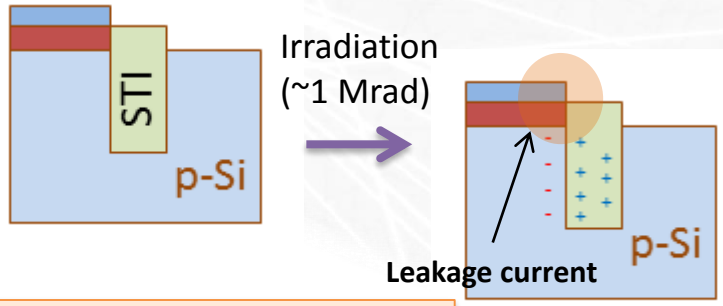
IBL - LV FE Current Drift



~1.3 Mrad for integrated Luminosity of 4.3fb^{-1} delivered

- Significant effect visible since the end of September during data taking
- Understood to be a FE N-MOS transistors leakage due to defects built-up at the Silicon Oxide (STI) interface and cumulated by ionizing dose → Known features but not tagged during construction
- It is an effect that is related to dose rate (traps built-up at the STI) and temperature (annealing)
- Lab investigations are ongoing → operational recommendations are expected

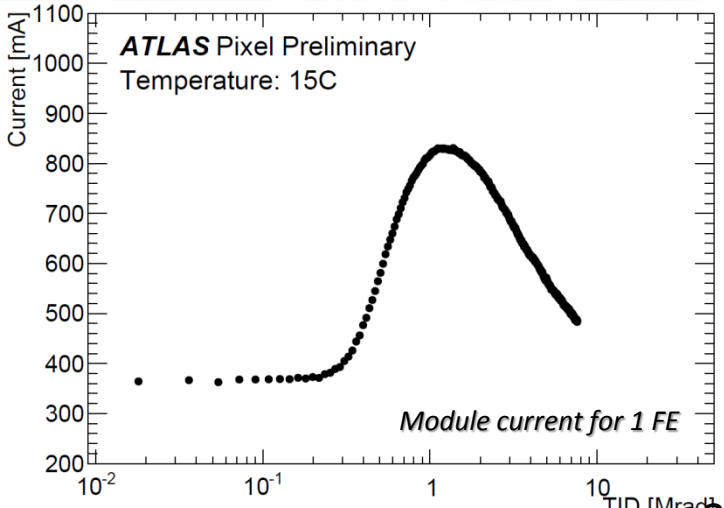
N-MOS transistor cross section



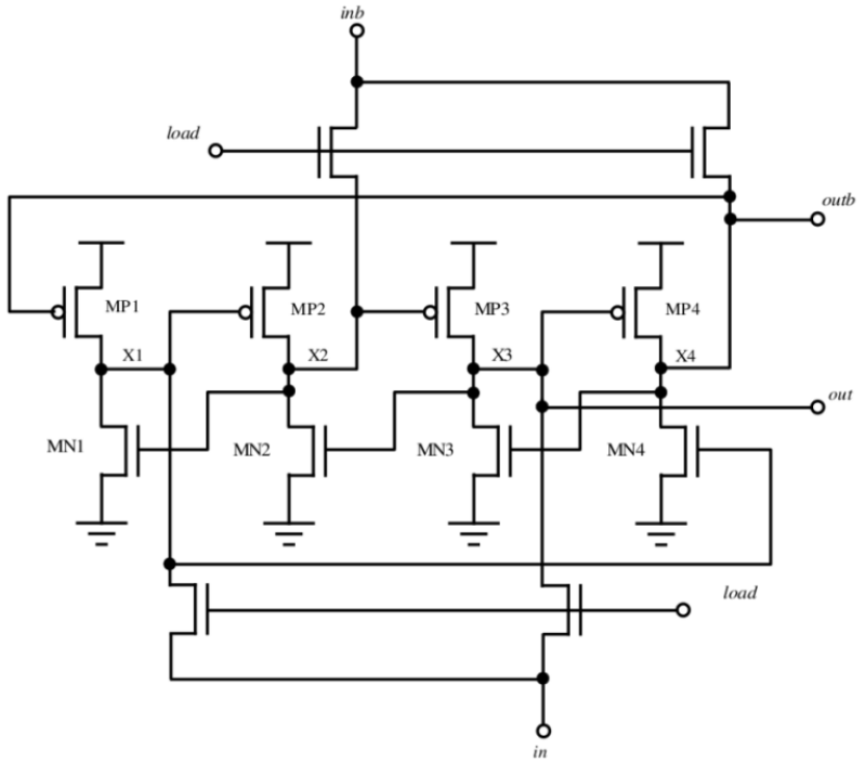
Consequences:
- Temperature increase
- Electrical failure risks

Lab measurement confirmed the phenomena
Issue expected to be relaxed after few Mrad

Lab measurement – FE X-ray irradiation



- Increase tolerance against SEUS:
  - Spatial separation of critical nodes, isolated wells, guard rings and interleaving of cells.
- Dual Interlocked Cell (DICE) latches based memory
  - Single DICE latches for pixel registers.
  - Global registers use triple redundancy.



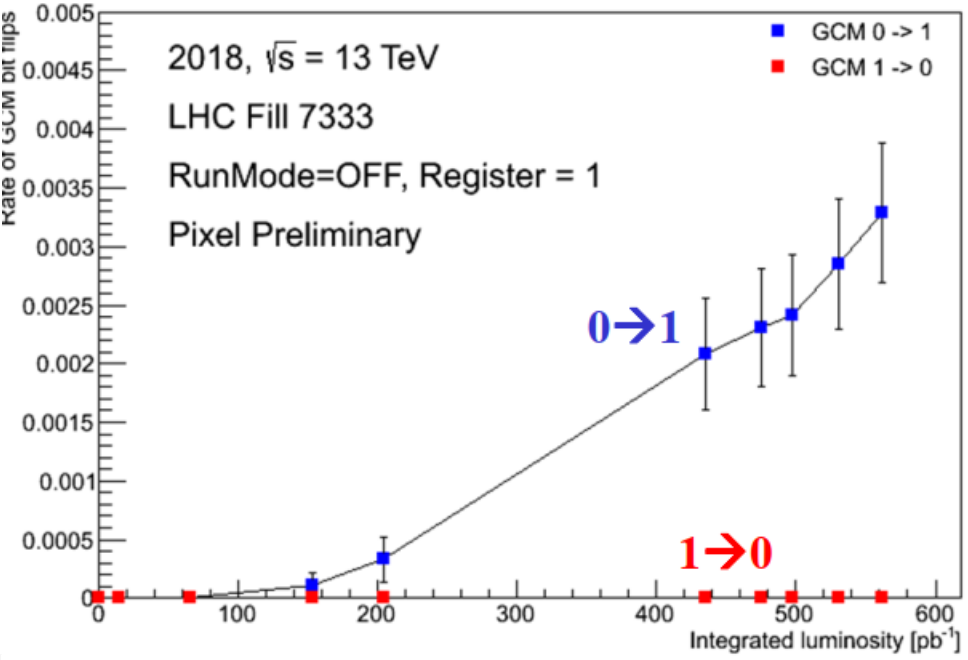
DICE latches:

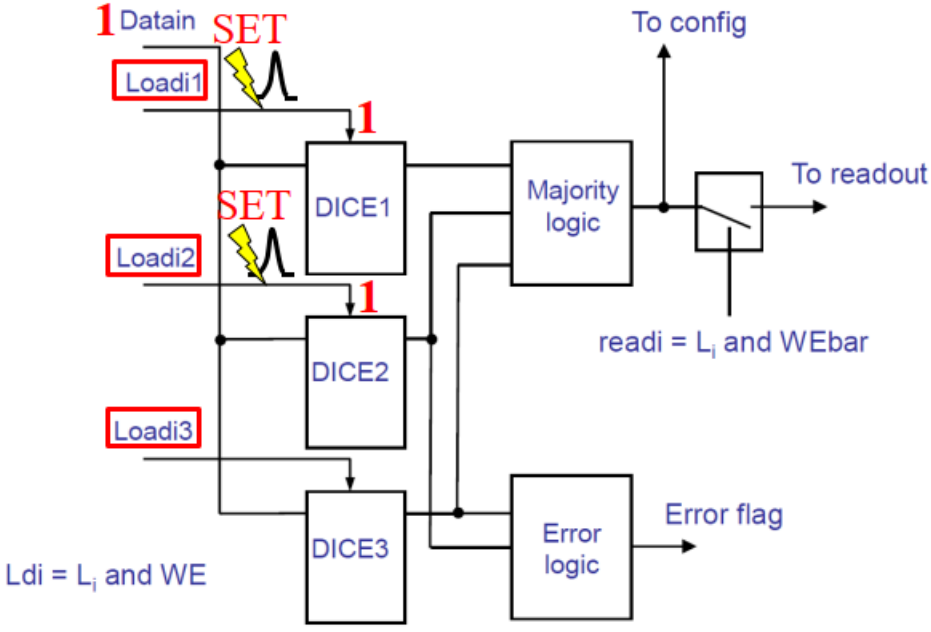
- Cross coupled inverter latch structure with 4 nodes (n_1-n_4) stores data in two pairs of complementary values.
- DICE latch is upset if *2 nodes storing the same logic state* (X1-X3) or (X2-X4) change the state due to the single particle impact effects.

SEU vs. SET

- The cumulative rate of bit flips in Global memory was investigated to see effect of SEU/SET.
- High rate of 0→1 flips indicate SET (glitches) on the LOAD line with Data-in "1".
- No 1→0 transitions are observed due to the triple redundant logic.

Bit flip rate in Global memory (Data IN = 1)

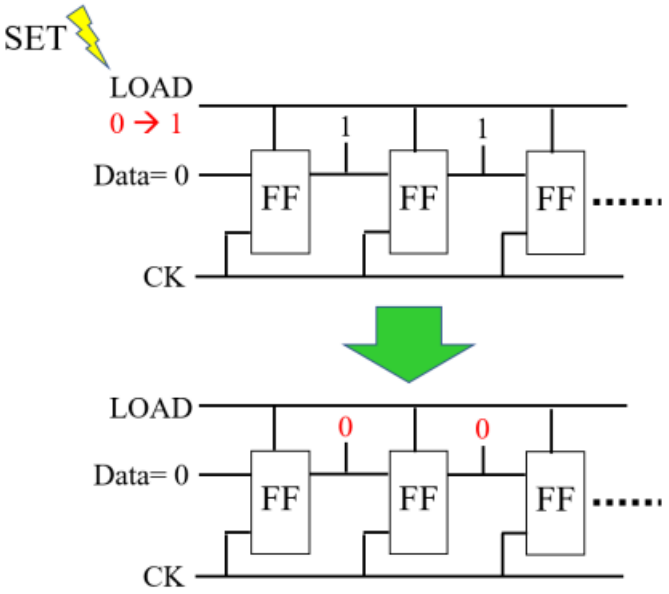


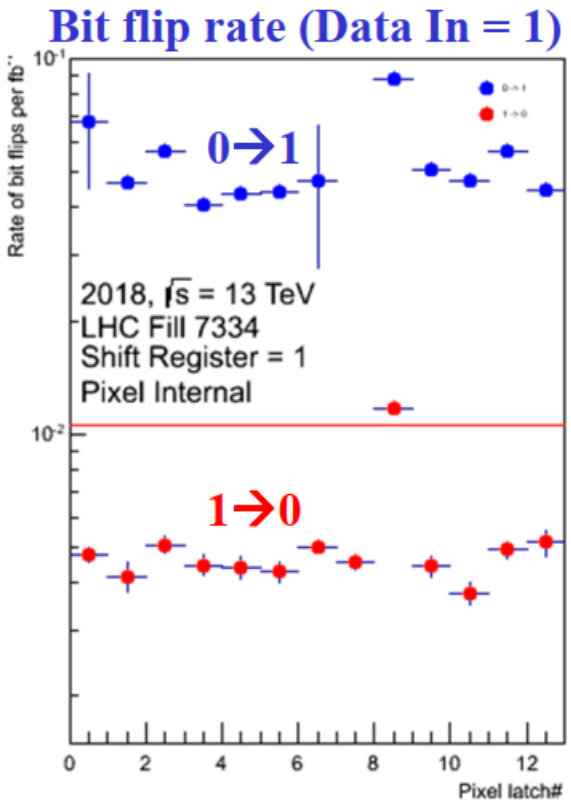


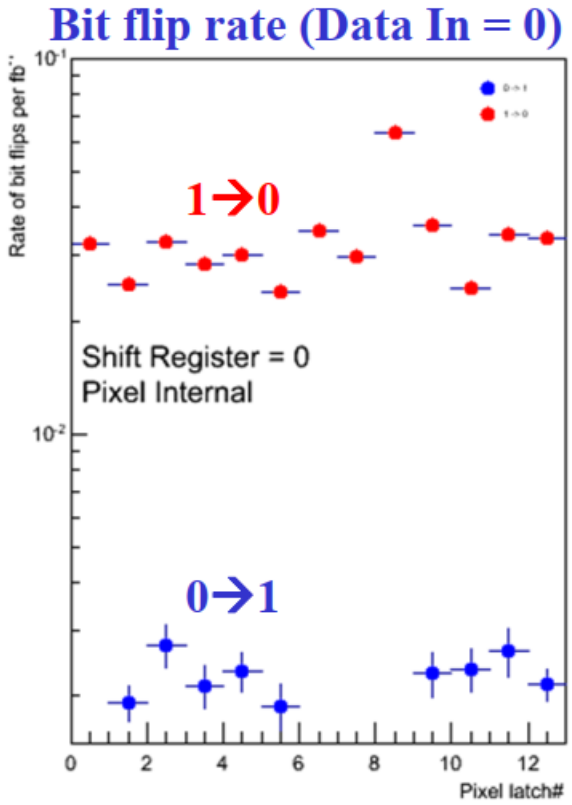
SEU vs. SET

- Average rate of bit flips in Pixel memory was checked for each bit memory (13 bits in total).
- 0→1 flips dominate for Shift Register = 1
- 1→0 flips dominate for Shift Register = 0

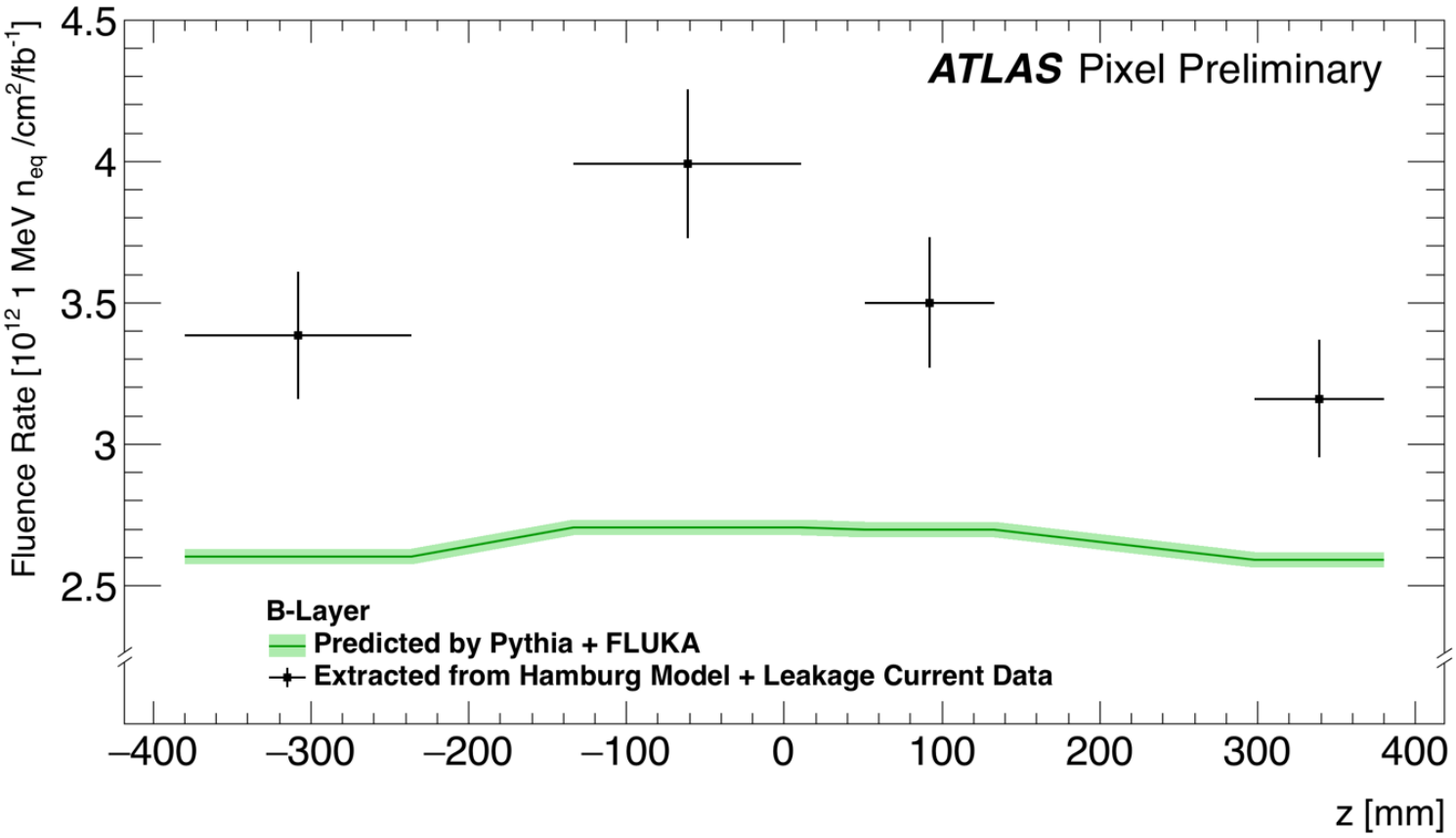
} SET (glitches)







Fluence



Comparison of fluence predictions by Pythia8 and FLUKA to the fluence determined from leakage current data combined with the Hamburg Model, for the B-Layer.

Fluence predictions by Pythia8 and FLUKA are weighted averages of the fluence predicted at three energy levels throughout the full period of operation as of November 2017. The uncertainty on the fluence as predicted with Pythia8 and FLUKA is less than 1% (statistical only) and the uncertainty on the fluence determined from leakage current data combined with the Hamburg Model is 6.6%. Uncertainties due to temperature offset are not included. Pythia8 results are tuned with A2M_MSTW2008LO. The horizonal lines on the fluence determined from leakage current data combined with the Hamburg Model reflect the bin ranges.