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APIX: a two-tier avalanche pixel sensor for charged particle detection and timing

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Vienna Conference on Instrumentation
Vienna, Austria, February 18-22, 2019

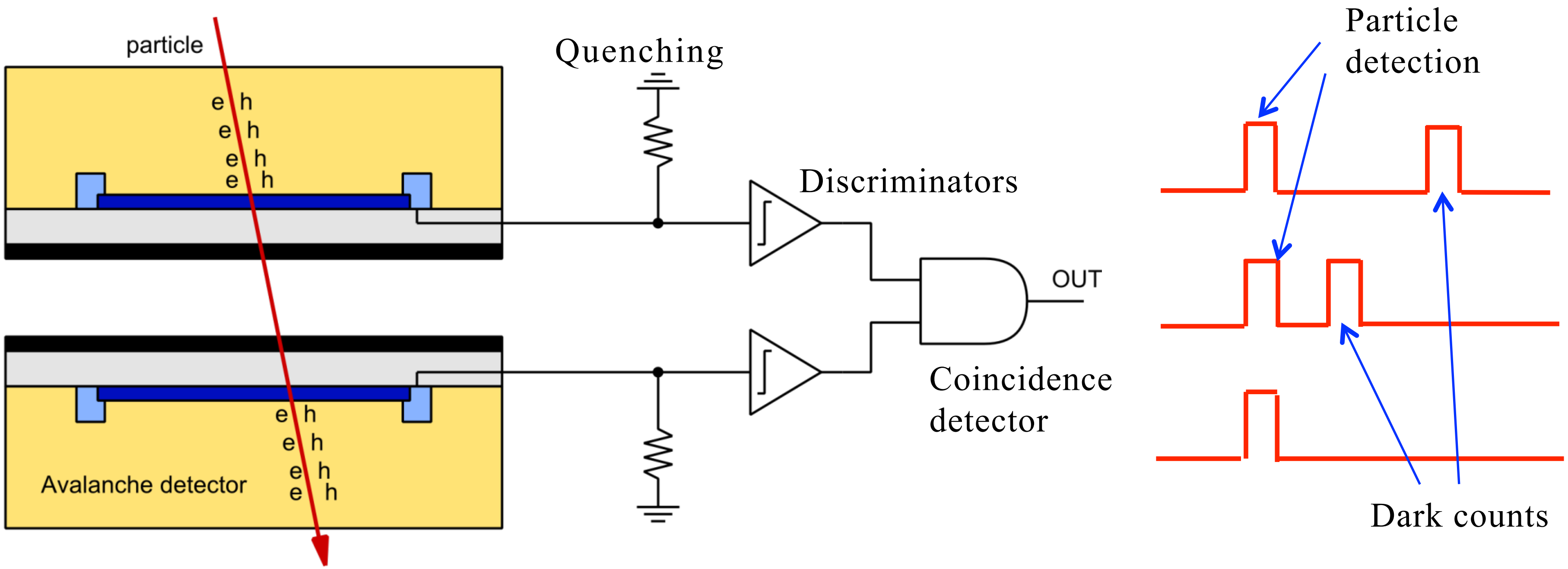
Outline

- Sensor concept and architecture
- 1^{st} prototype characterization
- Beam Test of 1^{st} prototype at CERN-SPS
- 2^{nd} prototype layout
- Possible applications
- Summary and perspectives

APIX particle detector concept

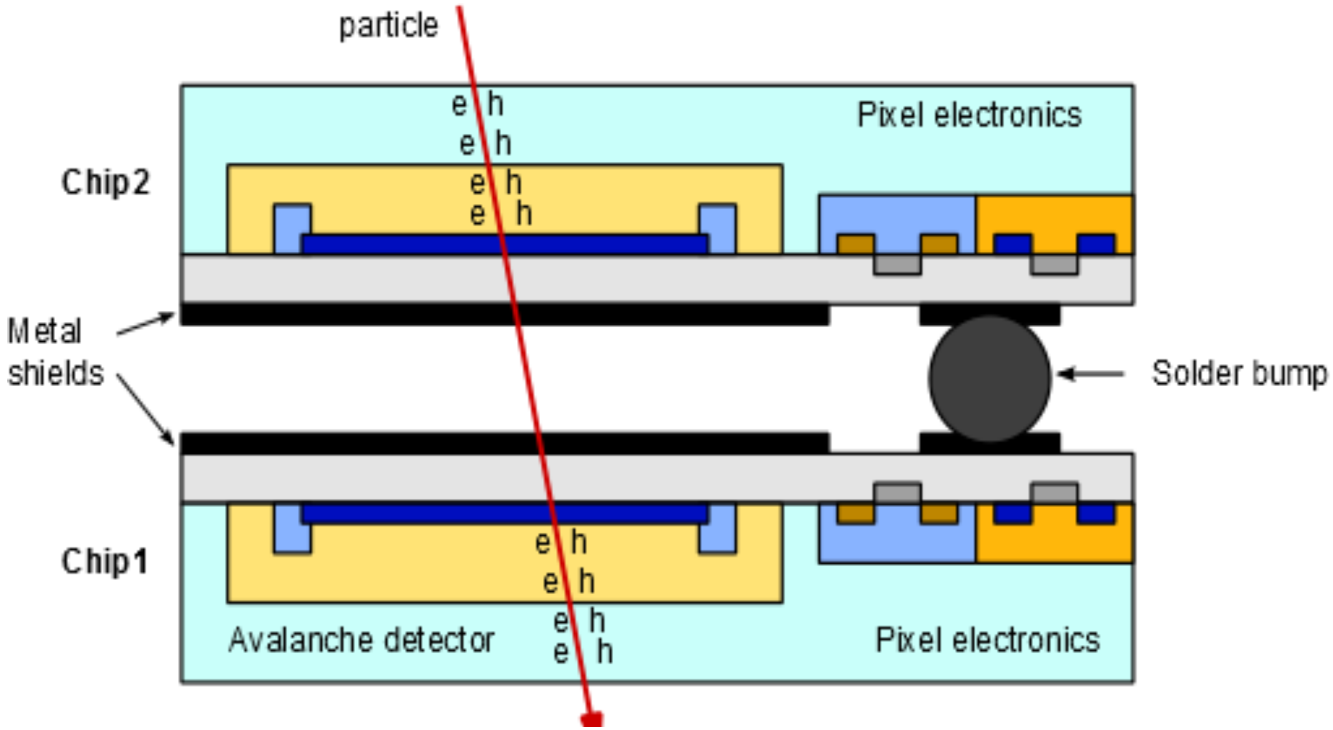
Basic idea:
Use of two Geiger-mode avalanche detectors (SPADs) in coincidence to detect particles

- Digital read-out
- Reduced Dark Count Rate: $DCR = DCR_1 * DCR_2 * 2\Delta T$
- Timing performances
- Low power consumption
- Low material budget



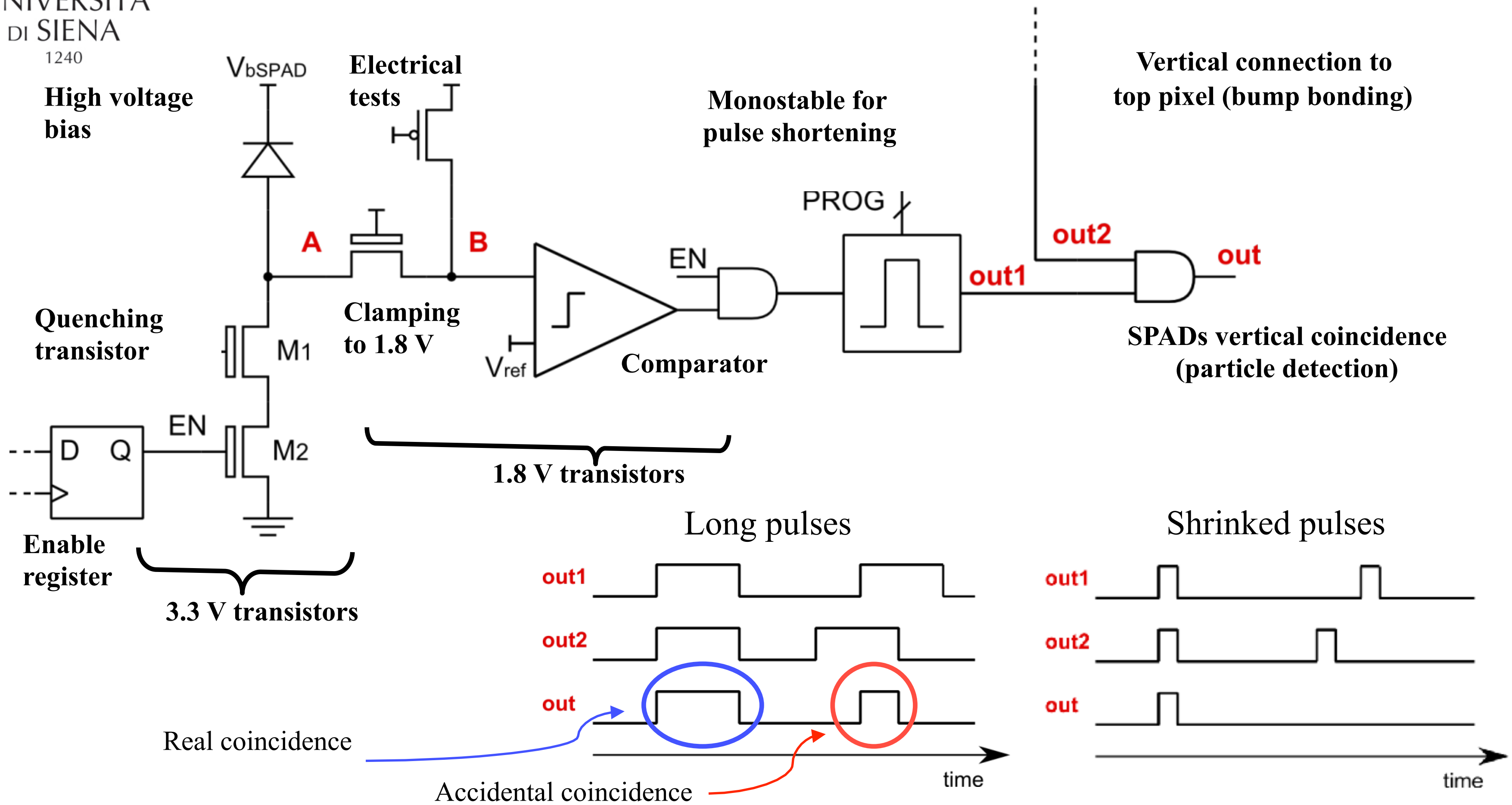
**N. D'Ascenzo et al., JINST 2014*

APIX demonstrator: pixel cross-section



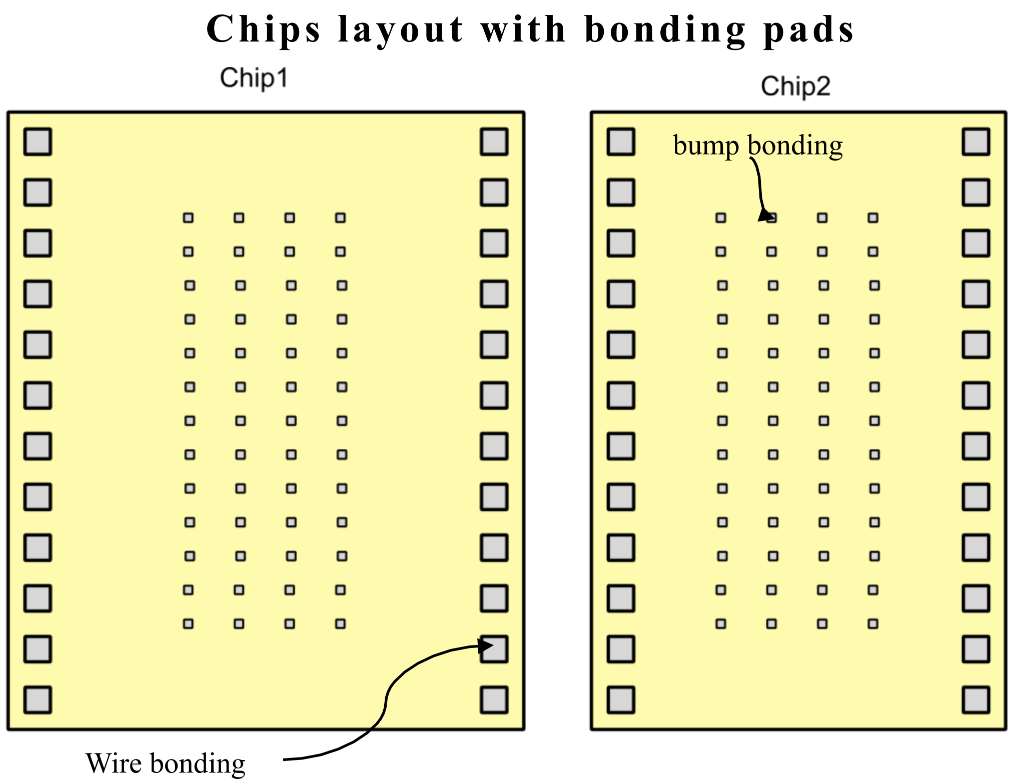
- ➔ CMOS process allow integrated electronics (not feasible in SiPM integrated process)
- ➔ Metal shielding to avoid optical cross-talk
- ➔ Vertical interconnection by **bump bonding**
- ➔ Two SPAD types: p+/n-well and p-well/n-iso

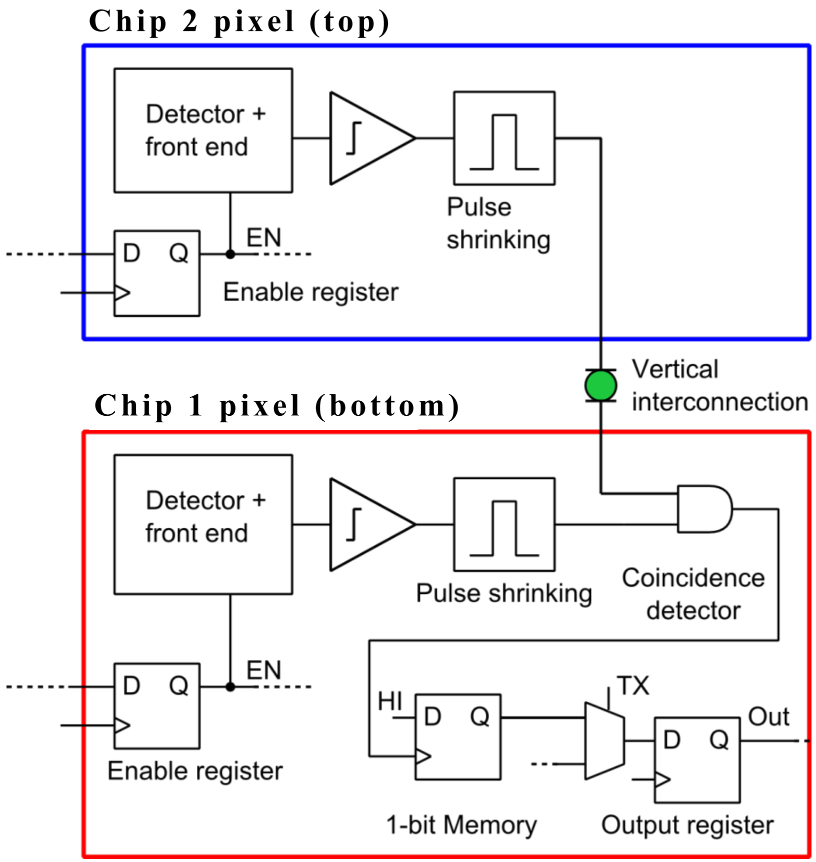
APIX pixel: pulse shortening

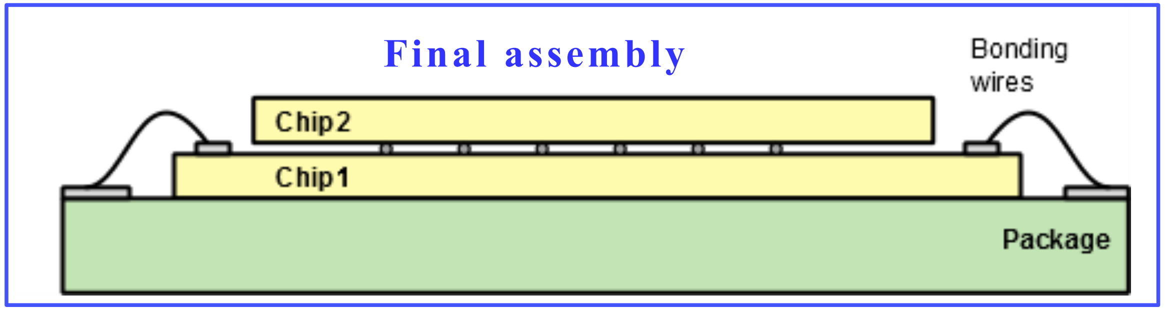


- Digital circuitry at 1.8V: compact, fast, low-power
- Individual pixel enable/disable: M2 disables recharge, AND gate disables output pulses
- Pulse shortening: reduces the rate of accidental coincidence
- Programmable pulse width: **750 ps, 1.5 ns, 10 ns**

APIX top and bottom pixels connection



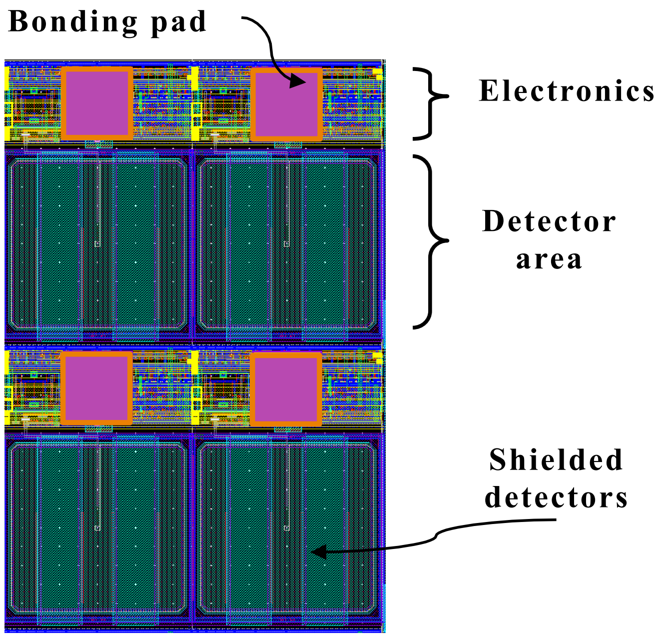




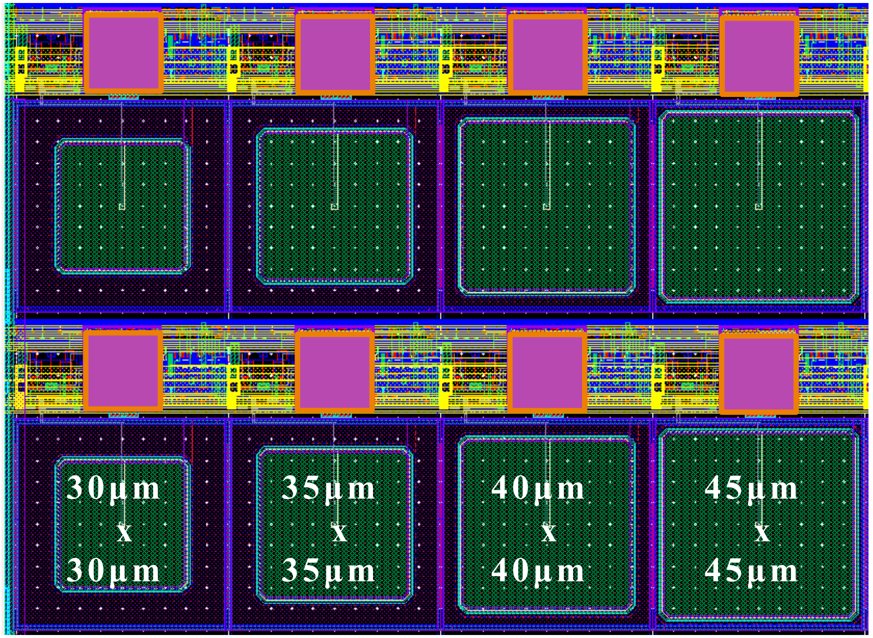
Vertical integration via Bump-bonding (IZM)

APIX pixel array

- Sensor array of 16 rows x 48 SPADs
- Pixel size: 50 µm x 75 µm
- Total sensor dimensions: 1.2 x 2.4 mm^2



Unshielded pixels with different active area

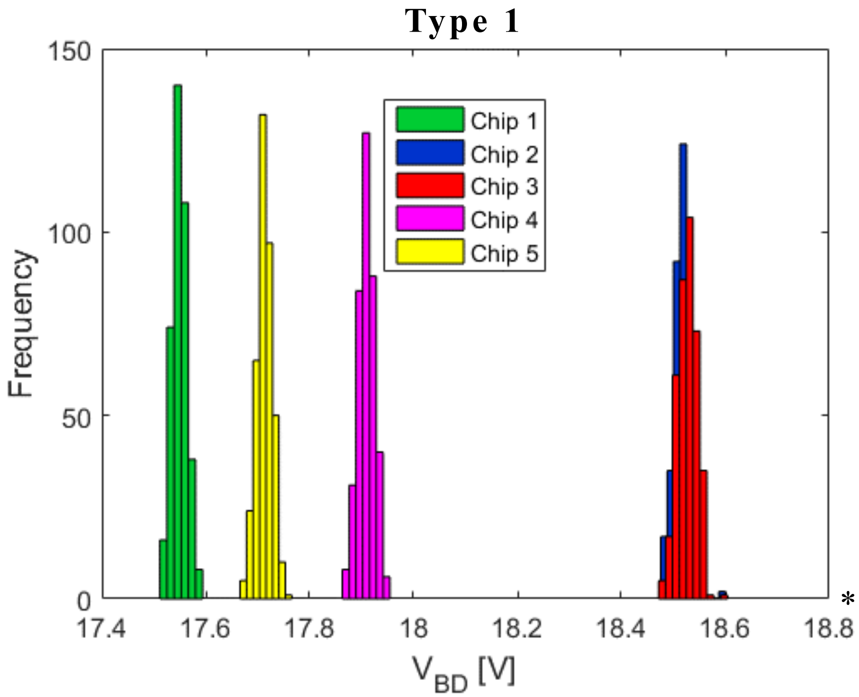


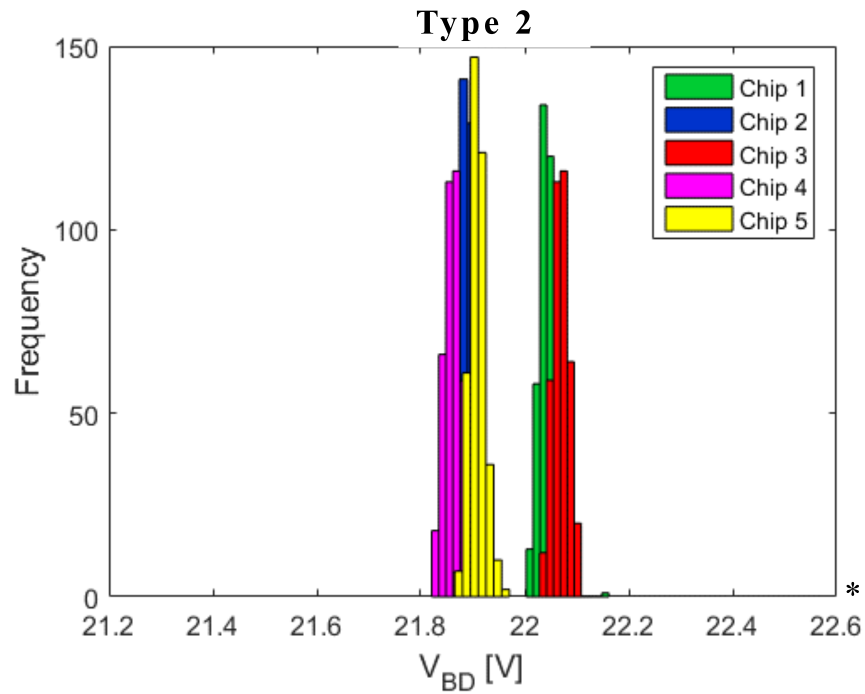
Array partitioning:

- Different SPAD active areas: 30 – 35 – 40 – 45 micron side
- Some unshielded structures for testing with light
- Coincidence between SPAD with the same size and with different sizes

Breakdown voltage characterization

Measurements on 5 different chips,
two SPAD types and 196 pixels per chip.





- Very good SPADs uniformity inside the same chip (**σ < 20 mV**)
- Large difference (1V) between different chips for type 1

**L. Pancheri et al. "First prototypes of two-tier avalanche pixel sensors for particle detection", Nuclear Instruments & Methods in Physics Research A (2016).*

Single chip Dark Count Rate

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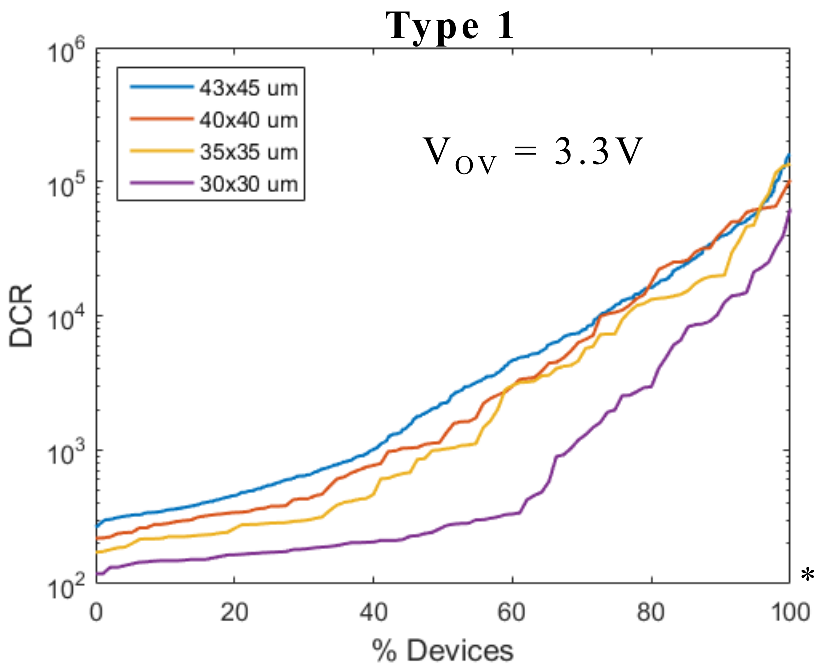

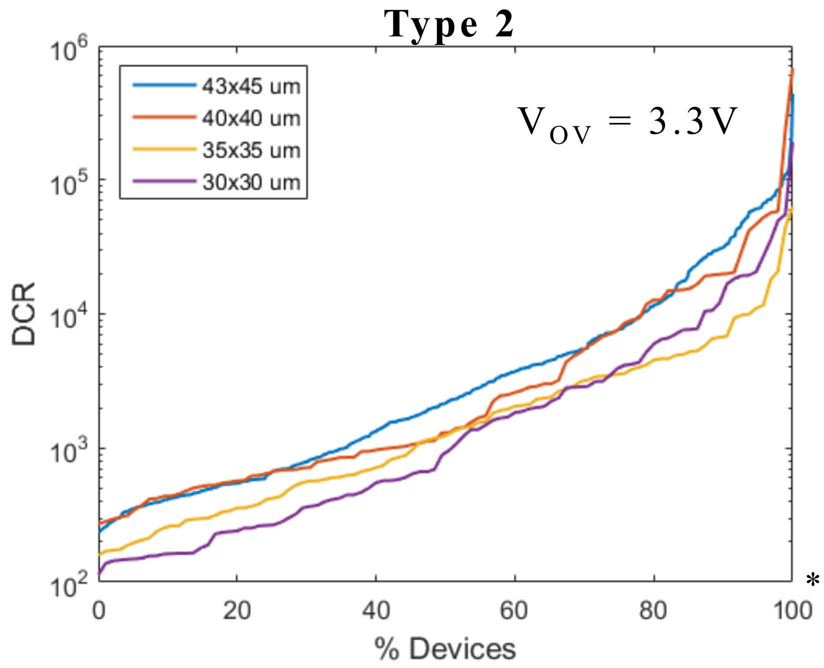

- Cumulative distributions, combined measurements on 3 chips
- 600 devices for largest size, 72 for smaller ones
- Median DCR = 2.2 kHz for largest cell size of both types

courtesy of L. Pancheri

APIX final assembly Dark Count Rate

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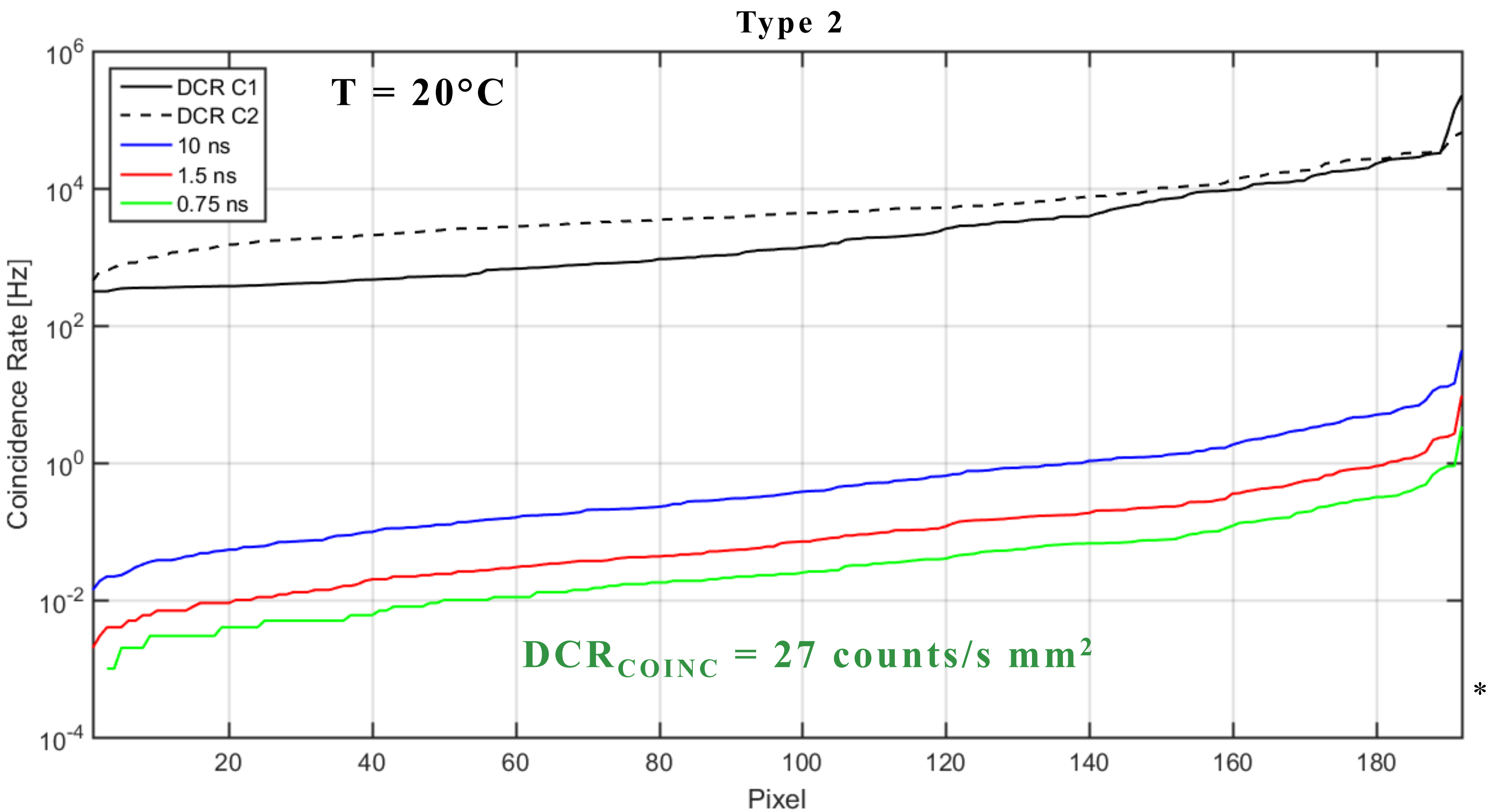
Dark Count Rate for different coincidence time ΔT: 10 ns, 1.5 ns, 0.75 ns



$$DCR_{COINC} = DCR_1 \times DCR_2 \times 2\Delta T$$

**courtesy of L. Pancheri*

Radiation tolerance tests

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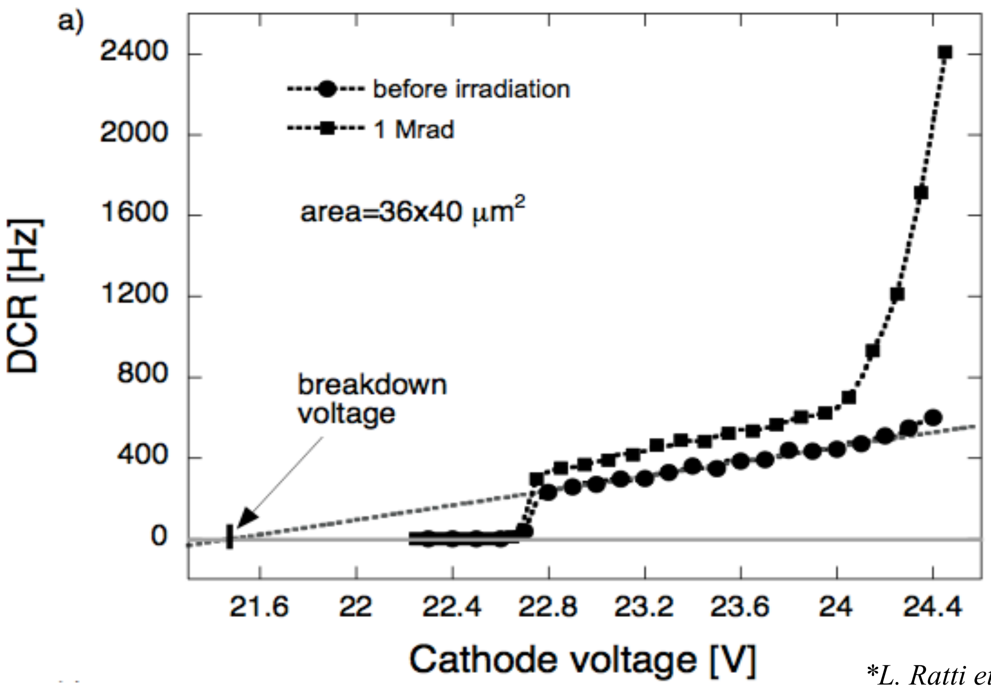
Accurate characterization, in terms DCR, of SPAD array tolerance to ionizing and not ionizing radiation has been performed.

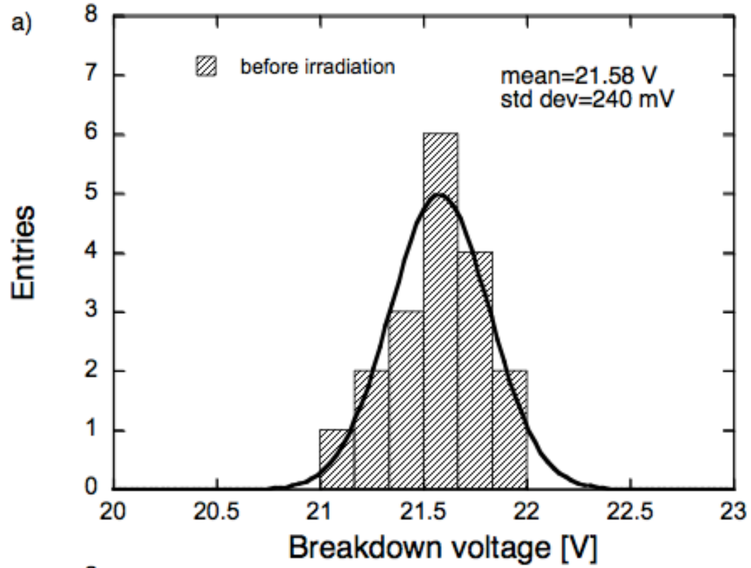
The tests has been operated on 6 APIXFAB0 chips (180 nm CMOS technology , similar to type 1 SPADs, 36x40 μm^2):

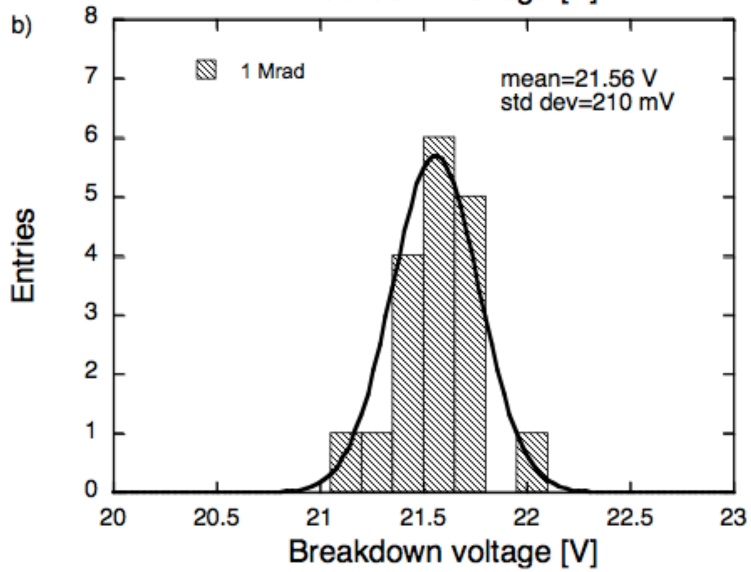
• 2 chips were irradiated with X-rays to a maximum dose of 1 Mrad(SiO2). (this slide)

• 4 chips were exposed to neutron fluences up to 10^{11} 1 MeV neutron equivalent cm^{-2}.

A 10 keV, RP-149 X-ray Semi-conductor Irradiation System from Seifert available at the Physics and Astronomy Department of the University of Padova (Italy) was used.







*L. Ratti et al, IEEE Transactions on Nuclear Science. Vol. 66 Issue 2 pp. 567-574

Radiation tolerance tests

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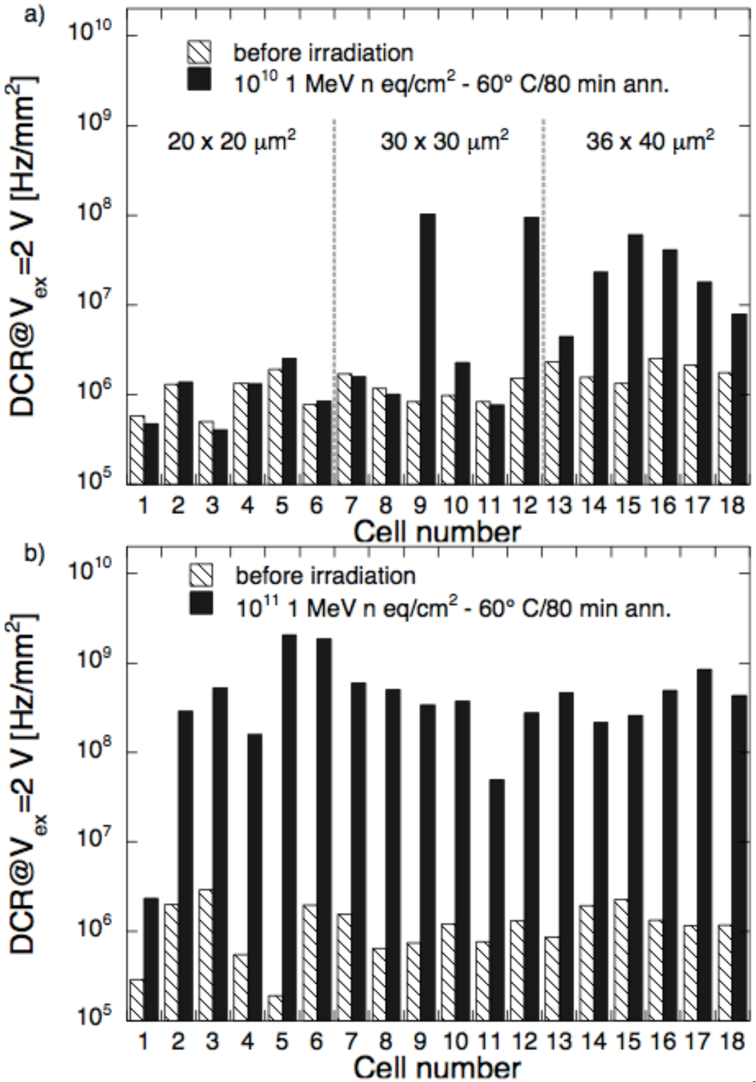
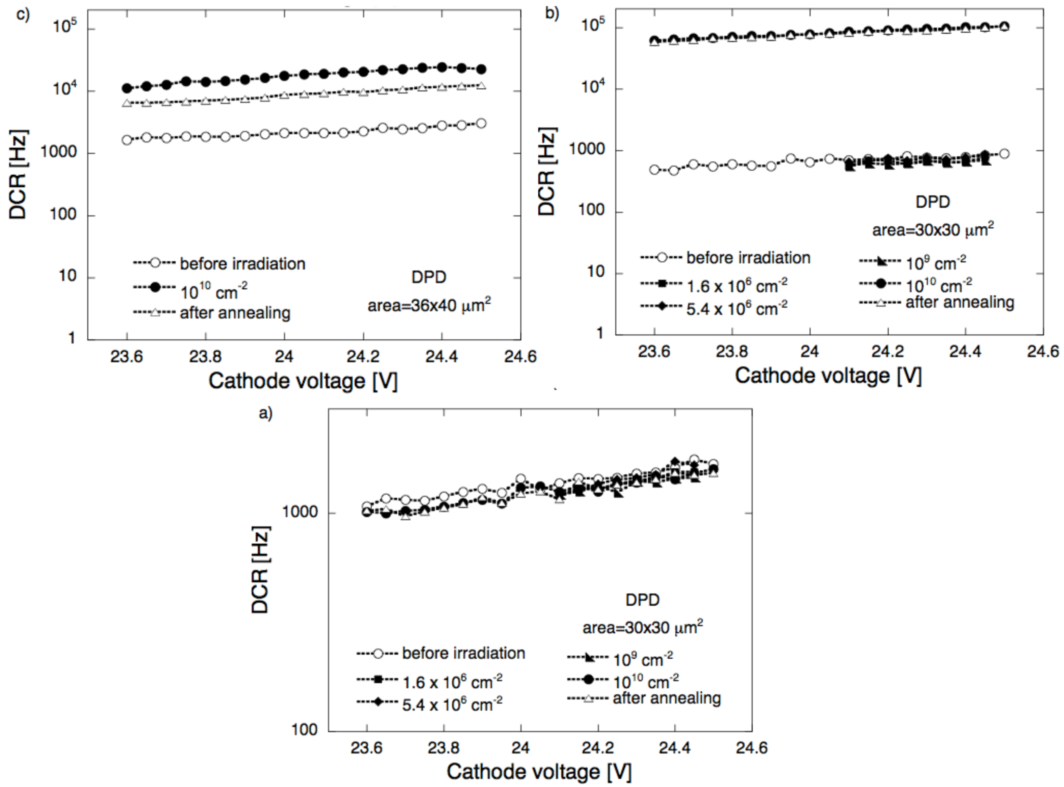
- Neutron irradiation took place at Legnaro National Laboratory (5 MeV proton on Be target)
- Neutron spectrum with energy from 0.5 to 3 MeV



Dark count rate at an excess voltage of 2 V normalized to active area for two sets of sensors exposed to a) 10^{10} and b) 10^{11} 1 MeV neutron equivalent cm^{-2}. Before irradiation and after neutron irradiation and after 60◦ C/80 min annealing.

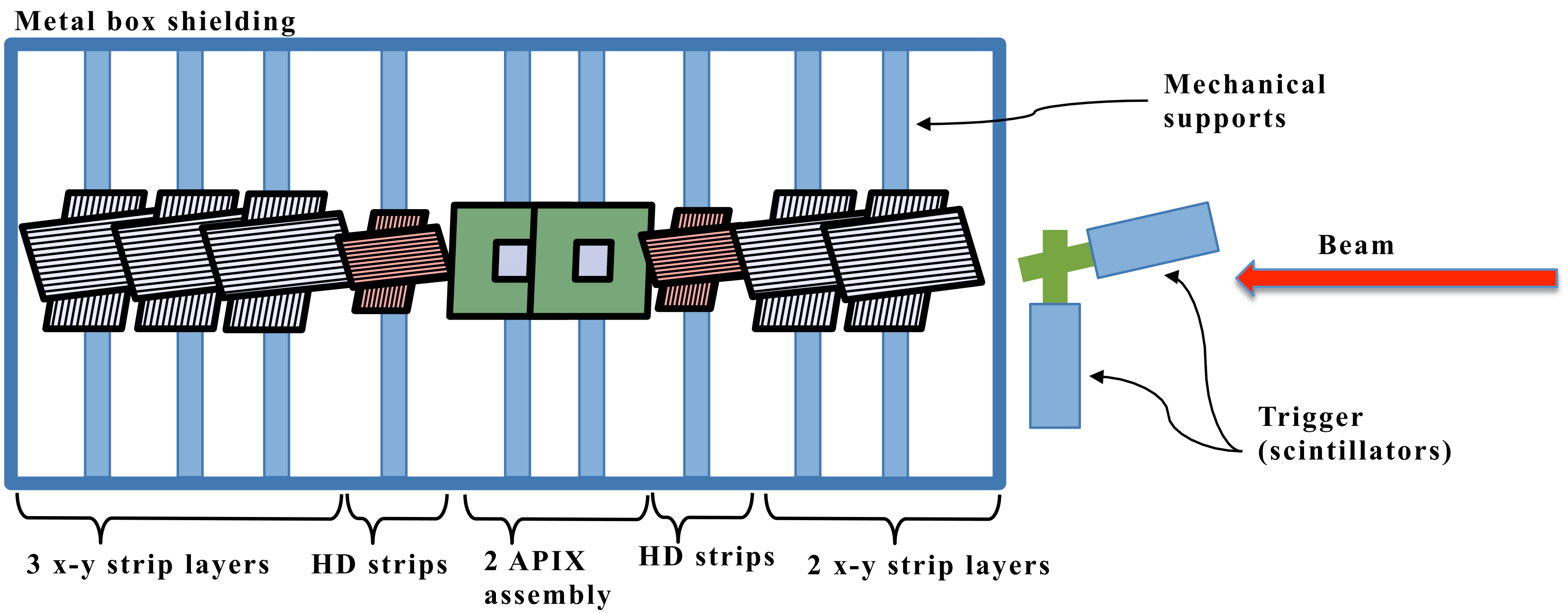
Three representative cases of Type1 cell response to neutron irradiation.



*L. Ratti et al, IEEE Transactions on Nuclear Science. Vol. 66 Issue 2 pp. 567-574

Beam Test layout (at CERN-SPS)

Scheme of Experimental apparatus on beam line:

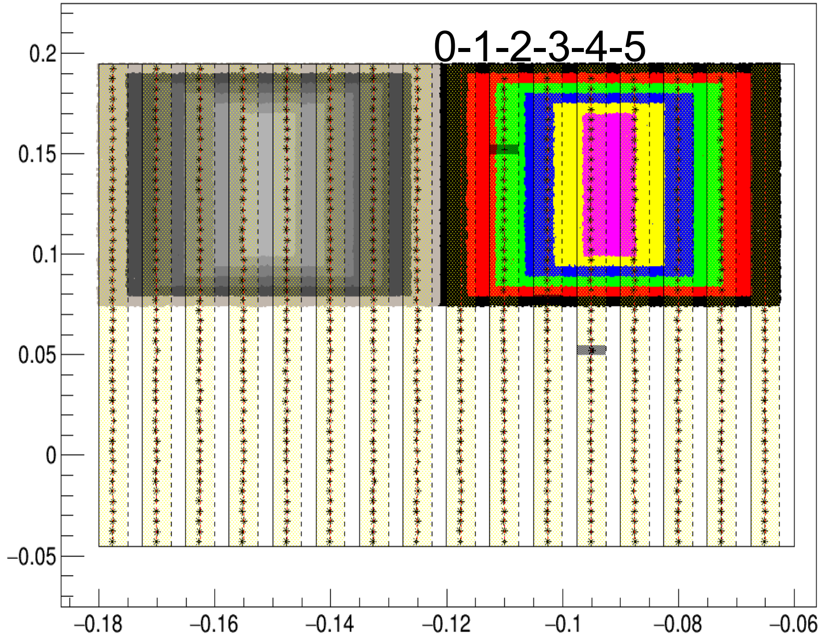


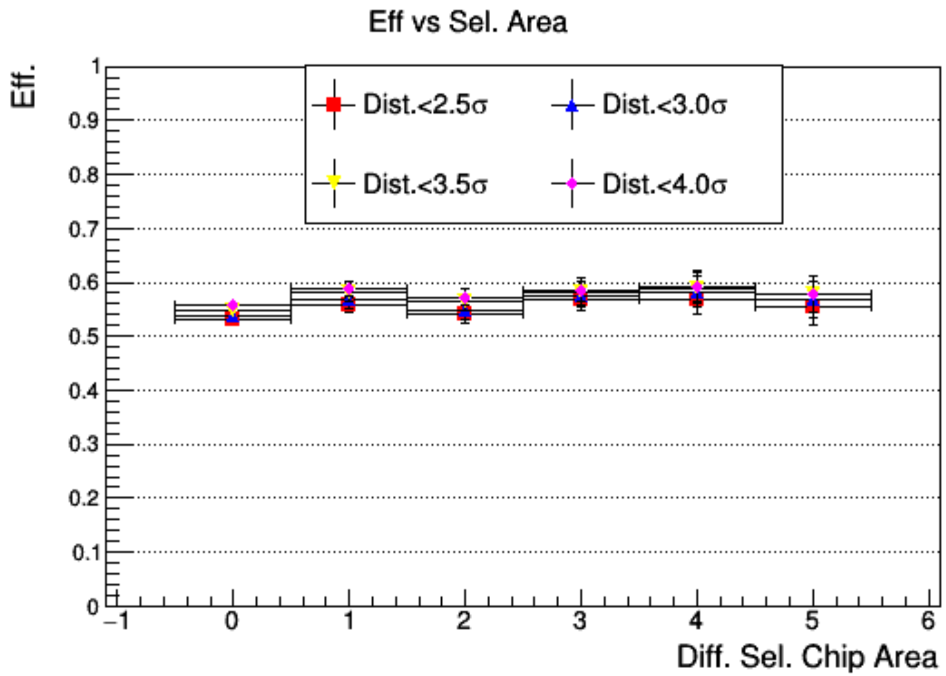
- Test took place at CERN SPS (H4 beam line) on September 2016
- Positrons and π+ beams at 50, 100, 150, 200 and 300 GeV
- 2 APIX demonstrator and 14 silicon strip detectors (for tracking)
- 5 X-Y strip layers with 730 μm pitch + 2 X-Y HD layers with 80 μm pitch
- Asynchronous APIX reset at 1 MHz.
- Off-Spill random triggers to measure APIX DCR and strip pedestal

Efficiency for particle detection

Despite some difficulties with tracking (noisy HD strip) efficiency has been measured in 6 different fiducial regions.

Definition of 6 areas covered by the reconstructed track impact point (IP)

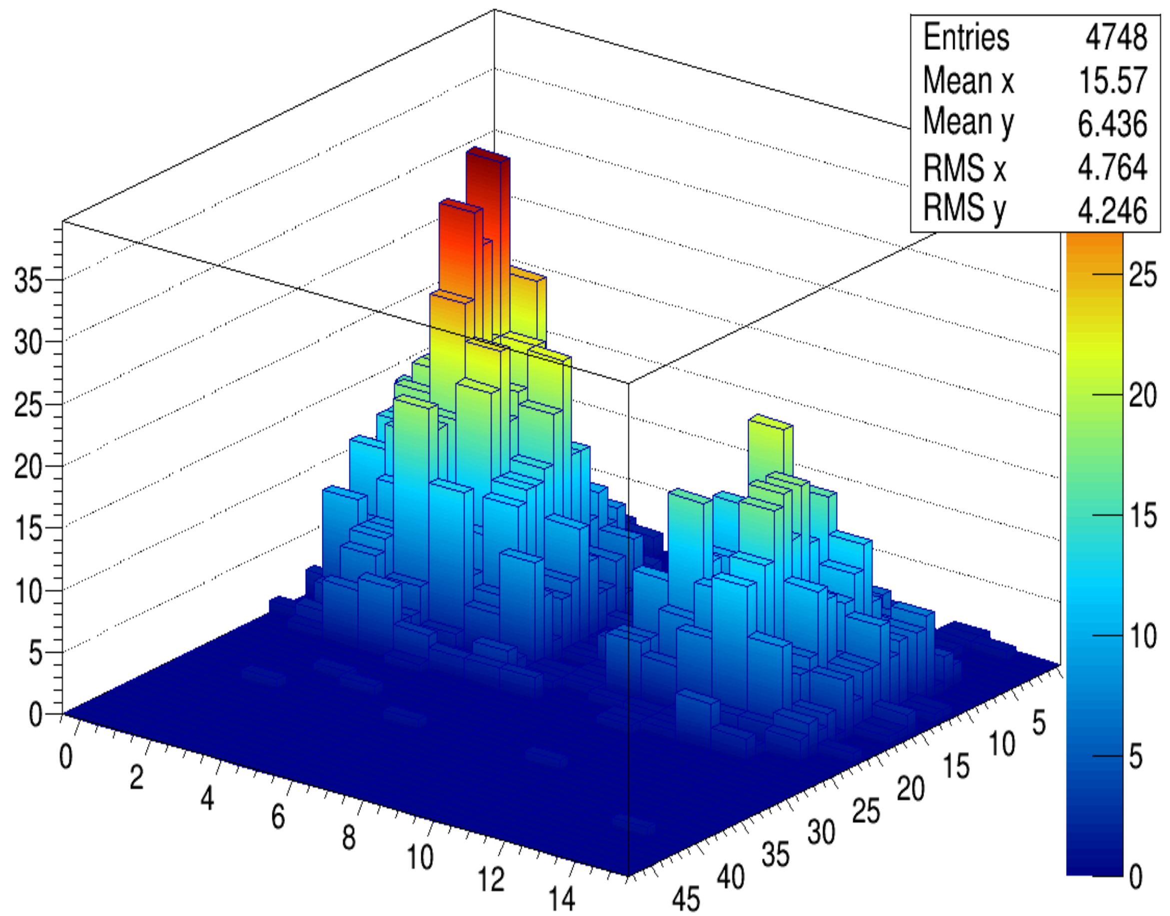




- Measured efficiency 56.2 ± 5 % (stat+sys)
- Expected (purely geometrical) FF = 52%
- Effective detector efficiency close to 100% (only limited by FF)

APIX imaging

Example of two Regions-Of-Interest separated by ~ 100 um



ROI selected via tracking

APIX pixel array (2nd prototype)

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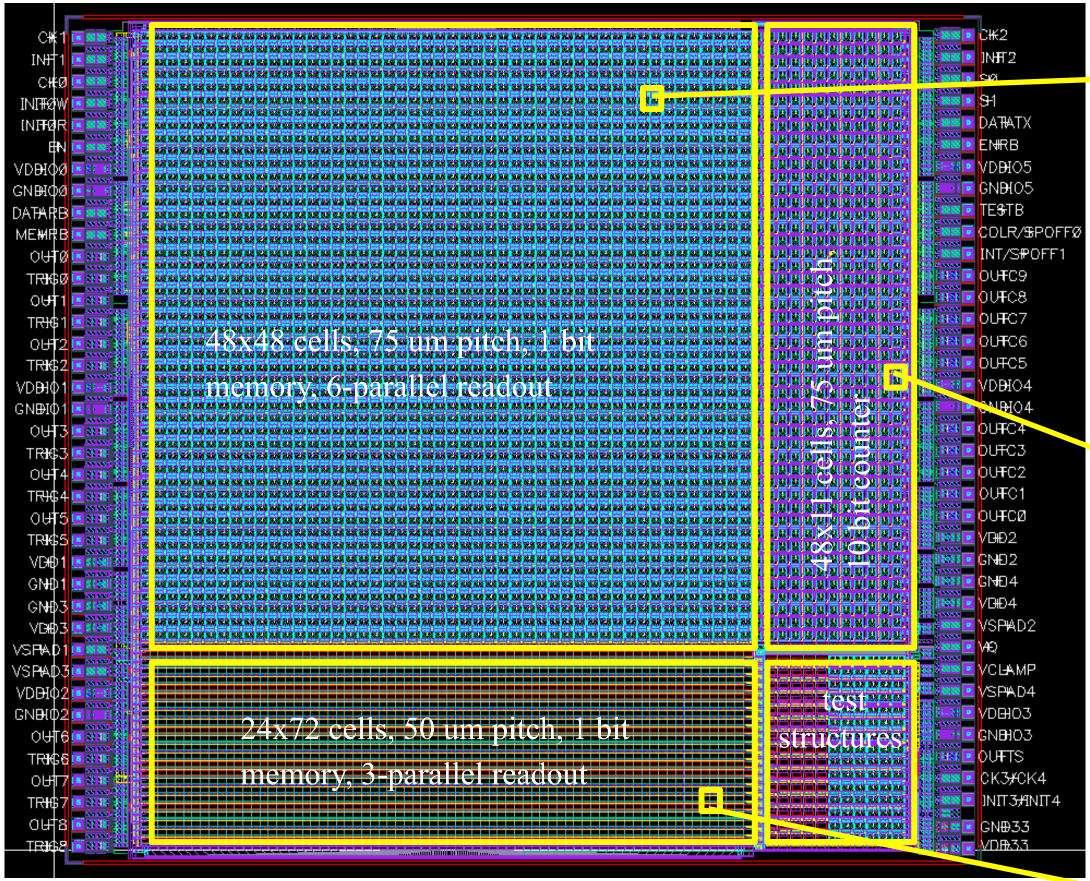
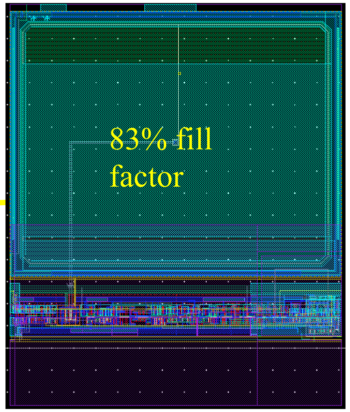
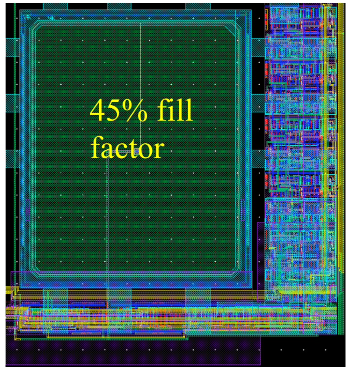
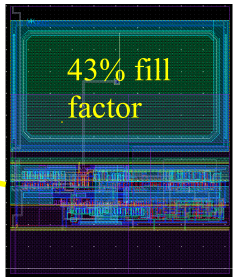
150 nm CMOS technology

- Fill Factor expected improvement: 52% ➔ 83%









- “1st layer” chip is 5 mm x 5.4 mm
- “2nd layer” chip is 5 mm x 6 mm
- Both chips delivered, now ready for bonding

Possible applications of APIX sensors

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APIX strengths:

- **low material budget**
- low power
- no cooling
- **good timing properties** (e.g.: time of flight with ~**100 ps resolution)**
- insensitivity to gamma radiation background
- narrow band acceptance (directionality)
- portability
- easy to configure to the specific application
- operation in real time: ß-time resolved studies (very high frame rate)

➢ **Tracking + Minivertexing:** use timing to disentangle event pileup (4D detector)

- ❑ however: difficult to operate with fluences above ~ 10^{10} n/cm^2
- ❑ radiation tolerant **for space-borne applications** and intermediate radiation environment
  (e.g.: - wearable mini-radiation sensor for astronauts (fly-eye mosaic of APIX sensors
  - minivertexing for ILC-like colliders)

➢ **APPLICATIONS in NUCLEAR MEDiCINE**:

- ❑ imaging probe (β - markers) for radio-guided surgery, prostate cancer screening... etc)
- ❑ beam profile monitoring in hadron therapy

Example of application (nuclear medicine)

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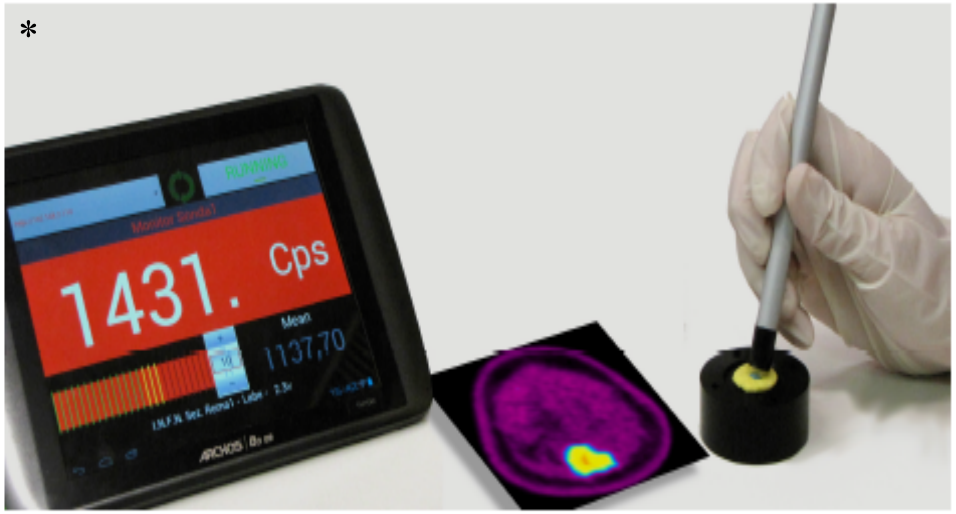
Intra-operative β- Probe for Radio-Guided Surgery

State-of-the-art:

- scintillator based + PMT (or readout by SiPM)
- counts per second
- **no high resolution imaging**

APIX β- Probe under development :

- **high resolution imaging** probe + counts/s
- **insensitivity to gamma radiation background**
- low power
- no cooling



* *A. Russomando et al. "An Intraoperative β − Detecting Probe For Radio-Guided Surgery in Tumour Resection" arXiv:1511.02059v1 [physics.med-ph] 6 Nov 2015*

Simulate APIX detection of hidden source

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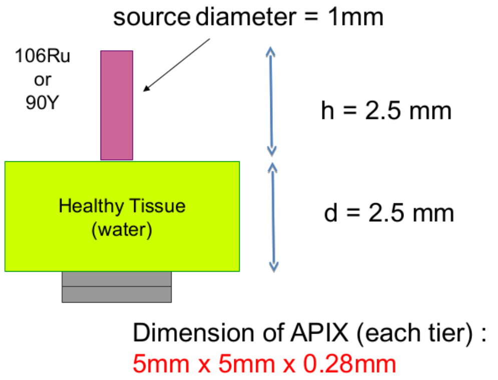
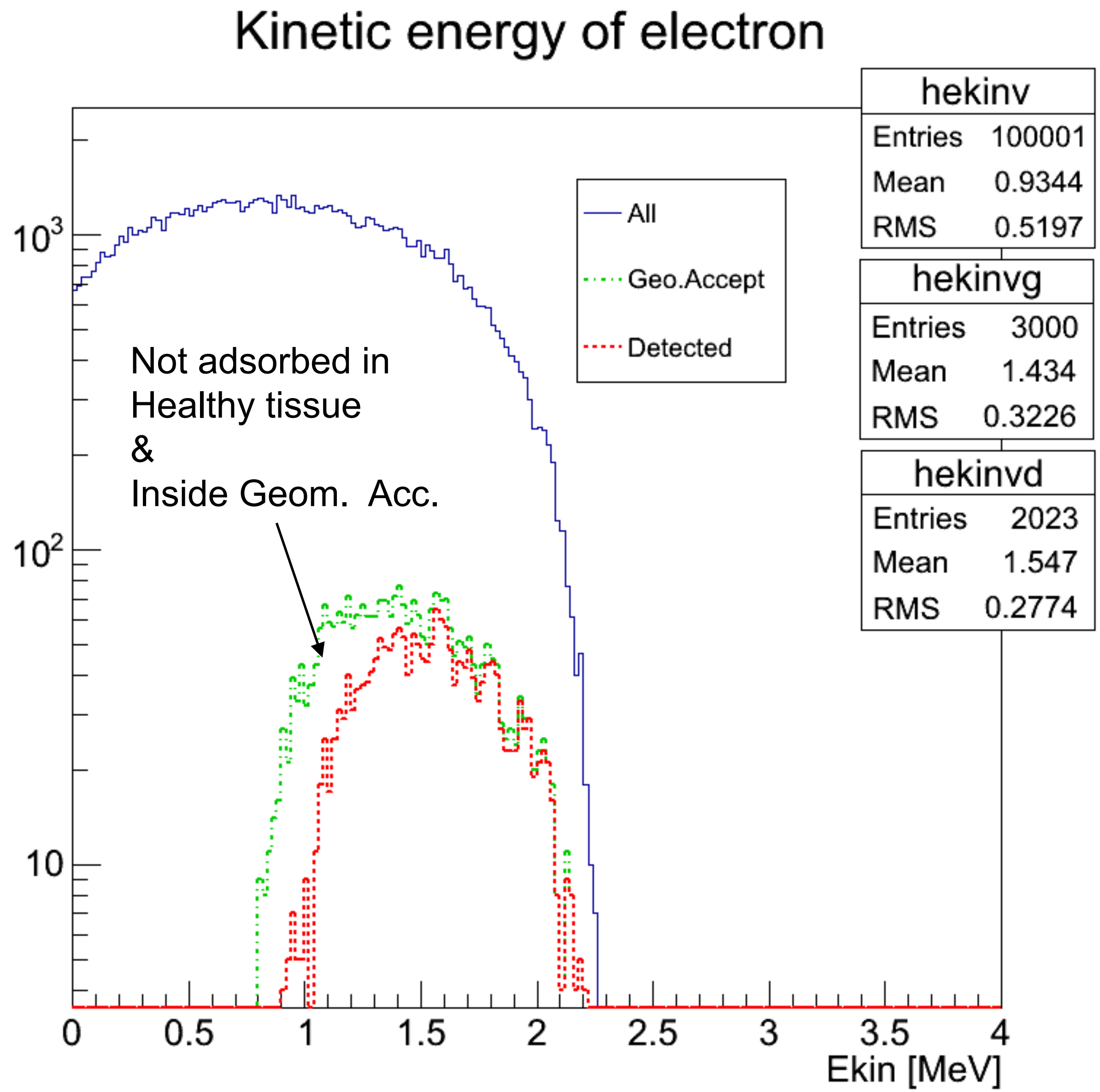
GEANT4 simulations:

- two-tiers
- β- source: 90Y



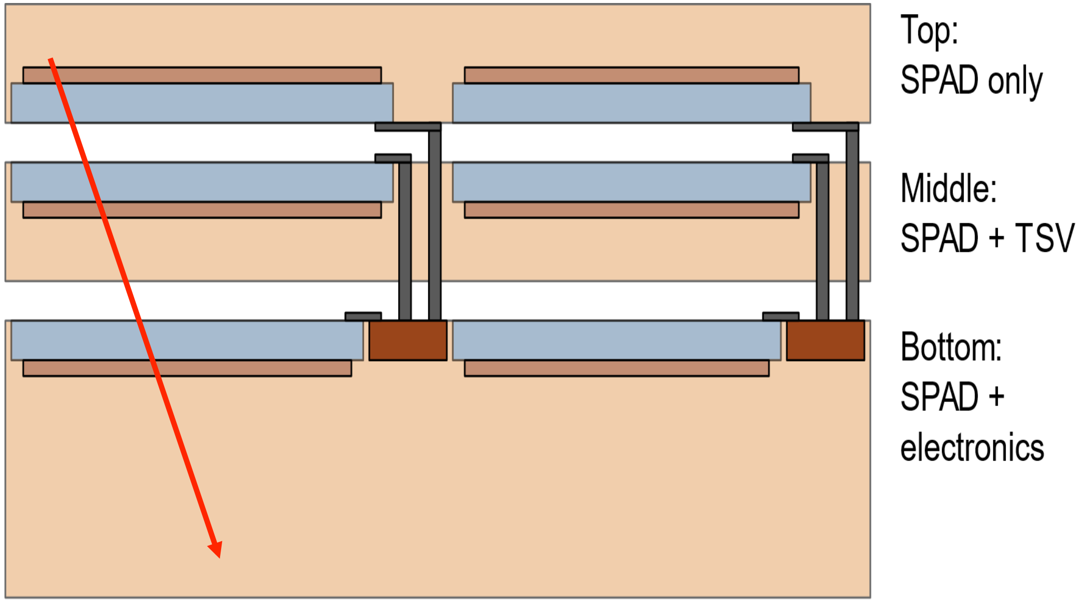
Detected / Geom. Accept = 67.61%

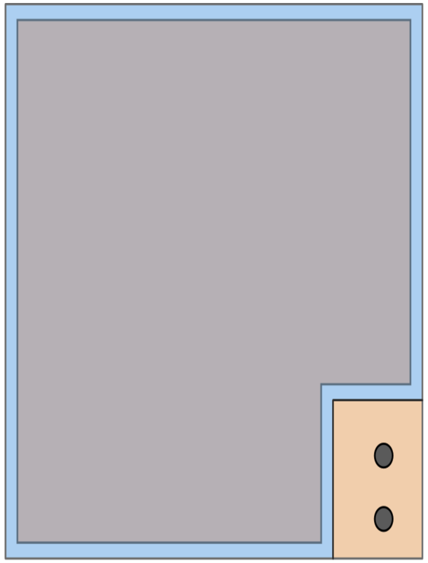


Triple vertical pixels coincidence

Possible advantage of triple coincidence

3-Tiers detector concept:





Pixel layout

TRIPLE/DOUBLE coincidence ratio estimate =

$$3*DCR^{3*}\Delta t^2 \,/\, 2*DCR^{2*}\Delta t \;\; = 1.5*DCR*\Delta t \;\; \mathbf{\sim 10^{-5}}$$

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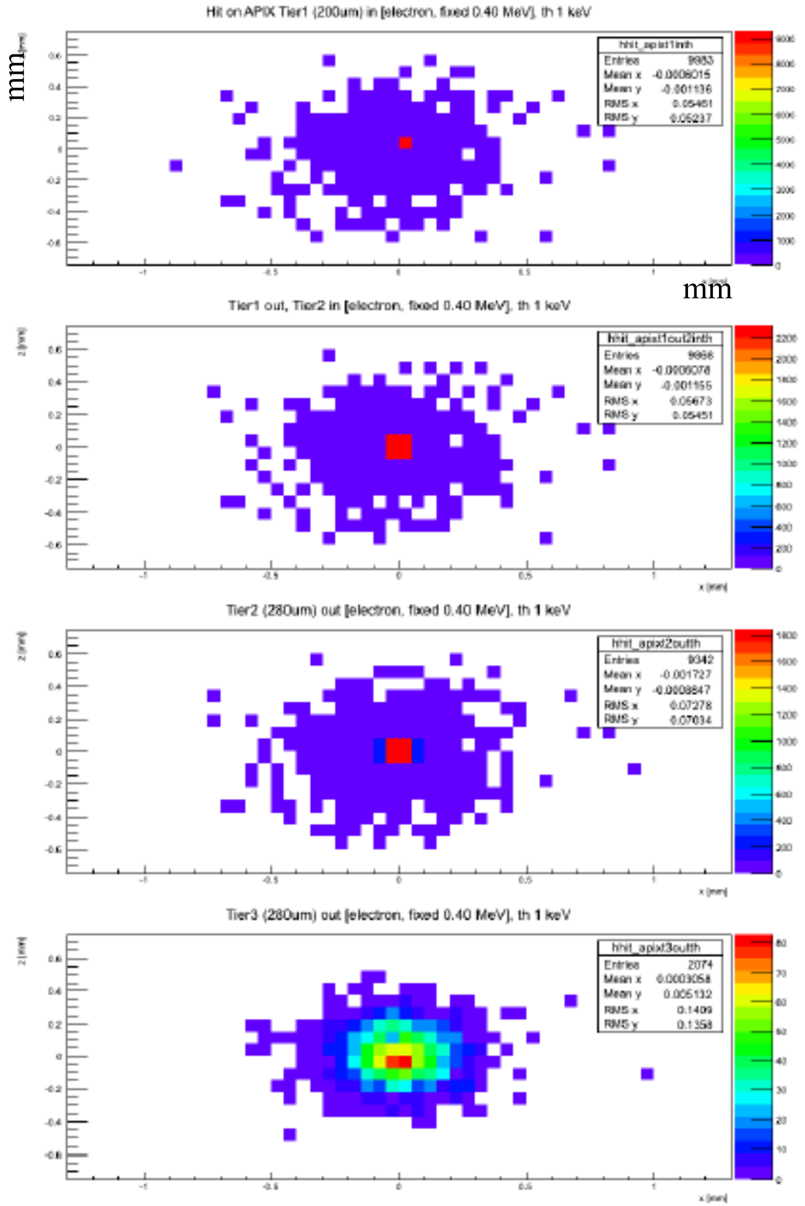
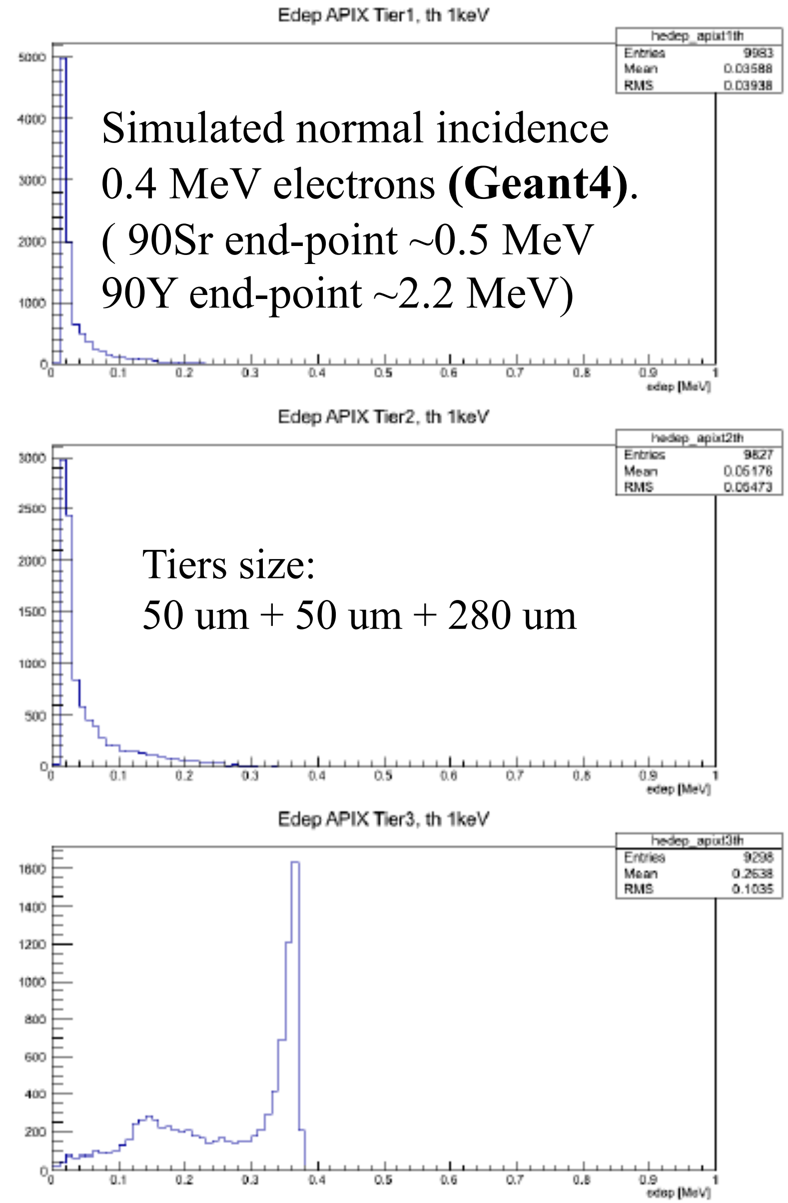
0.4 MeV electron on 3 tiers prototype





Simulated normal incidence
0.4 MeV electrons **(Geant4)**.
(90Sr end-point ~0.5 MeV
90Y end-point ~2.2 MeV)

Tiers size:
50 um + 50 um + 280 um

3 Tiers estimated efficiency (Geant4)

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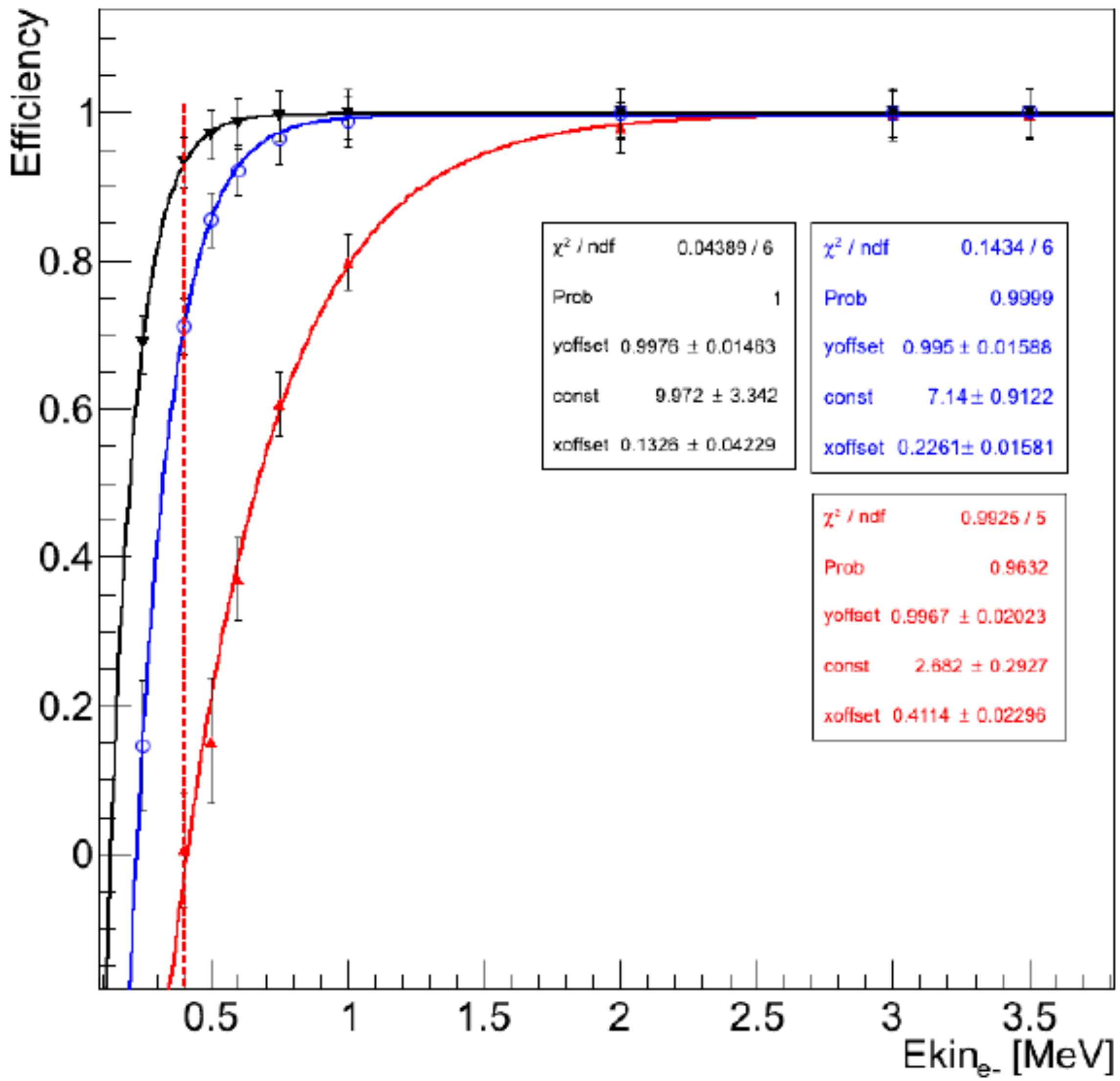
Efficiency vs total thickness of first two layers



- Total thickness (mm) of Tier1+Tier2:

50+50

100+100

280+280

Ongoing analysis and future plans

- Current prototype is fully operative
- First beam test of demonstrator successfully accomplished
- First evidence of high-efficient particle detection
- Accurate radiation hardness test has been performed
- First prototype of β-probe is under construction
- A new optimized detector prototype is now ready for bonding:
  - Larger array
  - Improved fill factor
  - Optimized timing
  - Optimized power consumption
- New test beams are needed to better characterize the actual and the new prototypes

Thanks for your attention!

Bibliography:

[1] N. D'Ascenzo et al, "Silicon avalanche pixel sensor for high precision tracking", 2014 JINST 9 C03027, doi:10.1088/1748-0221/9/03/C03027.

[2] L. Pancheri et al., "First prototypes of two-tier avalanche pixel sensors for particle detection", 14th Vienna Conference on Instrumentation, Vienna, Austria, 15 – 19 February 2016.

[3] A. Ficorella et al., "Crosstalk mapping in CMOS SPAD arrays," 2016 46th European Solid-State Devices Research Conference, ESSDERC, Lausanne, Switzerland, 12 – 15 September 2016.

[4] L. Pancheri et al., "Vertically-integrated CMOS Geiger-mode avalanche pixel sensors," 14th Topical Seminar on Innovative Particle and Radiation Detectors (IPRD16), Siena, Italy, 3 - 6 October 2016.

[5] L. Pancheri et al., Two-Tier Pixelated Avalanche Sensor for Particle Detection in 150nm CMOS, IEEE NSS/MIC, Strasbourg, France, 29 October – 5 November 2016.

[6] L. Pancheri et al., "First Demonstration of a Two-Tier Pixelated Avalanche Sensor for Particle Detection", Journal of the Electron Devices Society, Vol. 5 NO.5, September 2017.

[7] A. Ficorella et al., "Crosstalk Characterization of a Two-Tier Pixelated Avalanche Sensor for Charged Particle Detection", IEEE Journal of Selected Topics in Quantum Electronics Vol. 24 Issue 2 (2017.09.21)

[8] A. Russomando et al., "An Intraoperative $\beta -$ Detecting Probe For Radio-Guided Surgery in Tumour Resection", arXiv:1511.02059v1 [physics.med-ph] 6 Nov 2015

[9] L. Ratti et al. "Dark count rate degradation in CMOS SPADs exposed to X-rays and neutrons", IEEE Transactions on Nuclear Science. Vol. 66 Issue 2 pp. 567-574 (2019) DOI: 10.1109/TNS.2019.2893233.

BACKUP

APIX detects test beam particles

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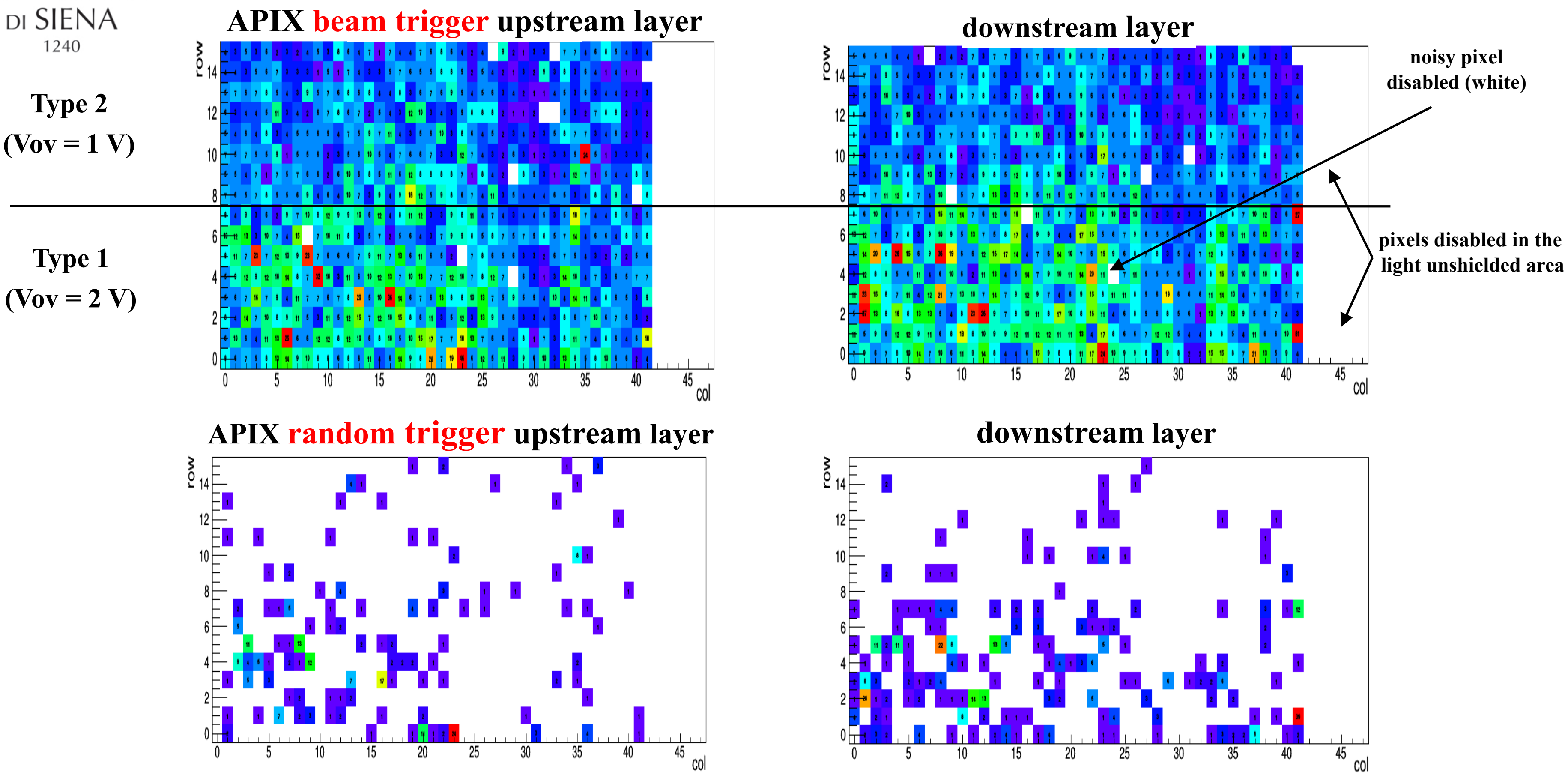
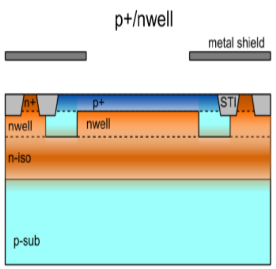
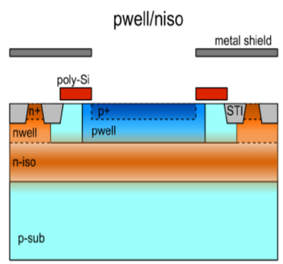


Type 1:
- Shallow step junction
- Active thickness ~ 1µm



Type2:
- Deep graded junction
- Active thickness ~ 1.5µm



APIX detects test beam particles

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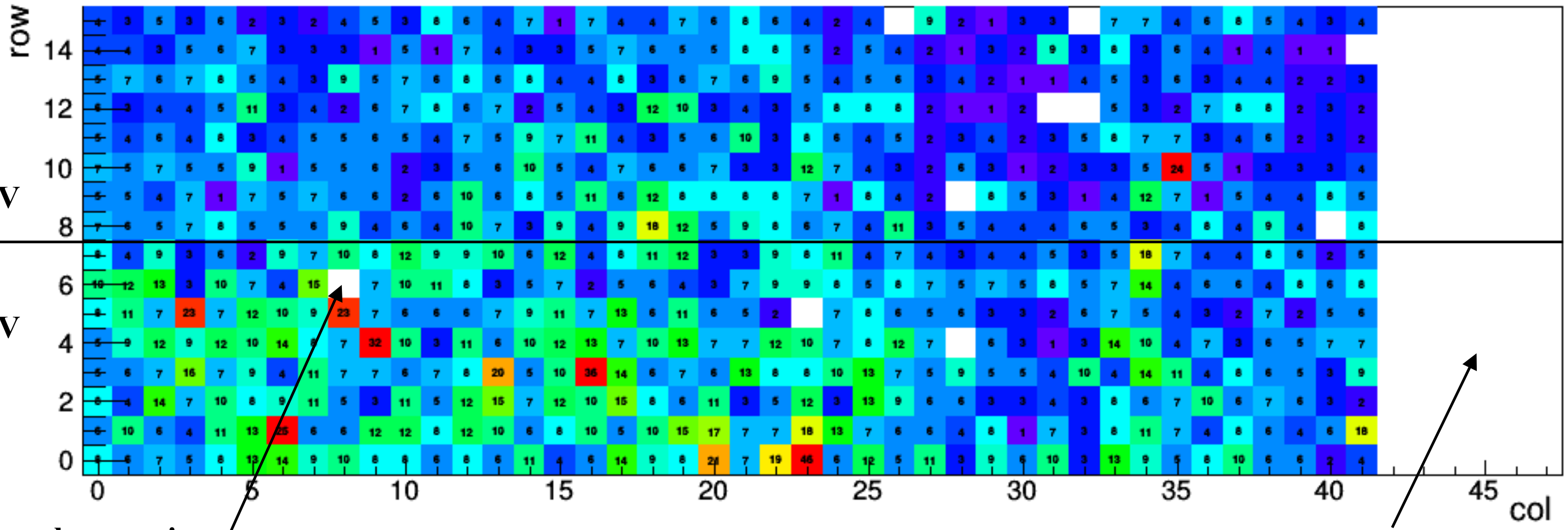
APIX hitmap upstream layer

Type 2
V_{ov} = 1V

Type 1
V_{ov} = 2V



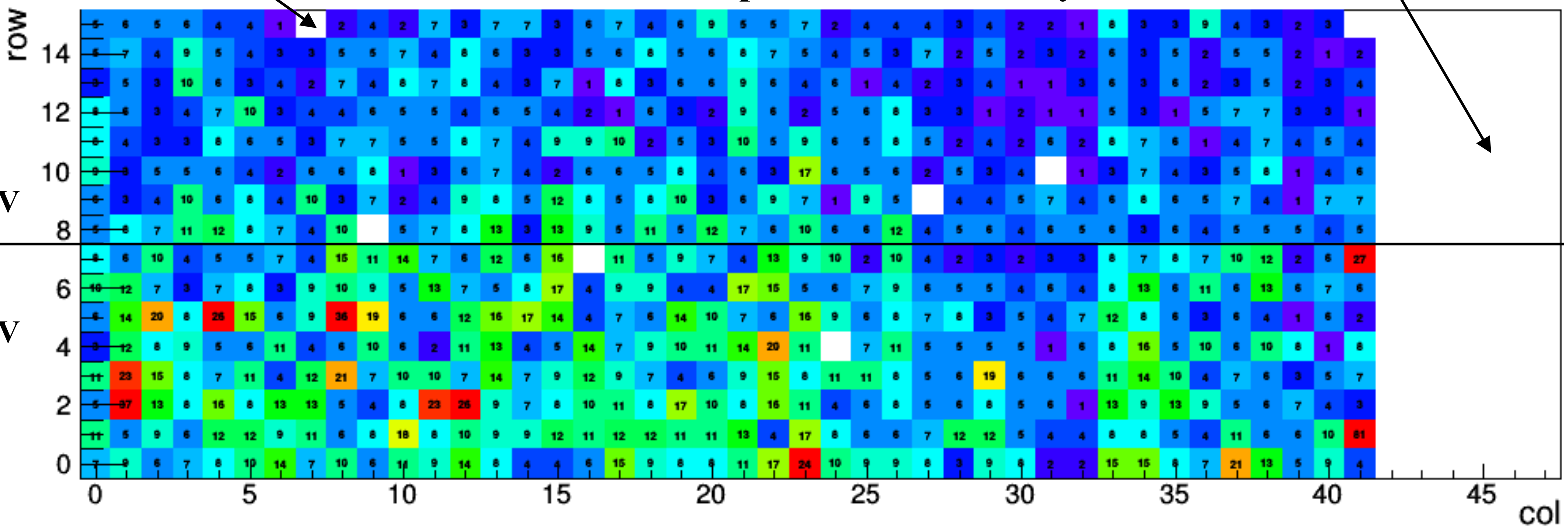
Anomalous noisy pixel disabled

Not light-shielded pixel disabled

APIX hitmap downstream layer

Type 2
V_{ov} = 1V

Type 1
V_{ov} = 2V



APIX detects test beam particles

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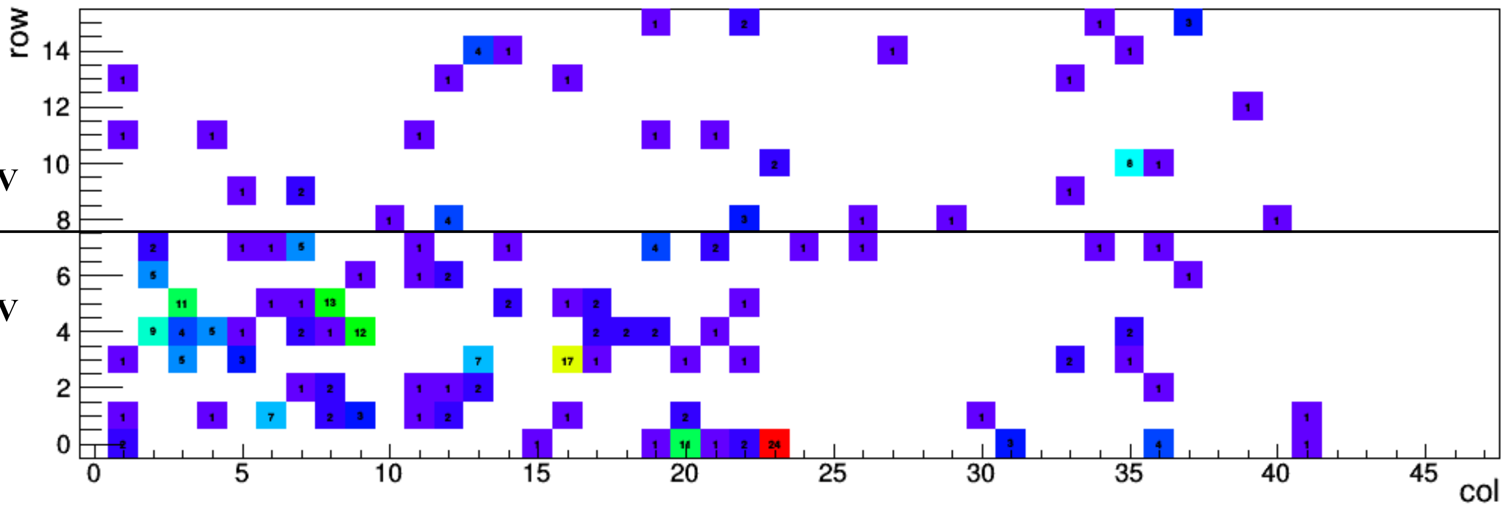
APIX random trigger upstream layer

Type 2 V_{ov} = 1V

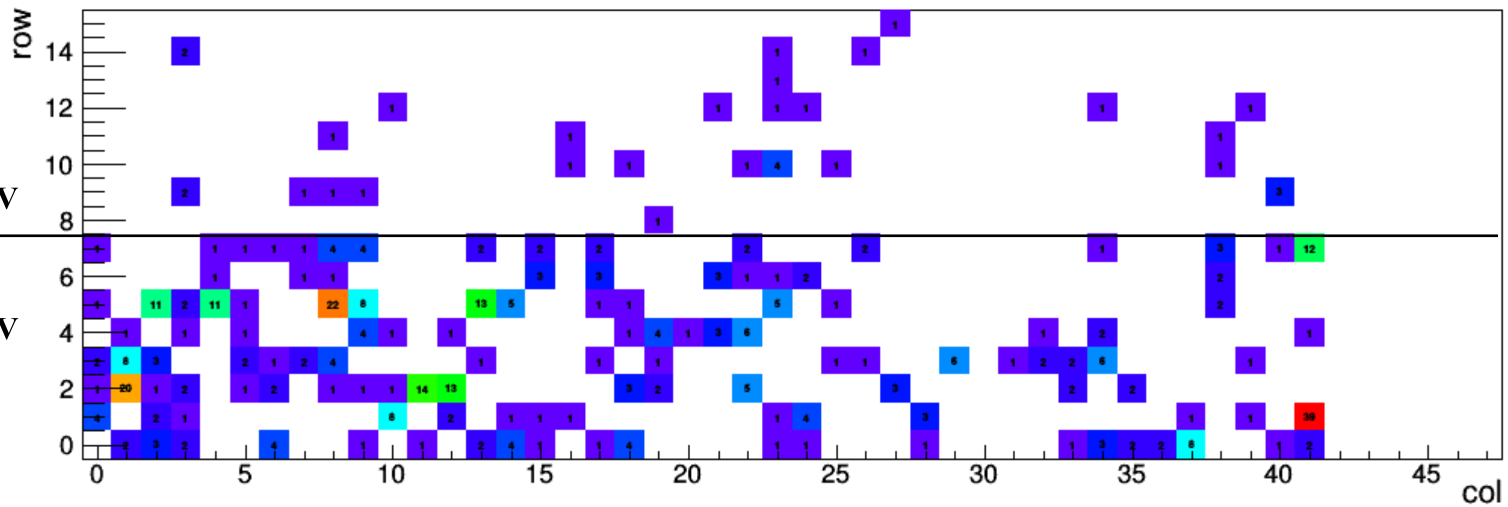
Type 1 V_{ov} = 2V



APIX random trigger downstream layer

Type 2 V_{ov} = 1V

Type 1 V_{ov} = 2V



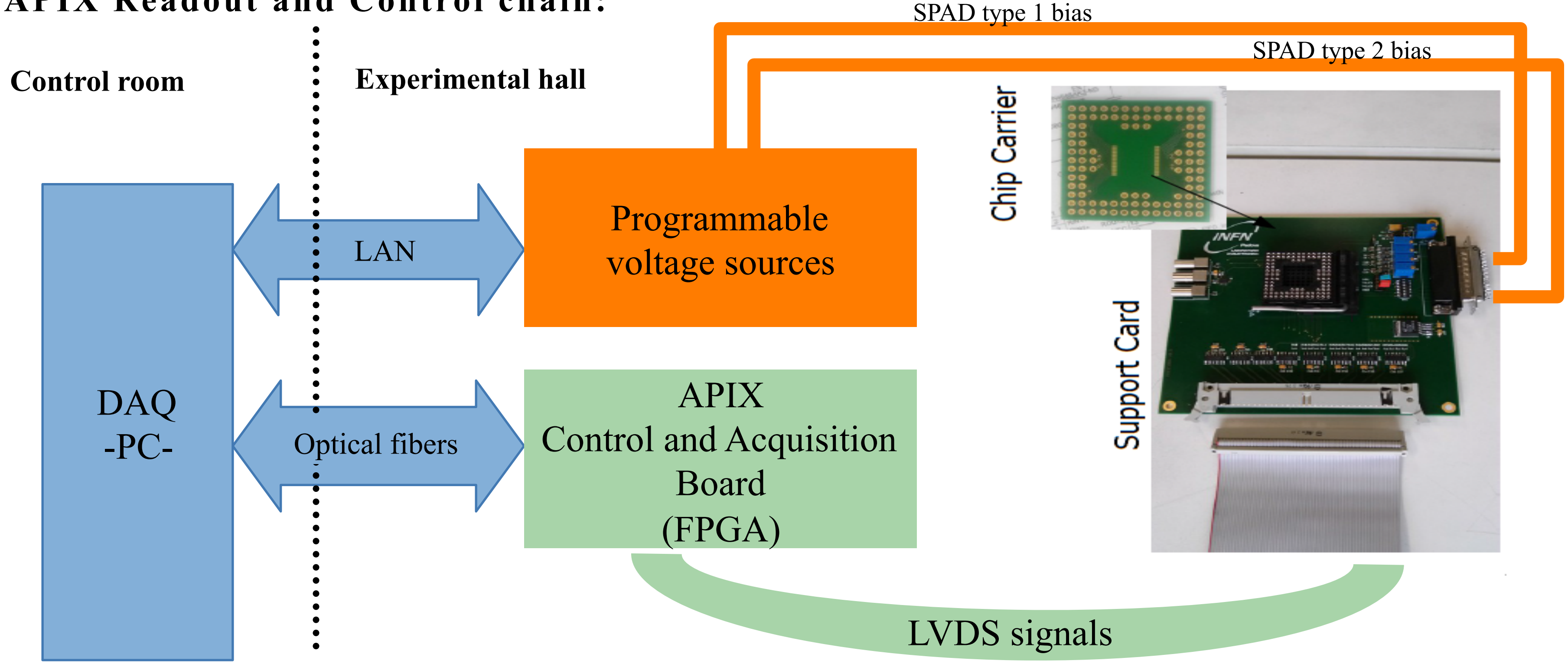
About 3 times less statistics than in the previous hitmaps

APIX Beam Test

First APIX beam test on September of this year

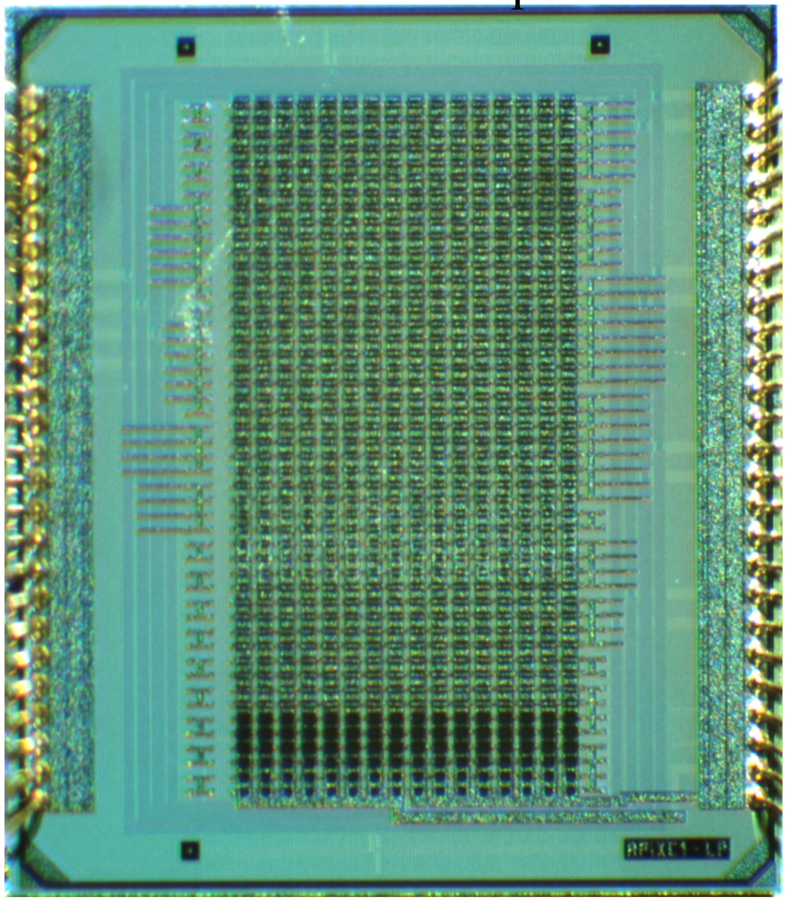
- Test took place at CERN SPS north area facility (H4 beam line)
- Two prototypes of APIX under test + auxiliary Beam Tracker detector
- Positrons and π^+ beams at 50, 100, 150, 200 and 300 GeV
- Good amount of data taken with different APIX voltage settings

APIX Readout and Control chain:

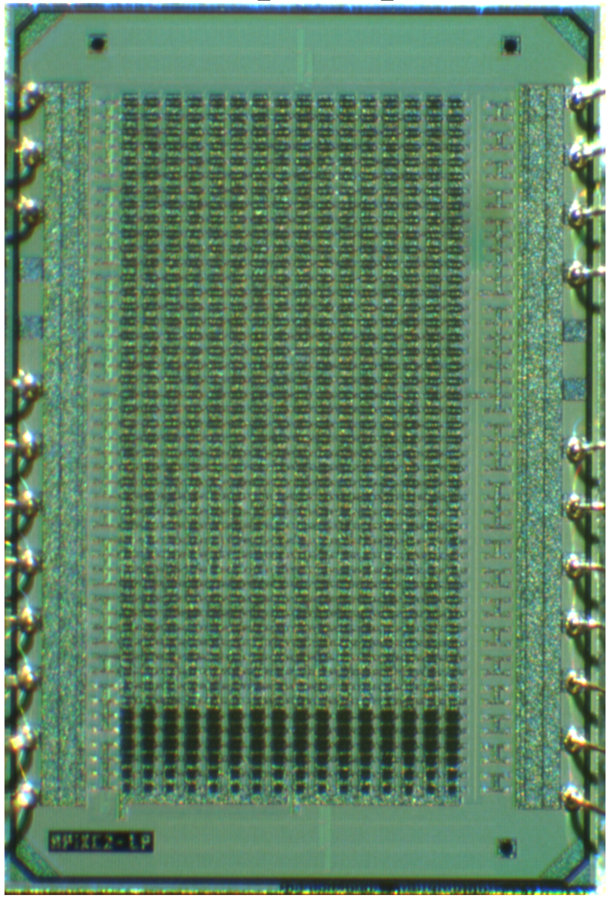


APIX sensor micrographs

Bottom chip



Top chip



SPADs single-photon timing resolution

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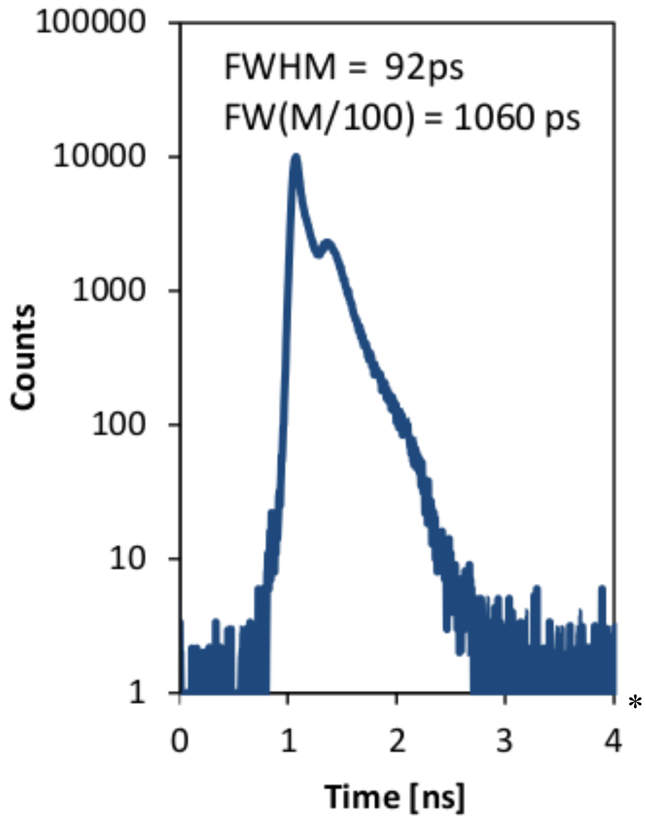
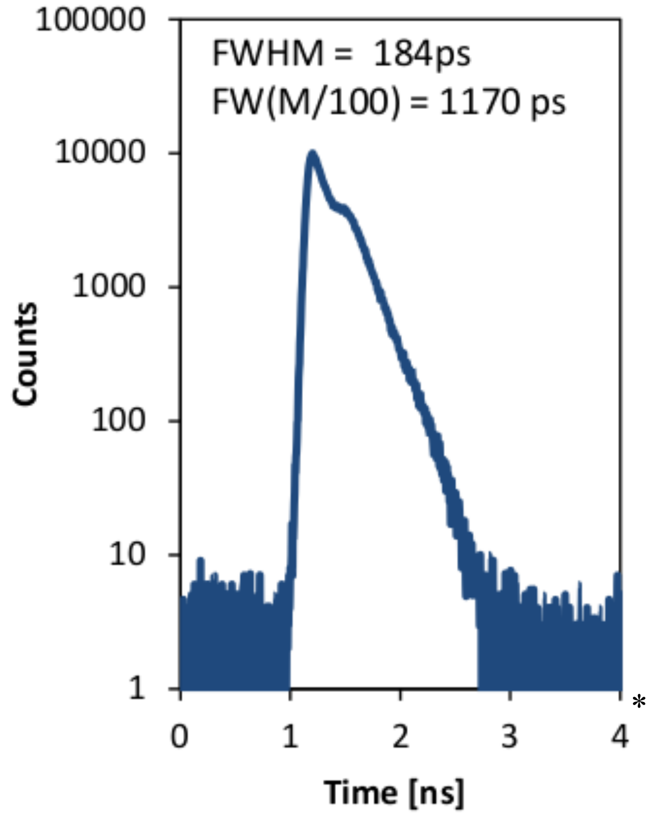
Measured on 10 μm devices, with blue laser (470 nm), 70 ps FWHM

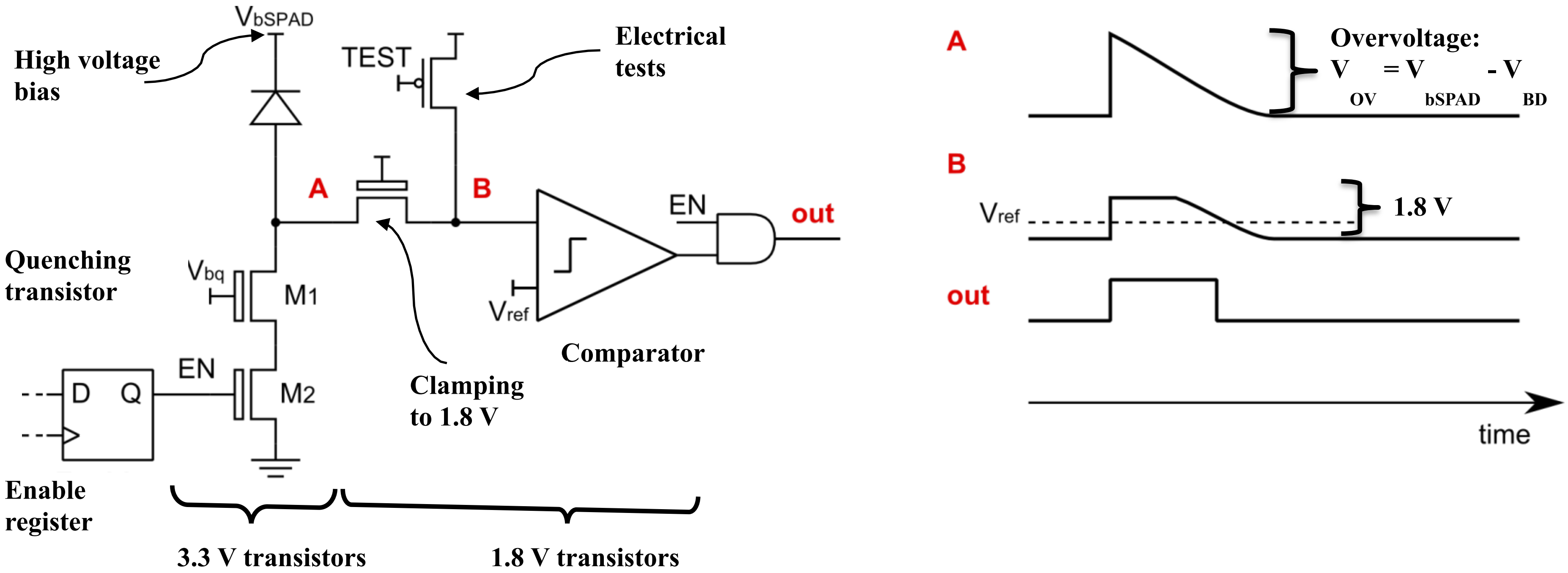




Same types of SPADs used in APIX pixels

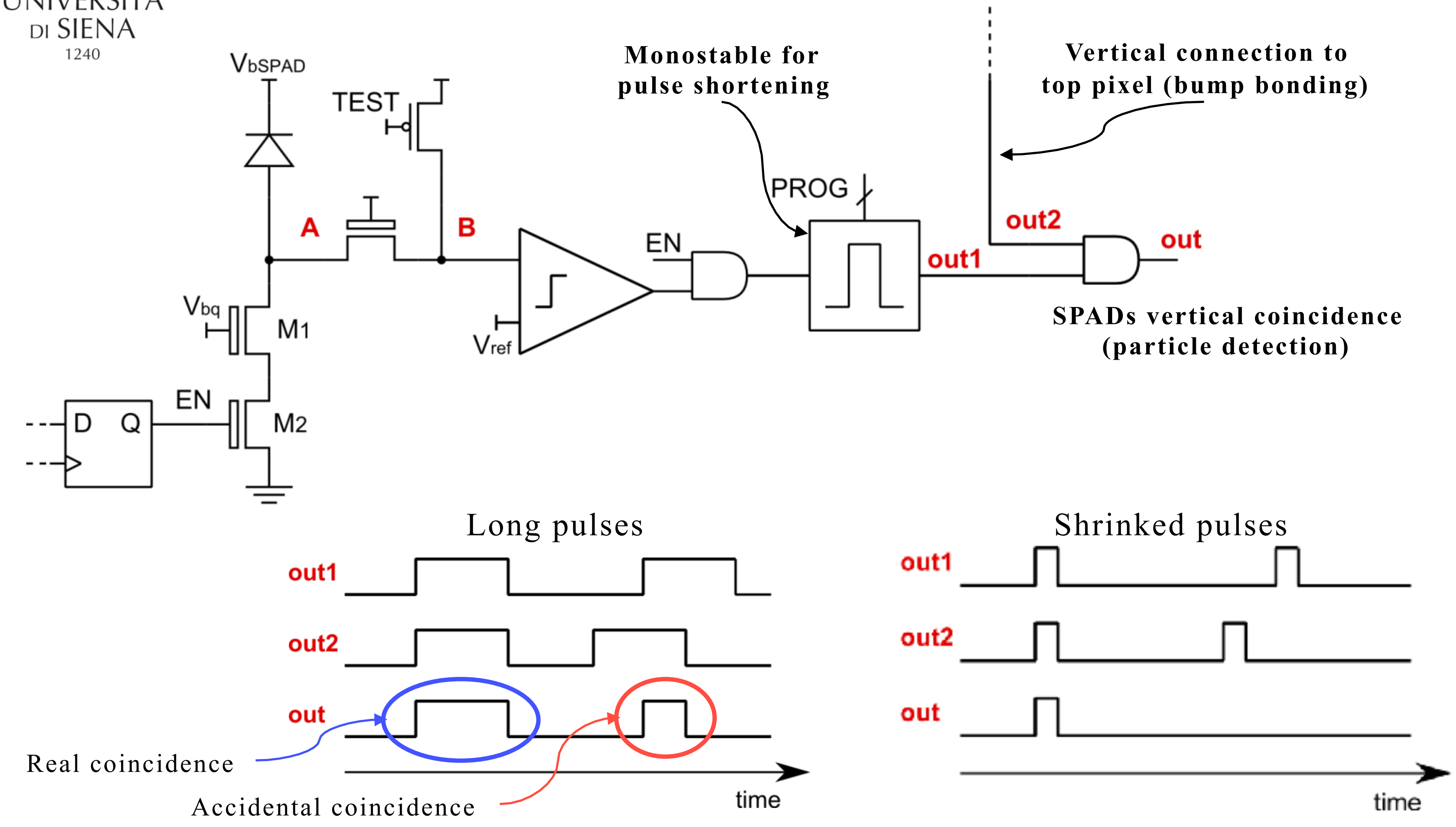
**L. Pancheri, D. Stoppa, "Low-noise Single Photon Avalanche Diodes in 0.15 μm CMOS Technology" Proceedings of IEEE ESSDERC.*

APIX pixel circuitry



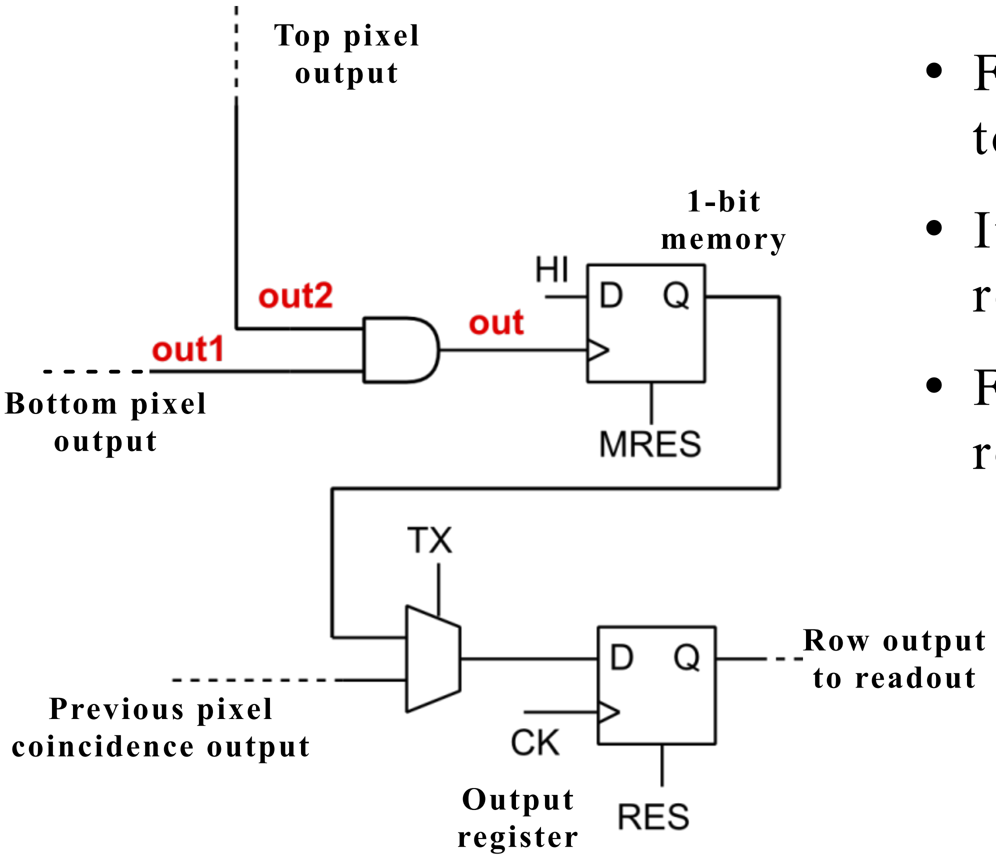
- Front-end transistors: 3.3V ⇒ Maximum overvoltage 3.3V
- Digital circuitry at 1.8V: compact, fast, low-power
- Individual pixel enable/disable: M2 disables recharge, AND gate disables output pulses

APIX pixel: pulse shortening



- Pulse shortening: reduces the rate of accidental coincidence
- Programmable pulse width: **750 ps, 1.5 ns, 10 ns**

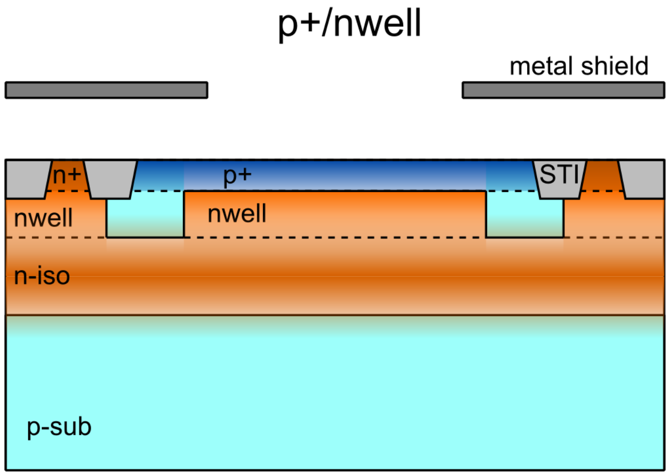
APIX pixel: Data readout architecture

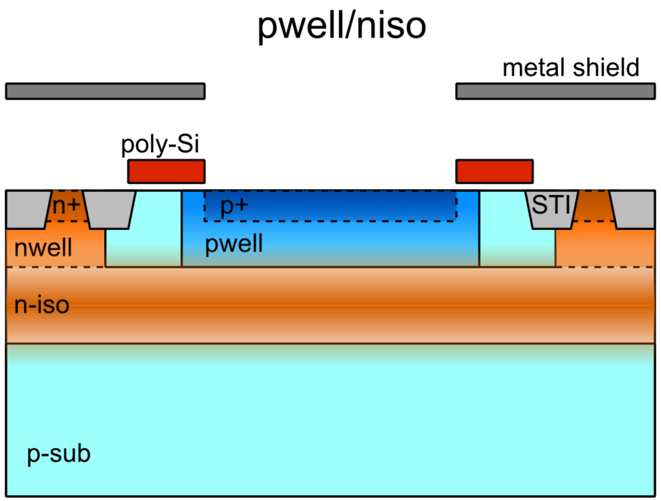


- Each pixel have 1-bit memory and an output register.
- Fast transfer from memory bit to output register
- It is possible to acquire and read-out data at the same time
- Fast parallel read-out of two rows at a time

The SPADs Avalanche detectors

- Two different SPADs architecture in the demonstrator
- Built in standard 150 nm CMOS process
- Avalanche diodes in deep nwell: isolated from substrate





Type 1:

➔ Shallow step junction

➔ Active thickness ~ 1μm

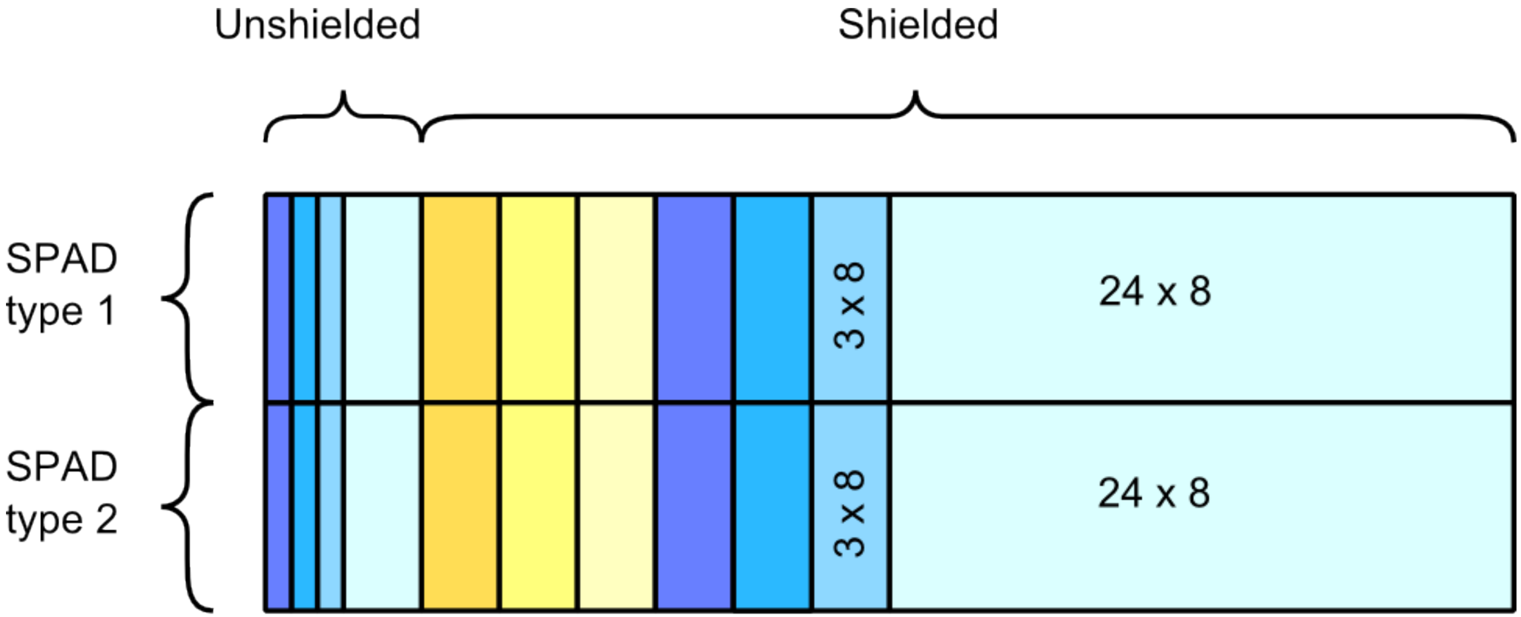
Type 2:

➔ Deep graded junction

➔ Active thickness ~ 1.5μm

*L. Pancheri et al., J. Selected Topics Quantum Electron, 2014

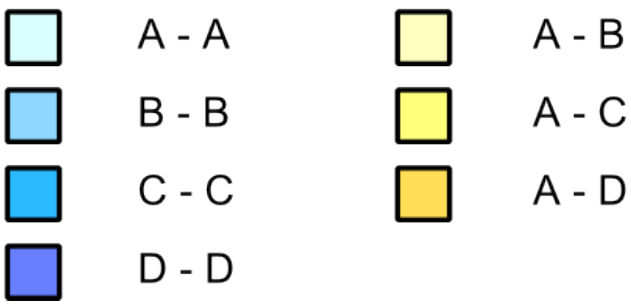
Sensor array partitioning



Array size: 48 x 16

SPAD active area sizes:
- A: 45um
- B: 40um
- C: 35um
- D: 30um

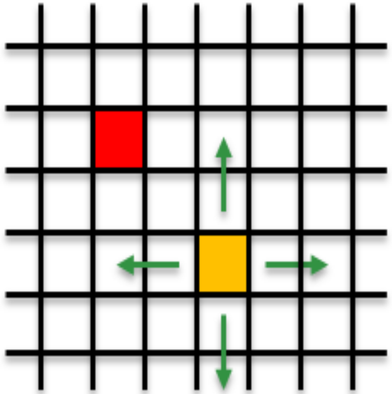
SPAD pairs size combinations (Chip1 - Chip2)



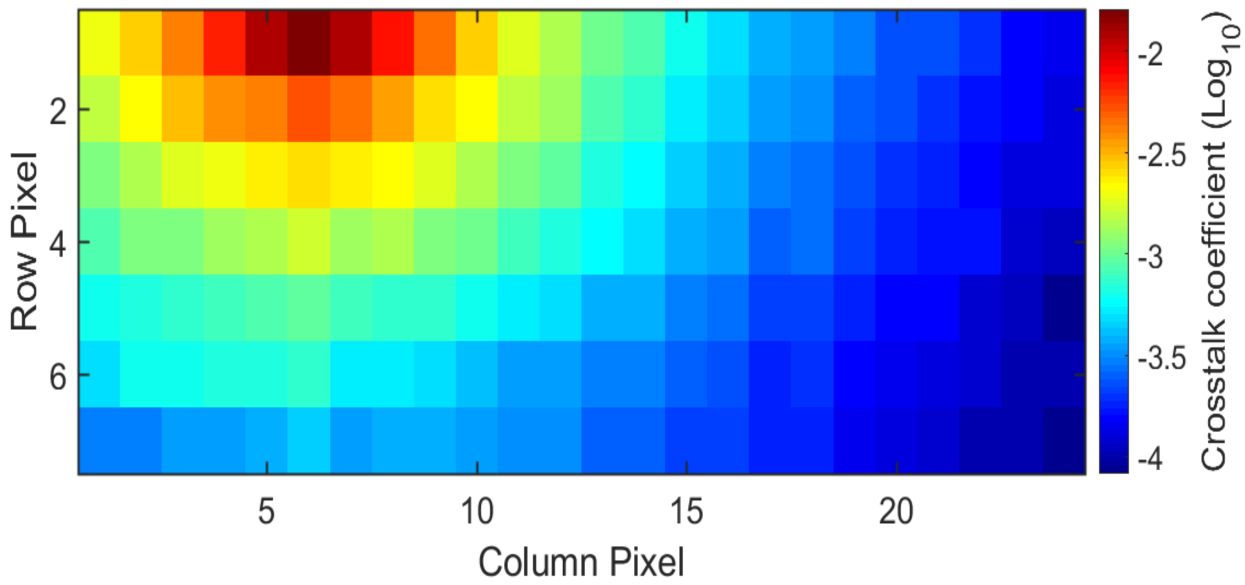
Crosstalk characterization

- Crosstalk coefficient

$$CR_m = DCR_e \cdot DCR_d \cdot 2\Delta T + \mathbf{K} \cdot (\, DCR_e + DCR_d \,)$$



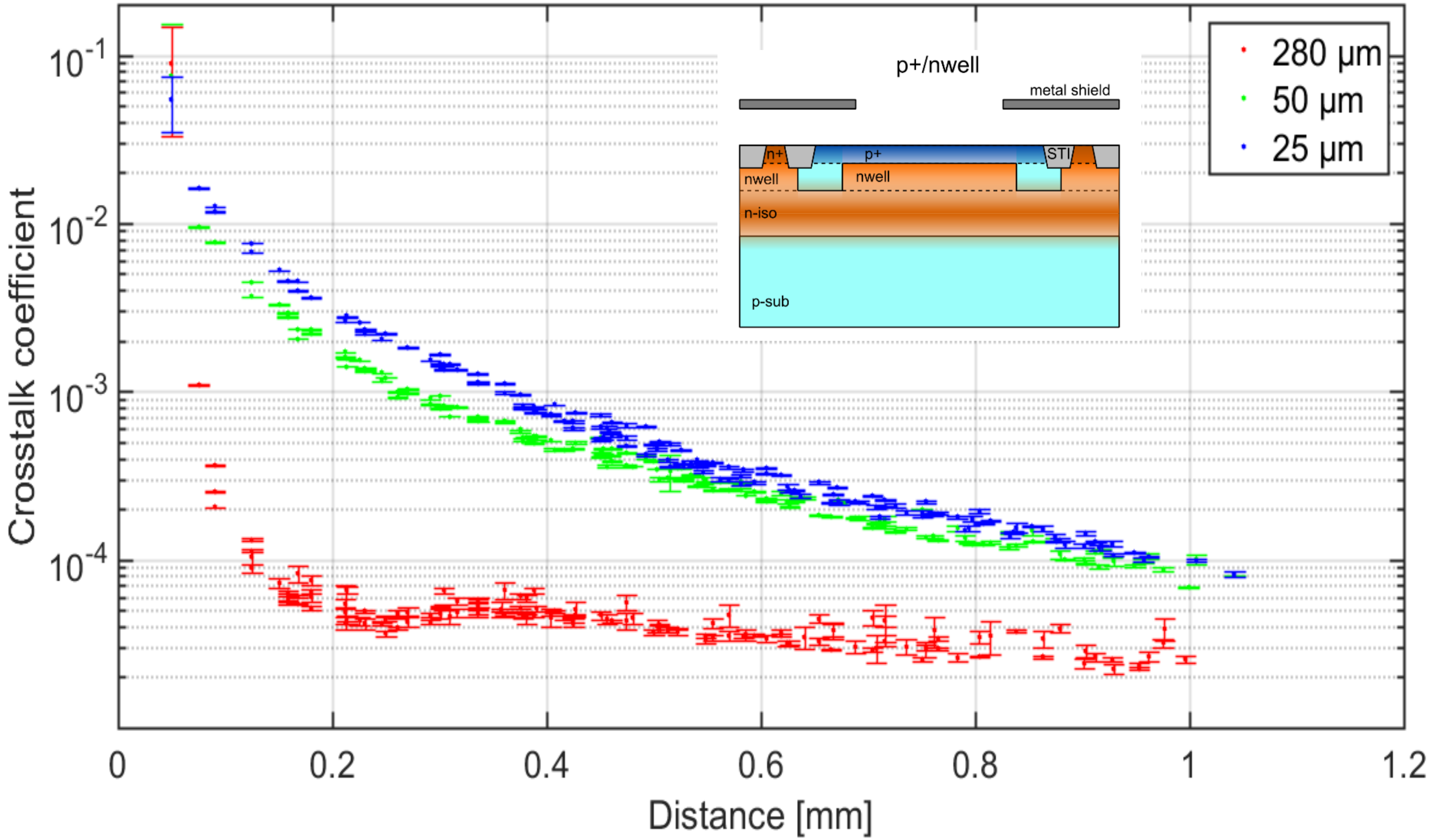
- **Emitter** (fixed)
- **Detector** (scan)



Crosstalk map – Type 1, 25µm thickness

*courtesy of L. Pancheri

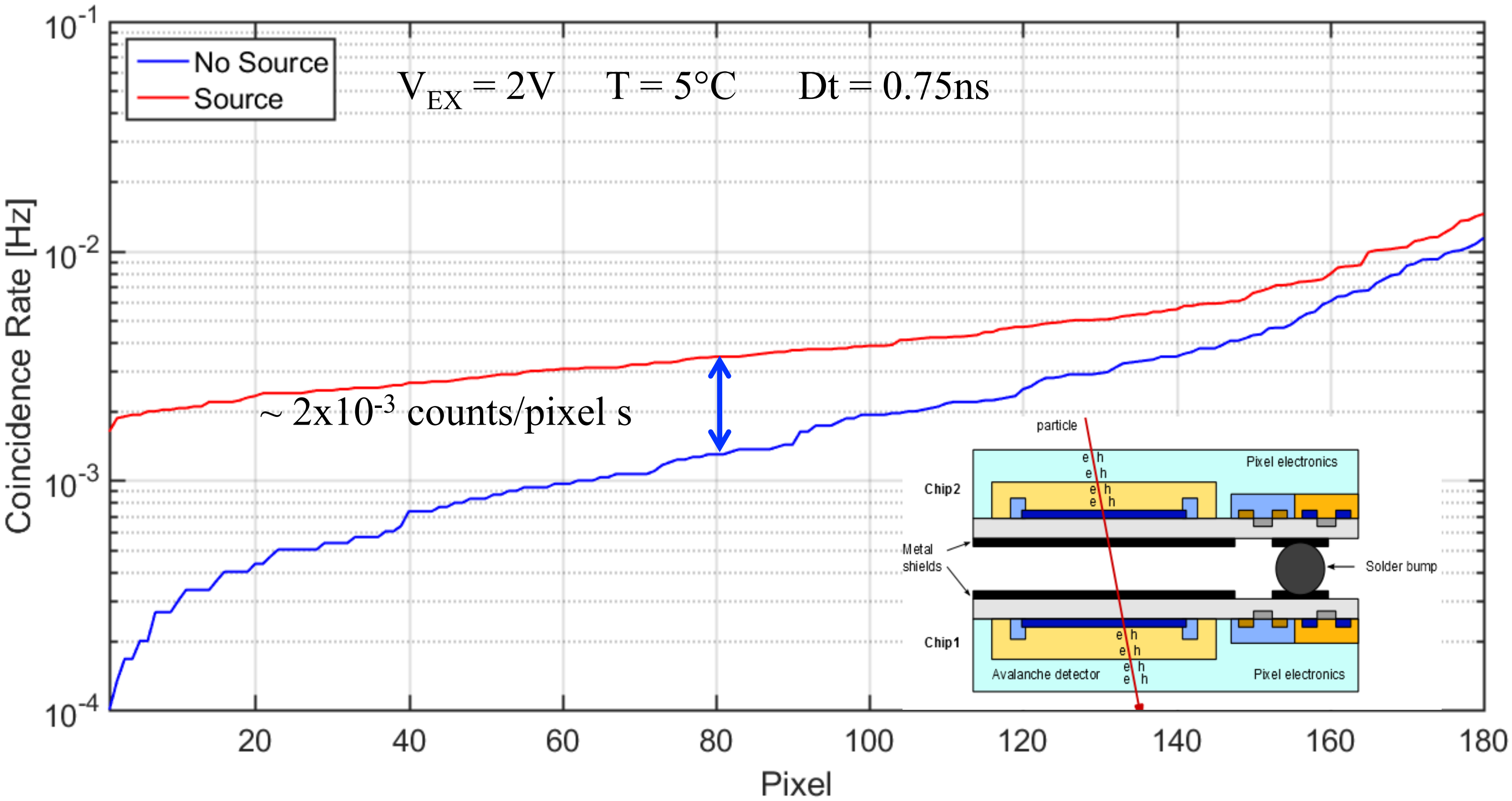
Crosstalk vs substrate thickness



*courtesy of L. Pancheri

β-source measurements

^{90}**Sr** β source – 37kBq at 2mm distance from sensor



Count rate ~**0.5 counts/s mm²**

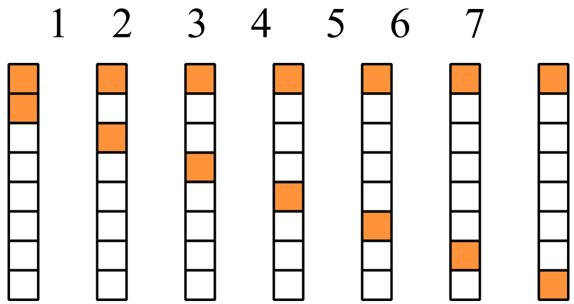
*courtesy of L. Pancheri

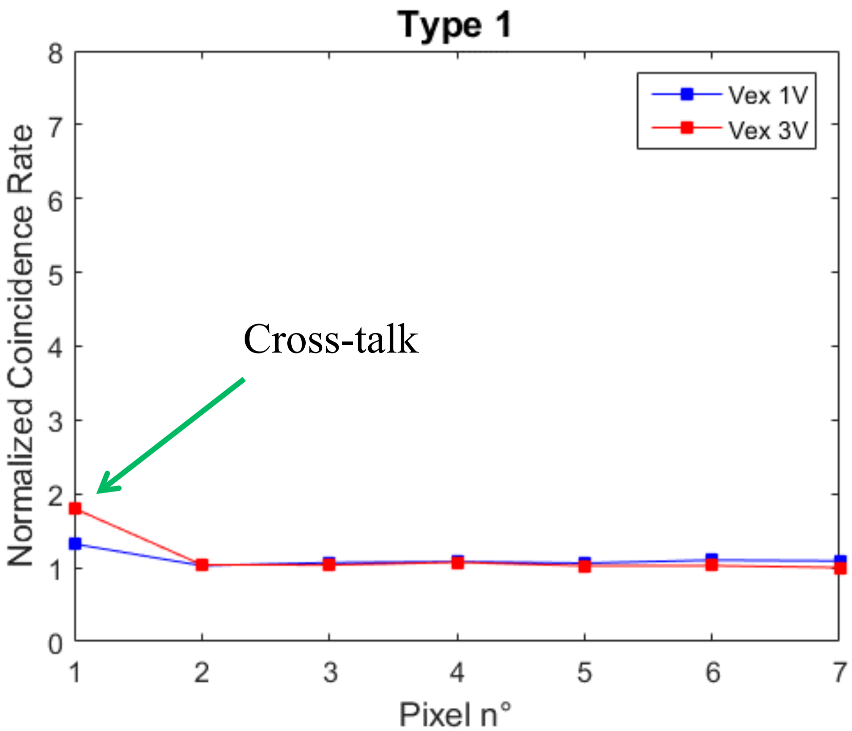
Coincidence detection

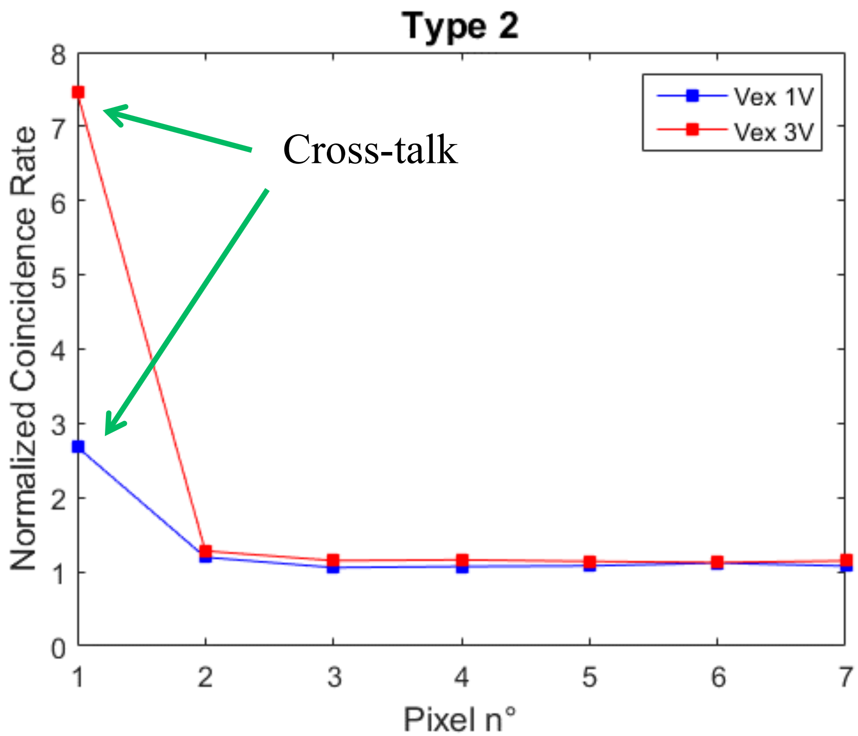
Count rate in coincidence between two pixels in the same column

Normalized rate:

$$\frac{CR_{Meas}}{2 \cdot CR_1 \cdot CR_2 \cdot \Delta T}$$

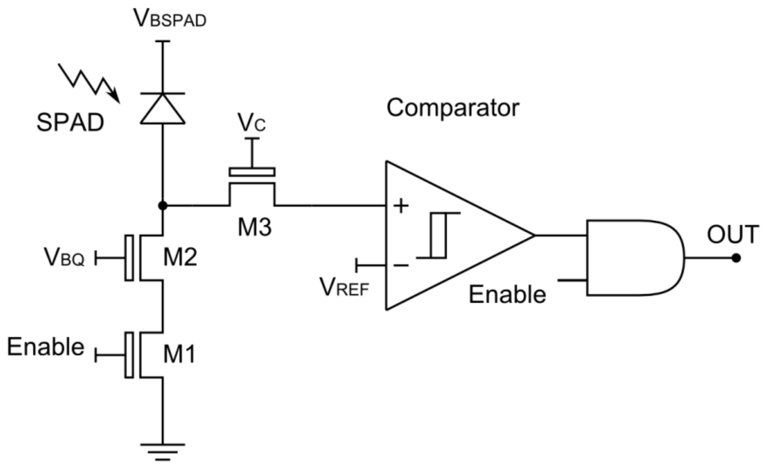


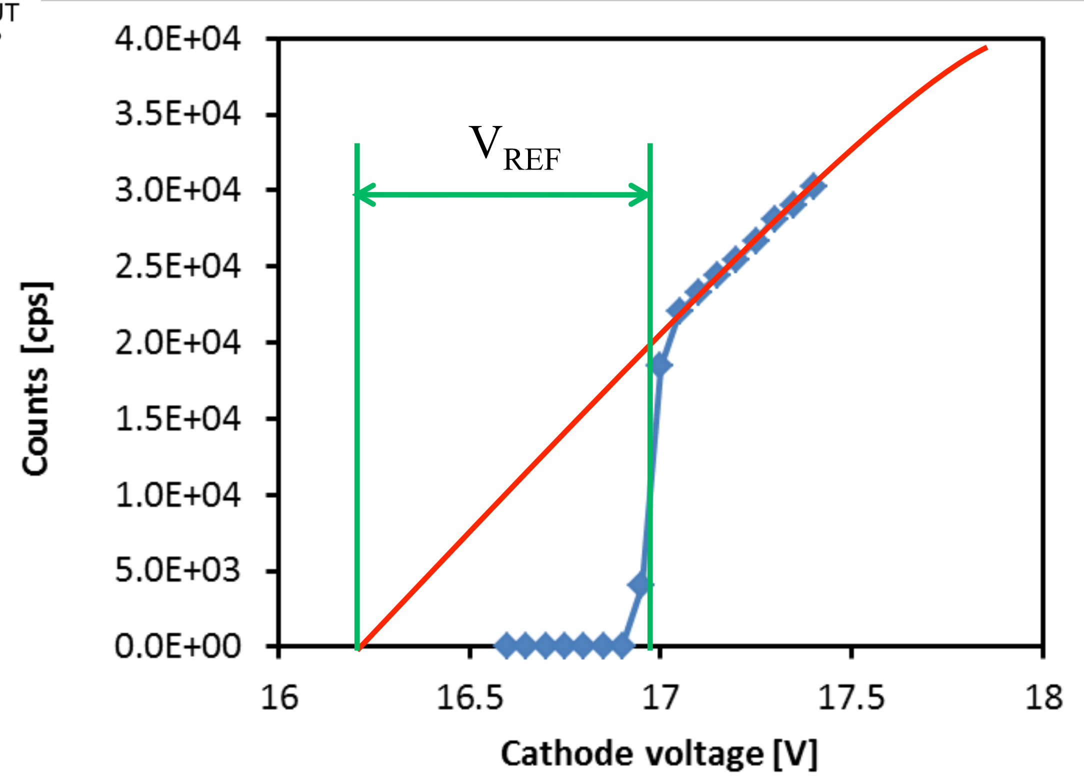




*courtesy of L. Pancheri

VBD extraction method





V_{BD} extraction from I-V curves: not possible

V_{BD} extracted from the dark count rate vs. voltage curve

*L. Pancheri et al., Proc. IEEE ICMTS, 2014

Preliminary Radiation Test with neutrons

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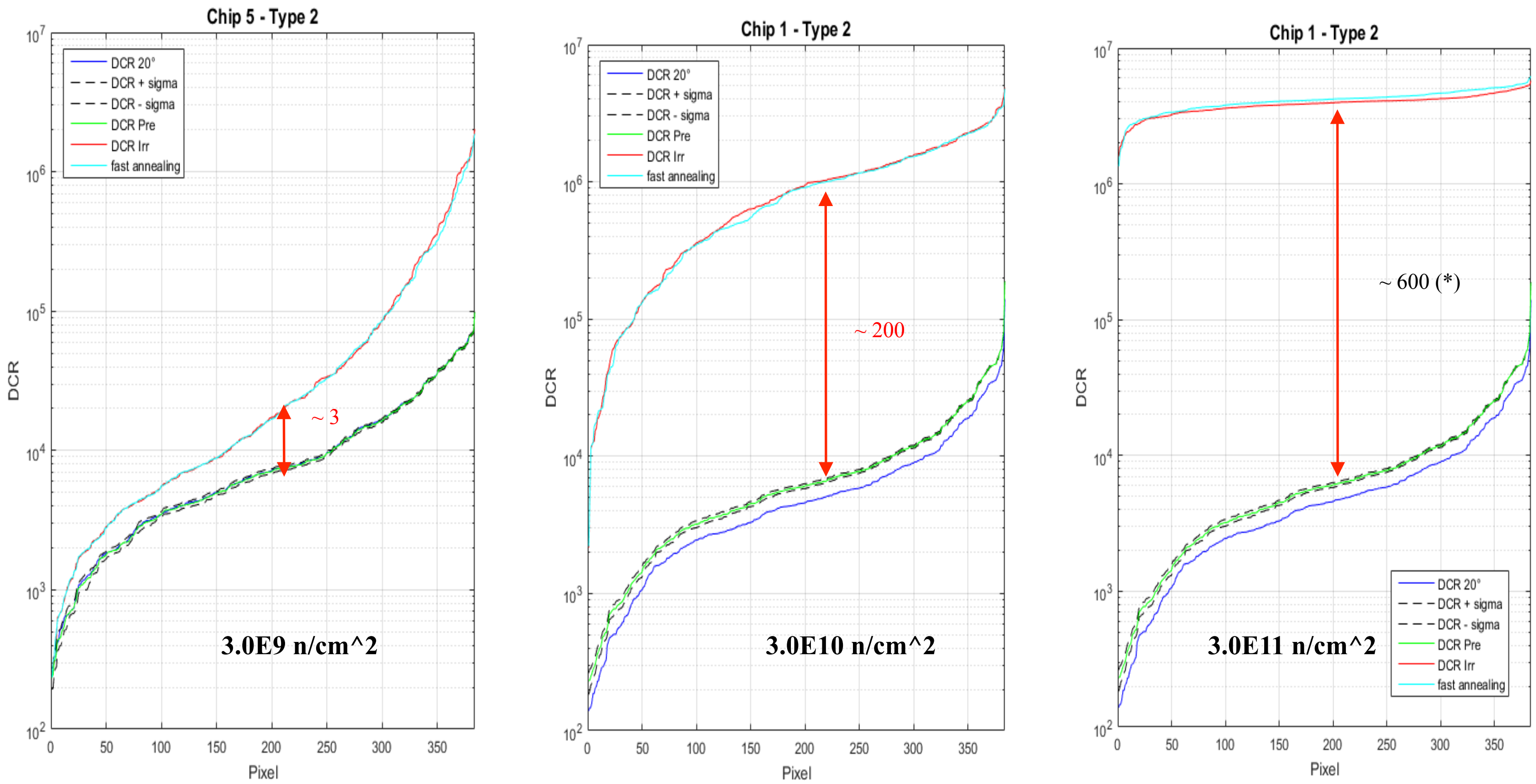
- Irradiation at Legnaro National Laboratory (5 MeV proton on Be target) in June 2017
- neutron spectrum with energy from 0.5 to 3 MeV
- max fluence: 3×10^{11} neq /cm^2
- annealing at room temperature

DCR distribution for different fluences before and after beam exposure



(*) Saturation for high DCR due to dead time (> 100ns during rad. test)

Summary

Strengths:

- Fine segmentation (tens of microns)
- Digital readout
- Low material budget (sensors can be thinned to a few microns)
- Timing resolution
- Low power consumption and low bias voltages

Weaknesses:

- Limited Radiation tolerance
- Geometric efficiency (due to surface device guard ring and electronics)
- Cost and accessibility of 3D integration processes