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Radiation characterization of two large and fully depleted CMOS pixel matrices fabricated in 150 nm and 180 nm technologies

T. Hirono[1], M. Barbero[3], P. Barrillon[3], I. Berdalovic[2], S. Bhat[3], C. Bespin[1], P. Breugnon[3], I. Caicedo[1], R. Cardella[2], Z. Chen[3], Y. Degerli[4], J. Dingfelder[1], S. Godiot[3], F.Guilloux[4], T. Hemperek[1], F. Hügging[1], F.J. Iguaz[4], H. Krüger[1], T. Kugathasan[2], K. Moustakas[1], P. Pangaud[3], H. Pernegger[2], P. Riedler[2], A.Rozanov[3], P. Rymaszewski[1], E, Schioppa[2] P. Schwemling[4], W. Snoeys[2], C. Solans[2] C.M. Tobon[2], M. Vandenbroucke[4], T. Wang[1], S. Zhang[1], and N. Wermes[1]

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INTRODUCTION

- ATLAS vertex tracker will be upgraded for High Luminosity-LHC operation: ATLAS ITk
  - Large area will be covered by pixel detector ~O(10m^2)
    - Monolithic CMOS active pixel sensor = high production throughput (*cf.* Hybrid detector needs fine-pitch bump bonding)

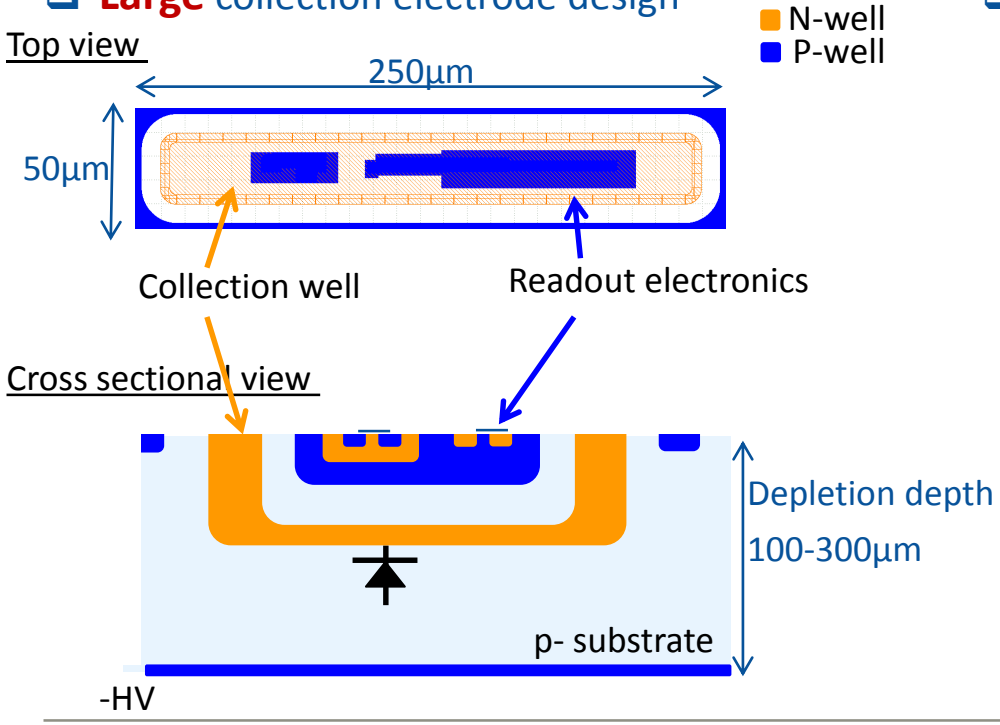
      → A complementary option for the outer layers
  - Charge collection by drift is mandatory for high radiation hardness and fast signal response
    - Depleted monolithic CMOS active pixel sensors (DMAPS) have been developed
      - Two DMAPS designs
        - Large collection electrode
        - Small collection electrode

ATLAS pixel detector requirements

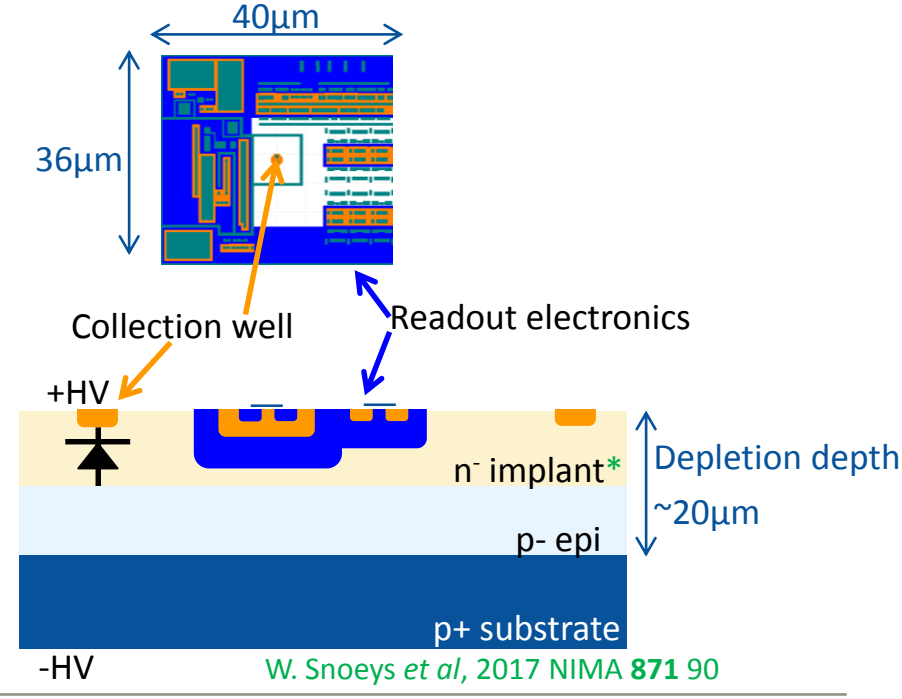
	ATLAS-LHC	ATLAS-HL-LHC	
		Outer	Inner
Timing [ns]	25	**25**	25
Particle Rate [kHz/mm^2]	1000	**1000**	10000
NIEL [n_{eq}/cm^2]	2x10^{15}	**10^{15}**	2x10^{16}
TID [Mrad]	80	**50-100**	>500

LARGE AND SMALL ELECTRODE DESIGN

❑ **Large** collection electrode design



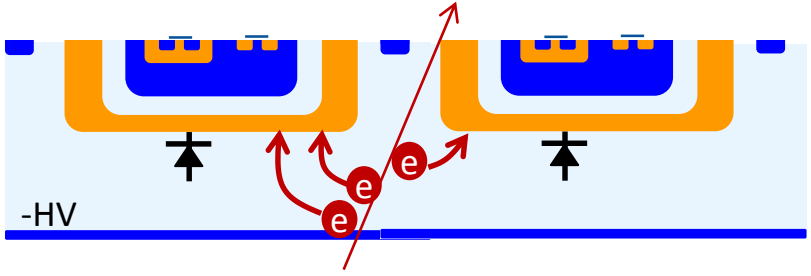
❑ **Small** collection electrode design



W. Snoeys *et al*, 2017 NIMA **871** 90

LARGE AND SMALL ELECTRODE DESIGN

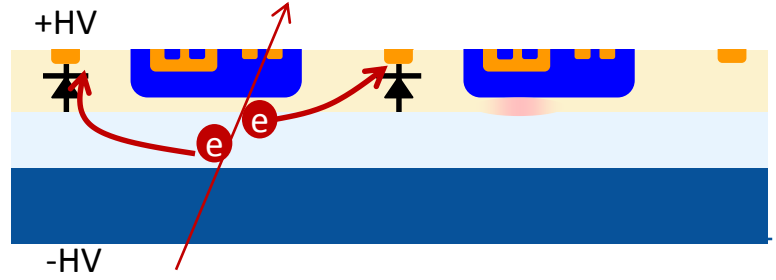
❑ **Large** electrode design
= Small gap between electrode
= Readout electronics is isolated from substrate



– Short charge drift path
→ High radiation hardness

– High bias voltatge + highly resistive wafer
→ Large depletion area
→ Large signal

❑ **Small** electrode design
= Gap depends on readout electronics size



– Long charge drift path

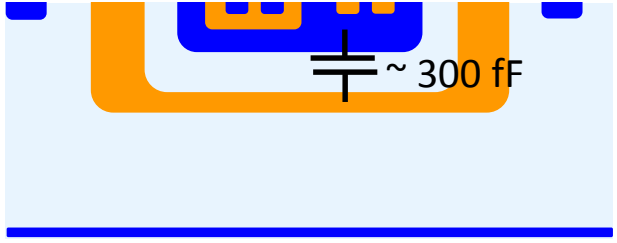
– The electric field directing the collection electrode is weak at the pixel edge and zero at the pixel corner

LARGE AND SMALL ELECTRODE DESIGN

❑ **Large** electrode design =Large C_{det}

Response time of amplifier: $\tau_{CSA} \approx \frac{1}{g_m}\frac{C_{det}}{C_f}$

Noise: $ENC^2_{thermal} \approx \frac{4}{3}\frac{kT}{g_m}\frac{C}{\tau_f}$



→ High power consumption

→ Delicate electronics design to aviod signal cross coupling between the colleciton node and readout electronics

❑ **Small** electrode design =Small C_{det}

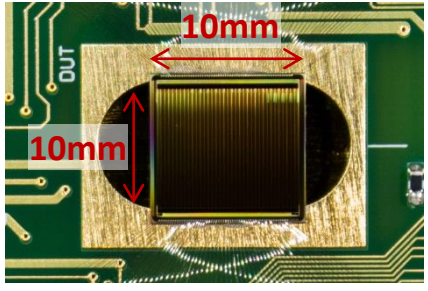
Signal to noise: $\frac{S}{N} \approx \frac{Q/C_{det}}{\sqrt{g_m}} \sim \frac{Q/C_{det}}{\sqrt[m]{P}}, \quad P \sim \left(\frac{Q}{C_{det}}\right)^{-m}$

→ Low power consumption

→ Less sensitive to cross coupling

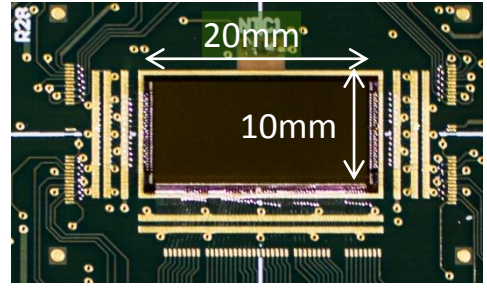
FULLY-MONOLITHIC LARGE-SCALE PROTOTYPES

❑ **Large** electrode design: LF-Monopix



- Fully monolithic
- 150nm CMOS process
- Sensitive volume: >2kΩcm highly resistive substrate
  Thickness = 100µm, 200µm (725µm)
- Pixel size: 250µm × 50µm
- Bonn/CPPM/IRFU

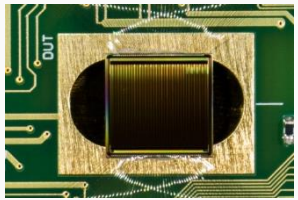
❑ **Small** electrode design: TJ-Monopix



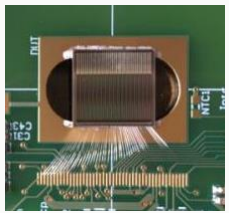
- Fully monolithic
- 180nm CMOS process w/ n^- implant
- Sensitive volume: n^- implant + 1kΩcm epi-layer
  Thickness = ~20µm
- Pixel size: 40µm × 36µm
- Bonn/CERN

IRRADIATION OF PROTOTYPE CHIPS

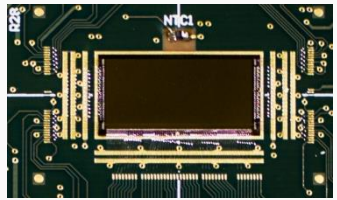
- **Large** electrode design: LF-Monopix



  - Neutron: $10^{15} n_{eq}/cm^2$ (JSI reactor)
    - Irradiated w/o powering at RT
    - Annealed 80min @60°C
  - Proton: $10^{15} n_{eq}/cm^2$, 50Mrad (CERN)
    - Irradiated w/o powering at RT
    - Annealed 80min @60°C
  - X-ray: 0-50Mrad (KIT X-ray tube) ← A prototype w/o digital R/O logic
    - Irradiated w/ powering
    - Measrued at each TID



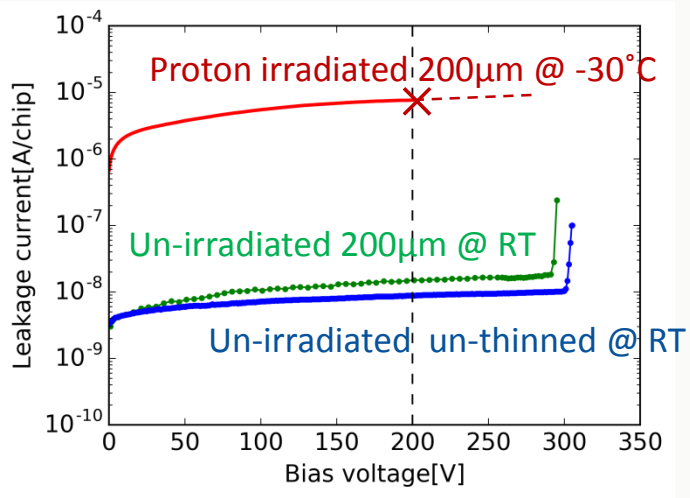
- **Small** electrode design: TJ-Monopix



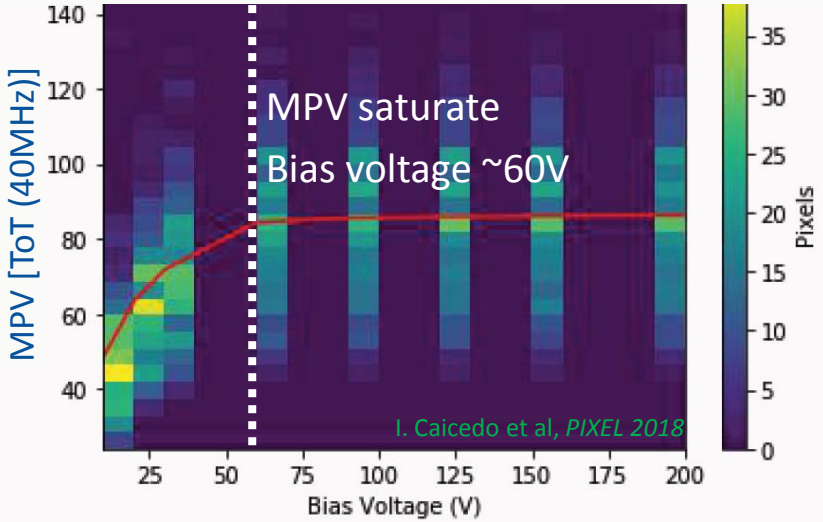
  - Neutron: $10^{15} n_{eq}/cm^2$ (JSI reactor)
    - Irradiated w/o powering at RT
    - Annealed 80min @60°C

THINNING AND BACK-SIDE PROCESS OF LARGE ELECTRODE DESIGN PROTOTYPE

Bias voltage and leakage current



MPV of un-irradiated thinned (200 µm) chip

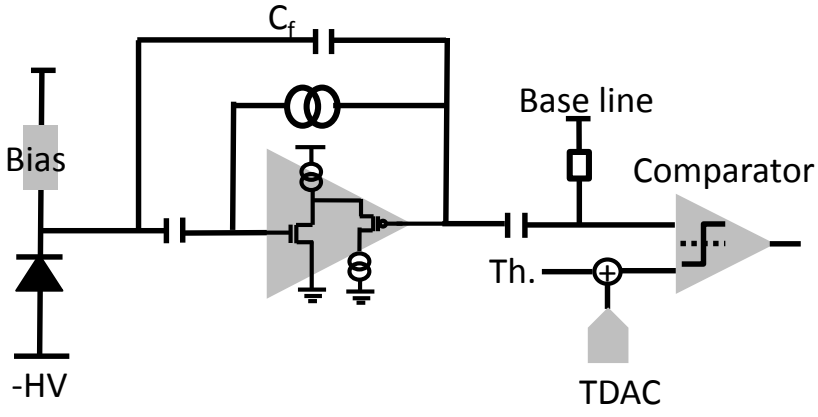


Break down voltage is > 200V

Full depletion voltage before irradiation: ~60V (200µm)

IN-PIXEL ELECTRONICS

❑ **Large** electrode design: LF-Monopix



- Power-saving analog frontend
  - CSA
  - Discriminator +w/ 4-bit trim DAC

❑ **Small** electrode design: TJ-Monopix

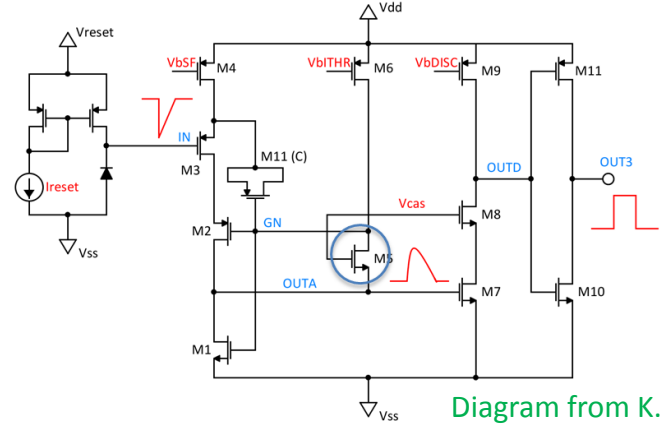
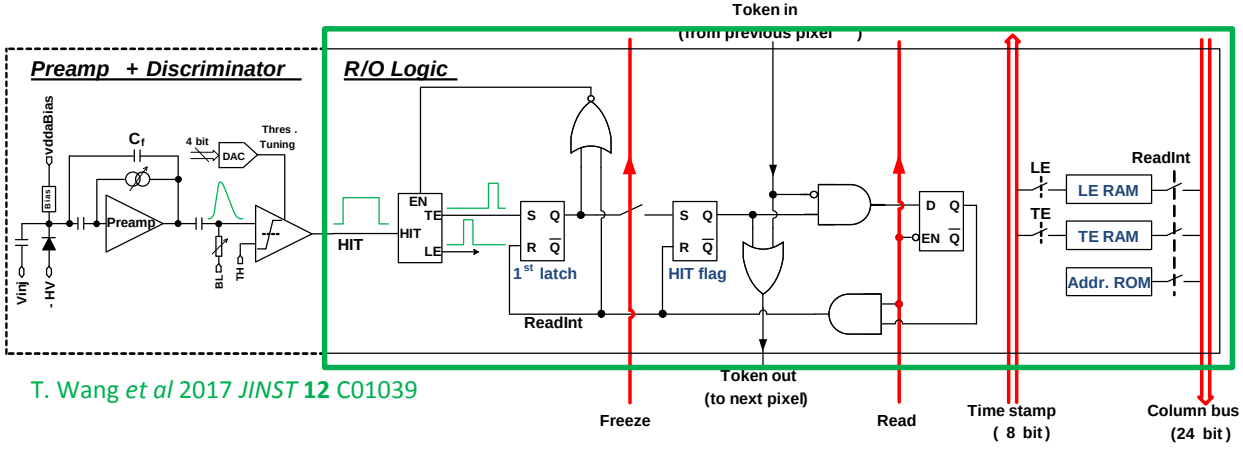


Diagram from K. Moustakas *et al*, *IEEE NSS2017*

- Space-saving, high-gain-low-noise analog frontend
  - Novel preamp and discriminator
  - w/o trim DAC

IN-PIXEL ELECTRONICS

Fully synchronous column drain architecture



T. Wang *et al* 2017 *JINST* **12** C01039

Common in both prototypes

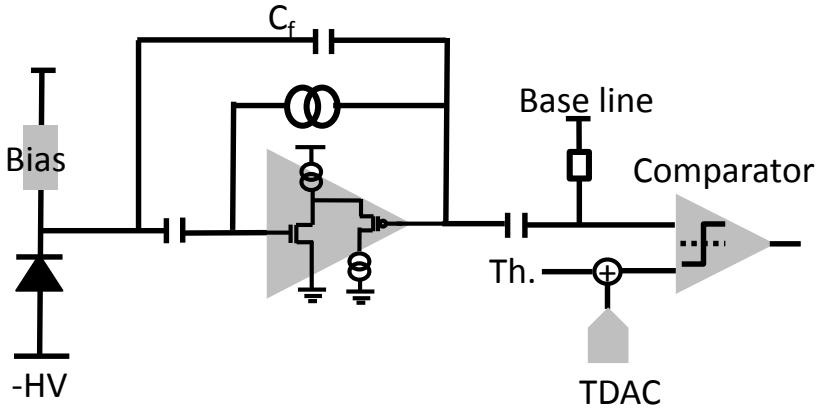
- **Large** electrode design: LF-Monopix
  - R/O logic: 8-bit ToA and ToT (40MHz)
- **Small** electrode design: TJ-Monopix
  - R/O logic: 6-bit ToA and ToT (40MHz)

Column drain architecture has been used in current ATLAS pixel readout chip (FE-I3)

Hit-rate: Outer layers of ATLAS ITk pixel detectors ≈ Current ATLAS ID pixel detectors

IN-PIXEL ELECTRONICS

❑ **Large** electrode design: LF-Monopix



- Power-saving analog frontend
  - CSA
  - Discriminator +w/ 4-bit trim DAC

❑ **Small** electrode design: TJ-Monopix

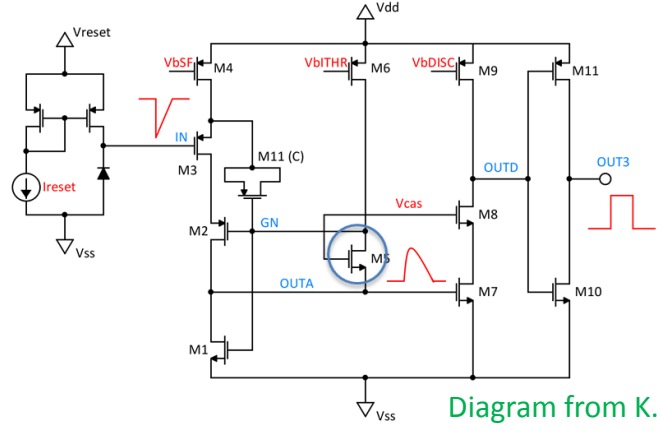


Diagram from K. Moustakas *et al*, *IEEE NSS2017*

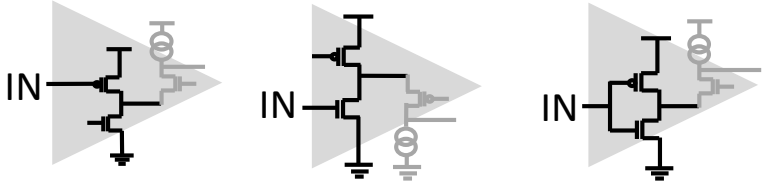
- Space-saving, high-gain-low-noise analog frontend
  - Novel preamp and discriminator drive from ALPIDE
  - w/o trim DAC

TID RADIATION HARDNESS OF LARGE ELECTRODE DESIGN (GAIN & ENC)

X-ray irradiation up to 50Mrad

- Input transistor of CSA

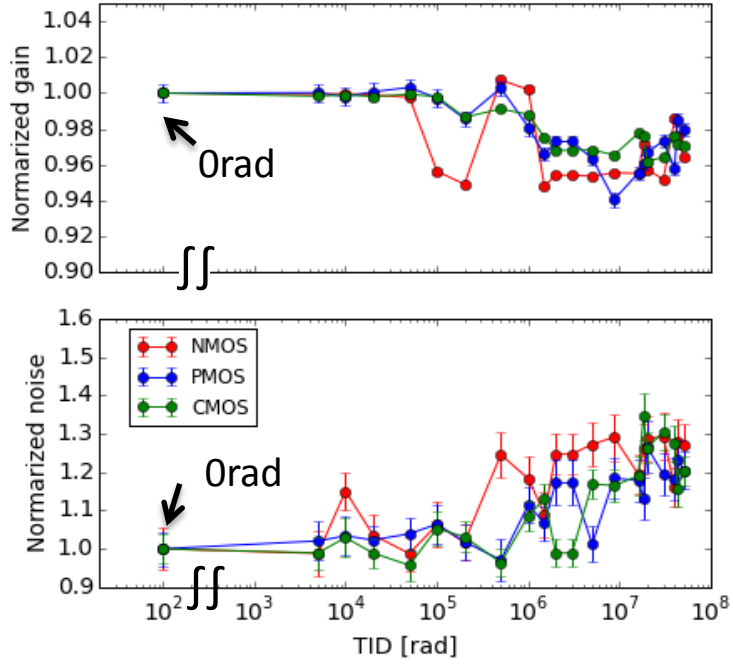
❑ PMOS-CSA ❑ NMOS-CSA ❑ CMOS-CSA



- Irradiated and measured in room temperature
- Gain degradation: <5%
- Noise increase: ~25%
  (due to the increase of the leakage current)

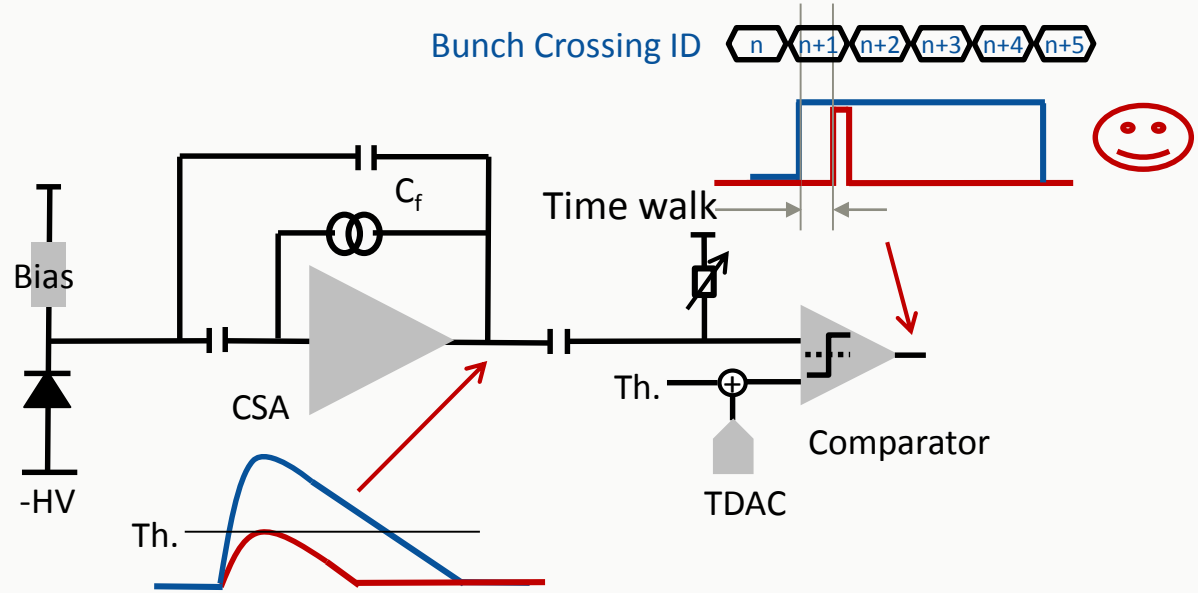
→ No significant difference between the CSAs

Normalized gain and ENC



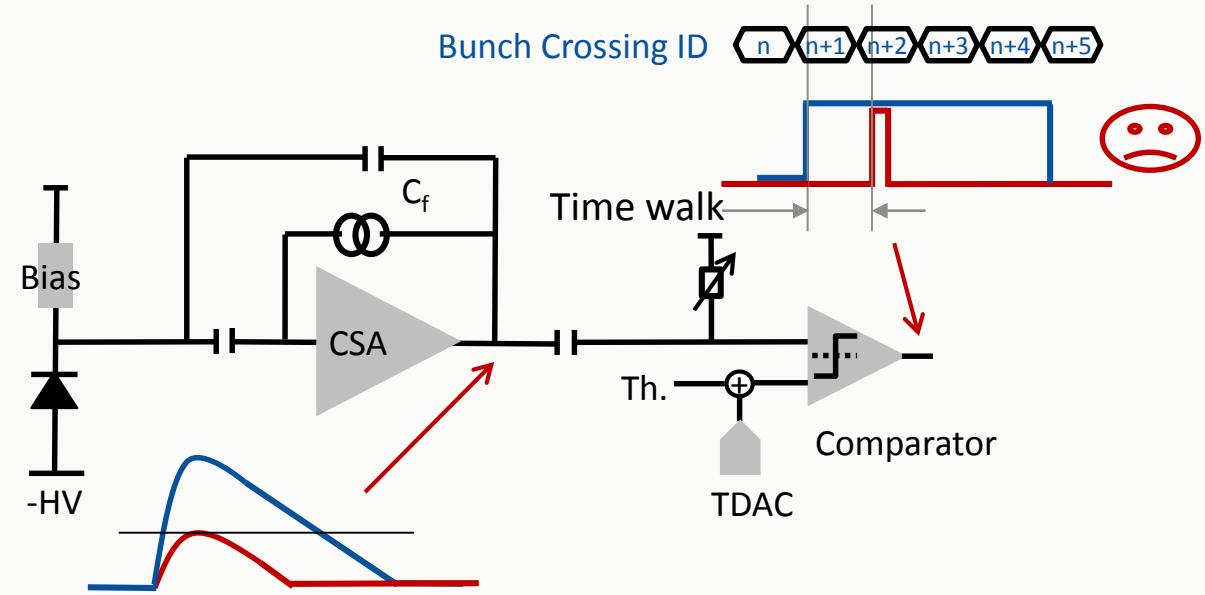
TIMING PERFORMANCE REQUIRED IN HL-LHC

Responses in 1 Bunch Crossing (25 ns) will be counted as signal → Smallest signal in 1BCD = In-time threshold



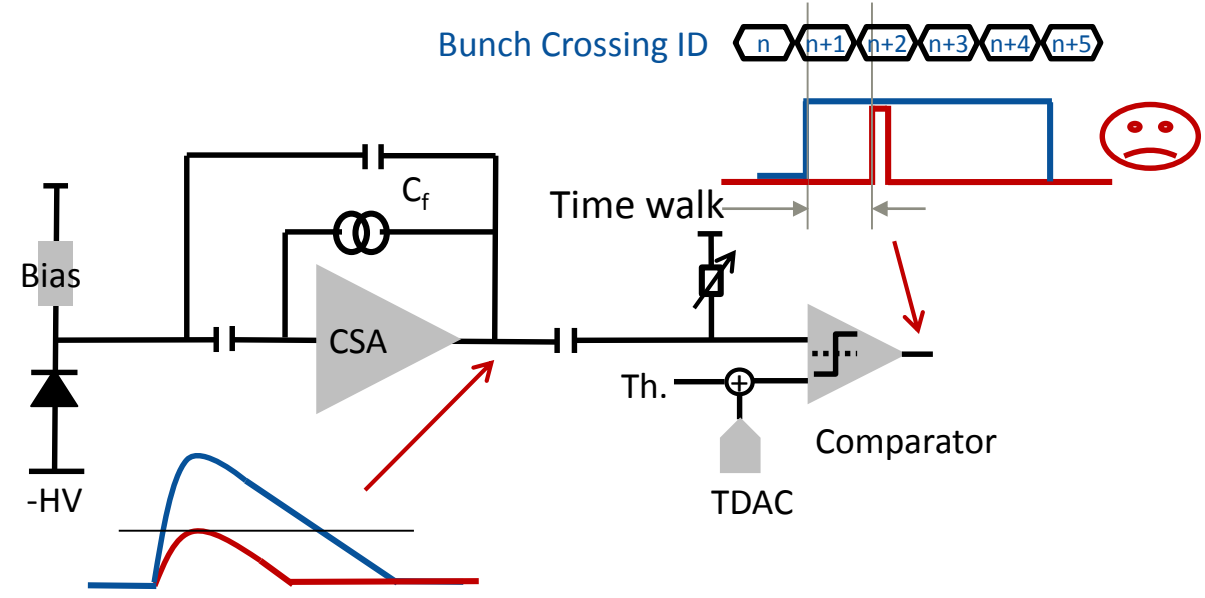
TIMING PERFORMANCE REQUIRED IN HL-LHC

Responses in 1 Bunch crossing (25 ns) will be counted as signal → Smallest signal in 1BCD = In-time threshold

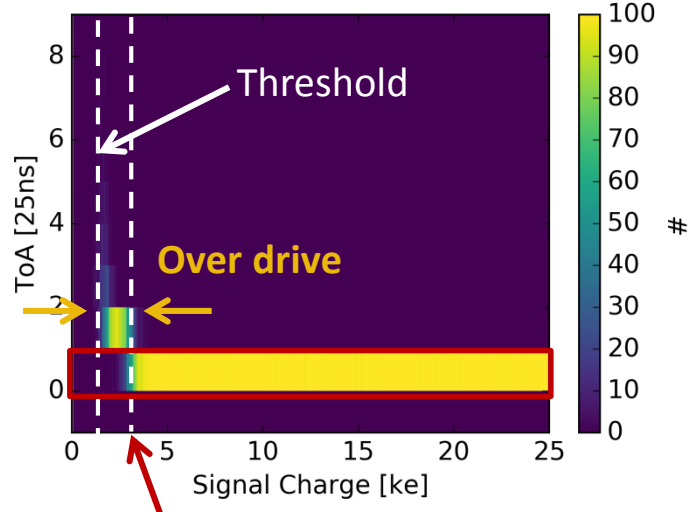


TIMING PERFORMANCE REQUIRED IN HL-LHC

Responses in 1 Bunch crossing (25 ns) will be counted as signal → Smallest signal in 1BCID = In-time threshold



❑ In-time threshold and over drive

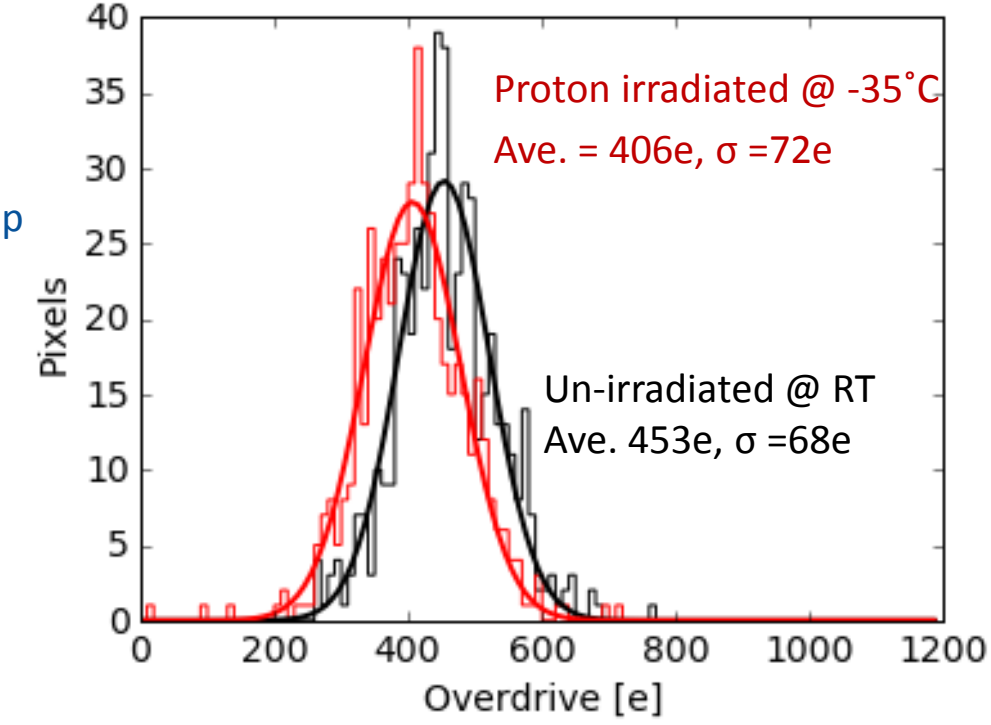


In-time threshold (ToA in 1clk)

TID RADIATION HARDNESS OF LARGE ELECTRODE DESIGN (OVER DRIVE)

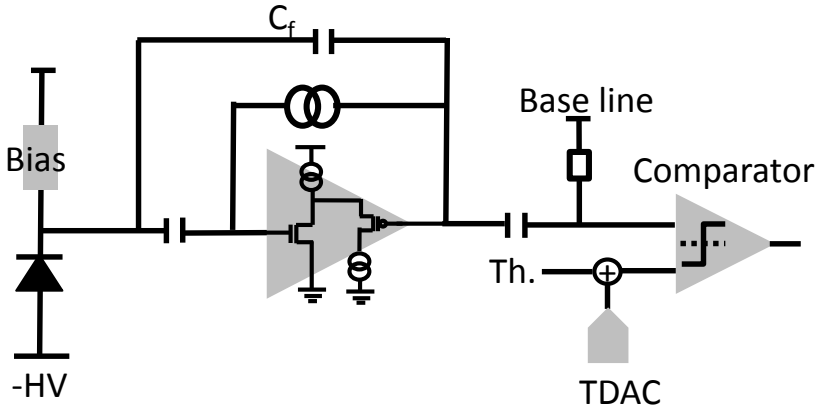
- Over drive measurement
  - Threshold: 1500 e
- Difference between irradiated/un-irradiated chip
  - Chip temperature
  - Chip variation
  - Optimization of tunable parameters

No degradation in timing performance



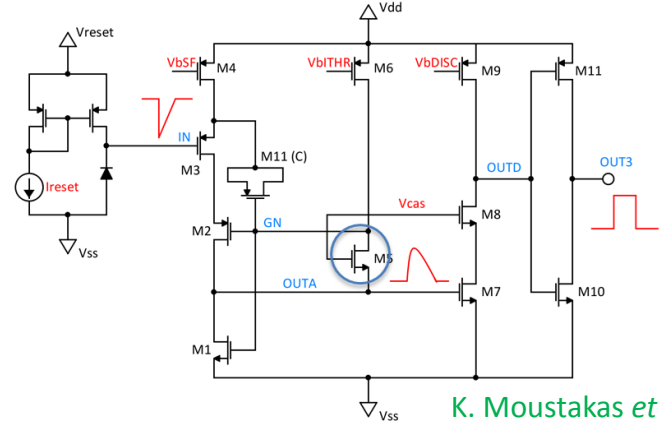
IN-PIXEL ELECTRONICS

❑ **Large** electrode design: LF-Monopix



- Power-saving analog frontend
  - CSA
  - Discriminator (self-biased diff. + inverter)
  - w/ 4-bit trim DAC

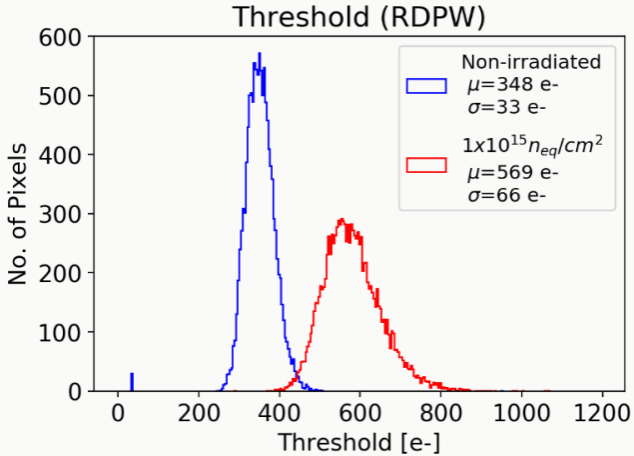
❑ **Small** electrode design: TJ-Monopix

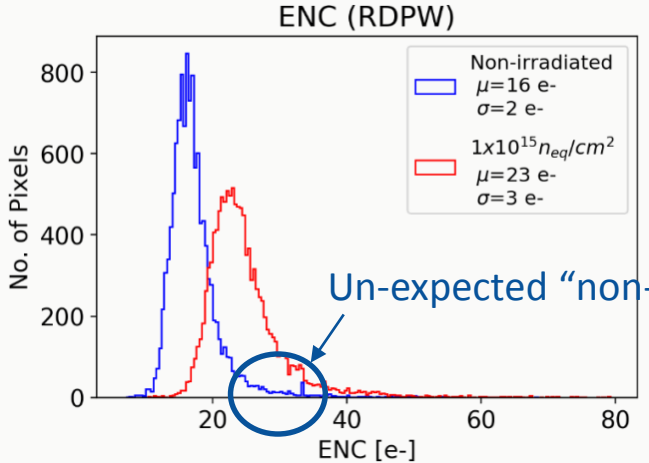


K. Moustakas *et al*, *IEEE NSS2017*

- Space-saving, high-gain-low-noise analog frontend
  - Novel preamp and discriminator
  - w/o trim DAC

ANALOG FRONTEND FOR SMALL ELECTRODE DESIGN





I. Caicedo et al, *PIXEL 2018*

- Threshold dispersion=30e (irradiated=70e) , ENC=16e (23e) → Lowest threshold=350e (570e)
- Improvement in lowering threshold dispersion, eliminating the "non-Gaussian tail" of ENC distribution will be done in next prototype
- The analog frontend functioned even though the leakage current from the sensor is increased by NIEL irradiation

This project has received funding from the European Union's Horizon 2020 Research and Innovation programme under Grant Agreement no. 654168.

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HIT EFFICIENCY

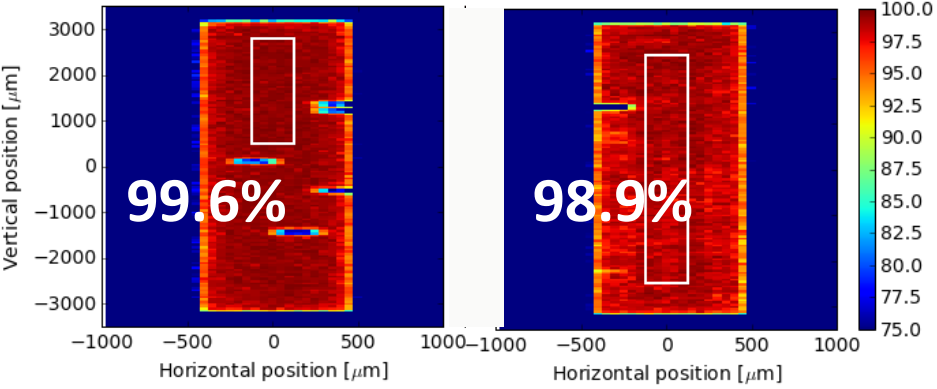
❑ **Large** electrode design: LF-Monopix (750µm)

Un-irradiated

- Noise < 1.2 Hz/pix
- Dry ice cooling

Neutron irradiated

- Noise < 0.1Hz/pix
- Dry ice cooling



Hit efficiency is as high as 98.9% after the NIEL irradiation ($10^{15} n_{eq}/cm^2$)

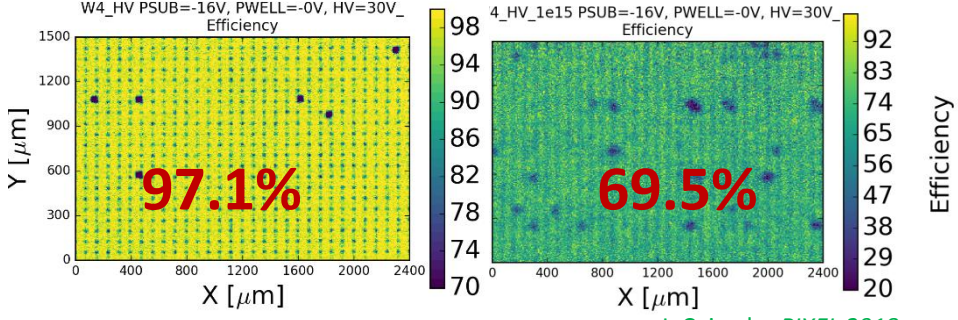
❑ **Small** electrode design: TJ-Monopix

Un-irradiated

- Noise < 10 Hz/pix
- Room temp.

Neutron irradiated

- Noise < 10 Hz/pix
- -10°C



I. Caicedo, *PIXEL 2018*

Inefficiency was observed even before irradiation

This project has received funding from the European Union's Horizon 2020 Research and Innovation programme under Grant Agreement no. 654168.

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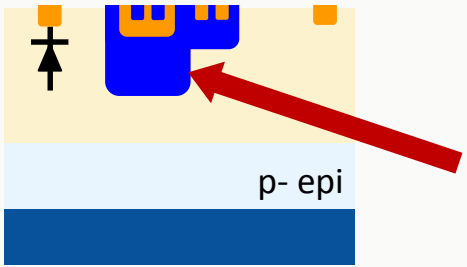
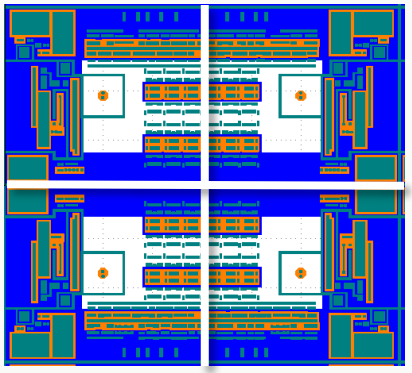
HIT EFFICIENCY

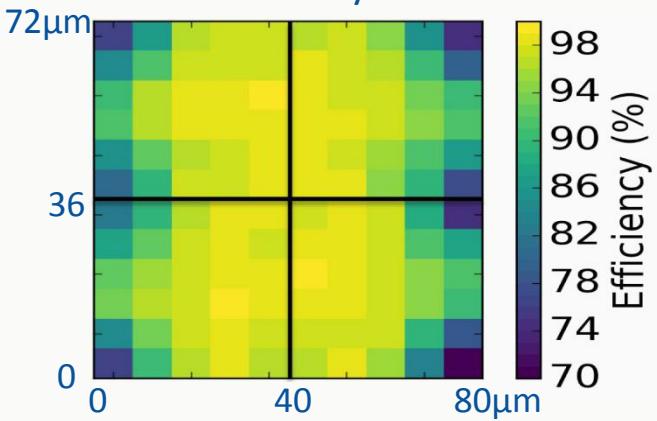
In-pixel hit efficiency of
un-irradiated **small** electrode prototype (4 pixels)

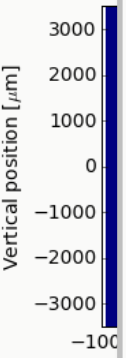
❑ Layout

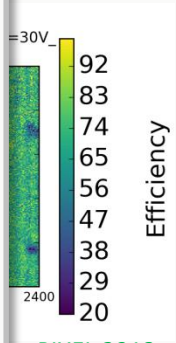




❑ Hit efficiency







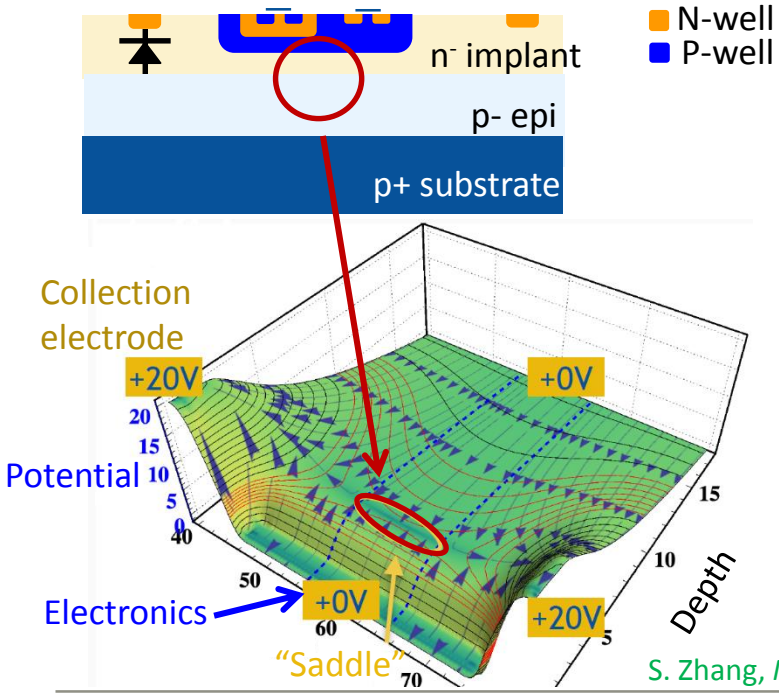
o, PIXEL 2018

➡ Inefficient regions exist near pixel corner where PWELL are implanted

Hit
irrad
tion

HIT EFFICIENCY DEGRADATION IN SMALL ELECTRODE DESIGN

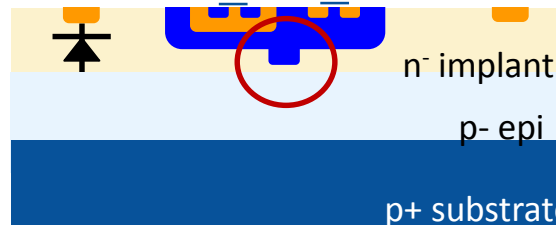
❑ TCAD simulation



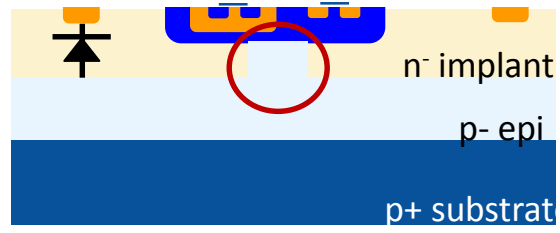
S. Zhang, *Master thesis Uni. Bonn*

Improvements (previous presentation by E. Schioppa)

❑ Modification1: Additional PWELL



❑ Modification2: Gap in n-implant



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SUMMARY

- Two fully-monolithic large-scale matrixes have been tested to discuss the suitability of DMAPS as pixel detector in HL-LHC experiments

- Large electrode design:
  - Full depletion voltage of 200um is 60V whereas a bias voltage of 200V can be applied to the irradiated (50Mrad, $10^{15} n_{eq}/cm^2$) chip
  - No significant degradation due to TID irradiation (50Mrad).
  - Hit efficiency is as high as 98.9% after NIEL irradiation ($10^{15} n_{eq}/cm^2$)

- Small electrode design:
  - The novel analog frontend and R/O logics functions in the large scale matrix
  - Degradation in the hit efficiency was observed but the improvement is on going

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BACKUP

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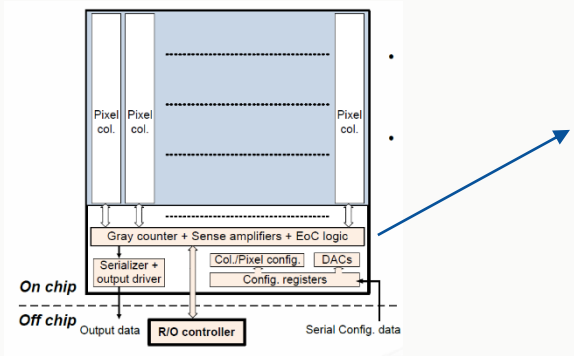
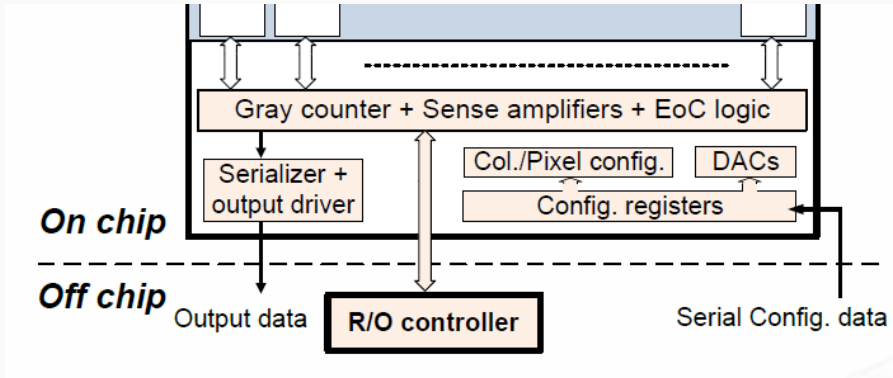
OUTLINE

- Intorduction
  - Large vs small collection electrode design
- Prototype chips
- Electronics characterizaion and TID raditiation hardness
- NIEL radiation hardness
- Summary

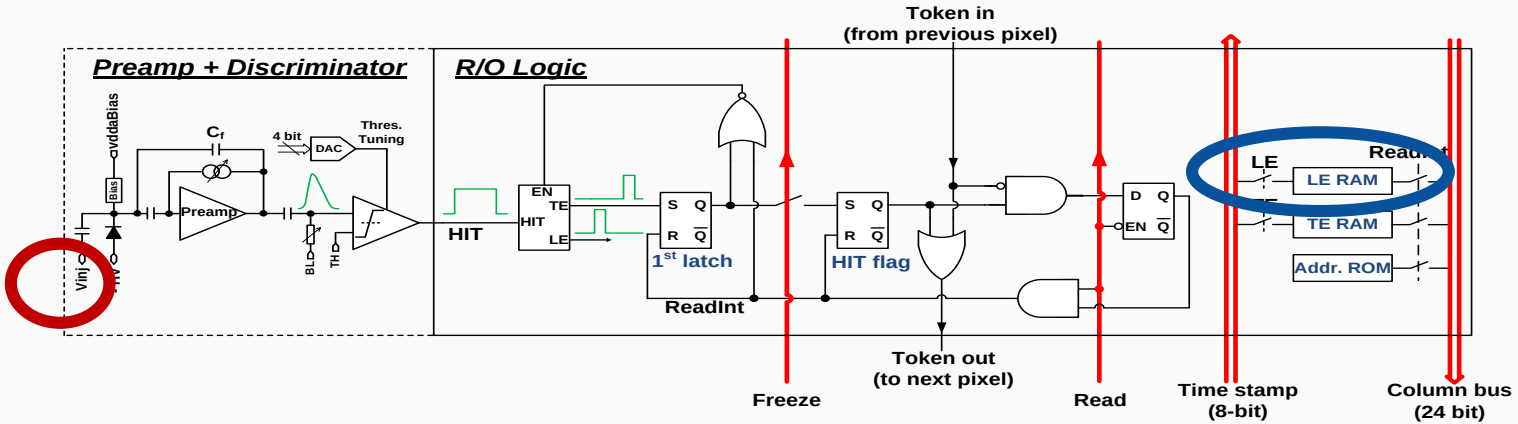
IN-PIXEL ELECTRONICS

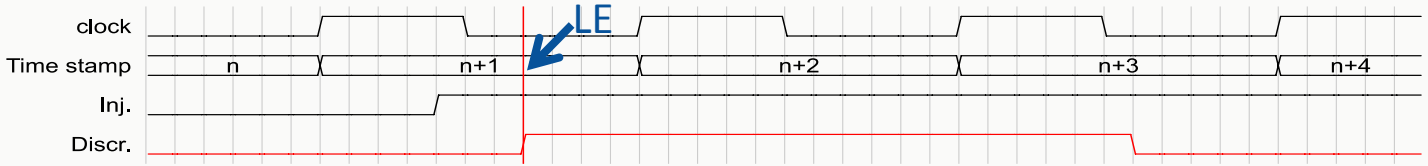




MEASUREMENT USING TOA(BXID)

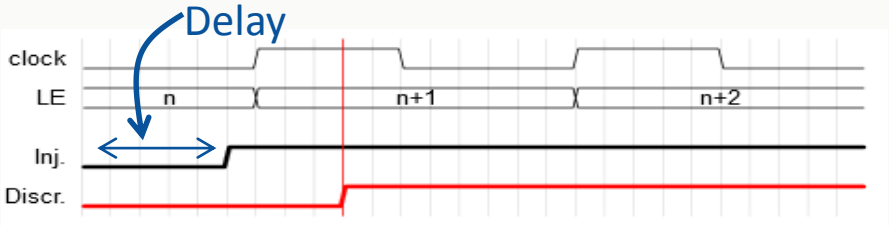
– Time of arrival is recorded as 40 MHz timestamp, “LE” = ToA

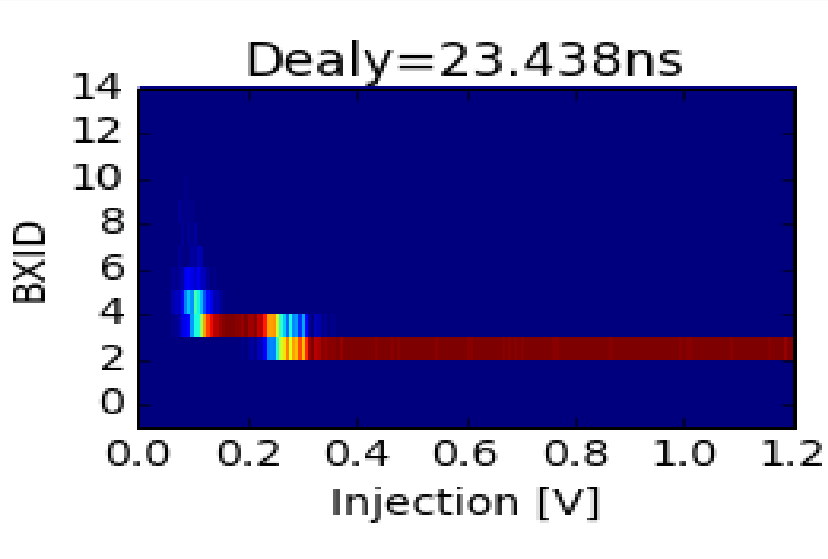




INJECTION DELAY VS TOA (BXID)

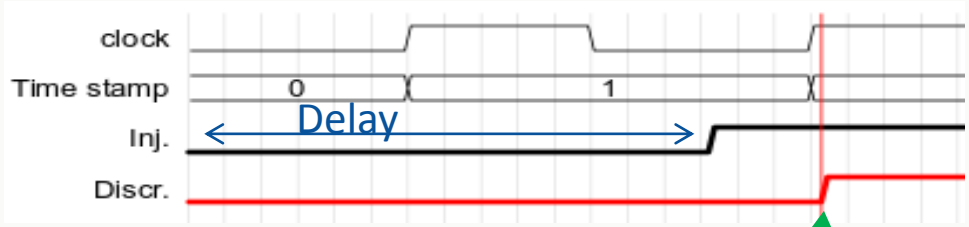
- ToA (BXID) move according to the amplitude of the test pulse but also according to the delay of injection

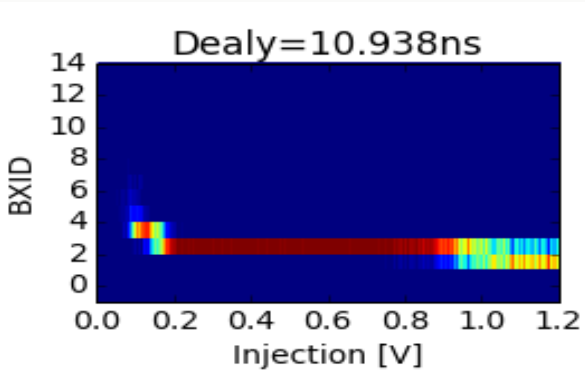


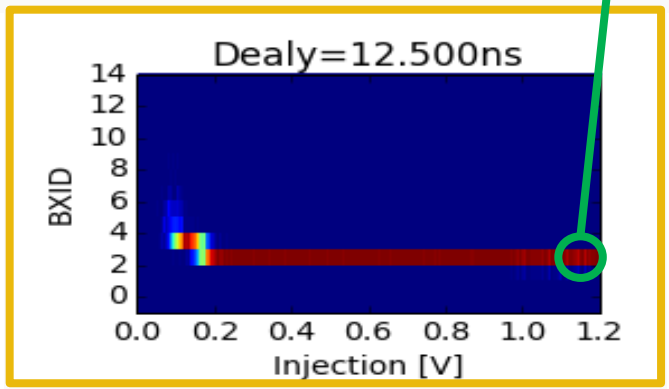


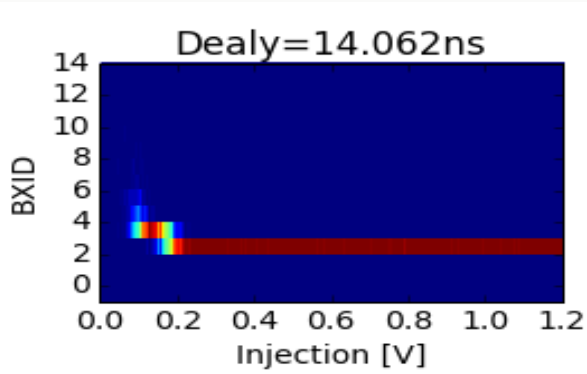
INJECTION DELAY VS LE

- The injection delay should be optimized to the value where the ToA of the largest signal is on the earlier edge of the timestamp clock







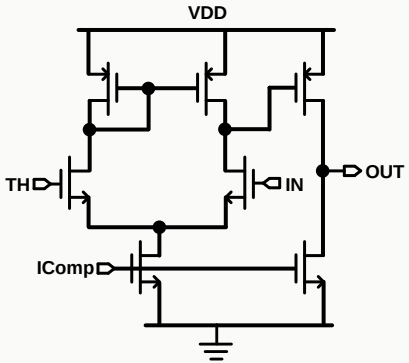


ANALOG FRONTEND FOR LARGE ELECTRODE DESIGN

Development of power saving and fast responding discriminator

❑ Conventional type

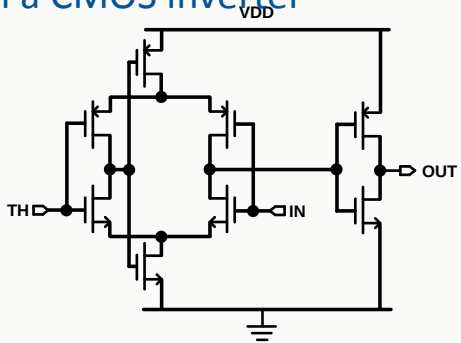
Two-stage open loop structure

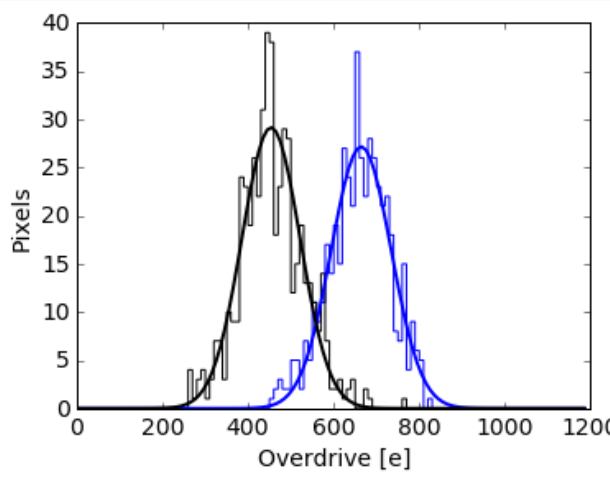


- Bias current: 4.5 µA
- Well tested but slow at threshold edge

❑ New type

Self-biased differential amplifier with a CMOS inverter

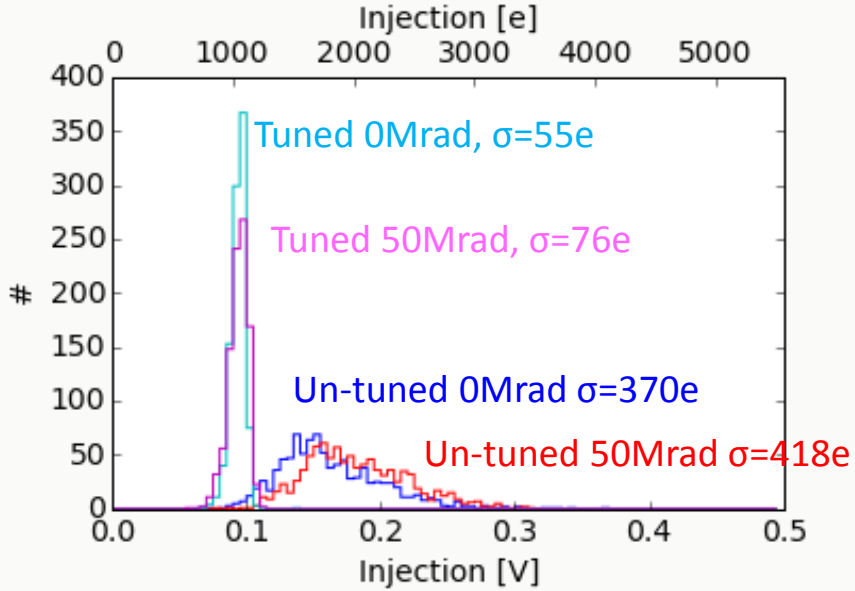




- Self biased: < 4µA
- Faster especially at threshold edge

RADIATION HARDNESS (TID)

Un-tuned and tuned threshold dispersions of LF-CPIX (flavor=PMOS)



- The threshold is still tunable after TID=50Mrad (σ<100e *cf. readout noise ≈ 200e*)
- Increase of the tuned threshold dispersion is 20e

This project has received funding from the European Union's Horizon 2020 Research and Innovation programme under Grant Agreement no. 654168.

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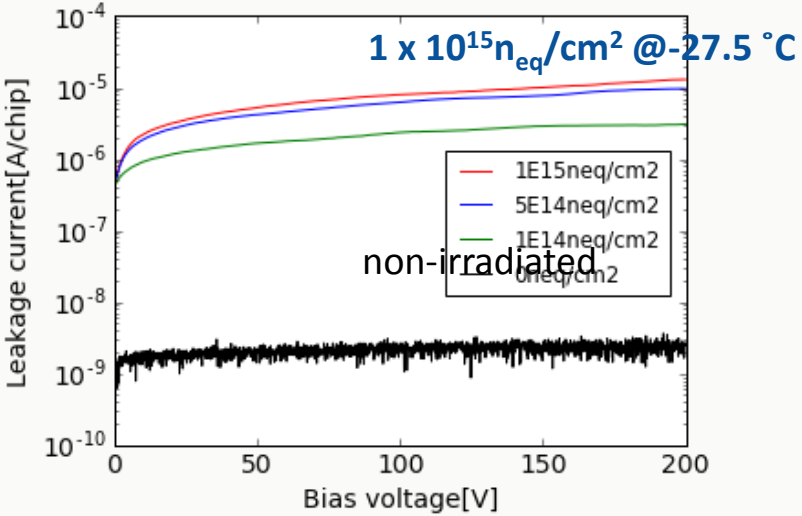
RADIATION HARDNESS (NIEL)

- The neutron irradiation test was done in JSI and the MonoPix were annealed 80min @60C

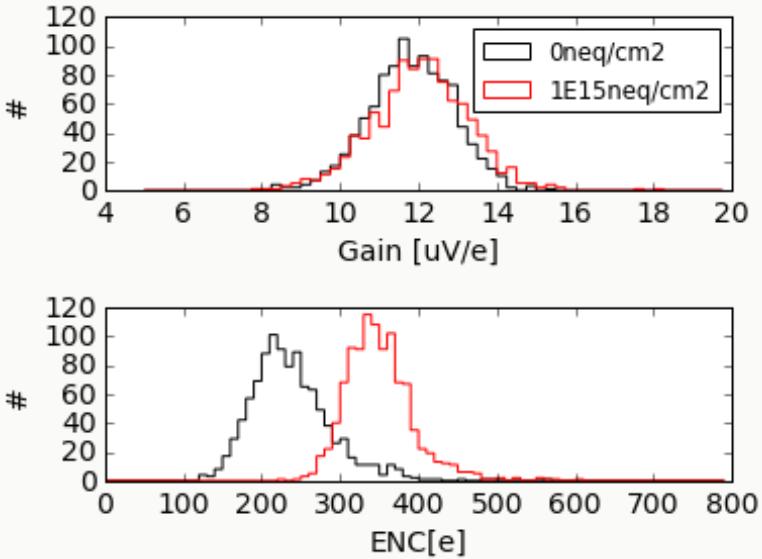
Chip: MONOPIX
DAC setting: Default
Bias voltage: -200V
Temperature: -23C, -27.5C

❑ I-V curve of MonoPix



- Breakdown voltage is higher than 200V

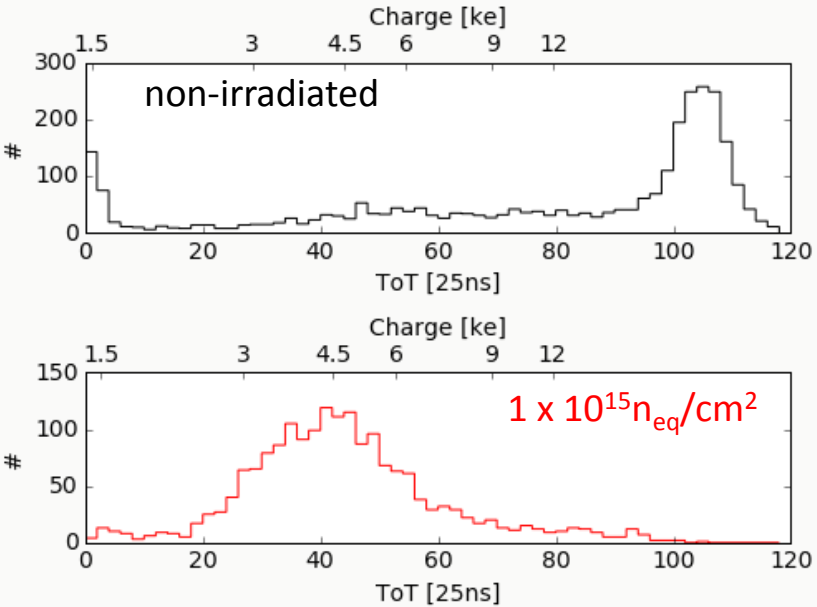
❑ Gain and noise



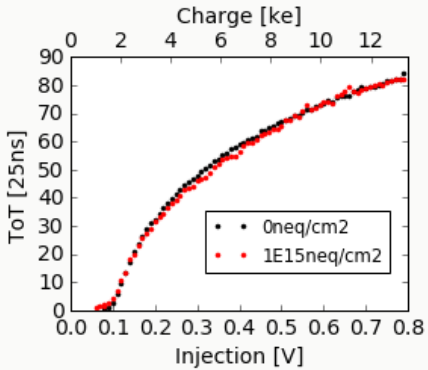
RADIATION HARDNESS (NIEL)

Threshold: 1500 e
Bias: -200V (0 n_{eq}/cm^2)
-130V (1 x $10^{15} n_{eq}/cm^2$)
Chip: MONOPIX
DAC setting: Default
Source: 2.5GeV electron
Temperature: cooled by dry ice

- ToT values of seed pixel



- Injection vs ToT

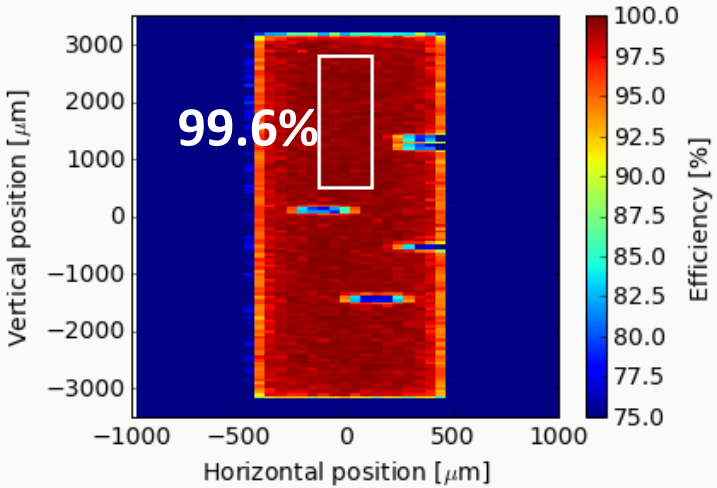


- The MPV is decreased after neutron irradiation of 1 x $10^{15} n_{eq}/cm^2$.

HIT EFFICIENCY

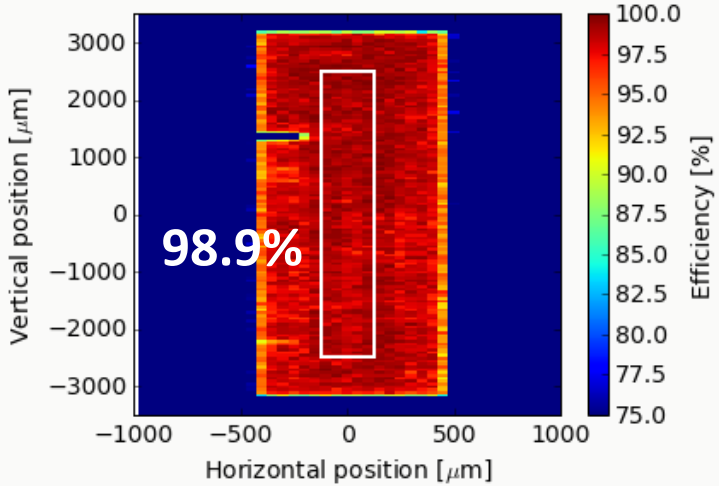
- Un-irradiated

Chip: MONOPIX un-irradiated
DAC setting: default
TH: tuned by noise + 4mV (~1750e)
HV: -200V
Temp: dry ice
Source: 2.5GeV electron



- $1 \times 10^{15} n_{eq}/cm^2$

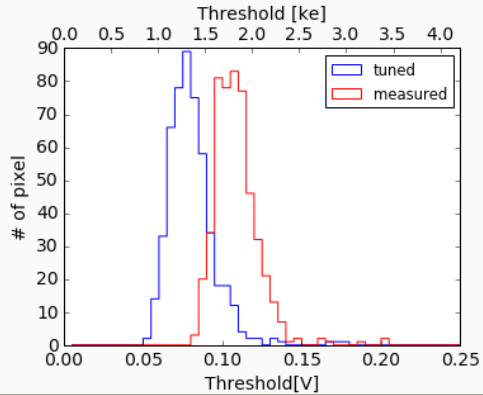
Chip: MONOPIX irradiated
DAC setting: default
TH: tuned by noise (~1500e)
HV: -130V
Temp: dry ice
Source: 2.5GeV electron



THRESHOLD DISPERSION

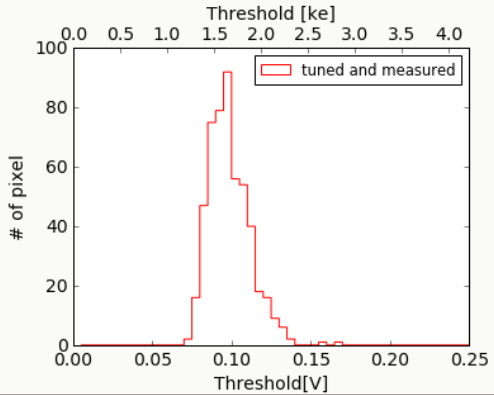
– Un-irradiated

Chip: MONOPIX un-irradiated
DAC setting: default
TH: tuned by noise + 4mV
Flavor: CMOS-CSA, V1-D-Discr. Curr-Token In-pix
Enabled readout: col 16-20
HV: -200V
Temp: dry ice
Source: 2.5GeV electron



- $1 \times 10^{15} n_{eq}/cm^2$

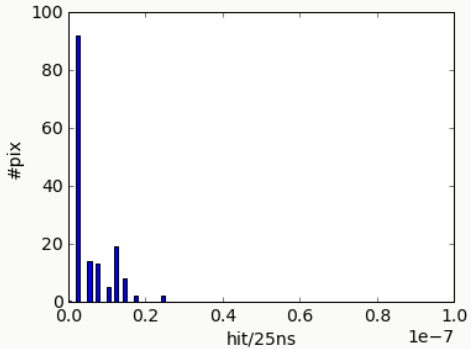
Chip: MONOPIX irradiated
DAC setting: default
TH: tuned by noise
Flavor: CMOS-CSA, V1-D-Discr. Curr-Token In-pix
Enabled readout: col 16-20
HV: -130V
Temp: dry ice
Source: 2.5GeV electron



NOISE OCCUPANCY

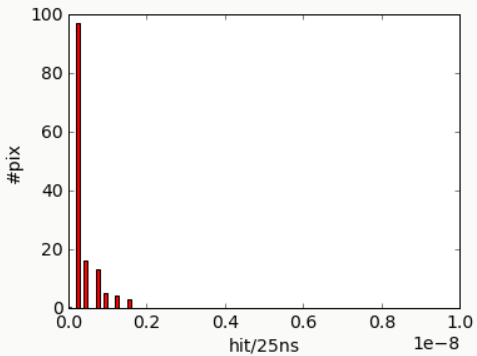
- Un-irradiated

Chip: MONOPIX un-irradiated
DAC setting: default
TH: tuned by noise
Flavor: CMOS-CSA, V1-D-Discr. Curr-Token In-pix
Enabled readout: col 16-20
HV: -200V
Temp: dry ice
Source: 2.5GeV electron

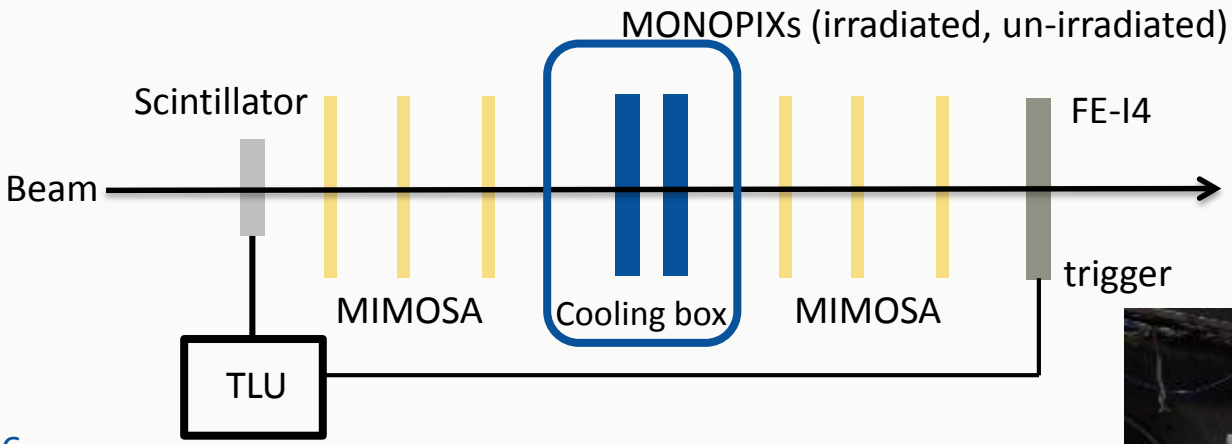


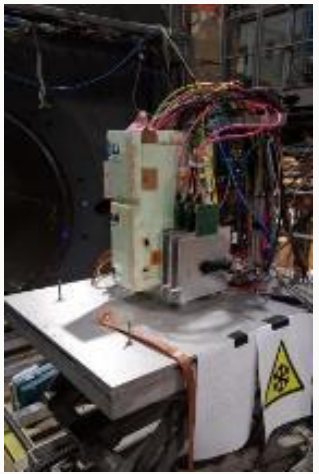
- $1 \times 10^{15} n_{eq}/cm^2$

Chip: MONOPIX irradiated
DAC setting: default
TH: tuned by noise
Flavor: CMOS-CSA, V1-D-Discr. Curr-Token In-pix
Enabled readout: col 16-20
HV: -130V
Temp: dry ice
Source: 2.5GeV electron



MEASUREMENT SETUP



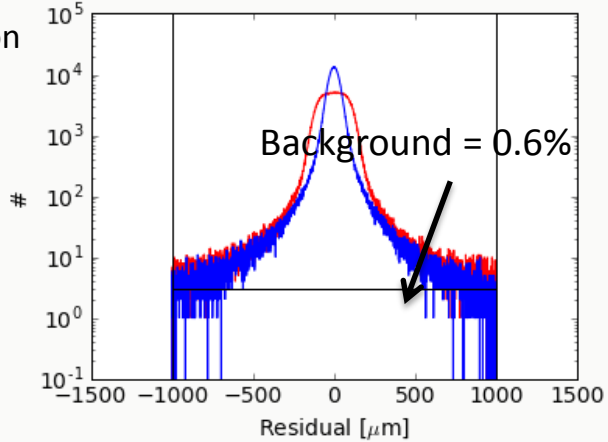


- MIMOSA x 6
  - Pixel size: 18.2 µm x 18.2µm
  - 1152 µs/frame (rolling shutter)
- FE-I4 x 1
  - Pixel size: 250 µm x 50 µm
  - Timing resolution: 25ns (triggered by scintillator + TLU)

RESIDUAL

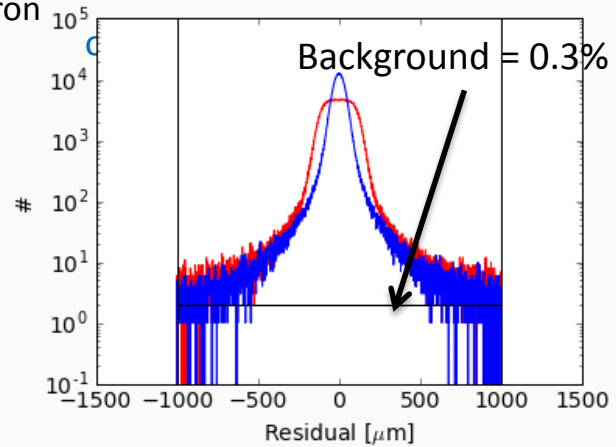
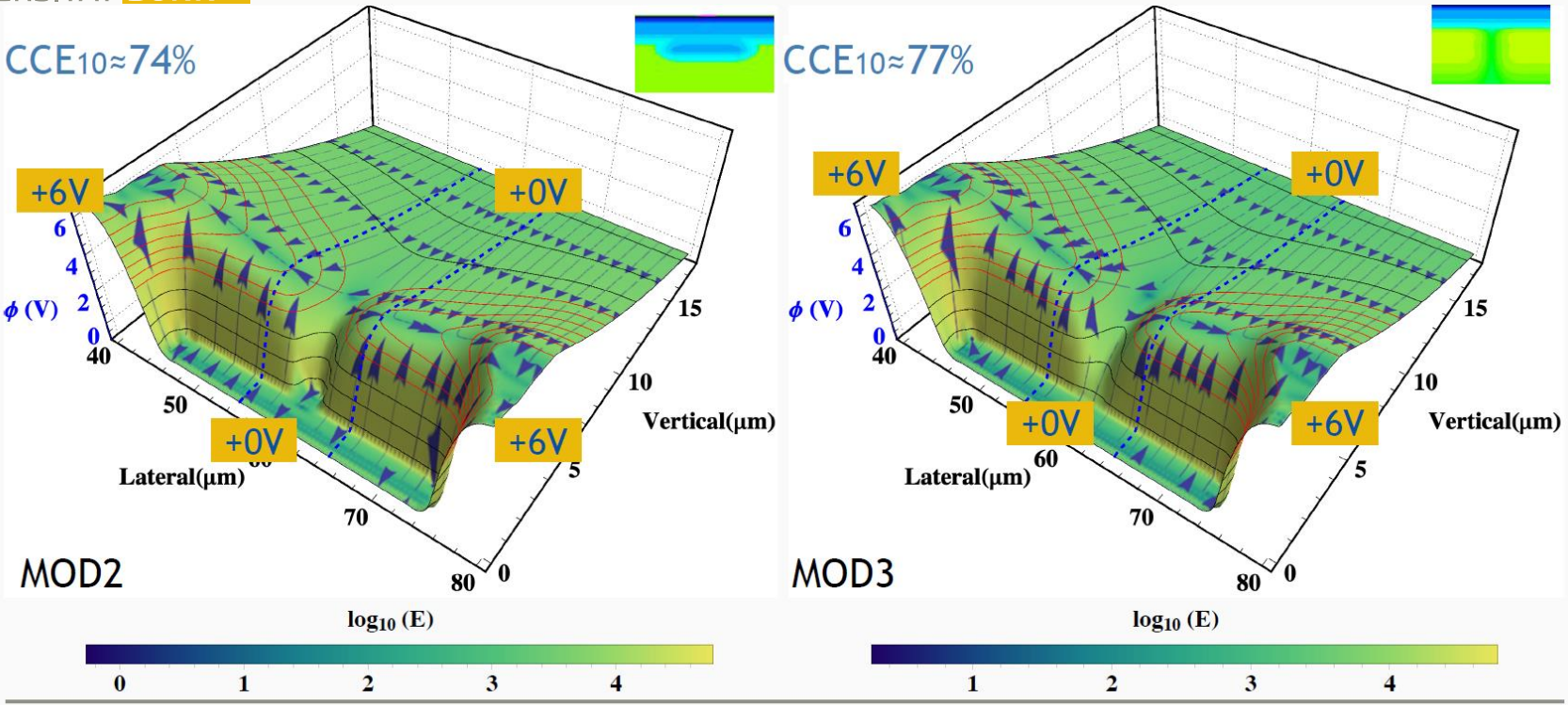
Thickness of chip: 750um
Chip: MONOPIX un-irradiated
DAC setting: default
TH: tuned by noise + 4mV
Flavor: CMOS-CSA, V1-D-Discr. Curr-Token In-pix
Enabled readout: col 16-20
HV: -200V
Temp: dry ice
Source: 2.5GeV electron

– Un-irradiated



Thickness of chip: 750um
DAC setting: default
TH: tuned by noise
Flavor: CMOS-CSA, V1-D-Discr. Curr-Token In-pix
Enabled readout: col 16-20
HV: -130V
Temp: dry ice
Source: 2.5GeV electron

- $1 \times 10^{15} n_{eq}/cm^2$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