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Series Production Testing, Commissioning and Initial Operation of the Belle II Silicon Vertex Detector Readout System

The Silicon Vertex Detector (SVD) of the Belle II experiment at the High Energy Accelerator Research Organization (KEK) in Tsukuba, Japan, consists of 172 double-sided microstrip technology silicon sensors arranged cylindrically in four layers around the interaction point. A total of 1748 readout chips (APV25) process and send the analog signals over 2.5 meter long copper cables to 48 Junction Boards (JBs) located inside the detector housing which provide an interface for connecting the cables on the inside of the detector with those of the outer world, and to power the detector with radiation-hard and magnetic insensitive DC-DC converters. From there the analog data are sent over 13 meter long copper cables to 48 A/D Converter boards (FADCs) located in crates on top of the Belle II detector structure. They control the detector, convert the SVD data into digital domain, and perform first data processing using powerful FPGAs. From the FADC boards the data are then sent out to the central DAQ by optical fibers.
This paper shows hardware and procedures to test all components of the SVD data readout system (Cables, FADC boards, JBs) individually after the series production, the findings of the commissioning of the whole readout chain using final hardware in two test setups, and the first results of the initial operation of the final detector.

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