A novel 4D fast track finding system on FPGA

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Abstract

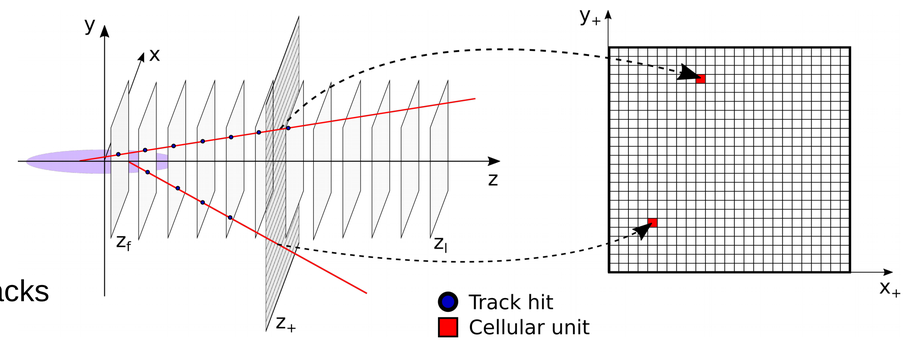
We present a novel 4D fast track finding system capable of reconstructing four dimensional particle trajectories in real time using precise space and time information of the hits. The fast track finding device that we are proposing is designed for the high-luminosity phase of LHC and it is based on a massively parallel algorithm to be implemented in commercial field-programmable gate array using a pipelined architecture. We present studies of expected tracking performance for a possible pixel detector of a future upgrade of the LHCb experiment and first results based on a hardware prototype.

TimeSPOT project

- **TIME** & **SP**ace real-time **O**perating **T**racker
- R&D project funded by INFN
- Rad-hard pixed detector with precise space and time tracking capabilities
- Silicon and diamond pixel: goal 30ps time and 40μm space resolution
- Goal is to produce a fully working prototype demonstrator, integrating sensors, electronics, real-time processing

4D stub based tracking algorithm

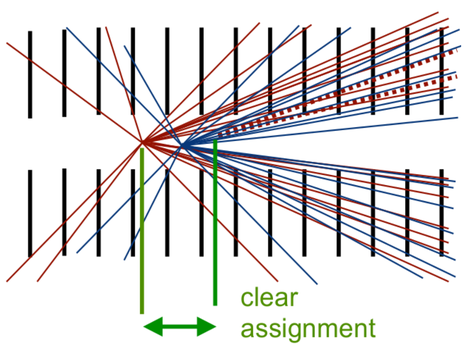
- "Stubs" are identified as doublet of hits in adjacent tracking planes.
- Stubs not compatible with particles from the luminous region are discarded based on geometrical and timing cuts.
- Stubs are projected to a 2D reference plane.
- Engines are distributed in the ref. plane and identify tracks from groups of stubs with similar projections.



Role of Timing in LHCb Upgrade II

- Luminosity at HL-LHC : x10 w.r.t to nominal LHC
- High pileup : 50-100 interactions x crossing
- LHCb VELO as a case study

- Timing in PV association:
  - ~200ps resolution needed to recover performance
  - Not enough to be useful in the pattern recognition



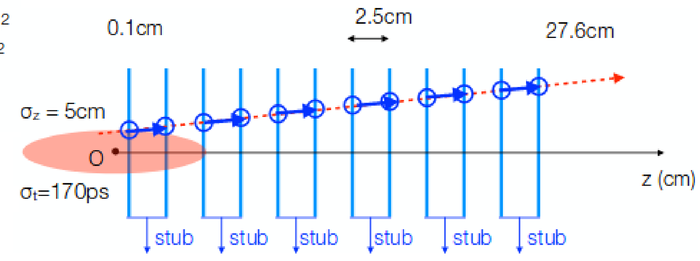
- Timing in tracking:
  - Use only time compatible hits in the pattern recognition
  - Stricter resolution requirements : ~30ps
  - Ghost rate reduction as a primary effect

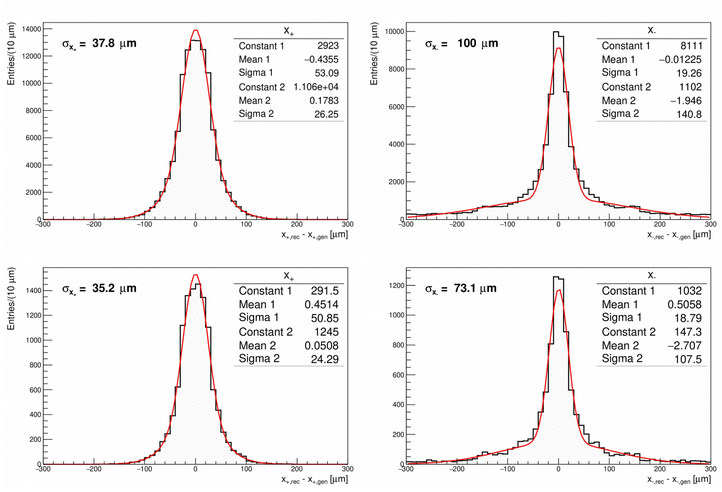
Simulation

- VELO like tracking detector with timing:
  - 12 planes in the forward region

- Pile-up: ~40 with ~1200 reconstructible tracks/event
- 90000 engines, uniformly distributed in the (x+,y+)
- 2D reference plane.

Sensor area = 6x6cm²
pixel size = 55x55μm²
thickness = 200 μm
time res σ_t=30 ps





First row: resolution on track parameters (x+,x-) without applying the timing cuts.

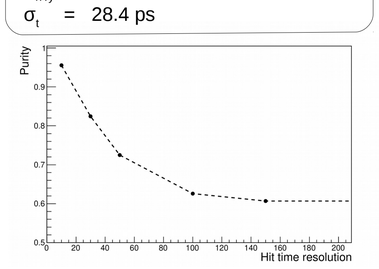
Second row: resolution on track parameters (x+,x-,t) obtained using the timing information with 30 ps hit resolution

Similar results are obtained for (y+,y-) track parameters.

$\sigma_{x+/y+}$ = 37.8 μm
$\sigma_{x-/y-}$ = 100.0 μm
Efficiency = 99 %
Purity = 64 %

Time

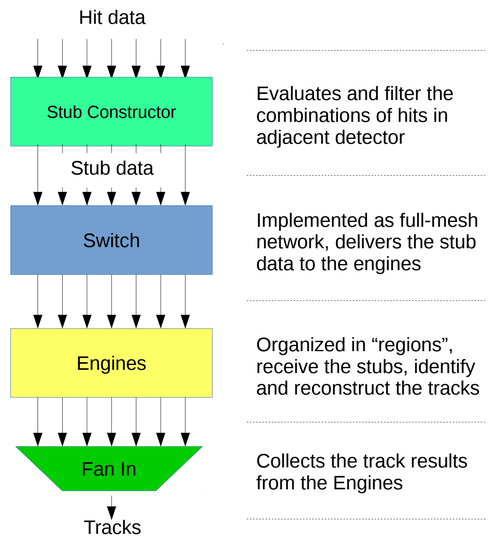
$\sigma_{x+/y+}$ = 35.2 μm
$\sigma_{x-/y-}$ = 73.1 μm
σ_t = 28.4 ps
Efficiency = 99 %
Purity = 85 %

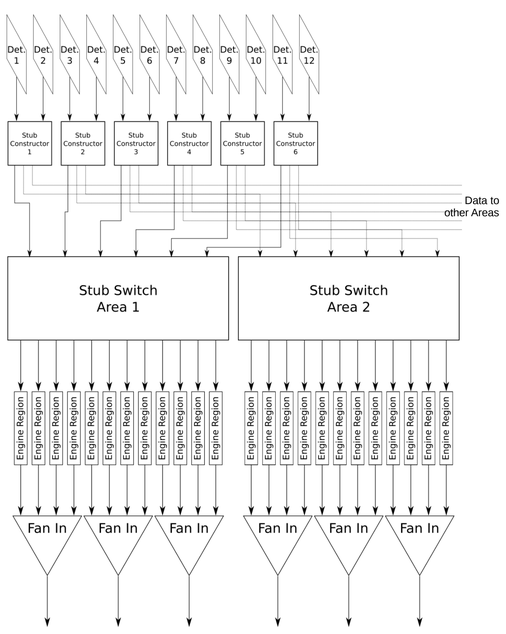


Device architecture

- The device receives the hits and provides the reconstructed tracks as output, to be used for further processing

- Key points:
  - Highly parallelized architecture
  - Pipelined architecture
  - Hold logic implementation for data flow management for minimum latency and reduced data serialization
  - Low latency : < 1μs total



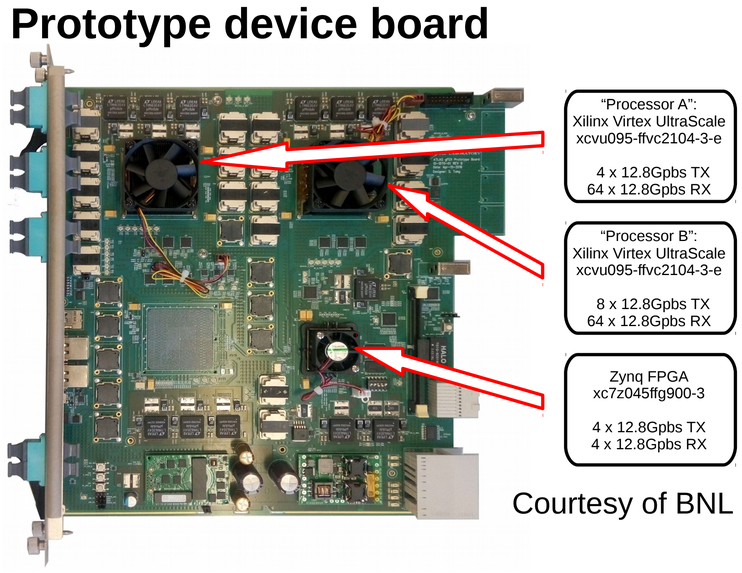


Architecture detail

- One dedicated Stub Constructor for each plane doublet:
  - Implemented in dedicated or front-end FPGAs
  - the Stub Constructor modules are completely independent from each others

- Engines in the 2D tracking reference plane are organized in multiple independent areas.
  - Each Area comprises a dedicated Stub Switch and a pool of Engines.
  - Absence of "lateral" communication between different Areas makes the system modular and scalable

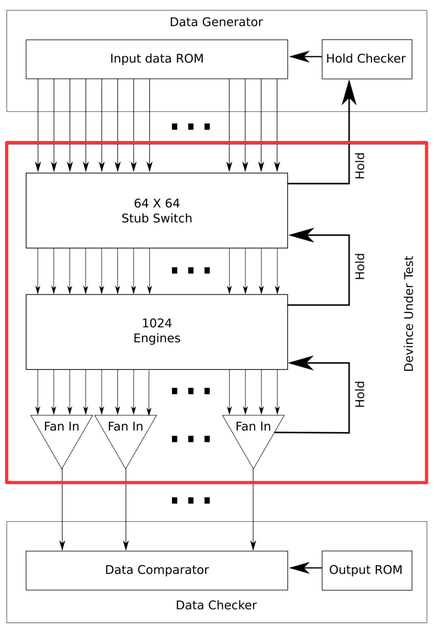
Prototype device board



Courtesy of BNL

- Firmware implemented in FPGA on a custom board
  - Two Xilinx Virtex UltraScale FPGAs
  - One Xilinx Zynq FPGA
  - High-speed optical transceivers: ~1.6 Tbps input

Test architecture and results



- Switch and Engines fully implemented

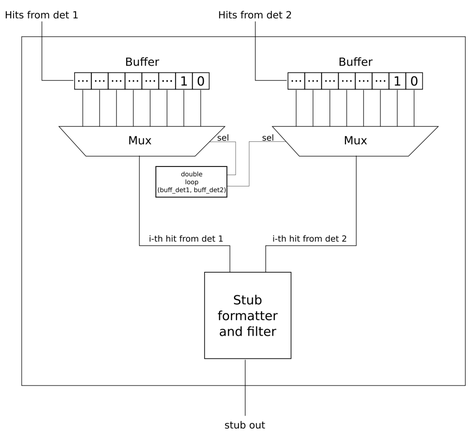
- Test architecture:
  - Stub Switch with 64 inputs, 1024 Engines, 16 Fan Ins.
  - 50% of resources of a single FPGA
  - 1/64 of the whole tracking device.

- The device is fed with Stub data.
- The processed output is compared to the expected results stored in a ROM.
- The hold logic prevents data loss by limiting the input rate.

- 320 MHz system clock
- Max. input event rate : 124.375 MHz
- Event throughput: 40.9 MHz

- The event throughput can be improved by increasing the system clock and/or the number of engines

Stub Constructor sub-logic



- Each Stub Constructor is composed by a pool of Stub Makers (in figure).
- The Stub Maker evaluates evaluates the combinatoric of hits from detector couples.
- Geometrical and timing filters are applied to select the stubs, which are provided in output.

References

- M.Petruzzo: "Gains from timing", March 22, 2018, Talk at 3rd Workshop on LHCb Upgrade II
- N.Neri: "4D fast tracking for experiments at HL-LHC", September 16, 2016, Talk at PIXEL2016
- N. Neri et al., "4D fast tracking for experiments at high luminosity LHC", JINST 11 (2016) no.11, C11040

Summary

- A real-time tracking device for application to a VELO-like detector with precise timing has been developed.

- Implemented and tested in commercial FPGA with promising results

Next plans

- Finalization of the Stub Constructor and integration in the device: the sub-modules of the Stub Constructor have been already individually tested.

- Test of the complete system with externally generated data: the data communication has already been tested and validated.

VCI2019 - The 15th Vienna Conference on Instrumentation – Vienna, 18th- 22nd February, 2019