Contribution ID: **644** Type: **Talk**

ATLAS LAr Calorimeter Performance in LHC Run-2 and Electronics Upgrades for next Runs

Friday 22 February 2019 09:50 (20 minutes)

Liquid argon (LAr) sampling calorimeters are employed by ATLAS for all electromagnetic calorimetry in the pseudo-rapidity region $|\eta| < 3.2$, and for hadronic and forward calorimetry in the region from $|\eta| = 1.5$ to $|\eta| = 4.9$. In the LHC Run-2 about 150fb-1 of data at a center- of-mass energy of 13 TeV have been recorded. The well calibrated and highly granular LAr Calorimeter reached its design values both in energy measurement as well as in direction resolution.

Electronics developments are pursued for the trigger readout of the ATLAS Liquid-Argon Calorimeter towards the Phase-I upgrade scheduled in the LHC shut-down period of 2019- 2020.Trigger signals with higher spatial granularity and higher precision are needed in order to improve the identification efficiencies of electrons, photons, tau, jets and missing energy, at high background rejection rates, already at the Level-1 trigger.

Following new TDAQ buffering requirements and high expected radiation doses in the pileup conditions of the high-luminosity LHC, the ATLAS Liquid Argon Calorimeter electronics will be upgraded (Phase-II) to readout the 182,500 calorimeter cells at 40 MHz with 16 bit dynamic range. Developments of low-power preamplifiers and shapers to meet these requirements are ongoing in CMOS 130nm. In order to digitize the analogue signals on two gains after shaping, radiation-hard, low-power 40 MHz 14-bit ADCs are developed using a SAR architecture in 65 nm CMOS.

This contribution will give an overview of the detector operation, changes in the monitoring and data quality procedures, to cope with increased pileup, as well as the achieved performance, including the calibration and stability of the electromagnetic scale, noise level, response uniformity and time resolution. Results of ASIC developments including QA/QC and radiation hardness evaluations, performances of the pre-production boards and results of the system integration tests, progress of QA/QC of final production boards will be presented along with the overall system design for the Phase-I upgrade. Results of tests of the first prototypes of front-end components will be presented, along with design studies on the performance of the off-detector readout system for the Phase-II upgrade.

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Session Classification: Plenary 4

Track Classification: Calorimeters