The PreProcessor modules for the ATLAS Tile Calorimeter at the HL-LHC

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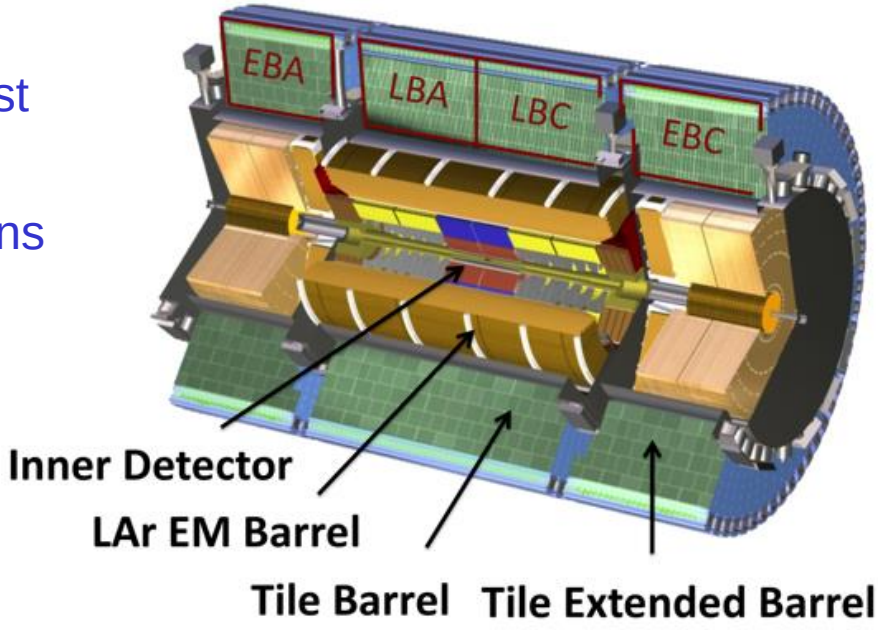
On behalf of the TileCal Upgrade group

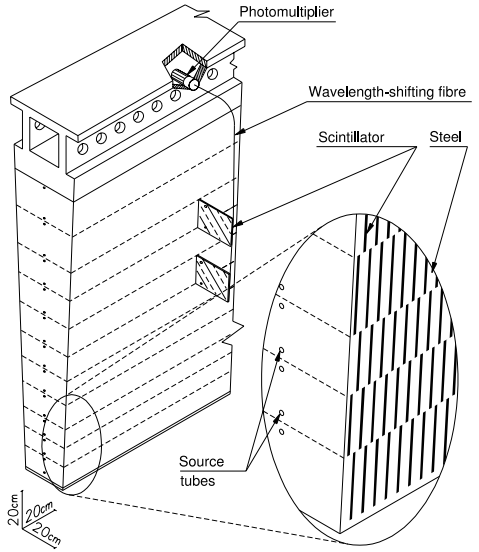
Outline

- Tile Calorimeter and Phase II Upgrade
- Development of new readout electronics
- Status of the full-size PreProcessor modules
- Summary

ATLAS Tile Calorimeter

- Segmented calorimeter of steel plates and plastic scintillator tiles which covers the most central region of the ATLAS experiment
- Measures energies of hadrons, jets, τ-leptons and E_T^{miss}
- 4 partitions: EBA, LBA, LBC, EBC
- Each partition has 64 modules
  - One drawer hosts up to 48 PMTs

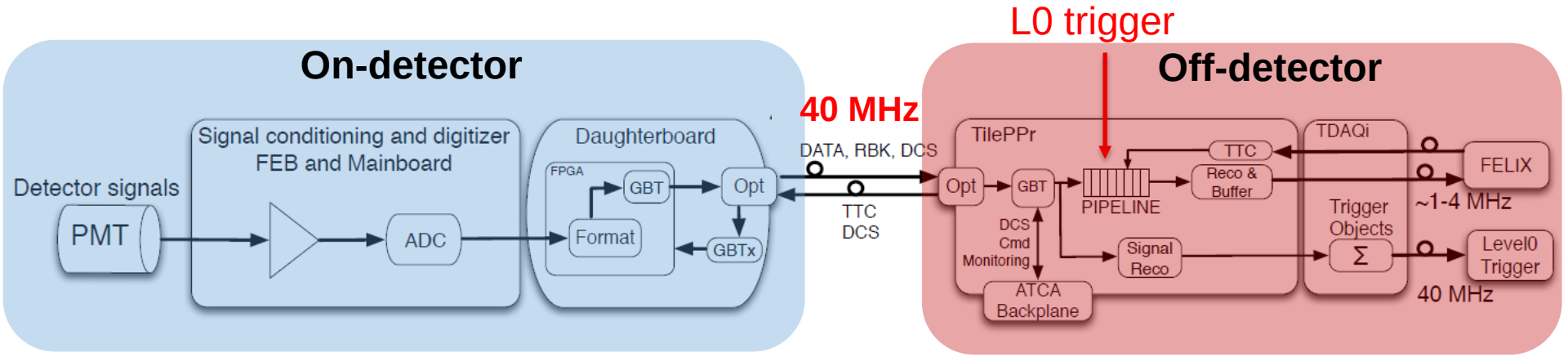




- Light produced by a charged particle passing through a plastic scintillating tile is transmitted to the PMTs
- Scintillator tiles are read out using wavelength shifting fibers coupled to PhotoMultiplier Tubes (PMTs)
- Around 10,000 readout channels

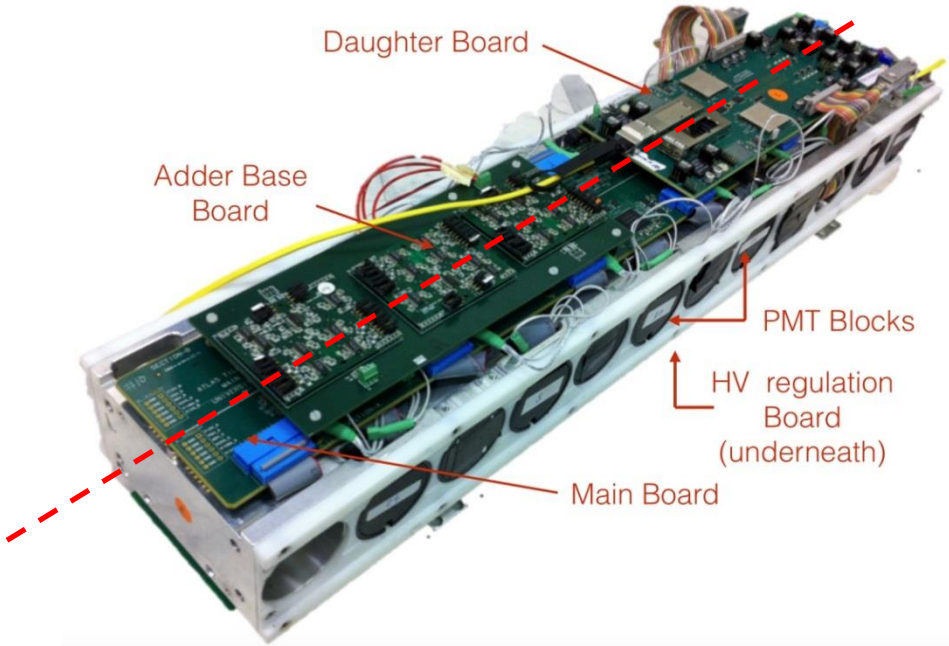
TileCal Phase II Upgrade

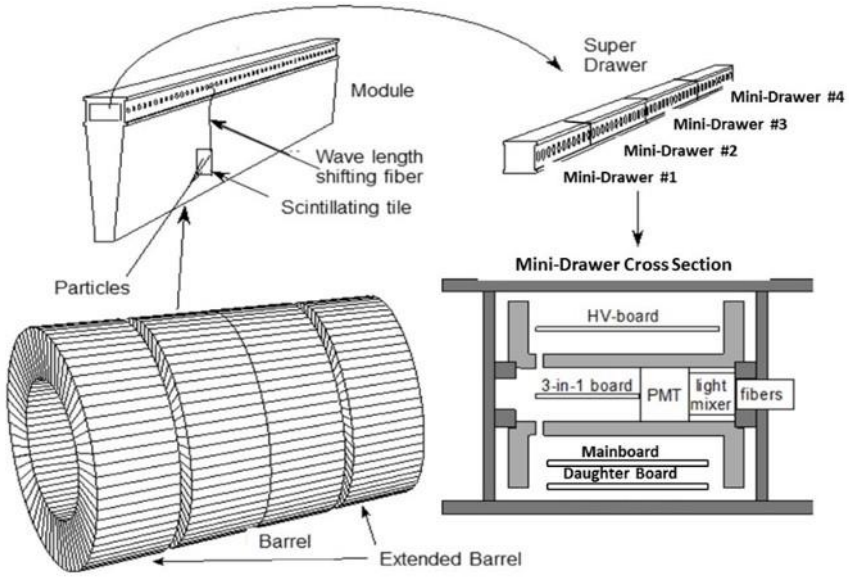
- **Large Hadron Collider plans to increase the instantaneous luminosity by a factor 5-7 around 2027→ High Luminosity-LHC**
- **Complete replacement of on-detector and off-detector readout electronics**
  - Aging of electronics due to time and radiation
  - Current readout system is not compatible with Phase II TDAQ architecture
- **New readout strategy for HL-LHC**
  - On-detector electronics will transmit digitized data to the off-electronics at the LHC frequency (40 MHz) → **40 Tbps to read out the entire detector!**
  - Buffer pipelines are moved to off-detector electronics
  - Redundancy in data links and power distribution → improve system reliability



Phase II on-detector electronics

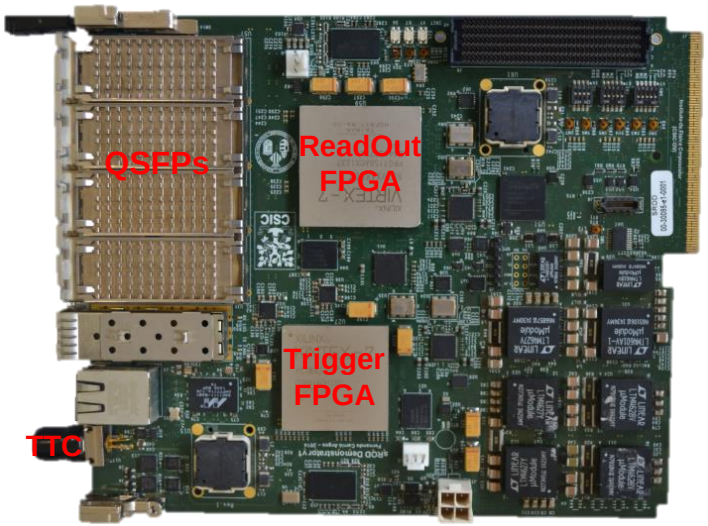
- The **Phase II module** is composed of 4 mini-drawers (48 PMTs). Each mini-drawer have 2 independent read out sections **for redundant cell readout**
  - 12 PMTs + 12 front-end boards reading out 6 TileCal cells
  - 1 × MainBoard: operation of the front-end boards
  - 1 × DaughterBoard: data high speed link with the off-detector electronics
  - 1 × High Voltage regulation board: Remote or Internal options
  - 1 × Low Voltage Power Supply (LVPS): low voltage power distribution



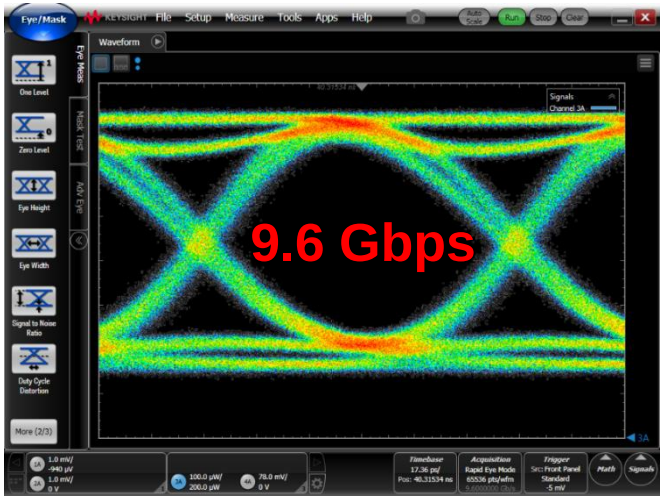


Tile PreProcessor

- **Core element of the off-detector electronics**
  - Data processing and handling from detector
  - Clock distribution towards the modules
  - Detector Control System data distribution
  - Interfaces with the ATLAS trigger and ATLAS readout systems (FELIX)
- **Fully functional prototype - Demonstrator**
  - Xilinx Virtex 7 (48 GTX), Kintex 7 (28 GTX)
  - 4 QSFPs, TX+RX Avago MiniPODs
  - Double mid-size AMC (µTCA / ATCA carrier)
  - 1/8th of the full-size PreProcessor
- **Operates 4 mini-drawers → 160 Gbps!**
- **Bit Error Rate Tests**
  - 16 links at 9.6 Gbps with PRBS31 pattern during 115 hours
  - BER better than $5 \cdot 10^{-17}$ for a CL of 95%



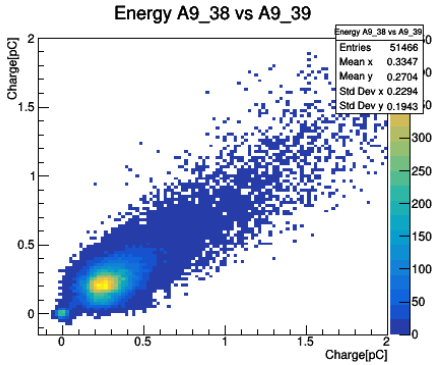
PPr Demonstrator

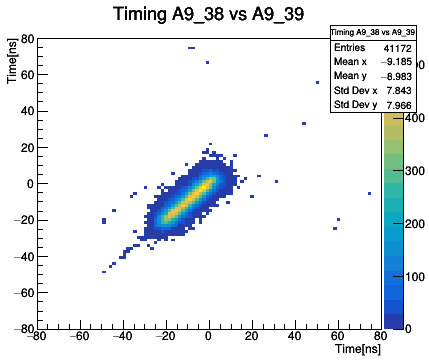


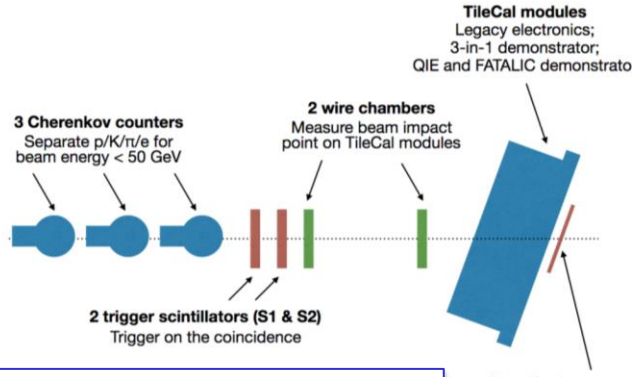
Eye diagram at 9.6 Gbps

Test Beam setup

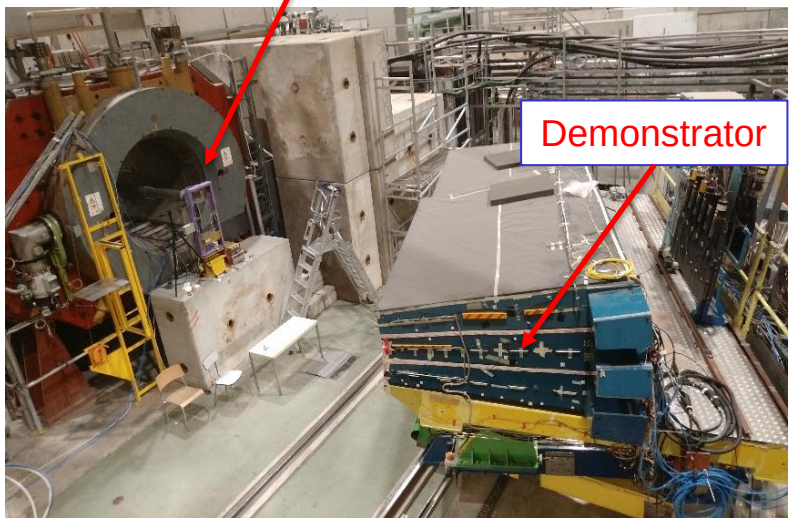
- Located at the **S**uper **P**roton **S**ynchrotron (SPS) North Area on the H8 beam line
- Detector modules equipped with upgraded and legacy electronics for performance comparison
- Fully integrated with the ATLAS TDAQ software and DCS system
  - Front-end electronics configuration
  - Physics, calibration and laser runs
  - HV and LV control/monitoring
- Data taking through FELIX / legacy system
- Phase II clock and readout architecture







Beams of Hadrons, Electrons and Muons were used to study the calorimeter response

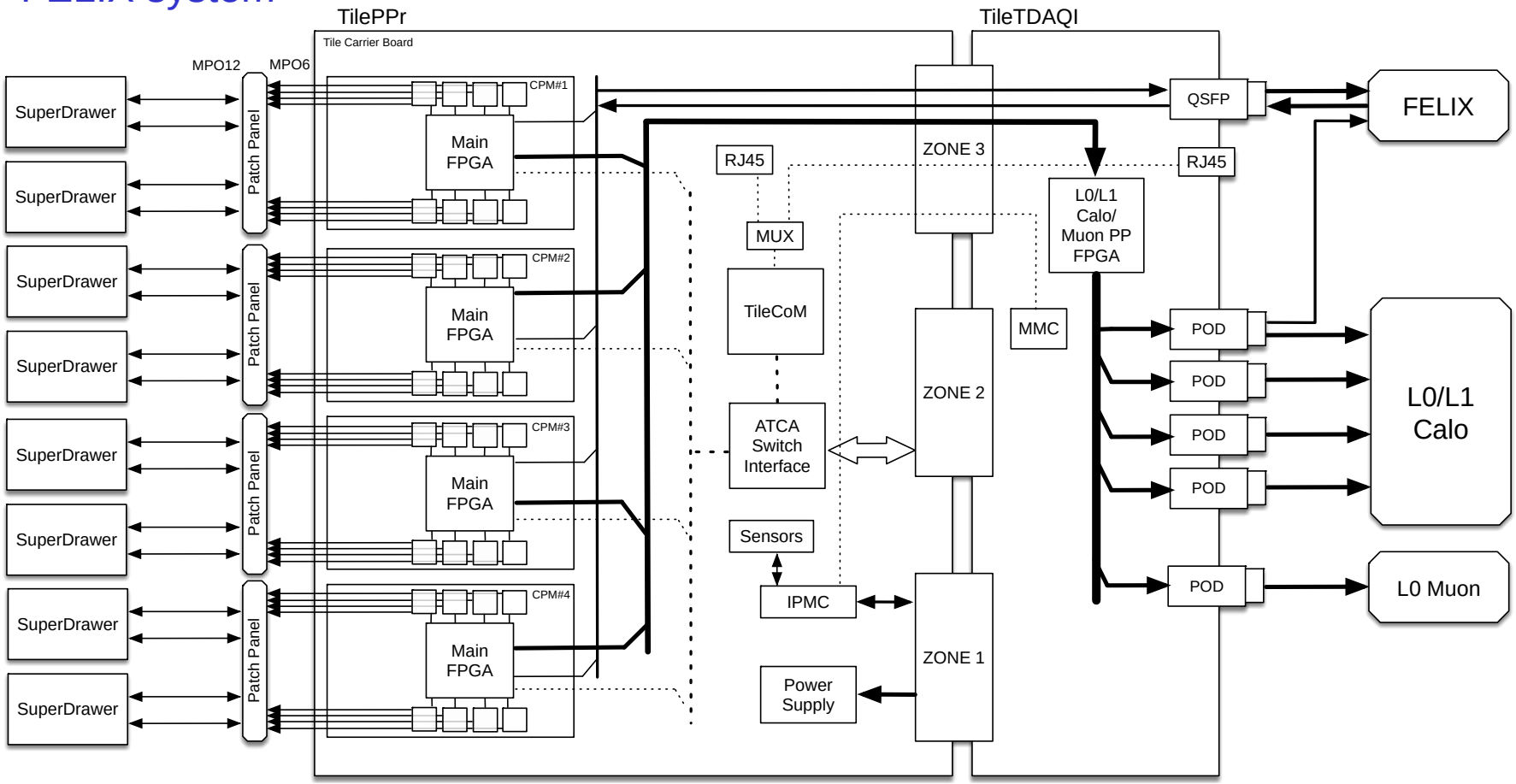


Test beam setup at H8 line

- **Insertion of a demonstrator module into the ATLAS experiment this Spring**

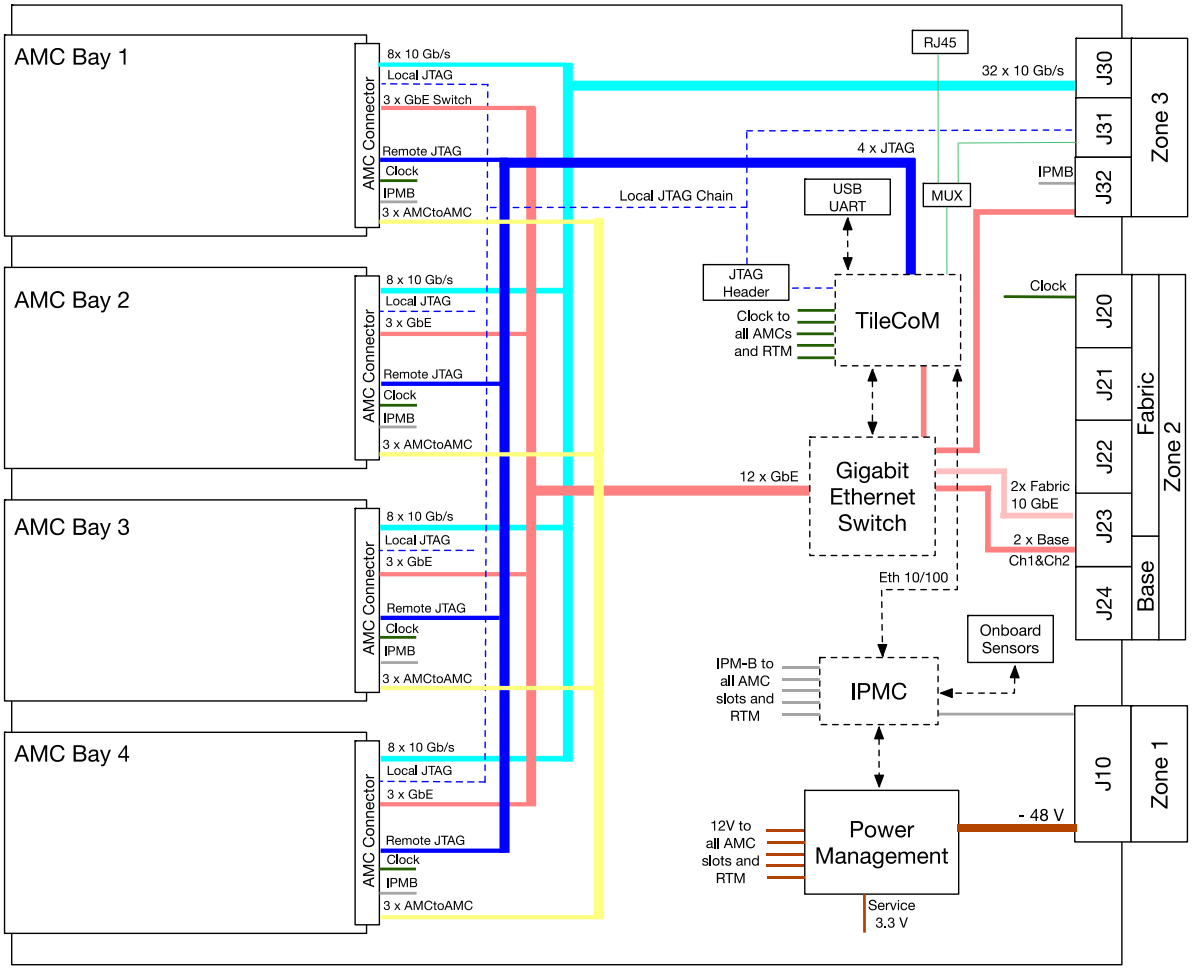
Full-size PreProcessor

- **32 TilePPr boards in ATCA format:** ATCA carrier + 4 Compact Processing Modules
- **32 TileTDAQ-I:** Preprocesses trigger data and interfaces with L0Calo, L0Muon and FELIX system



ATCA Carrier Base Board

- Full-Size ATCA board
  - 14 layers, FR4 dielectric
  - 2.4 mm thickness
  - PCB cutaway to improve cooling
- Zone 1: Power distribution to CPMs and TDAQ-I
  - Max power of 400 W
- Zone 2: GbE + XAUI 10G
  - Communication with rest of the ecosystem
- Zone 3: Communication between CPMs and TDAQ-I
  - GbE lines, 16 Gbps lines
- First prototypes being produced



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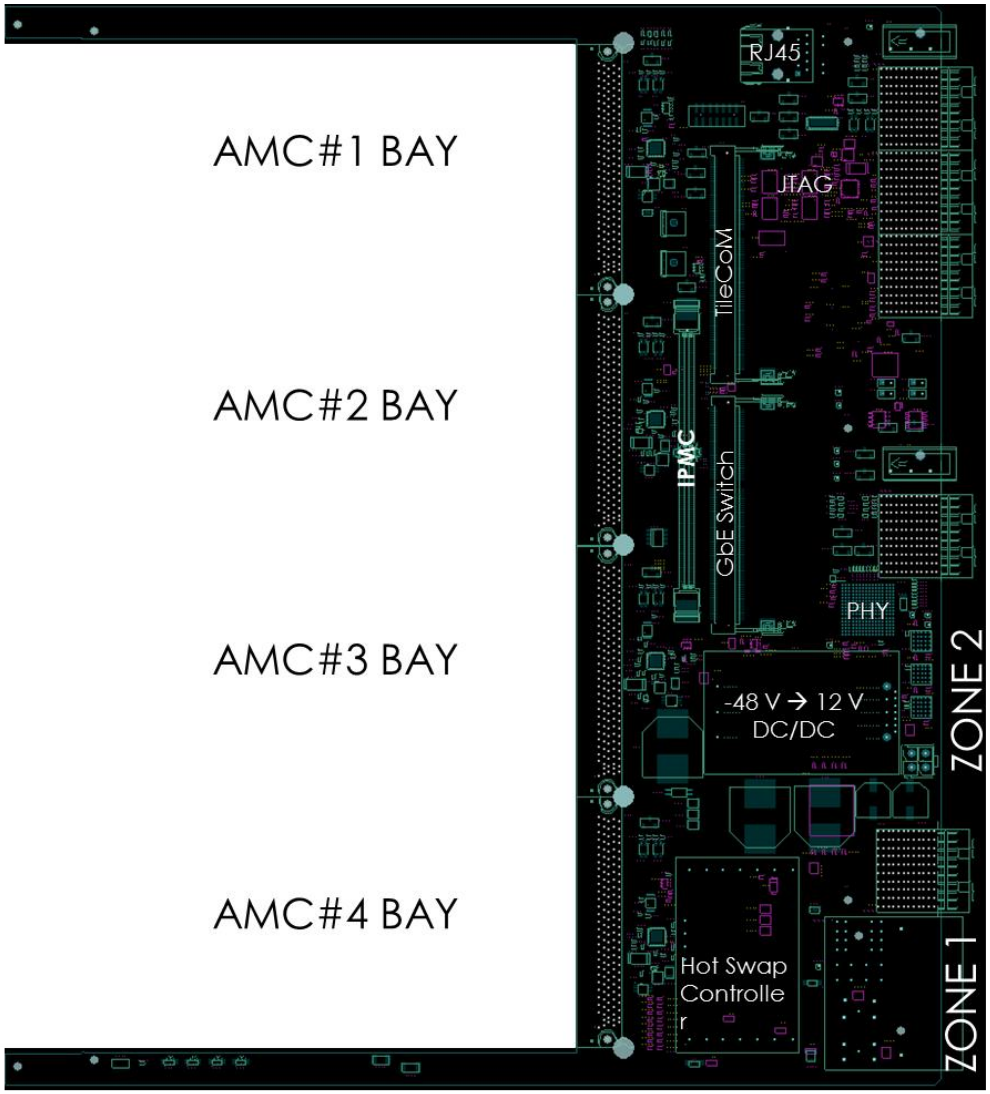
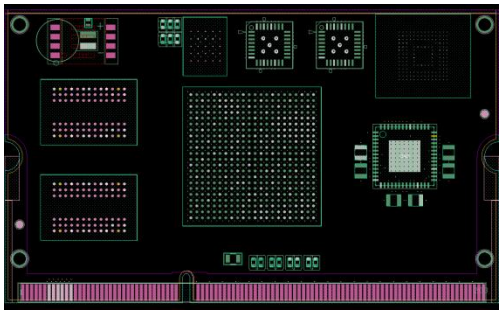


Mezzanine boards

- **Compact, replaceable and upgradeable solution**

- TileCoM - Computer on Module
  - Embedded Linux – PetaLinux distribution
  - Remote programming, DCS monitoring, clock generation for standalone tests
  - Xilinx Zynq UltraScale+ XCZU2CG + 512 MB DDR4
  - 10 layers - DDR3 form factor (67.6 mm x **40.00** mm)



Prelayout of the TileCoM

- Ethernet switch module
  - Unmanaged Ethernet Switch chip Broadcom BCM5396
  - 16 GbE connection between CPMs and TDAQ-I
  - 6 layers - DDR3 form factor (67.6 mm x 30.00 mm)

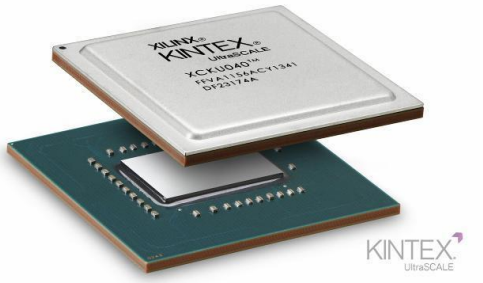
GbE switch

- IPMC mezzanine board (CERN)
  - Microsemi A2F200, DIMM-DDR3 VLP form factor
  - Hot swap, sensor monitoring, power management

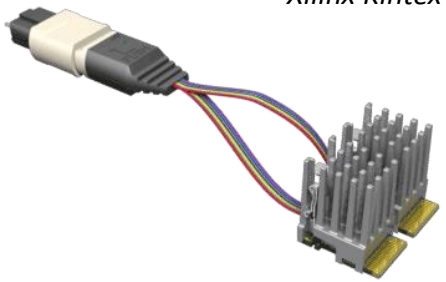
IPMC mezzanine board

Compact Processing Module

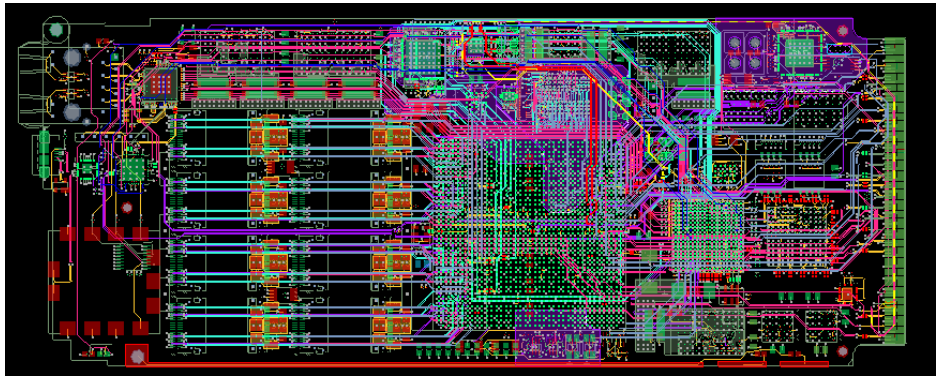
- Single AMC board with Kintex Utrascale FPGA
  - 32 bidir-channels in 8 Samtec Firefly modules
  - 16 bidir-channels through backplane (PCIe, GbE)
  - Different line rates & clocking schemas supported
- High bandwidth readout system
  - Up to 500 Gbps via optics
  - Up to 260 Gbps via electrical backplane
- First prototypes at the end of March



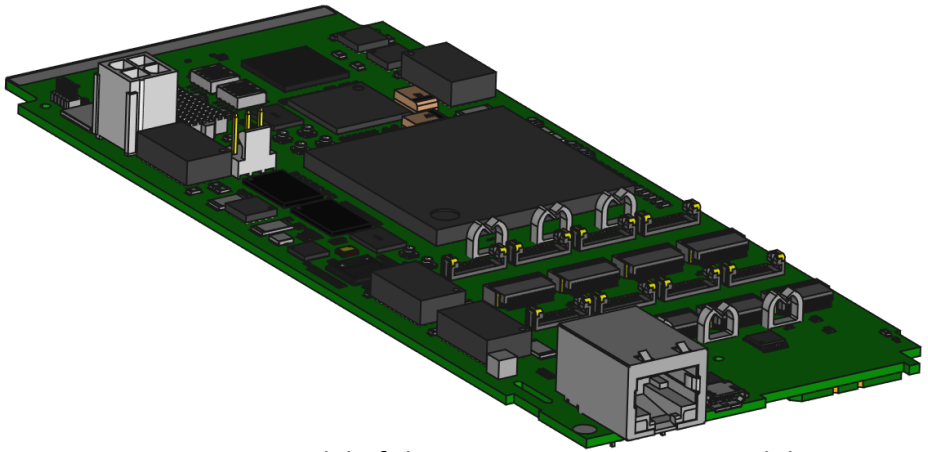
Xilinx Kintex UltraScale



Samtec FireFly module



Layout of the Compact Processing Module



3D model of the Compact Processing Module

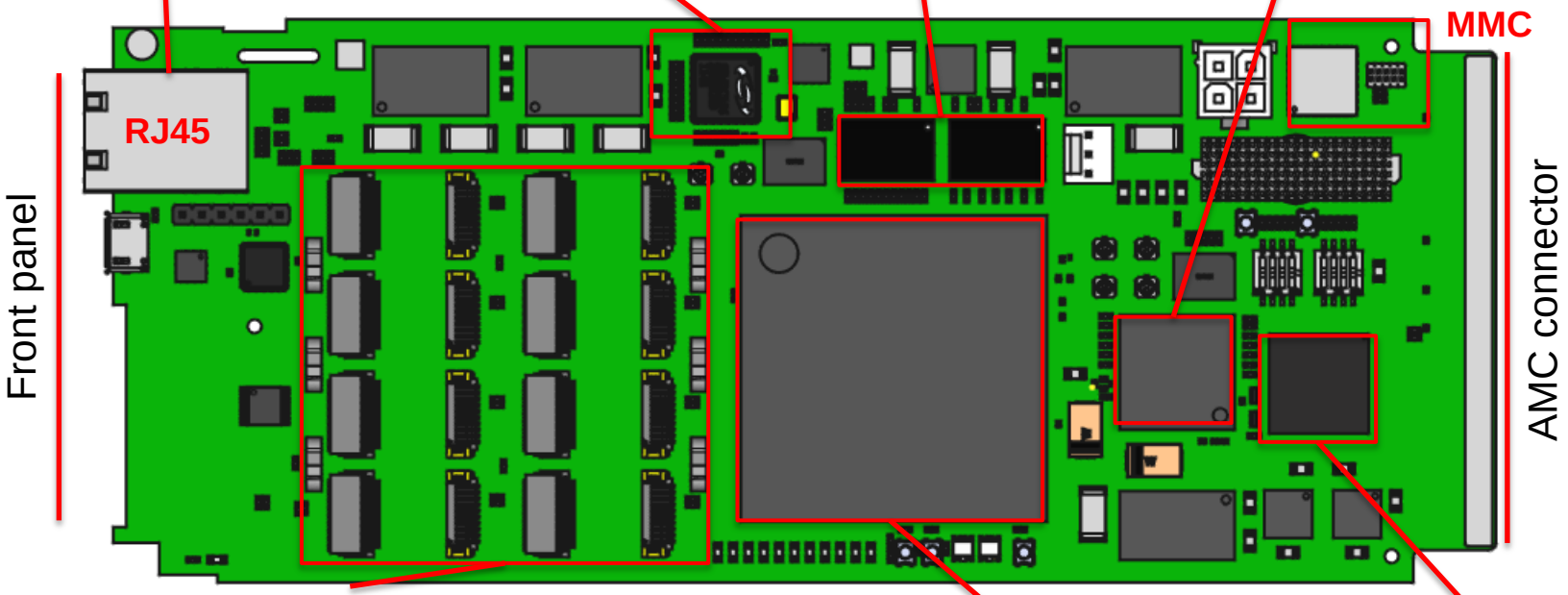
Compact Processing Module

Ethernet Communication

Silicon Labs si5345
Clock generator
Jitter cleaning

DDR4
512 MB

Artix 7 35T
Slow control + monitoring
Clock phase measurement



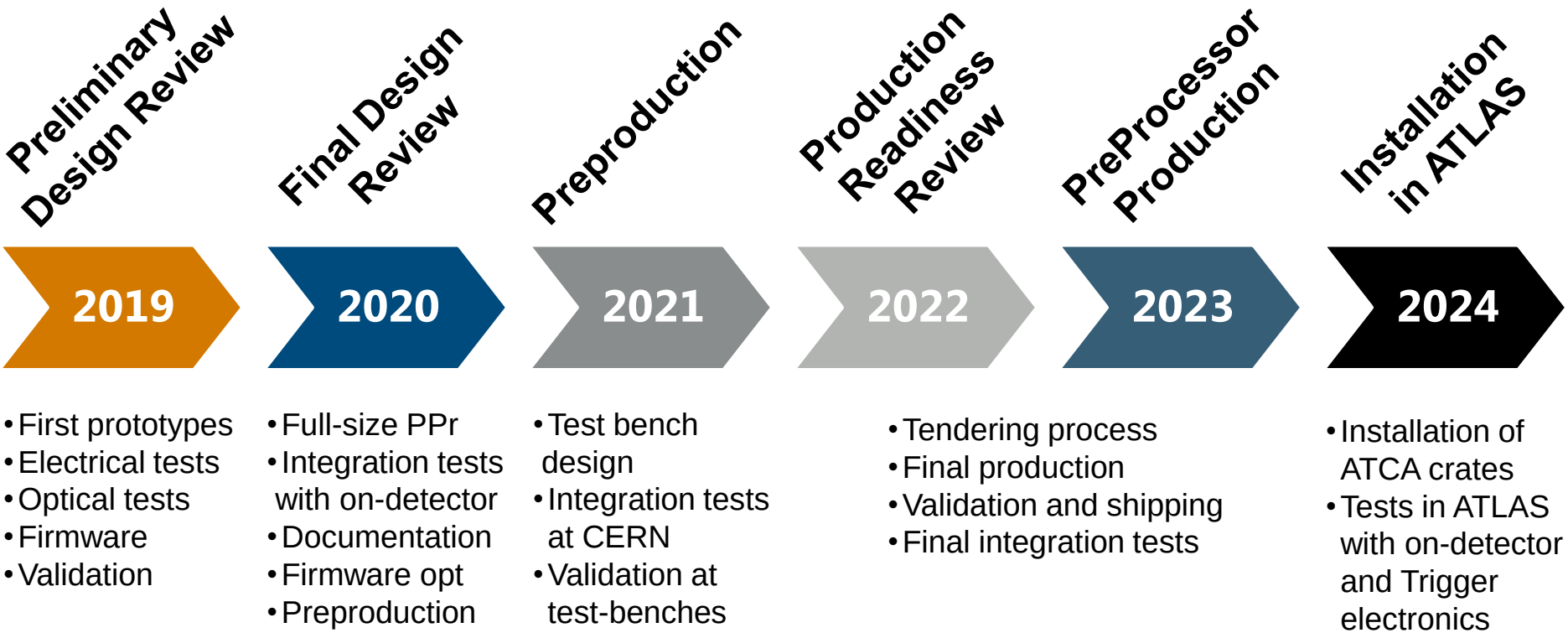
8 x Samtec Firefly optical modules
4 bidir optical links up to 14 Gbps
MXC connectors ending

Kintex UltraScale KU085
Acquisition
Data buffering
Processing

Analog LTC2977
Power monitoring
PMBus interface

- 14 layers → 1.6 mm thickness
- ISOLA FR408HR → $\varepsilon_r = 3.65$ with low dissipation losses

Planning



- Preproduction (25%) from Q3 2020 to Q1 2022
  - 8 ATCA carriers, 32 CPMs
- Final production (75%) from Q2 2022 to Q3 2023
  - 24 ATCA carriers, 96 CPMs

Summary

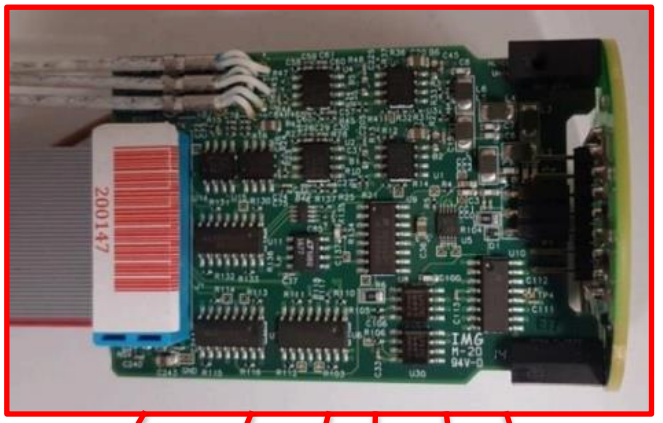
- Complete redesign of the on-detector and off-detector readout electronics for the HL-LHC
- Development of readout electronics prototypes are done and tested
- Fully operational PreProcessor prototype has been designed and qualified
- Extensively tested in several test beam campaigns during 2015 and 2018
  - All prototypes showed a good performance
  - Readout electronics implements the clock and data architecture for HL-LHC
- Insertion of a demonstrator in ATLAS experiment during May 2019
- Full-size PreProcessor modules are under design / production
  - ATCA carrier + 4 Compact Processing Modules
  - First units expected for Q1 2019


Thank you for you attention!
M0+
DANGER

BACKUP

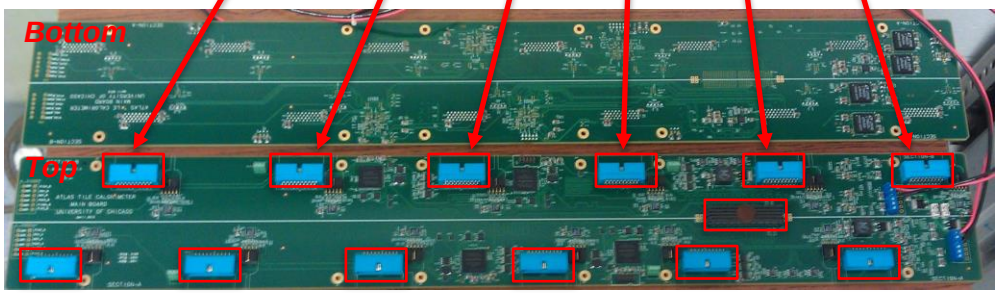
Front-End Boards and MainBoard

- **Front-end boards:** FENICS cards
  - **PMT pulse shaping**
  - Shaper with bi-gain output: 1 × LG + 1 × HG
  - High precision slow integrator
  - Design based on current 3in1 cards
    - Improved noise and linearity
    - Improved calibration circuitry



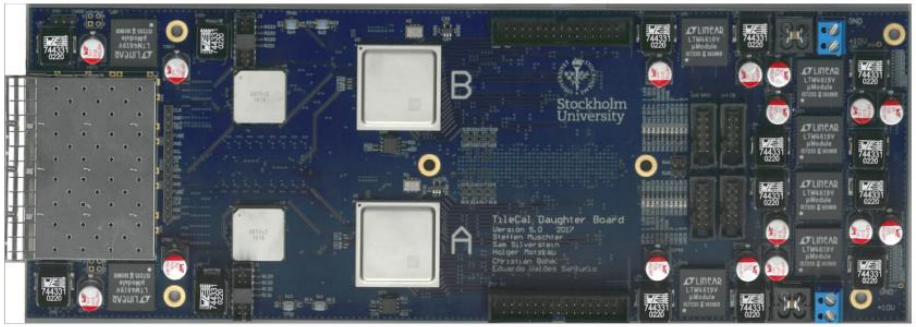
FENICS cards

- **MainBoard**
  - **Digitize analog signals coming from 12 FEBs**
  - Routes the digitized data from the ADCs to the DaughterBoards
  - Digital control of the FEBs
  - HG and LG, 12-bit samples @40 Msps
  - TID, NIEL, SEE tests performed

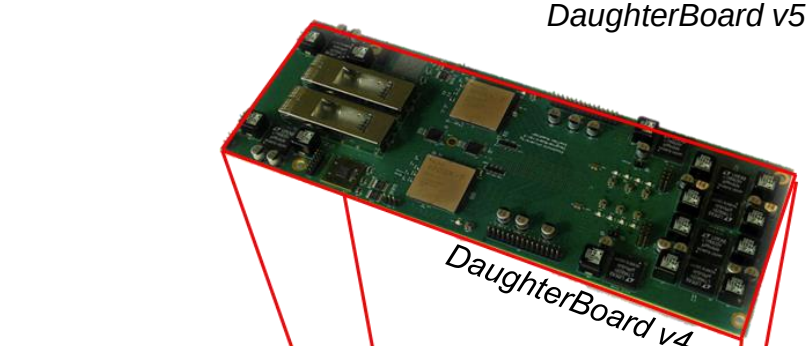


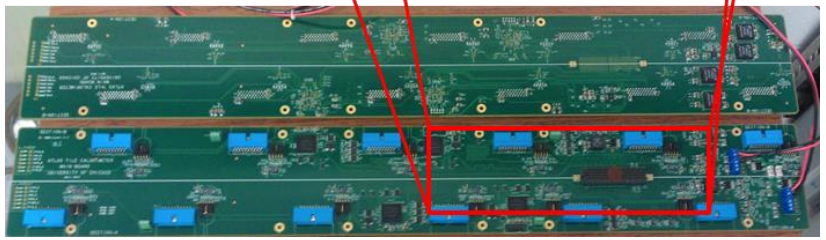
DaughterBoard

- **High-speed link with the back-end electronics**
  - Data collection and transmission
  - Clock and command distribution
  - Data link redundancy
- Daughterboard version 5
  - 2 × GigaBit Transceiver (GBT) chips
  - 2 × Xilinx UltraScale+ FPGAs
  - 4 × SFP modules → ~40 Gbps
- TID tests with ~ 9 MeV electron beam
- SEE and SEL tests done with 58 MeV and 226 MeV proton beam
  - Soft error rate is low → Triple redundancy
  - No destructive effects observed



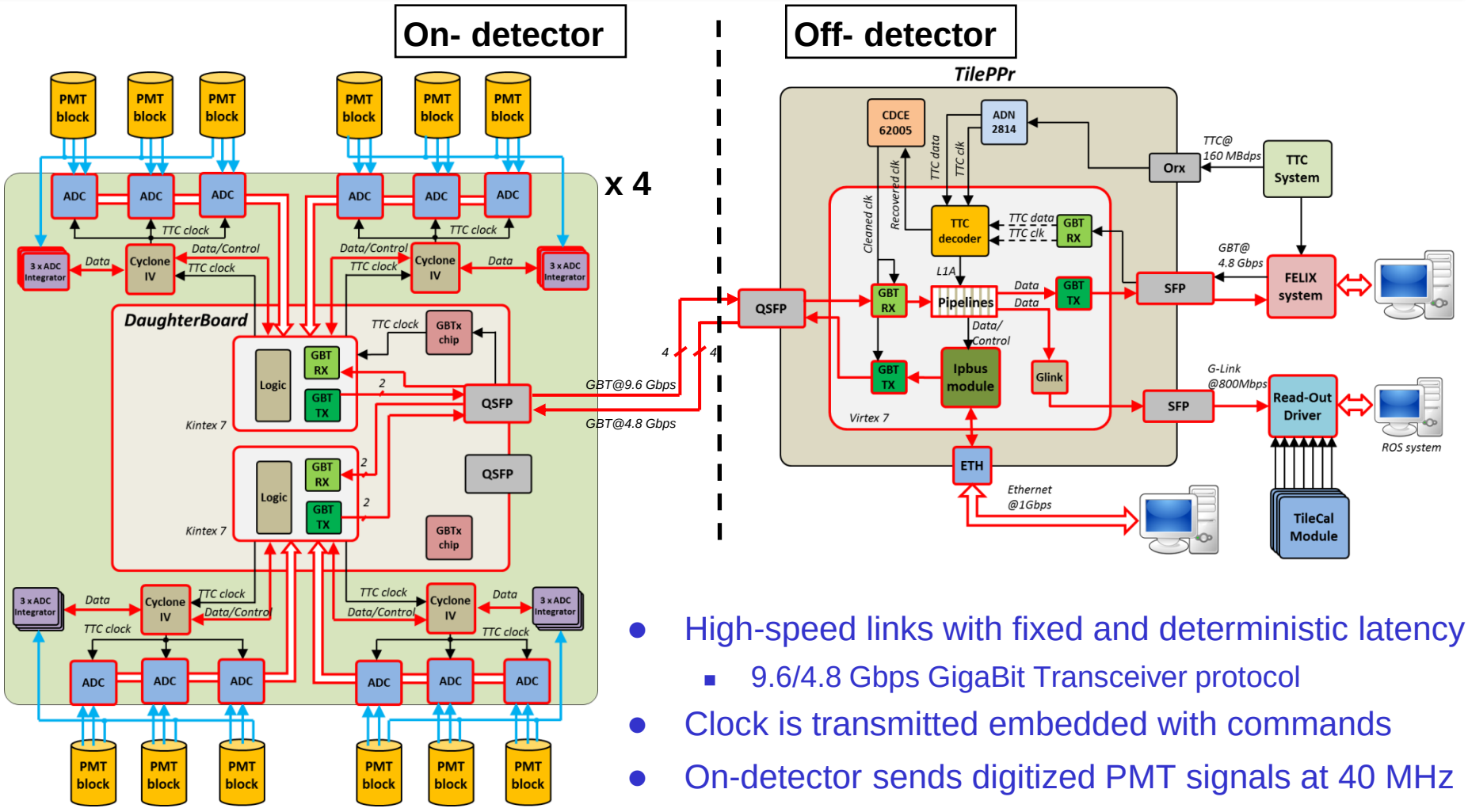
DaughterBoard v5





MainBoard

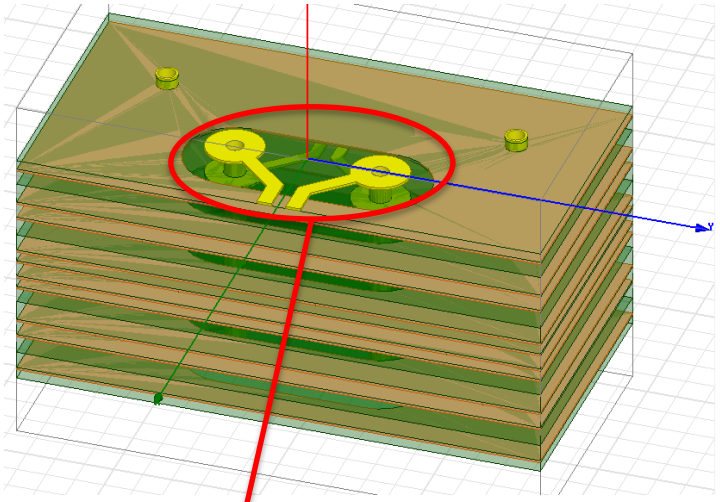
Clock and dataflow schema

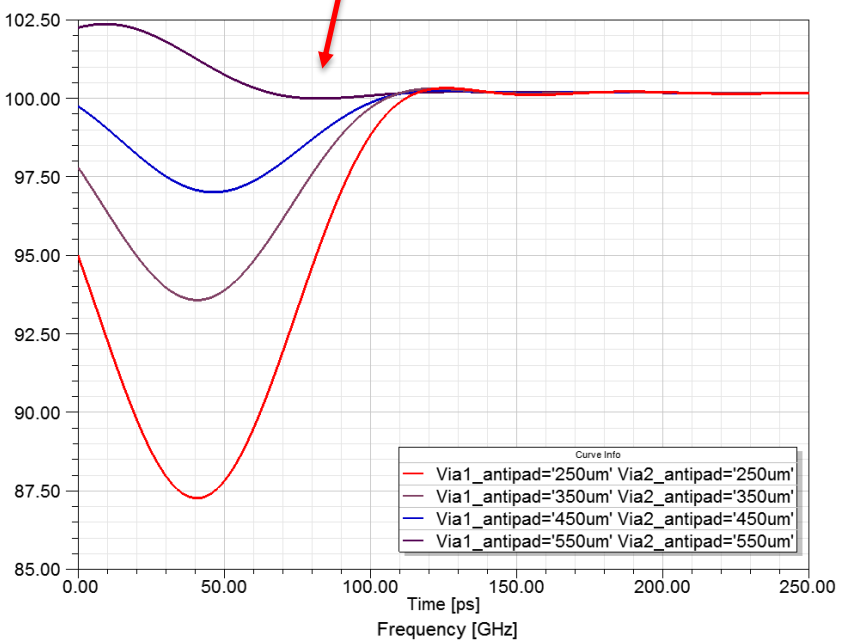


- High-speed links with fixed and deterministic latency
  - 9.6/4.8 Gbps GigaBit Transceiver protocol
- Clock is transmitted embedded with commands
- On-detector sends digitized PMT signals at 40 MHz
- Two independent readout paths:
  - FELIX system / Legacy Read Out Drivers

Layout design -Demonstrator

- Detailed design of 10 Gbps lines
  - Differential and characteristic impedances
  - Supression of impedance discontinuities
    - Differential via design
    - DC-coupling capacitors
  - S-parameters extraction for crosstalk studies: FEXT and NEXT
  - Post-layout simulations to evaluate the total jitter





- Power distribution design
  - 10 voltage regulators: low noise design
  - Simulation of voltage drops due to high currents (IR drops)