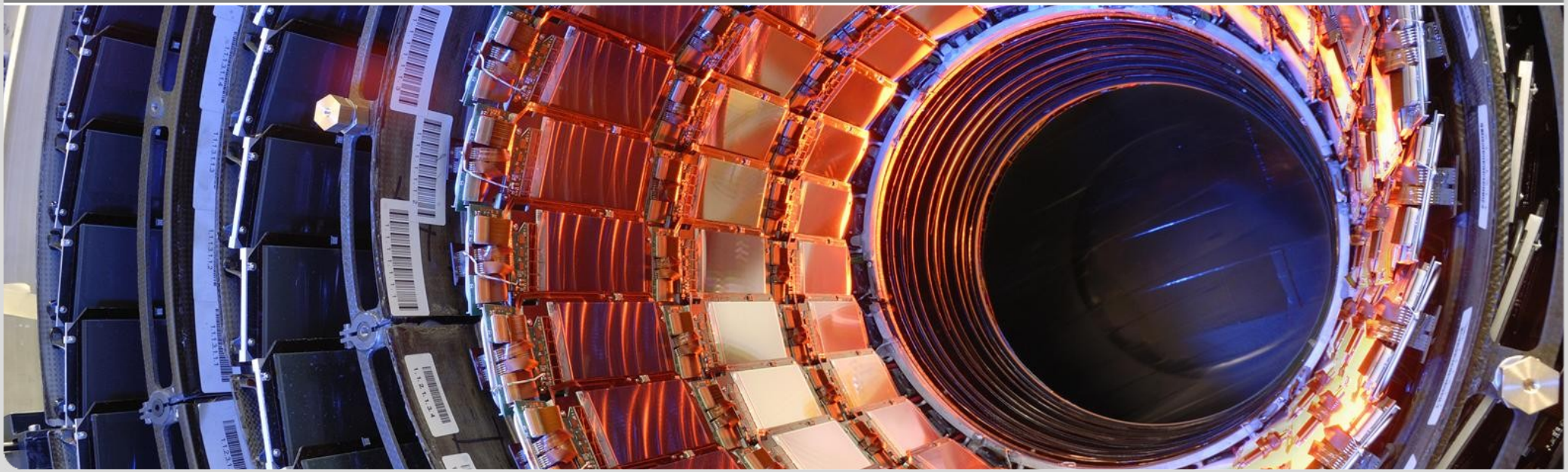
Karlsruhe Institute of Technology

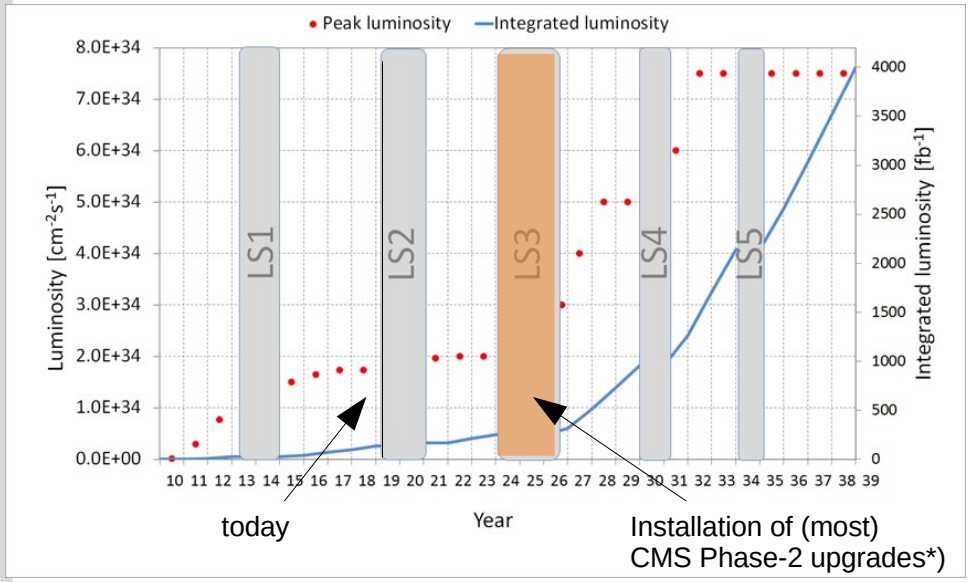
The CMS Outer Tracker for the High Luminosity LHC

Erik Butz for the CMS Collaboration

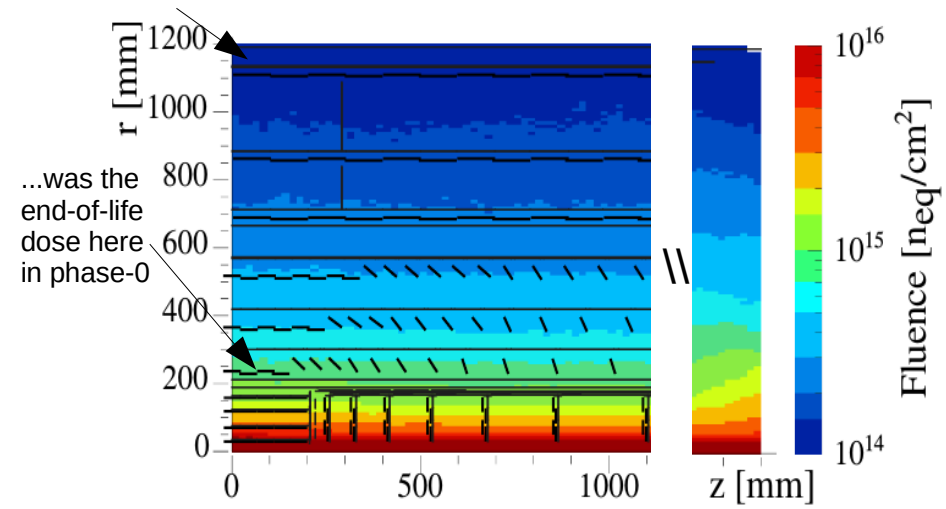
Institute of Experimental Particle Physics (ETP)



High Luminosity LHC



This fluence...

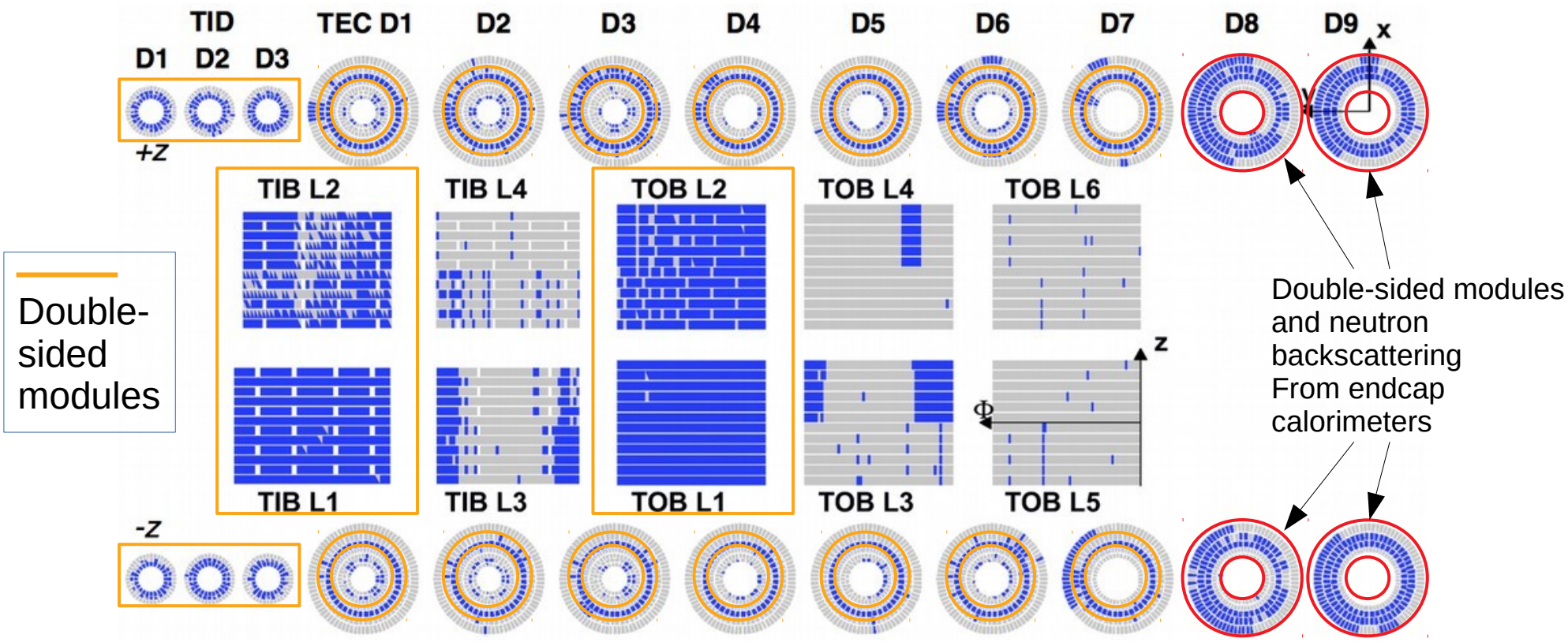


- Luminosity upgrade for post-LS3 running
  - 4000 fb^{-1} integrated luminosity
  - Peak luminosity ~7.5×10^{34} $cm^{-1}s^{-1}$
  - Pile-up of up to 200
  - Hit rates up to 3 GHz/cm^2 in innermost layers (~3 cm)
- Inner layers of pixel detectors (r = few cm) fluences in excess of 10^{16} MeV neutron equivalent/cm^2
- Even outer layers "far away" from interaction point will see >10^{14} MeV neutron equivalent/cm^2

*) The CMS High Granularity Calorimeter for the High Luminosity LHC,Rachel Yohay, today 14:00, EI7
The CMS ECAL Phase-2 Upgrade for High Precision Timing and Energy Measurements, Federico Ferri, today 17:45, EI9
already yesterday: Development of the CMS Mip Timing Detector, Marco Toliman Lucchini

Why change the current tracker?

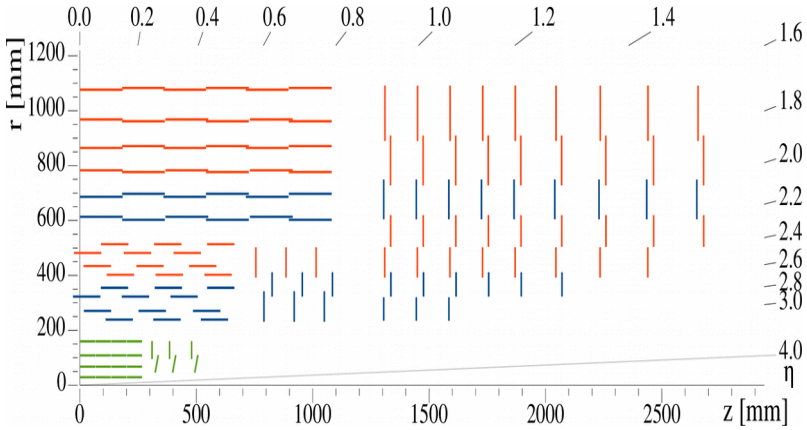
- Many layers of current strip tracker will become in-operational because of either leakage current or full depletion voltage limitations at 1 ab-1
  → full tracker replacement needed early in Run-4 at the latest



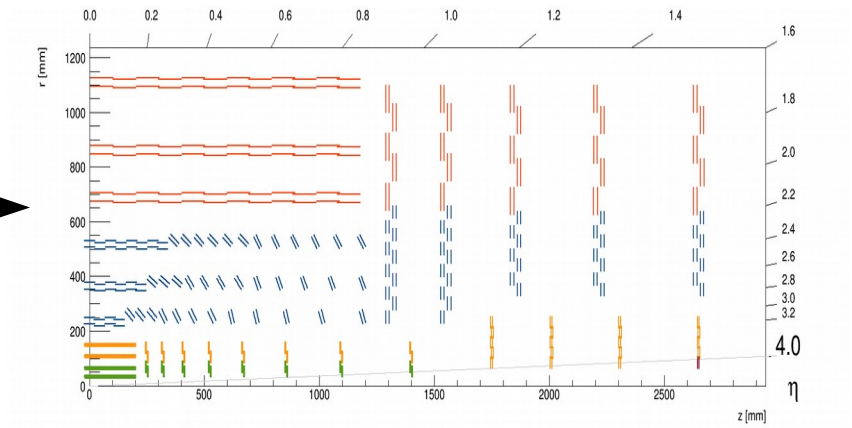
Phase-0 Outer Tracker at 1000 fb^{-1} at -20°C coolant set point

CMS Outer Tracker – post LS3

CMS Phase 0/1



CMS Phase 2

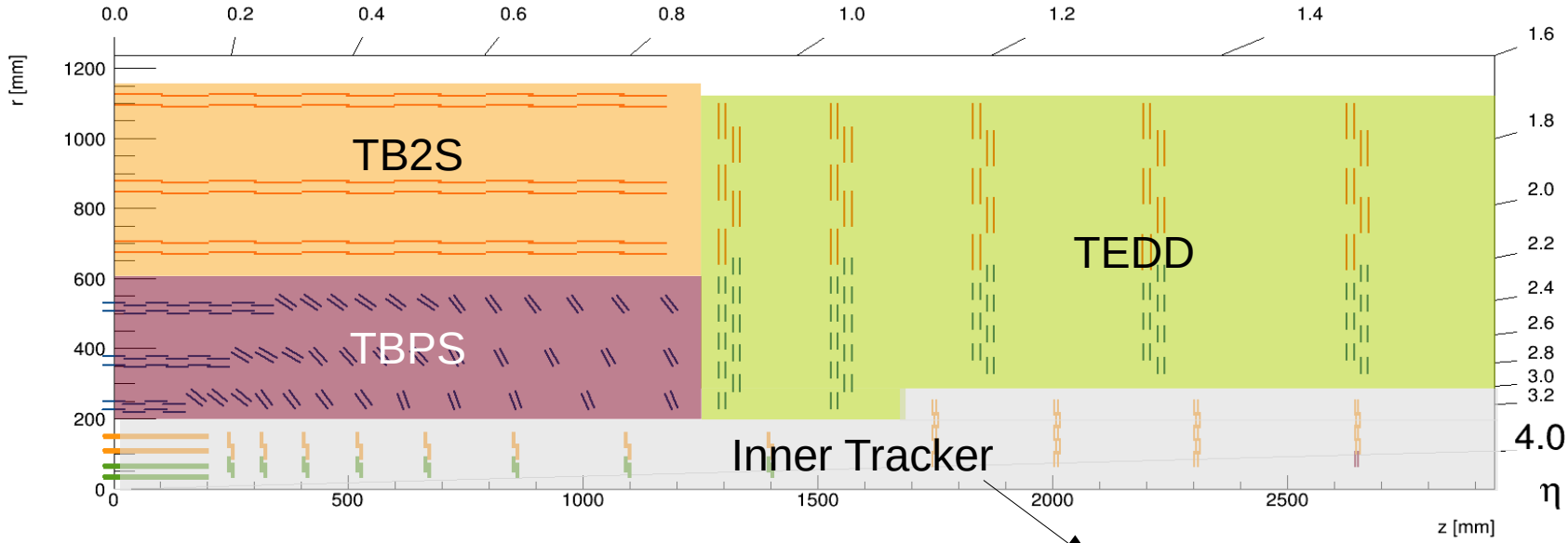


How do we get from here*)…

… to here ?

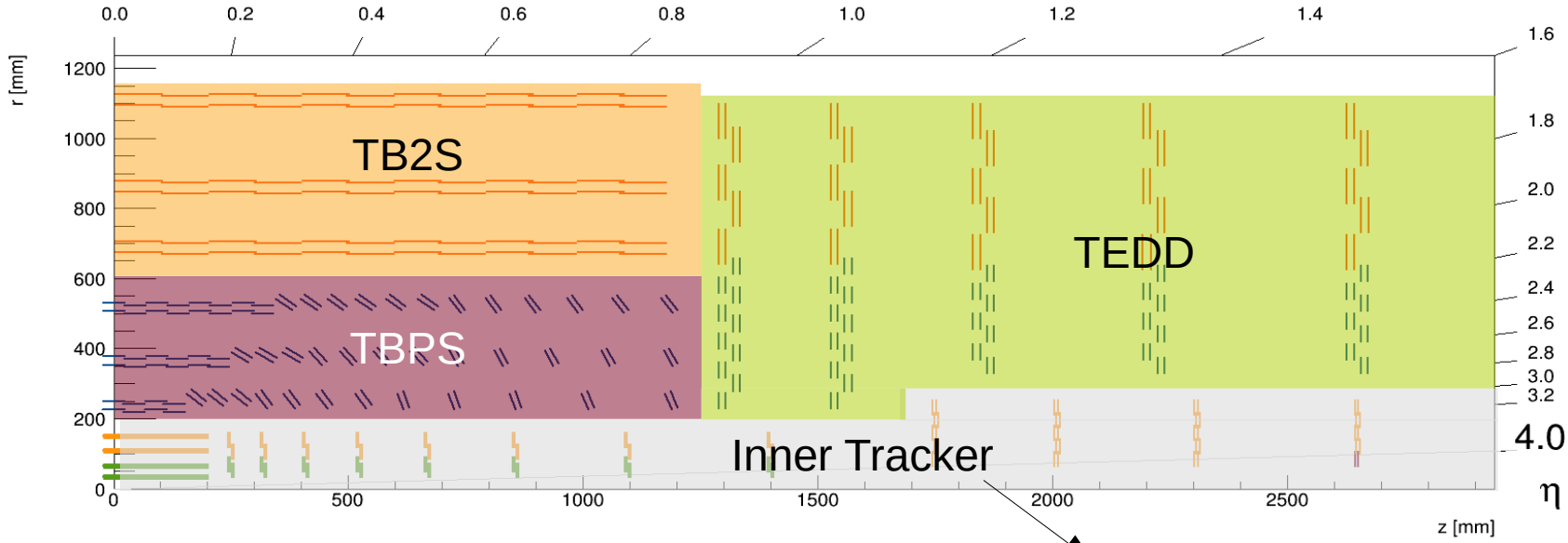
*) Operational Experience of the Phase-1 CMS Pixel Detector, Benedikt Vormwald, today, 16:55, EI7

The Phase-2 CMS Outer Tracker



The CMS Pixel Detector for the High Luminosity LHC
Giacomo Sguazzoni, 17:20 today, EI7

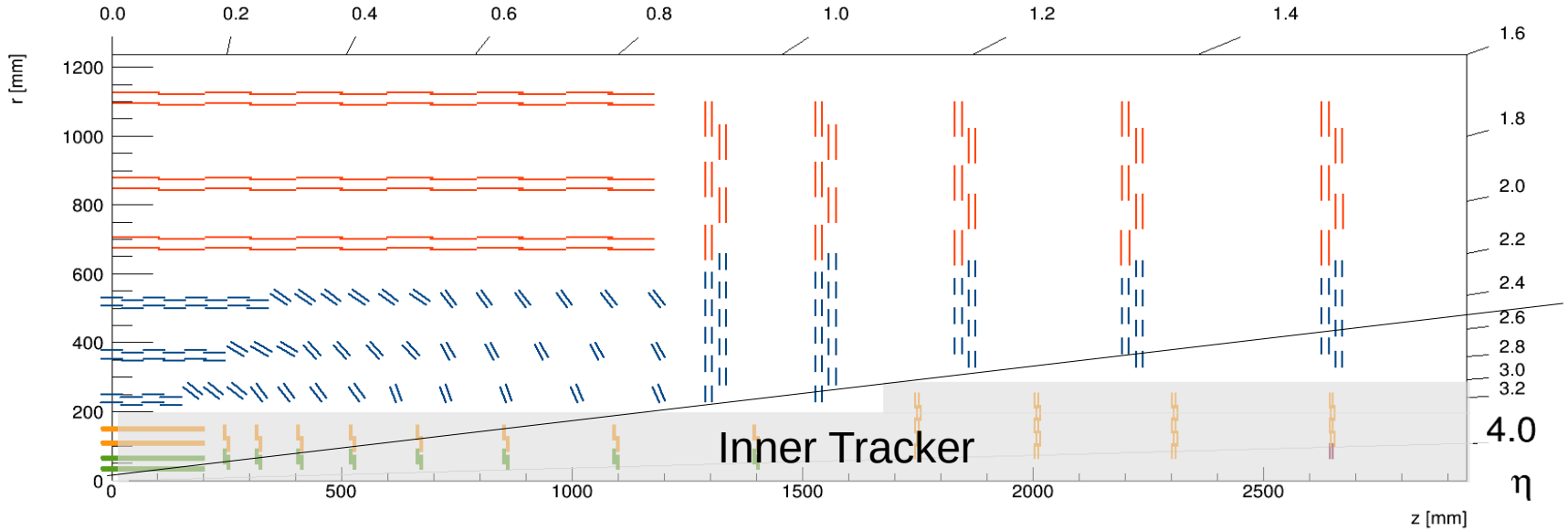
The Phase-2 CMS Outer Tracker



The CMS Pixel Detector for the High Luminosity LHC
Giacomo Sguazzoni, 17:20 today, EI7

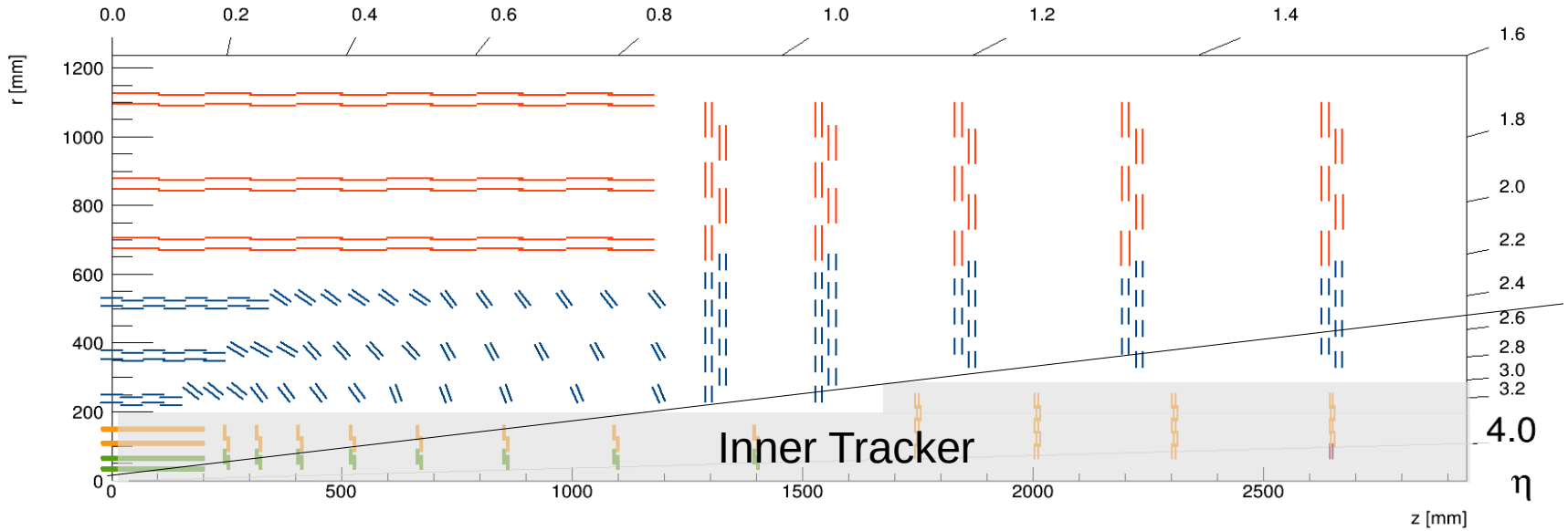
- TB2S = Tracker Barrel [with] 2S [Modules]
- TBPS = Tracker Barrel [with] PS [Modules]
- TEDD = Tracker Endcap Double Disk

The Phase-2 CMS Outer Tracker



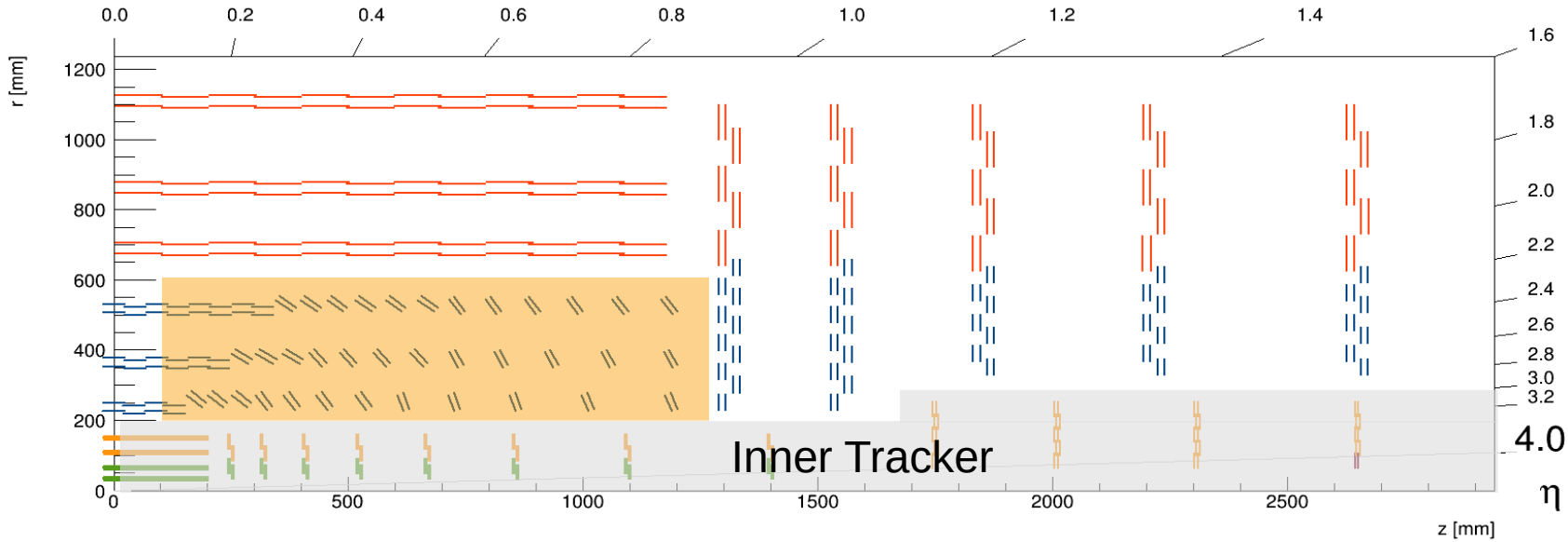
- Coverage up to $\eta \sim 2.5$

The Phase-2 CMS Outer Tracker



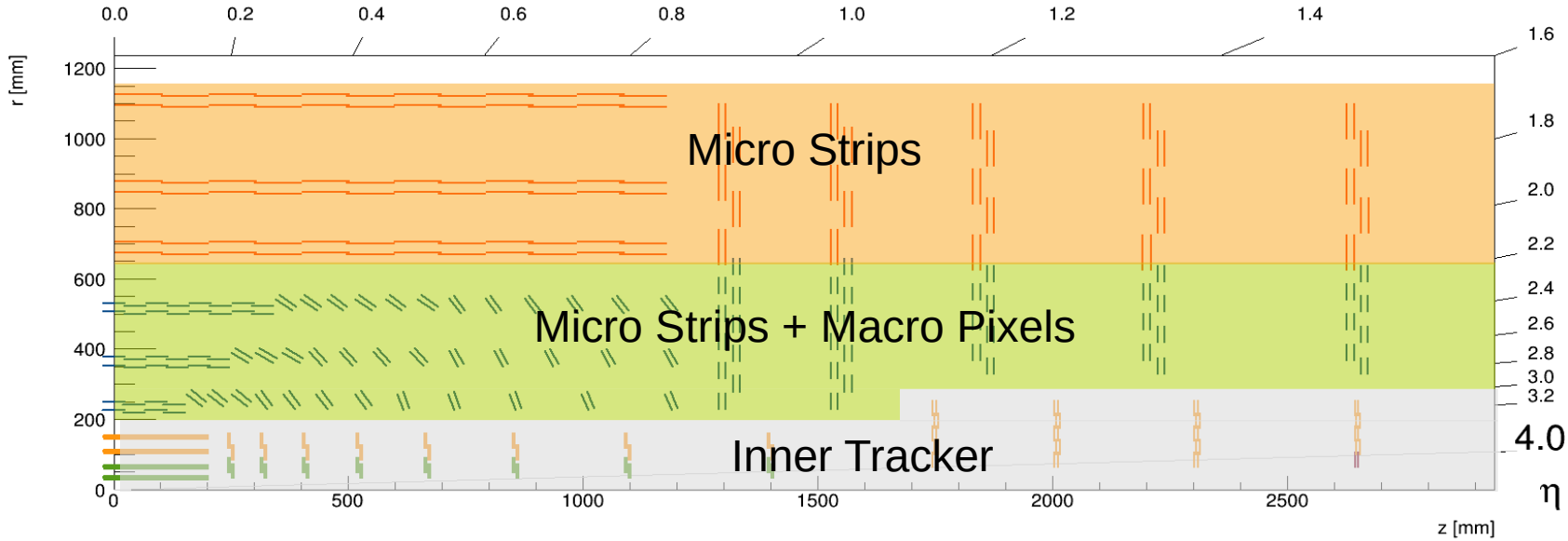
- Coverage up to $\eta \sim 2.5$
  - Tracking → with pixel up to $\eta \sim 4$
  - L1 triggering

The Phase-2 CMS Outer Tracker



- Coverage up to $\eta \sim 2.5$
  - Tracking → with pixel up to $\eta \sim 4$
  - L1 triggering
- Tilted geometry for better trigger performance and reduction in #modules

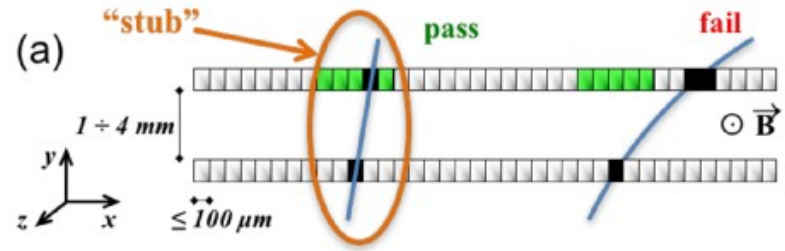
The Phase-2 CMS Outer Tracker

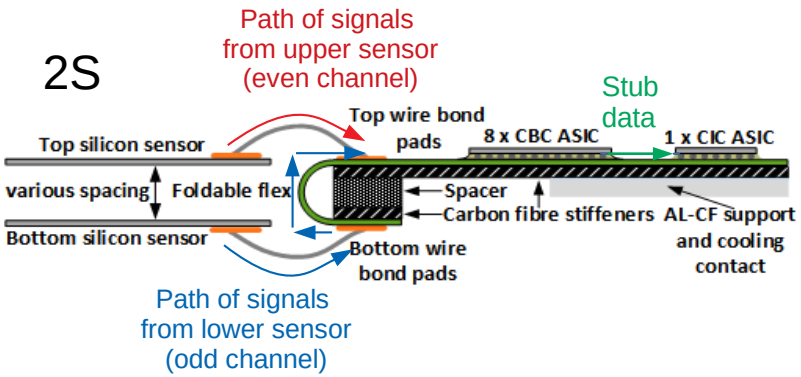


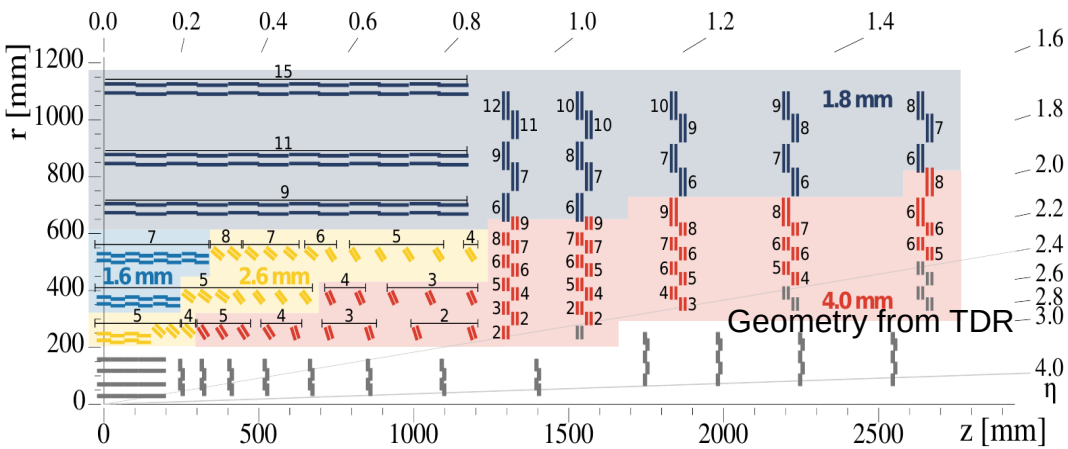
- Coverage up to $\eta \sim 2.5$
  - Tracking → with pixel up to $\eta \sim 4$
  - L1 triggering
- Tilted geometry for better trigger performance and reduction in #modules
- Combination of micro-strips and macro-pixels

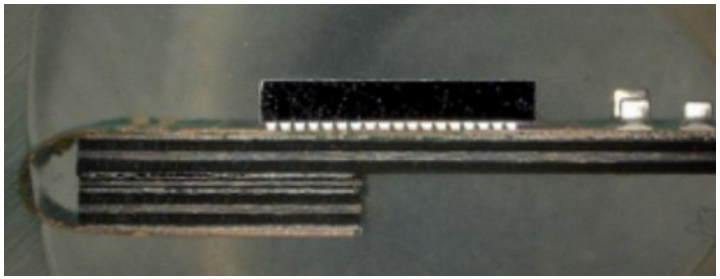
Tracks at L1

- Best exploitation of increased instantaneous luminosity delivered by HL-LHC
  → be more selective already at L1
  → solution: include tracks into L1 decision
- Central concept: pT modules
  - Two silicon sensors with small spacing in a module
  - Flex hybrid concept to get data from both sensors to one ASIC → select track “stubs”
- Different sensor spacing for different parts of the detector
- Acceptance window can be tuned
- Track selection threshold: 2 GeV



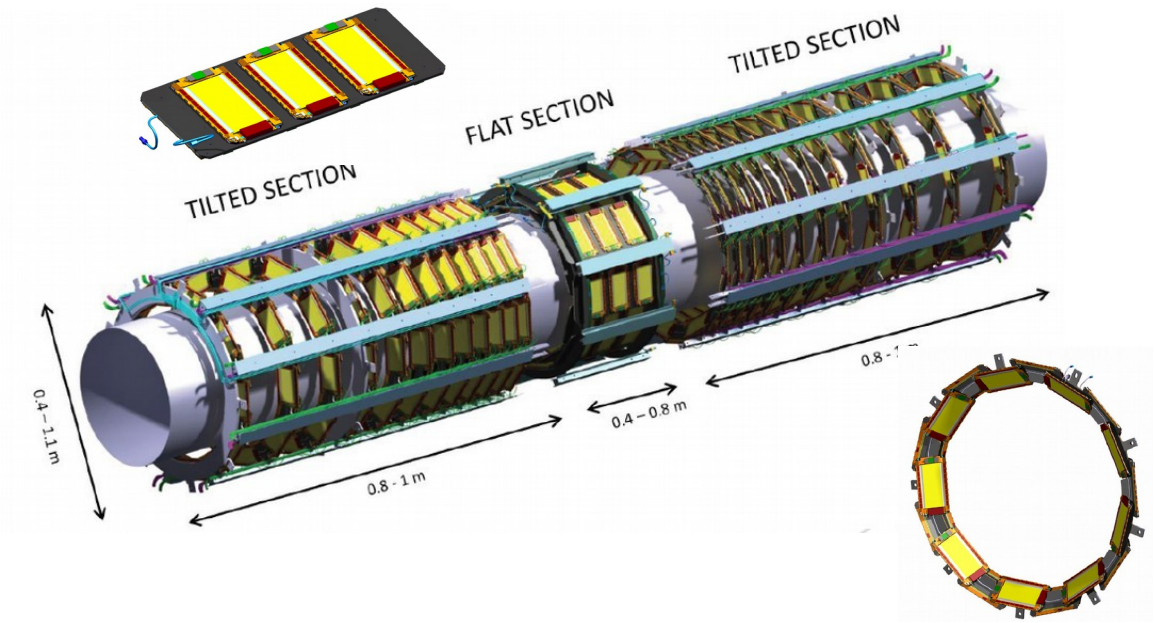






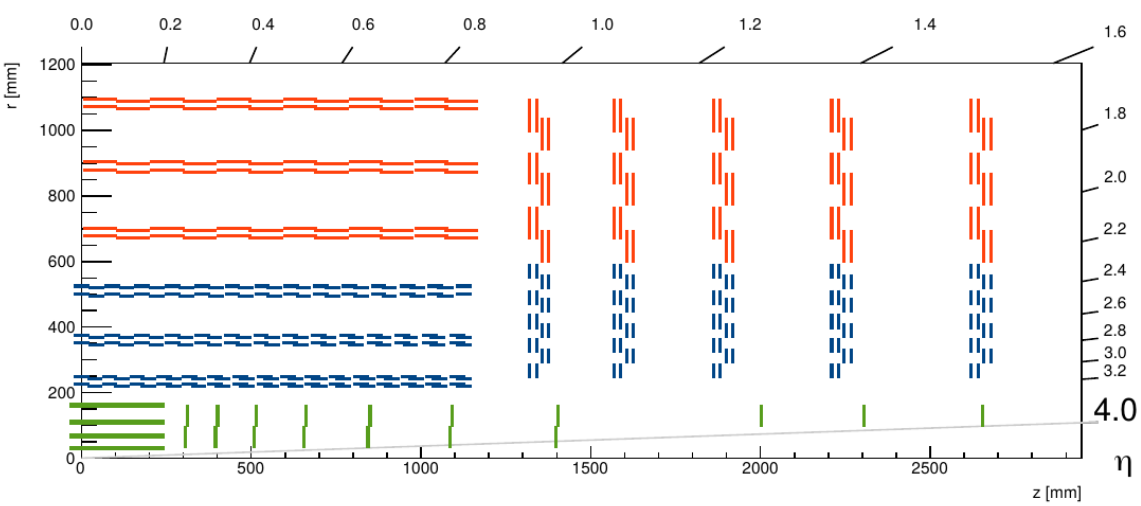
Prototype hybrid

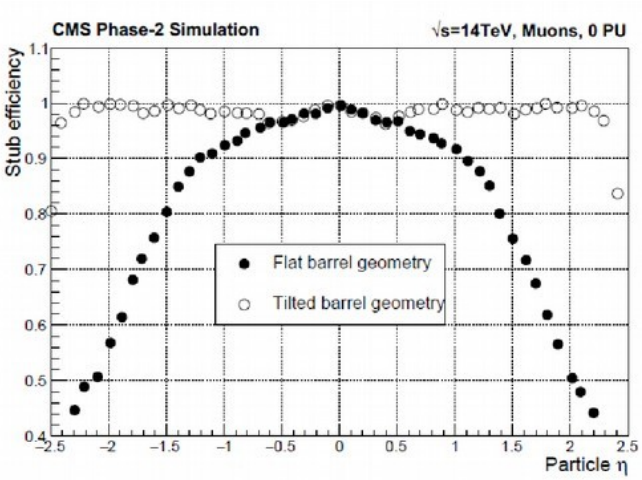
Tilted Barrel Geometry



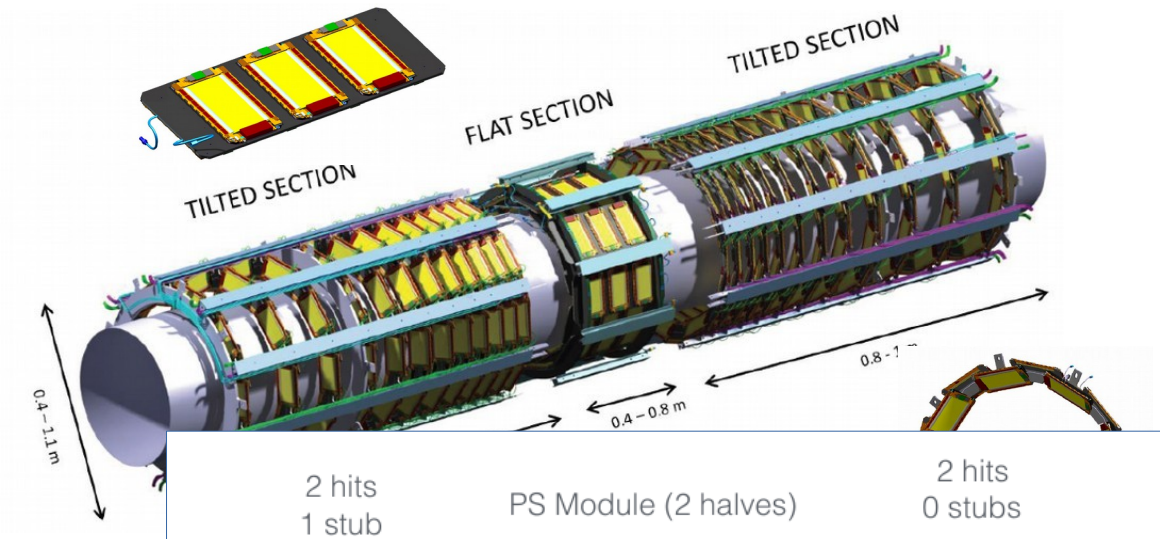
- Track stubs that cross different modules in lower and upper sensor are **lost**
- With tilted geometry ineffiencies are recovered

Geometry from technical proposal



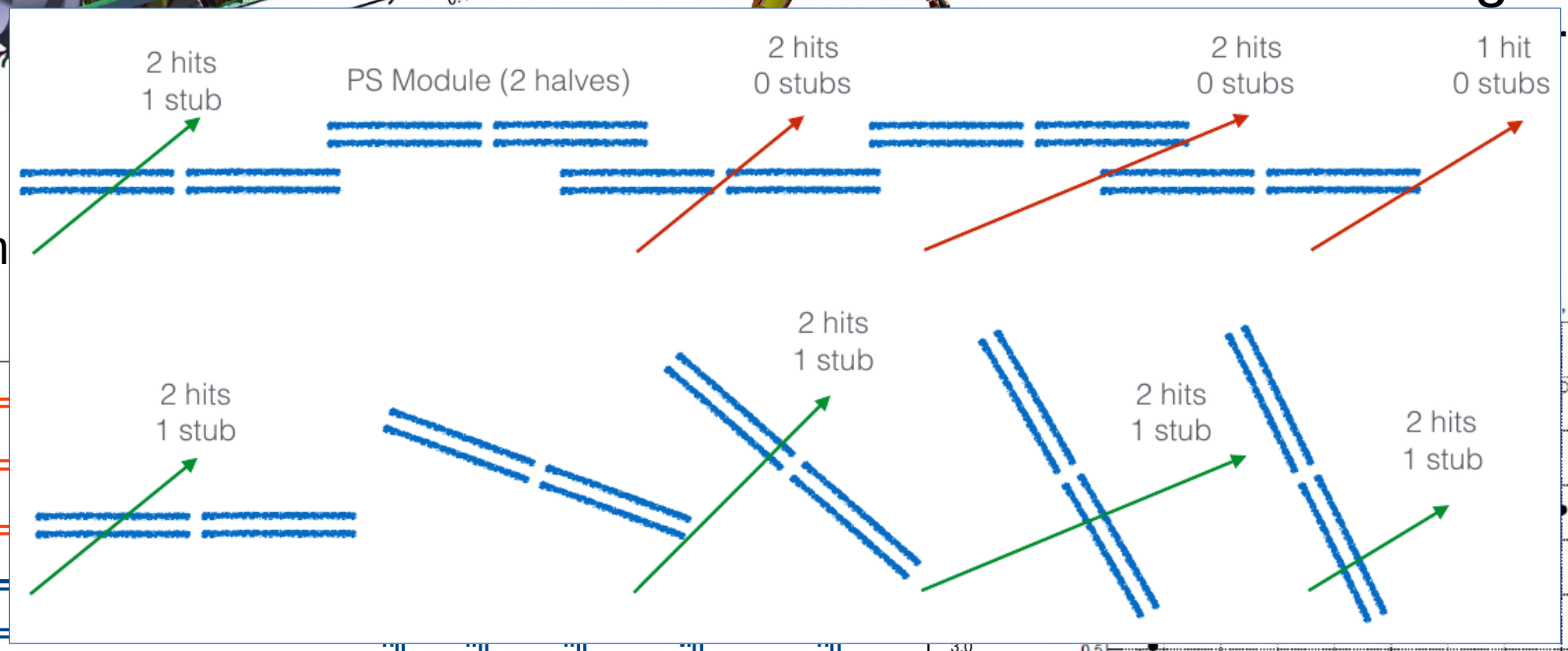


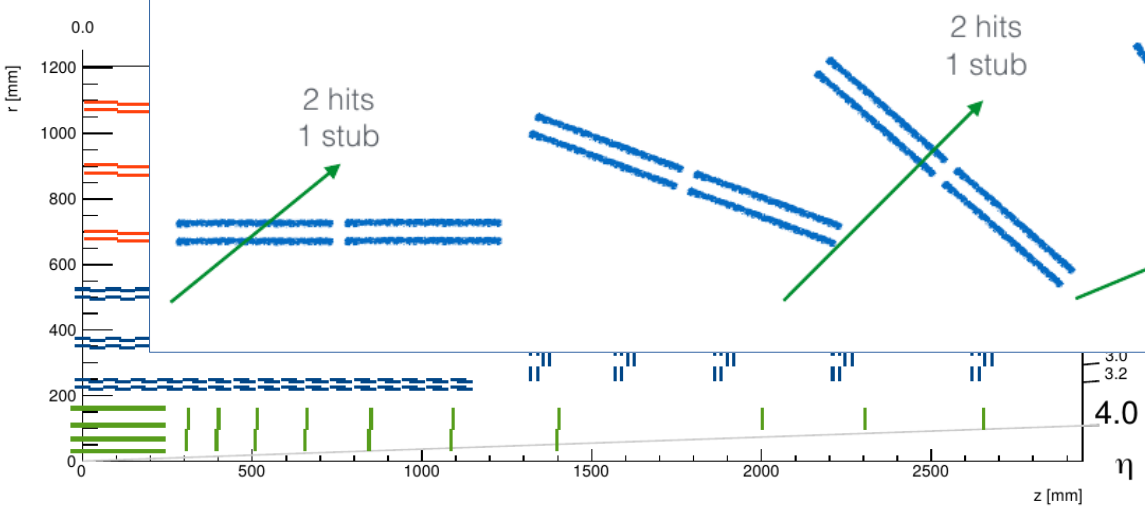
Tilted Barrel Geometry

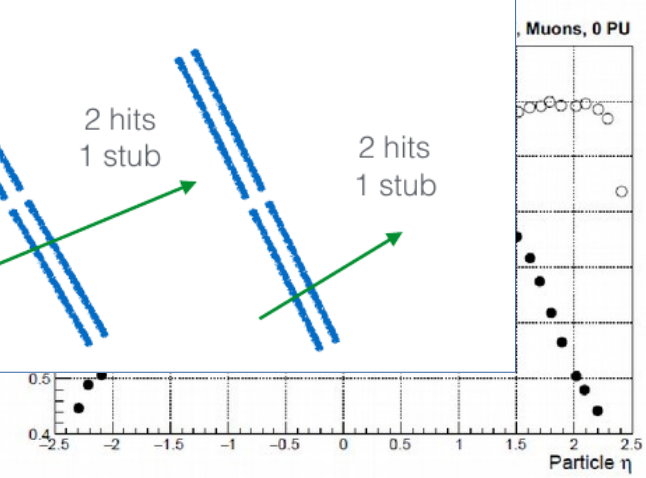


- Track stubs that cross different modules in lower and upper sensor are **lost**
- With tilted geometry

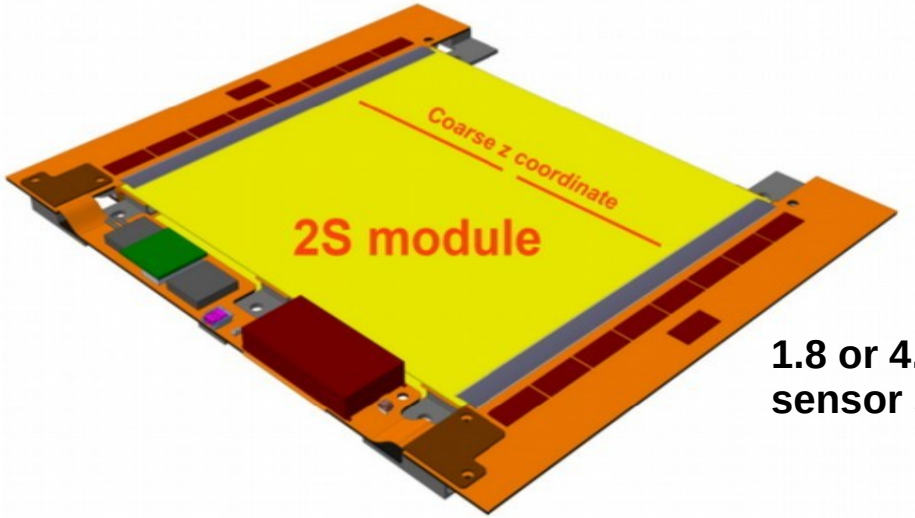
Geom



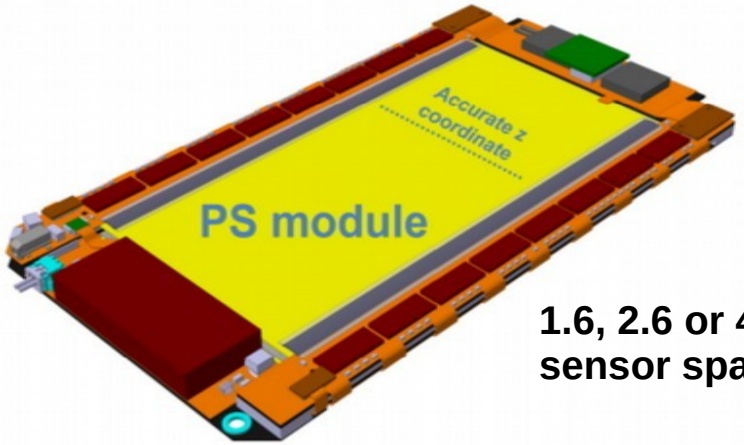




Module types in the CMS Outer Tracker



1.8 or 4.0 mm sensor spacing



1.6, 2.6 or 4.0 mm sensor spacing

- Only two basic type of modules (compare to 15 in phase-0 CMS tracker)
- 2S Modules
  - Two strip sensors with 5 cm x 90 μm strips
  - Sensor is 10x10 cm^2 large → two sets of strips
- PS Modules → Module with one (Macro-)Pixel and one strip sensor
  - Sensor size: 5x10 cm^2
  - Strips: 2.5 cm x 100 μm
  - Macro Pixels: 1.5 mm x 100 μm

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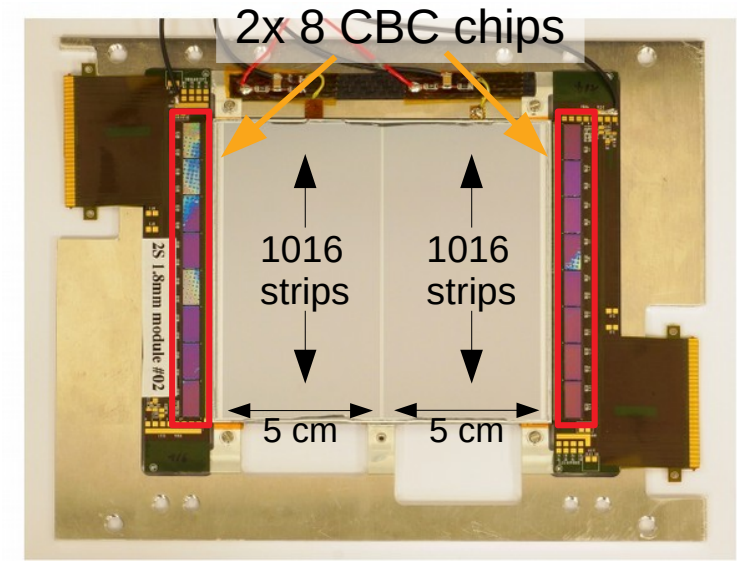

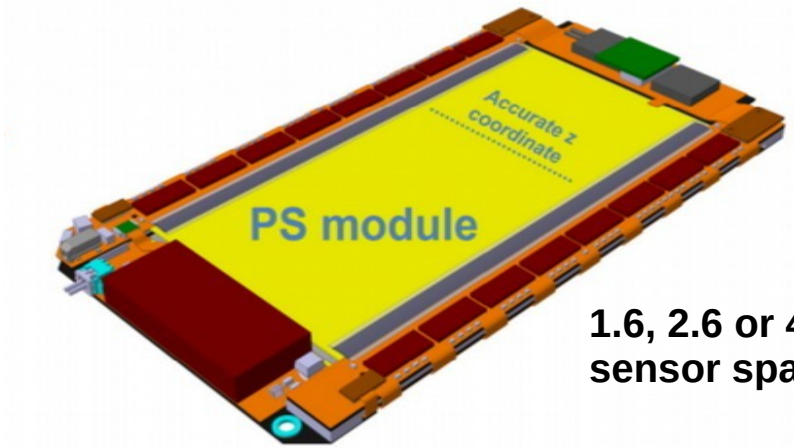

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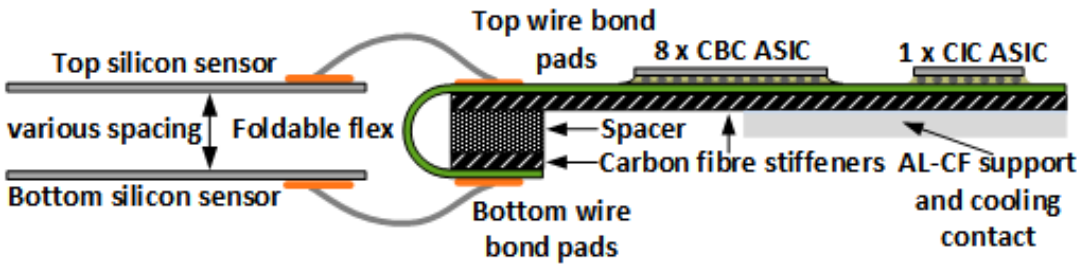
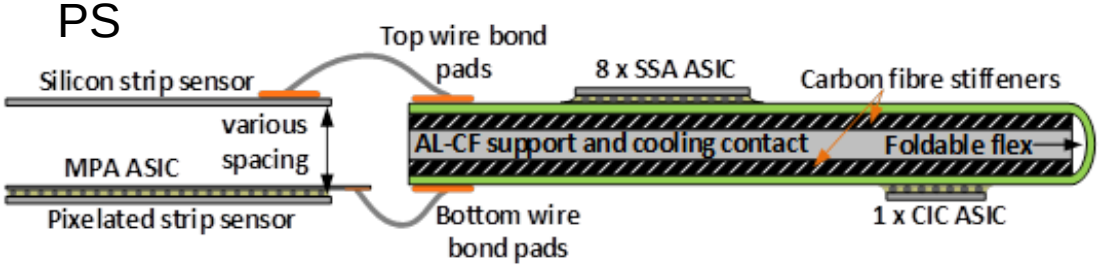
ASICs in the CMS Outer Tracker

- 2S Module ASICs
  - CMS Binary Chip (CBC)
    - Implemented in 130 nm technology
    - readout and stub finding for L1
      → both sensors read out by same chip
  - 254 channels per chip
    → 127 from each sensor (lower/upper)
- PS Module ASICS
  - Macro-Pixel ASIC(MPA) and
    Short-strip ASIC (SSA) for readout of sensors
  - Both chips done in 65 nm technology
  - Stub finding performed by MPA
    → SSA sends cluster and L1 information
    to MPA to enable match in space and time
- Common ASIC:
  - CIC concentrator chip
  - Receives L1 information and readout data
  - “Data hub” to service hybrid
  - Done in 65 nm technology

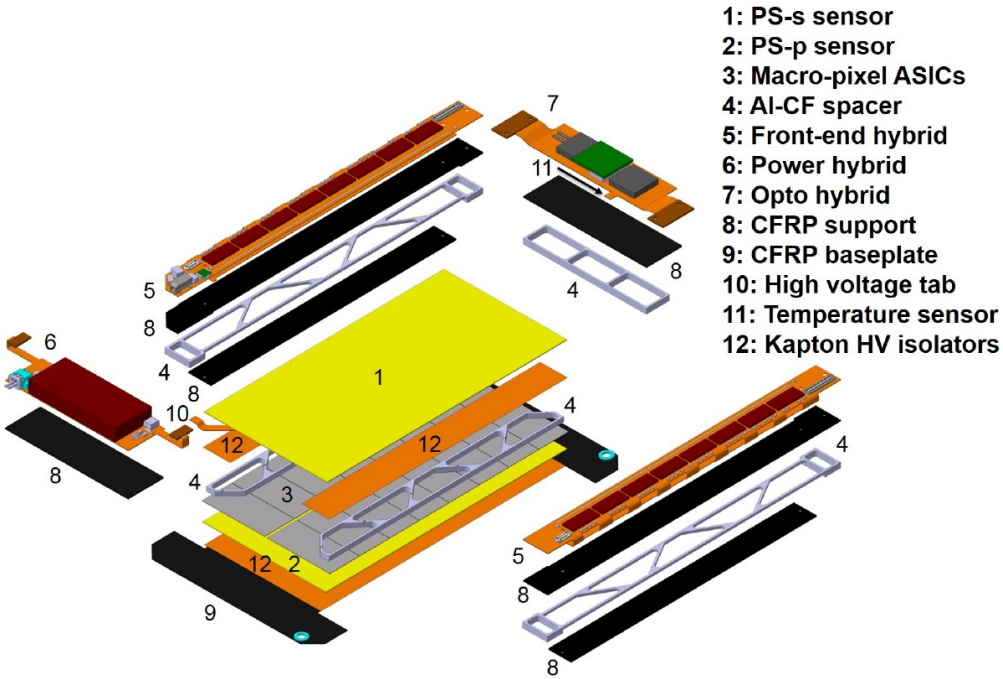
2S

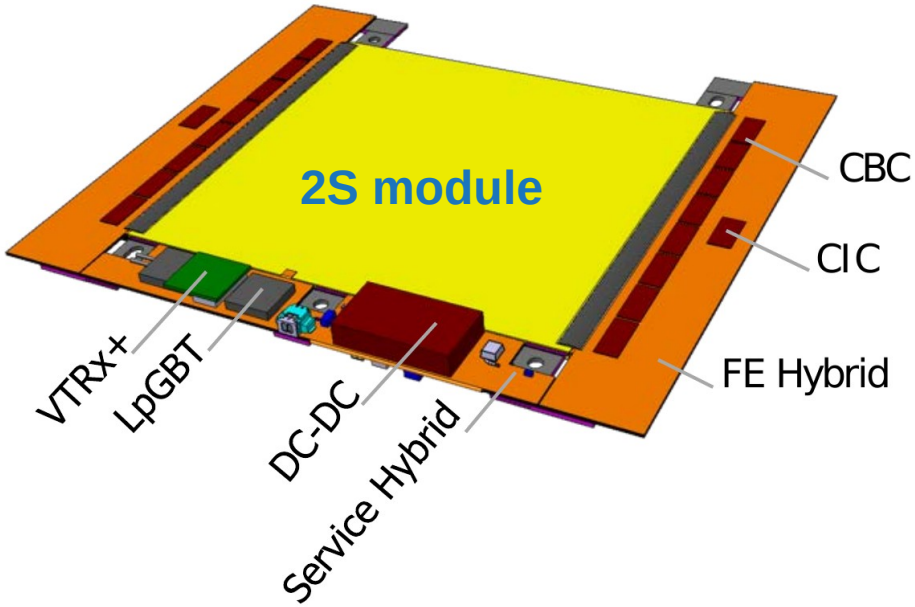


PS



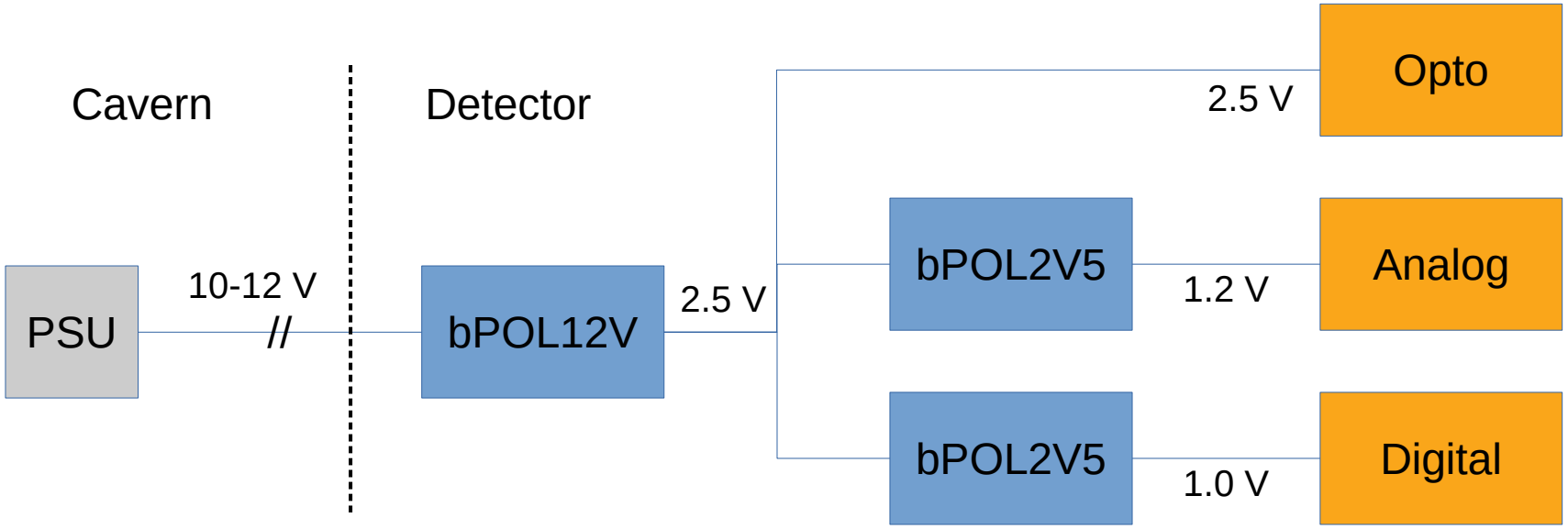
Service electronics on the silicon modules





- Each module has frontend- and service hybrid(s)
- Frontend hybrid houses readout (CBC,SSA,MPA), and concentrator (CiC) chip
- Service hybrid(s) houses:
  - lpGBT (low-power Gigabit Transceiver, common development for HL-LHC experiments)
  - VTRx+ (Versatile TRansceiver plus, common development for HL-LHC experiments)
  - DCDC converters (common development for HL-LHC experiments)
- **Module is the system** → no further card/aggregator between it and backend

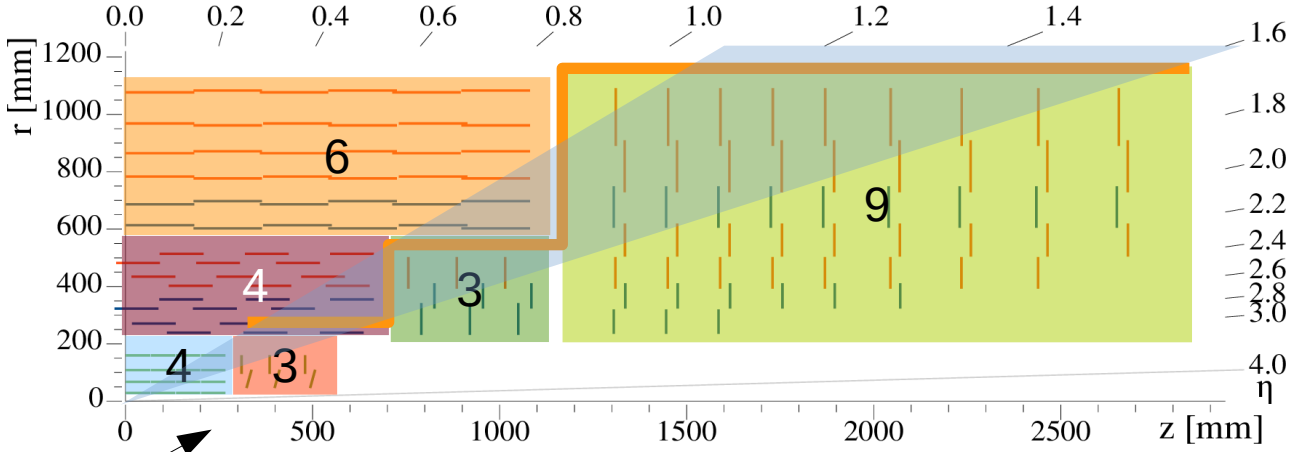
Powering Scheme

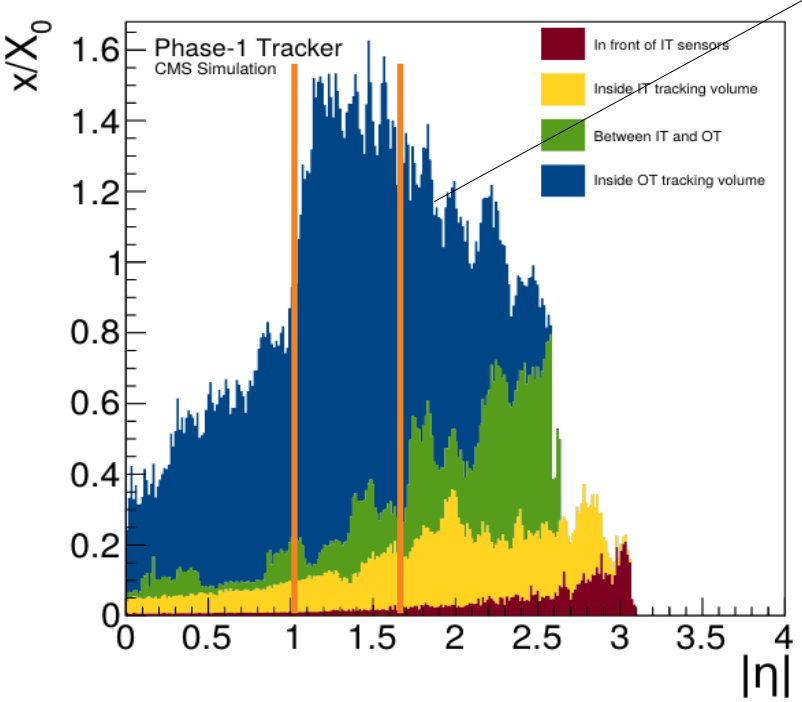


Schematic representation, more details in backup

- Multi-stage DCDC conversion
  - Same amount of space available in service channels for cables → more power through ~same cable x-section
  - Aim to reduce losses on the cables as much as possible (reminder: today 1.25/2.5 V directly from PSU to modules!)
  - Supply voltage from PSU 10-12 V
  - First stage DCDC converter 10-12 V → 2.5 V
  - Second stage DCDC converters 2.5 V → 1.2 V, 2.5 V → 1.0 V

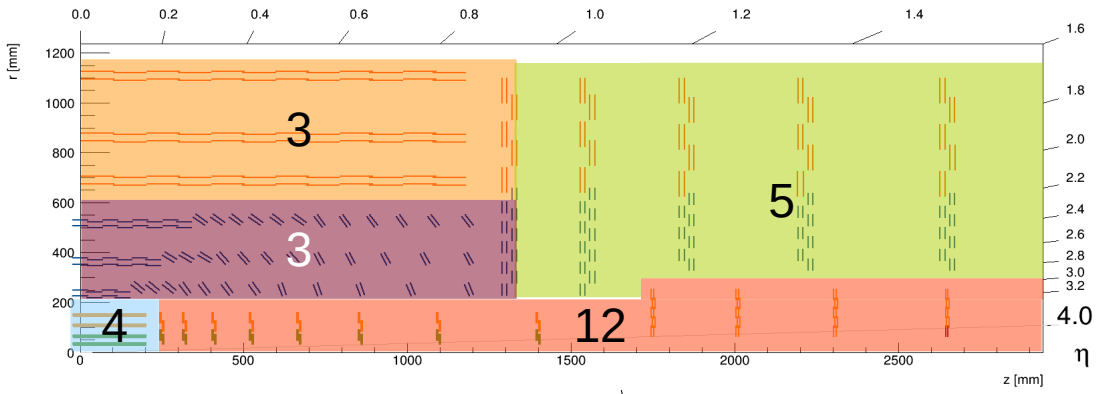
Material Budget

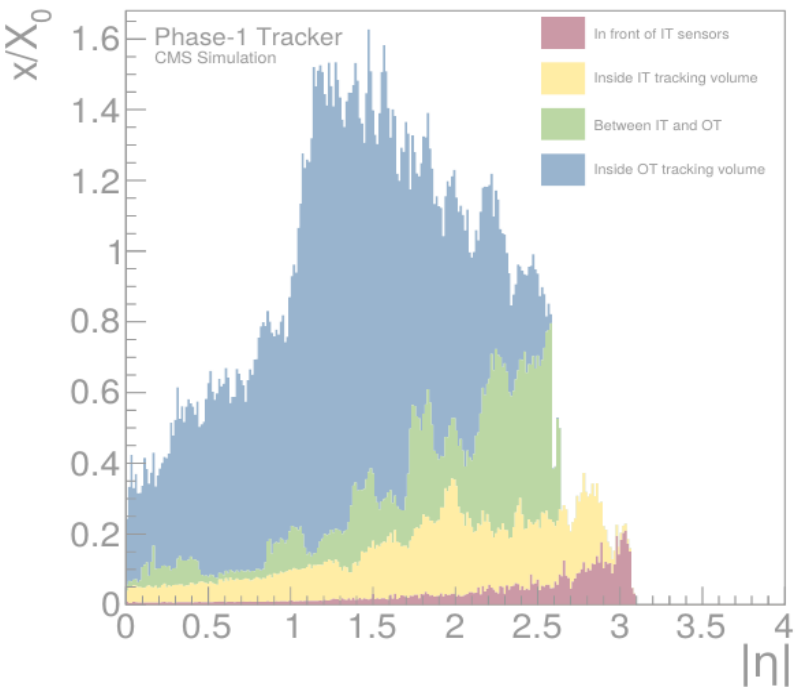


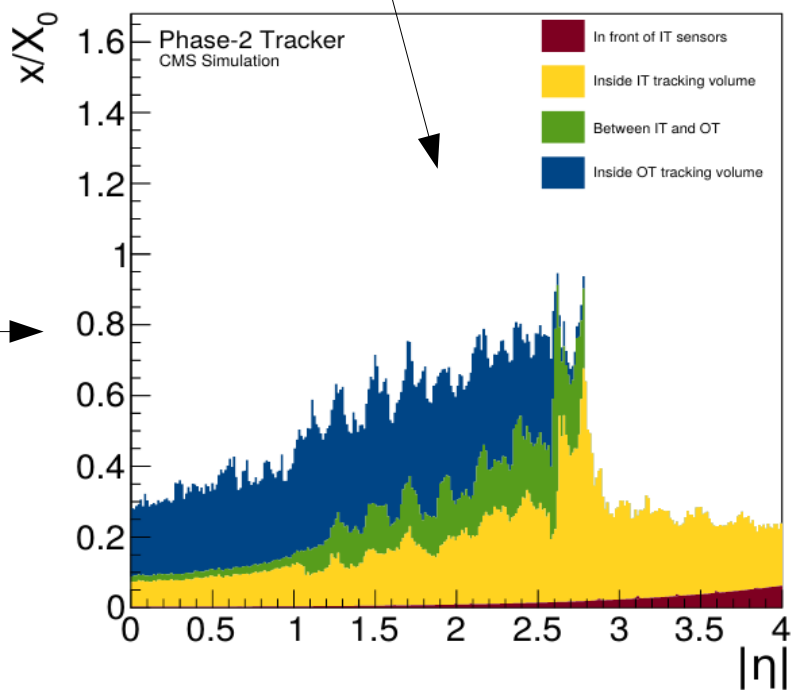


Material Budget

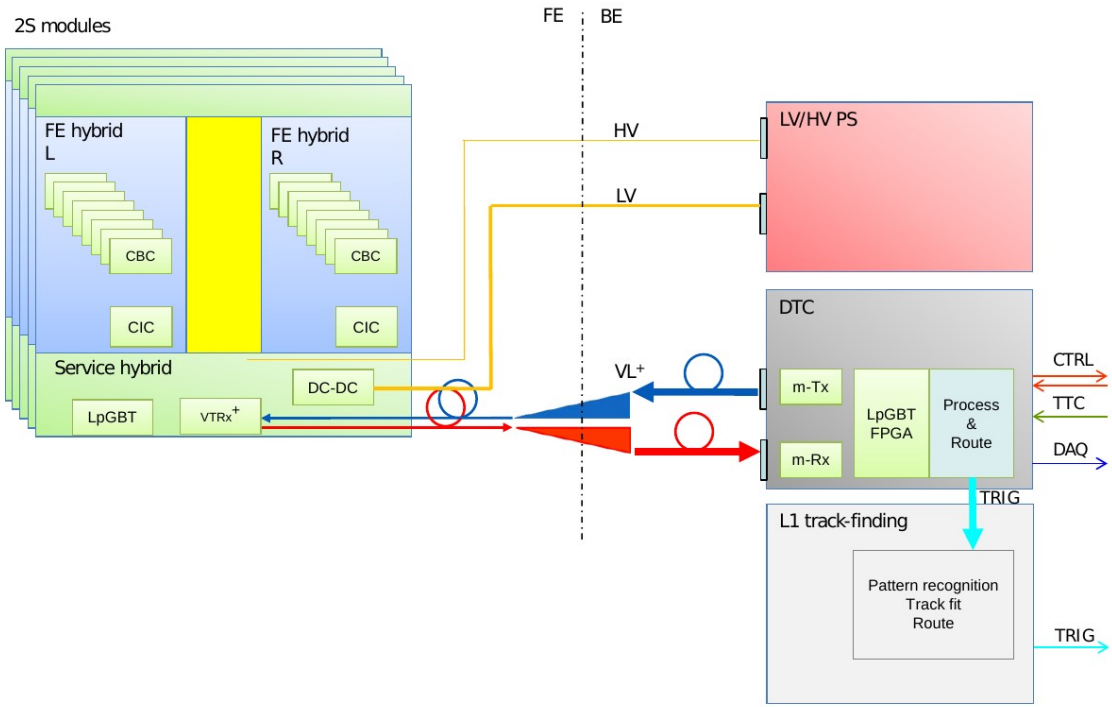
- Despite increased number of channels, material budget much reduced compared to phase-0/1 detector
- Main ingredients
  - DCDC converters
  - Fewer layers
  - Lighter materials
  - Optimized service routing
  - CO2 cooling
  - Inclined geometry







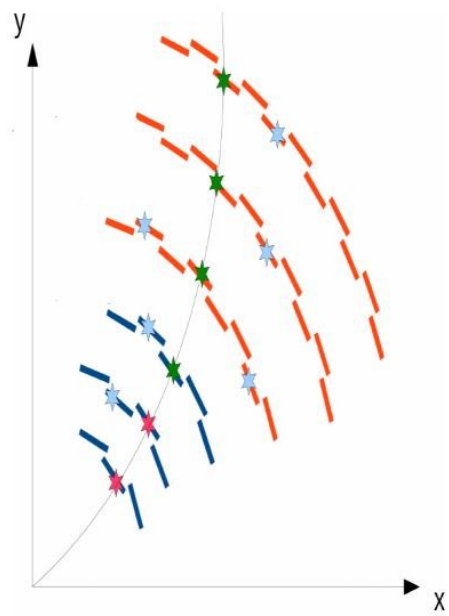
Backend

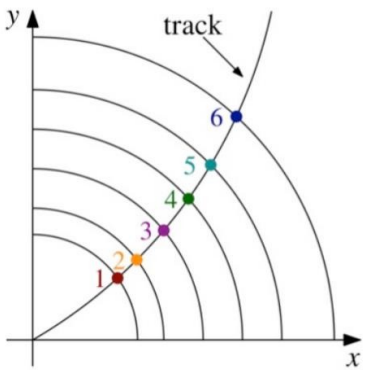


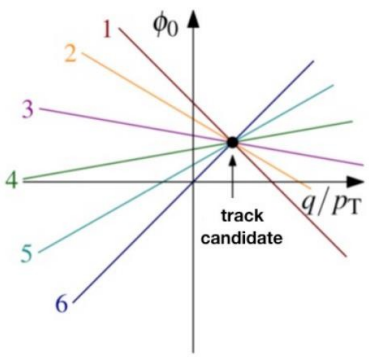
- DTC (= Data, Trigger and Control) boards readout and control modules
  - Based on ACTA standard
- Bi-directional optical links
  - **2.56 Gb/s DTC → Module**
    - clock, trigger, fast-commands and programming
  - **5.12 or 10.24 Gb/s Module → DTC** (depending occupancy/position in the detector)
    - L1 data (stubs) and DAQ data (detector payload)
- L1 data is relayed to track finder modules at 40 MHz
- DAQ data (after L1 decision) read out at 750 kHz

L1 track finding

- Track finding in back-end will be based on FPGAs
  - L1 tracks will need to be found in ~5 μs
- Two stages:
  - Pattern recognition
  - Track fitting
- Approaches for pattern recognition:
  - Form tracklets from stubs in adjacent layers
  - Find track candidates through Hough-transform approach
- Approaches for track fitting
  - Kalman filter
  - $\chi 2$ minimization
- Last step: duplicate removal



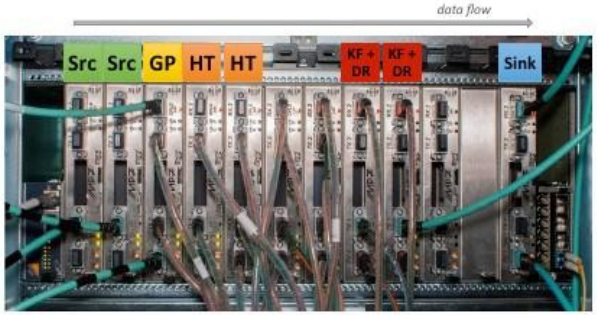


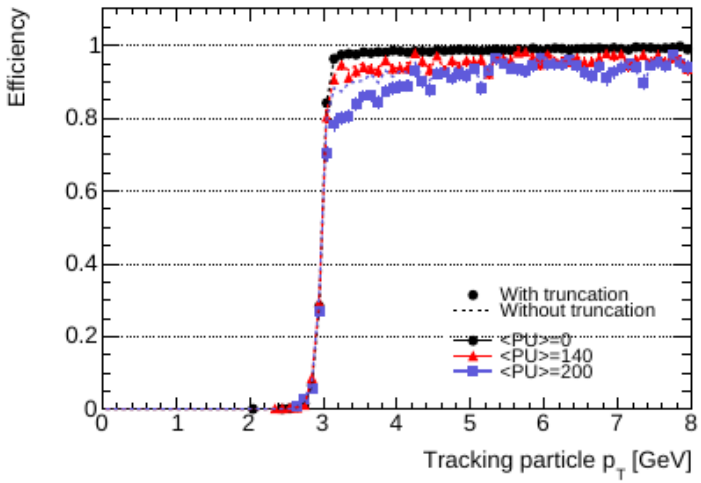


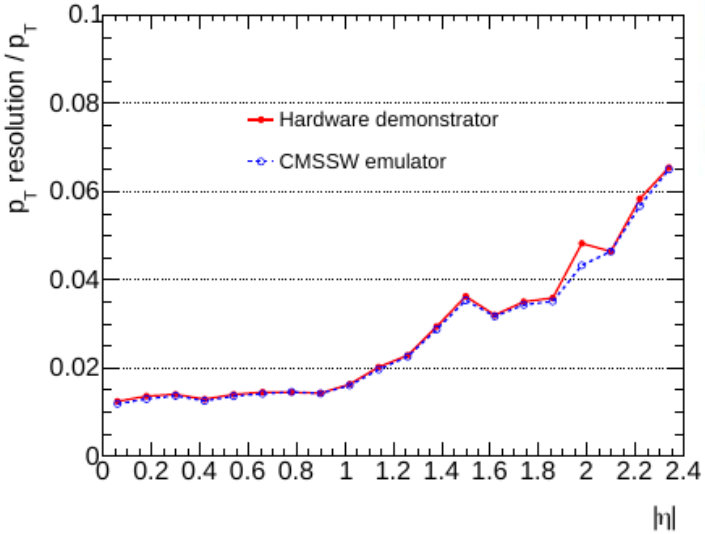
Poster: Level-1 track finding with an all-FPGA system at CMS for the HL-LHC, Kristian Hahn

L1 track finding – studies and prototypes

- Hardware demonstrators have been set up for both approaches
- Simulated events as inputs
- Both approaches produce compatible results
- Timing constraints met
  - Time to produce tracks < ~ 5 μs
  - CMS trigger latency in phase-2: 12.5 μs

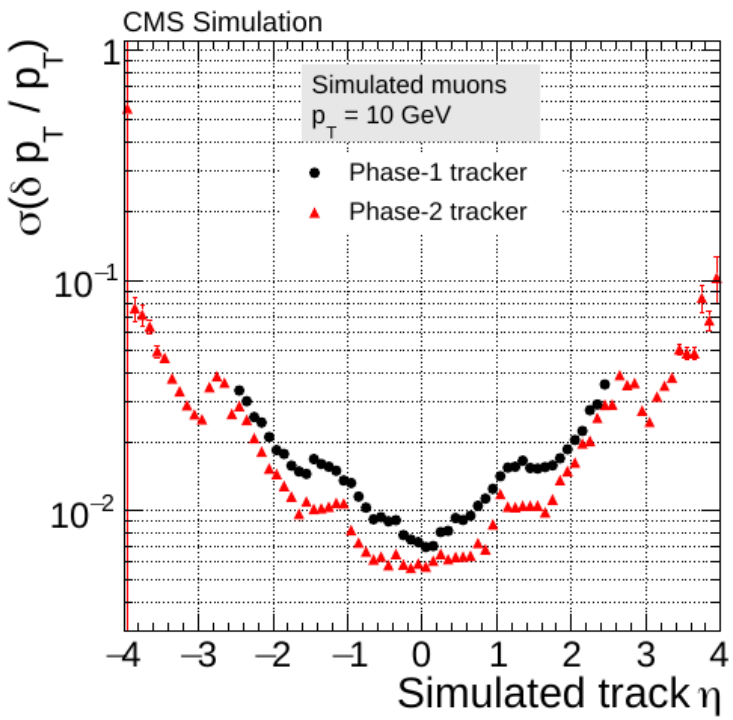


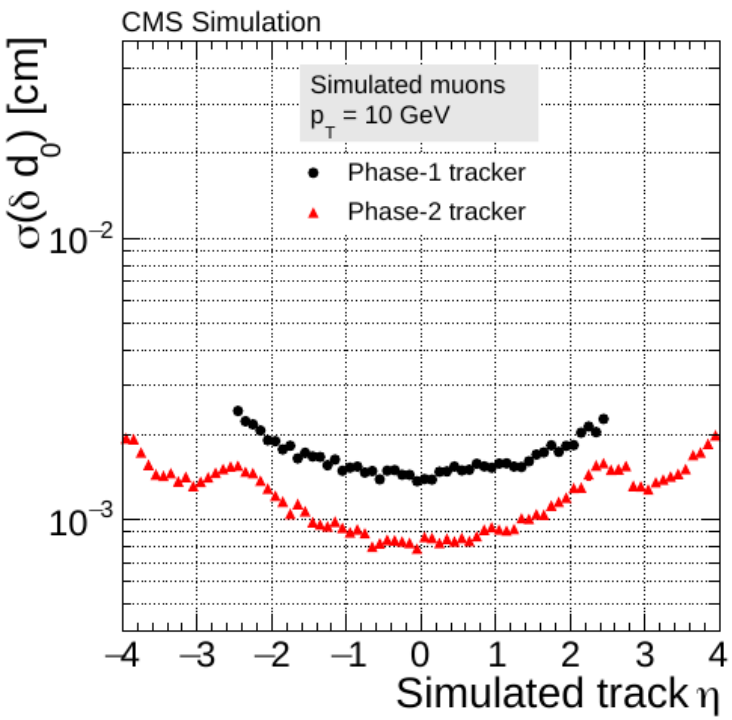




Performance – Track Parameter Reconstruction

- Track parameter resolution of phase-2 tracker comparable or better than for phase-0/1 tracker
  → smaller cell size
  → less material

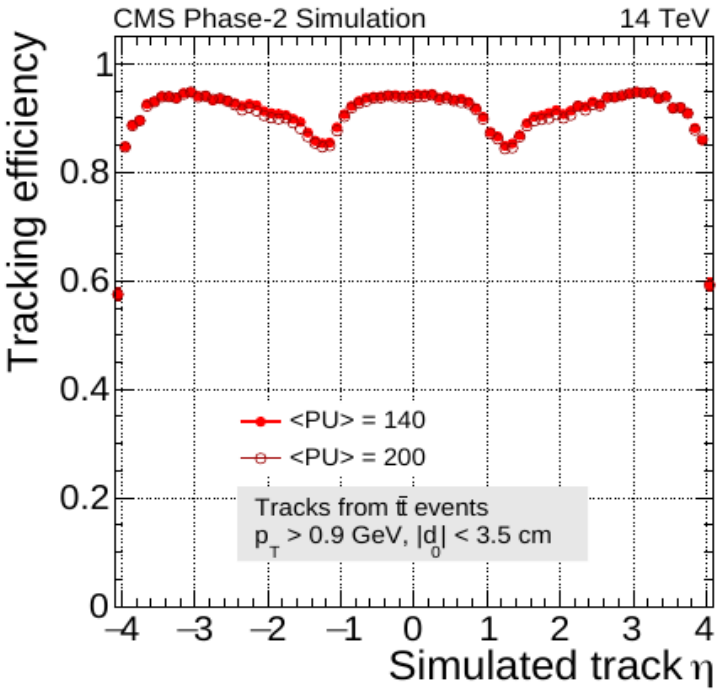


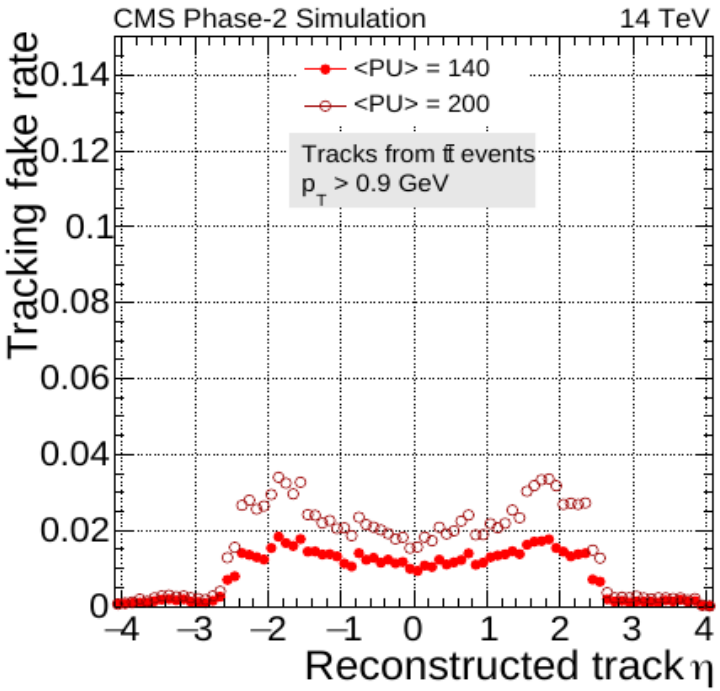


Performance – Tracking in the presence of pile-up

- High tracking efficiency also in presence of 140 or even 200 pile-up events
  → around 90% efficiency for tracks with pT > 0.9 GeV with < ~2% fake rate

N.B. underlying geometry from TDR
→ dip around || ~ 1.2 being addressed in geometry optimization

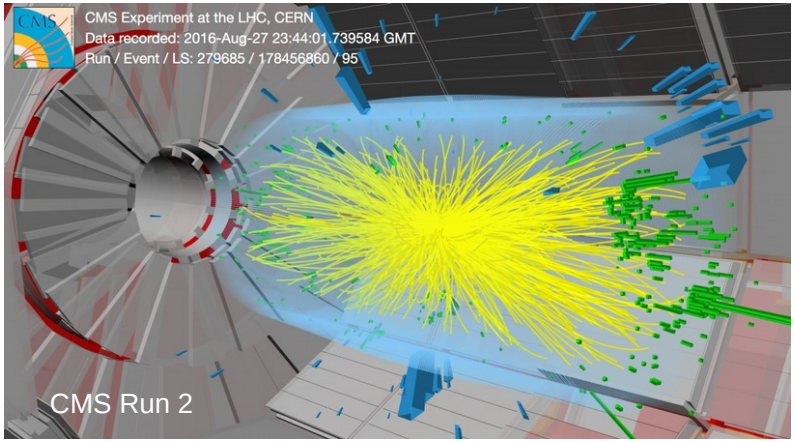




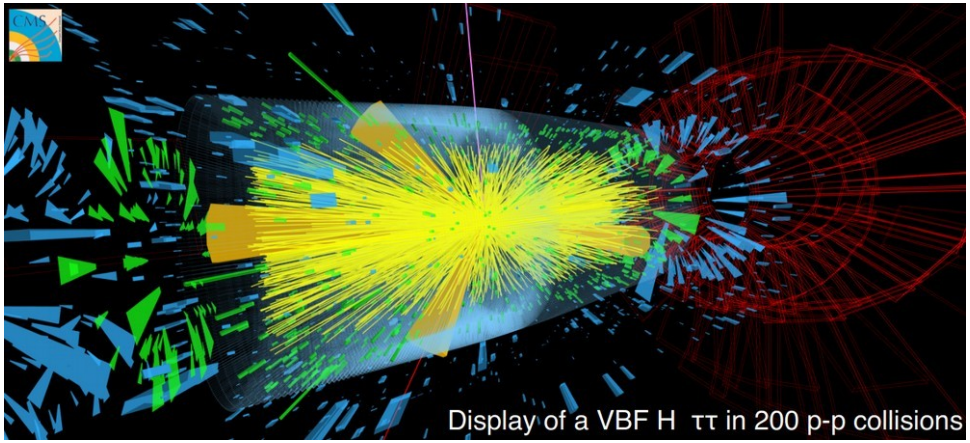
Summary and Outlook

- Ambitious upgrade project underway for the CMS Outer Tracker for the HL-LHC running
- Designed to maintained or improve tracking performance compared to current system even in the presence of up to 200 pile-up events
- Deliver tracks above 2 GeV as L1 primitives at 40 MHz
- Several improvements result in the tracker being more performant and yet more light-weight compared to its predecessor

To reconstruct not just this….



….but also this

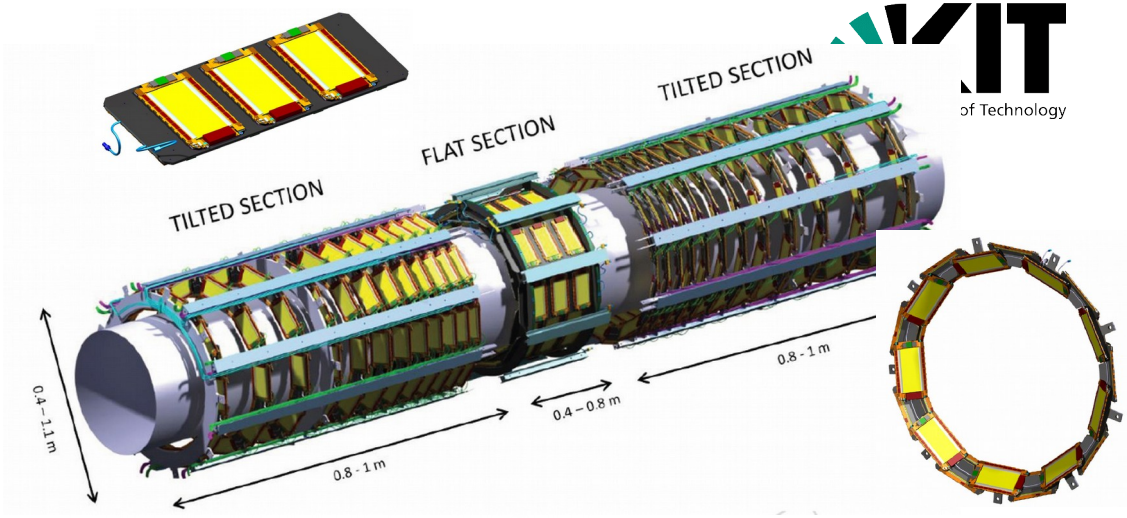


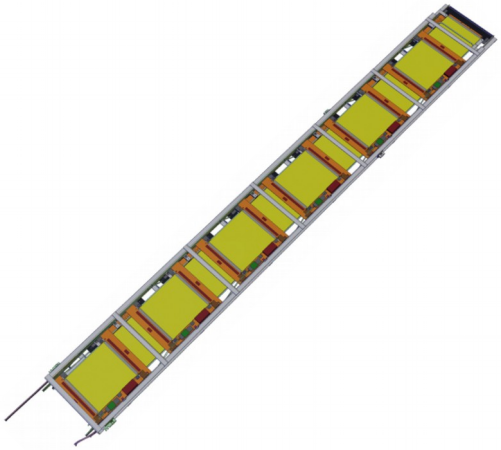
BACKUP

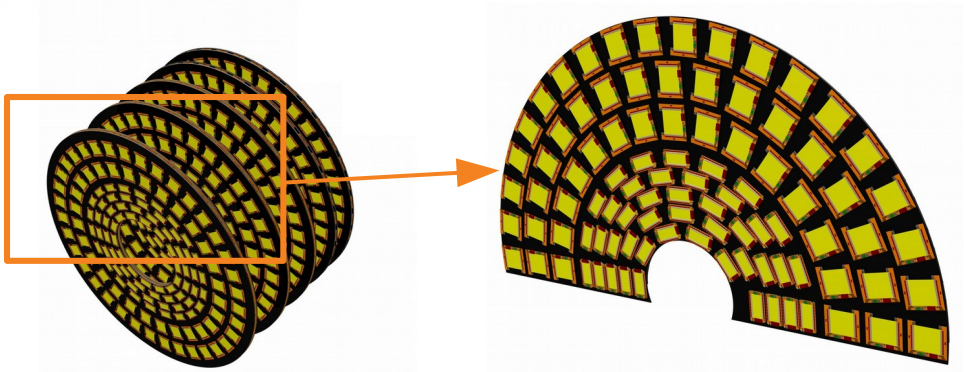
Mechanics

- TBPS: (inner barrel part)
  - Flat part: planks
  - Tilted part: rings
  - Detailed studies ongoing for optimal service routing
- TB2S: (outer barrel part)
  - “Ladder” support structures

    → support structure to insert them similar to current strip tracker outer barrel
- TEDD (endcap)
  - Building blocks: DEE (half disk)
  - Final disks are Double-Disks to be hermetic also with rectangular module geometry

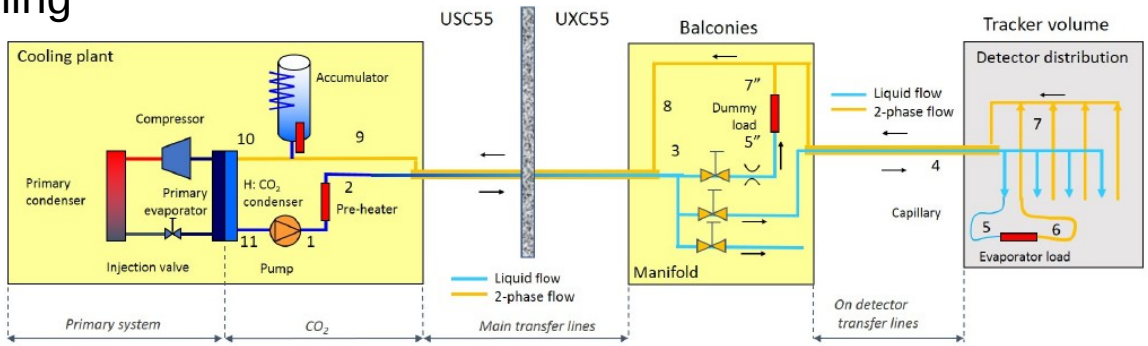






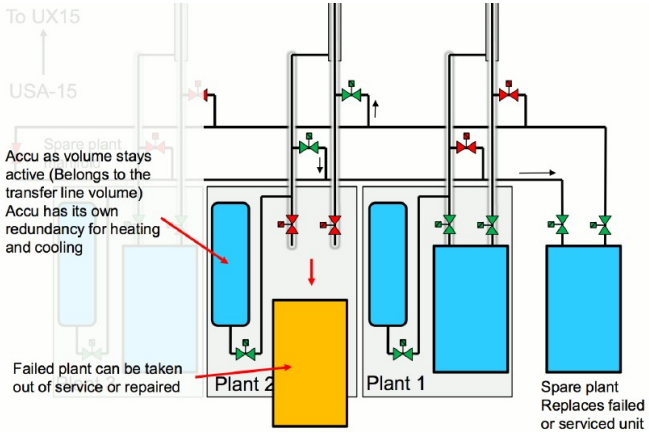
Cooling

- Total power of the CMS Phase-2 outer tracker: 100 kW
- CMS Outer Tracker will use CO2 cooling
  - Low mass pipe work
  - Lighter liquid
  - High heat transfer
  - Environmentally friendly
- Already successfully used in LHCb, ATLAS IBL, CMS Phase-1 Pixel

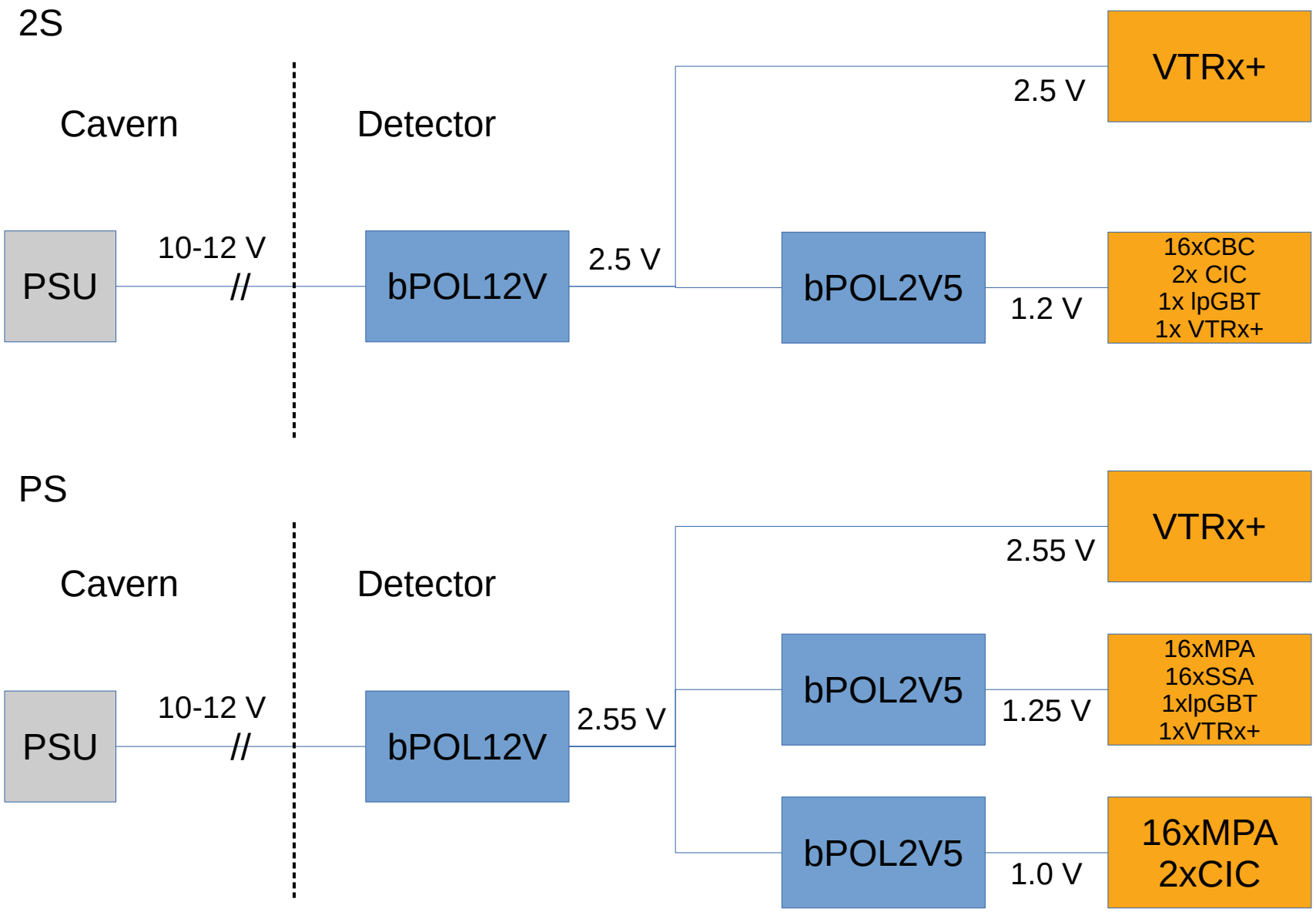


Schematics of CO2 cooling (here from CMS Phase 1 pixel)

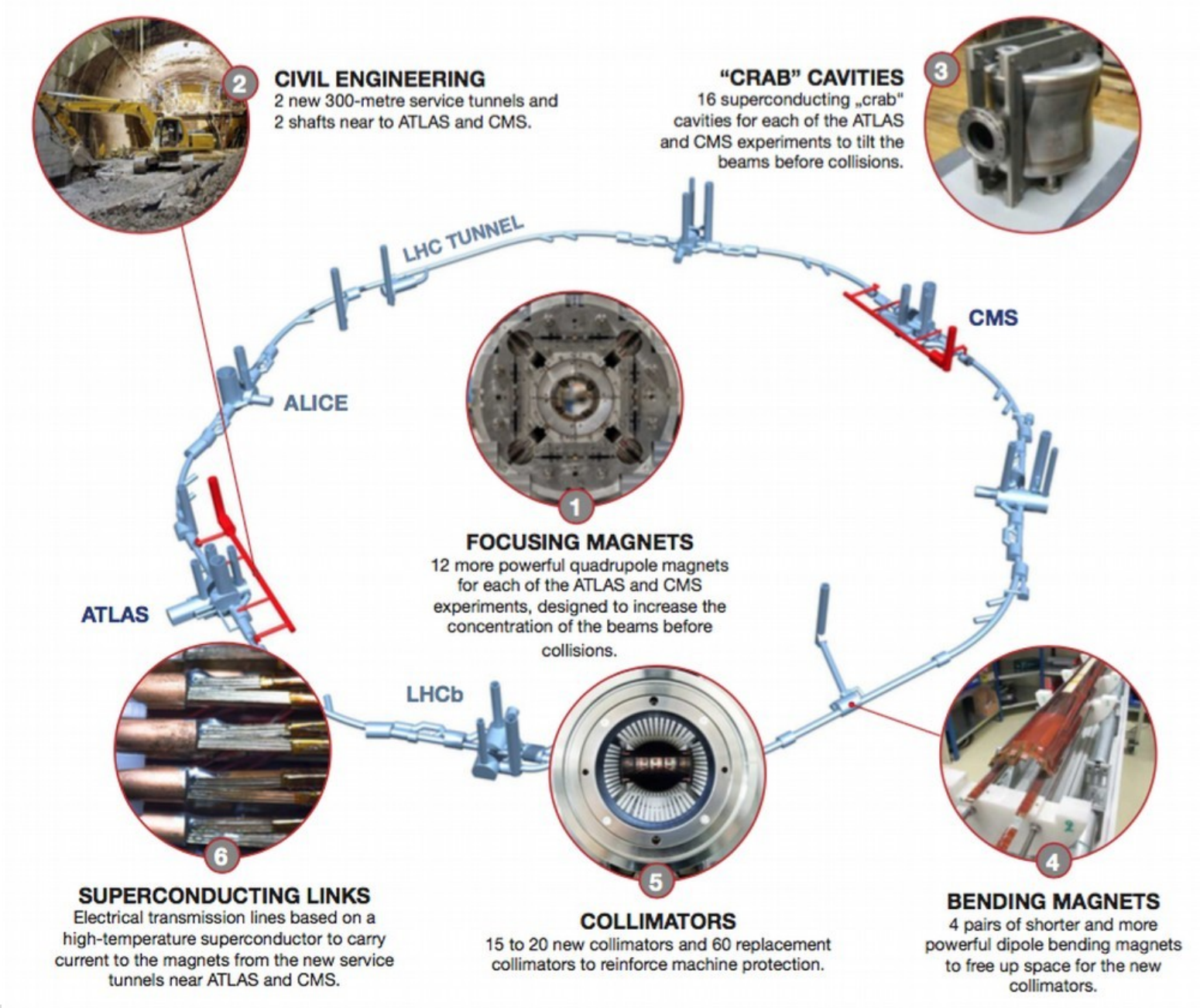
- Downside
  - High operating pressure BUT
  - Stored energy (pressure X volume) comparable to other refrigerants
- Several identical cooling units in service cavern
  - Redundancy (allow single cooling plants to be under maintenance or repair)
- Distribution
  - Transfer lines to experimental cavern
  - First manifolds in accessible locations on Experimental Cavern balconies
  - Further splitting to capillaries inside detector volume



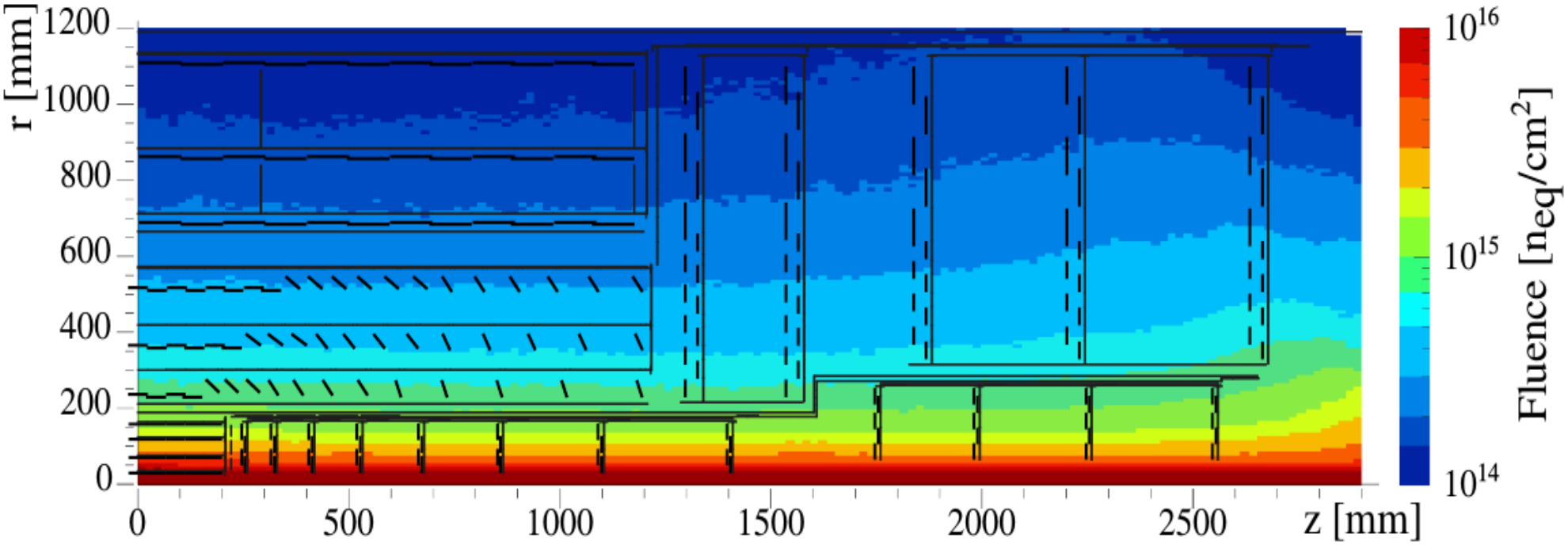
Powering Scheme



High Luminosity LHC



Integrated Particle Fluence



3000 fb^{-1} at 14 TeV