

# Module and System Test Development for the Phase-2 ATLAS ITk Pixel Upgrade

*Vienna Conference on Instrumentation*

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Vienna

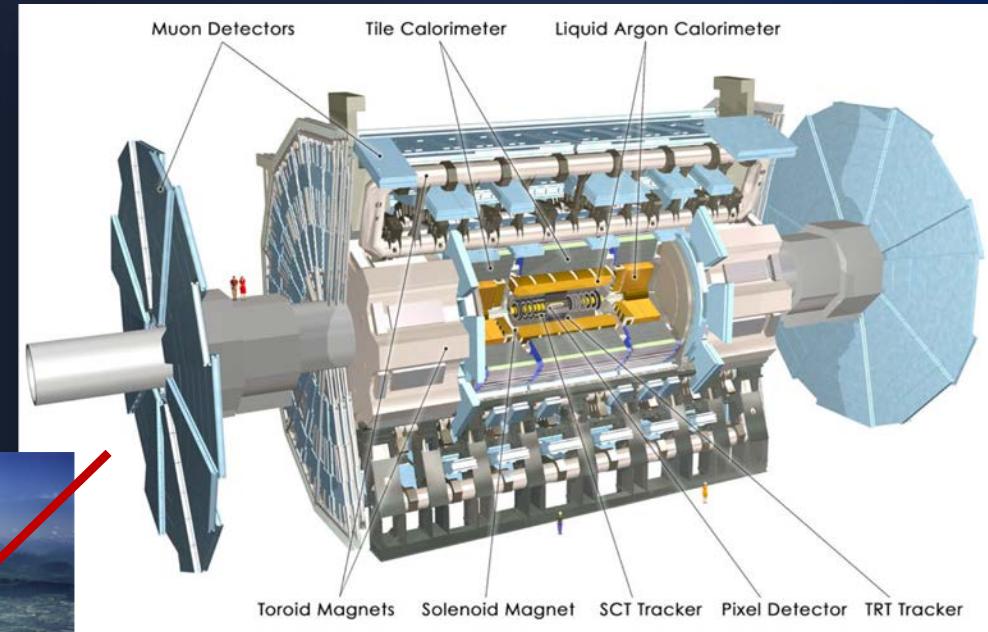
**Tobias Flick**

University of Wuppertal

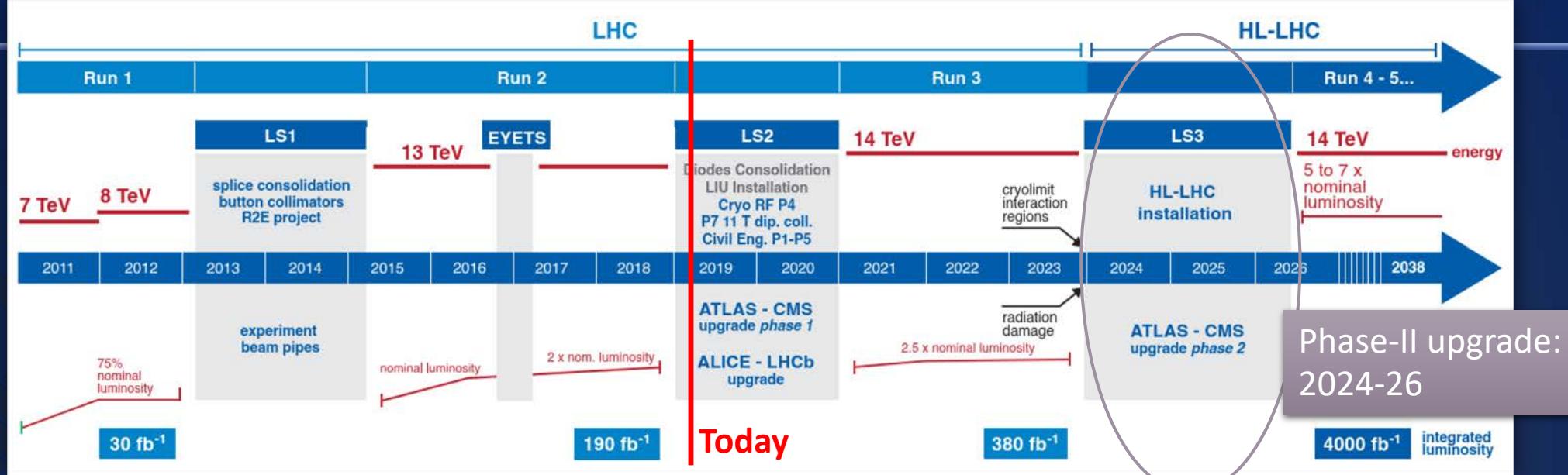


# Overview

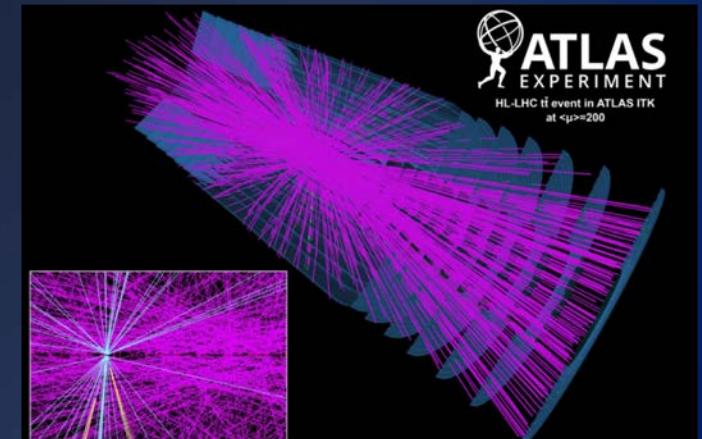
- LHC upgrade plans: ATLAS Inner Tracker (ITk) upgrade
- ATLAS ITk Pixel FE-ASIC, module, powering and readout
- Results from demonstrator setups
- Conclusion and outlook



# LHC Upgrade Plan: From LHC to HL-LHC

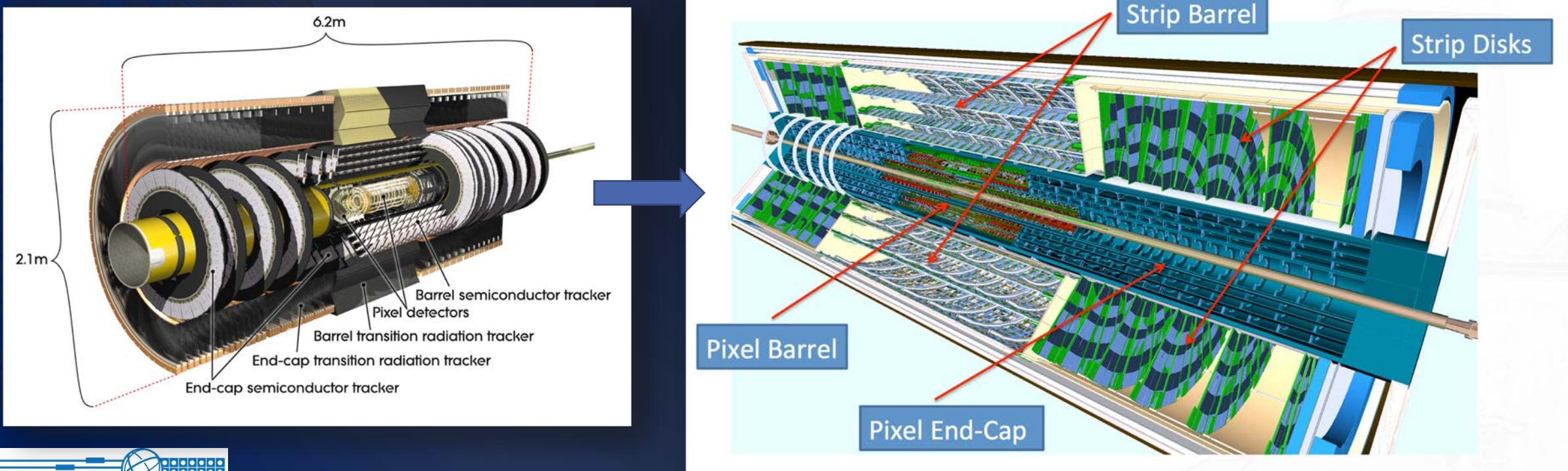


- Proton-proton collisions at 14 TeV with increased luminosity  
→ *Higher particle density and radiation damage*
- Need of an upgraded tracking detector:
  - finer granularity
  - higher readout capabilities
  - better radiation hardness



# ATLAS Phase-II Upgrade

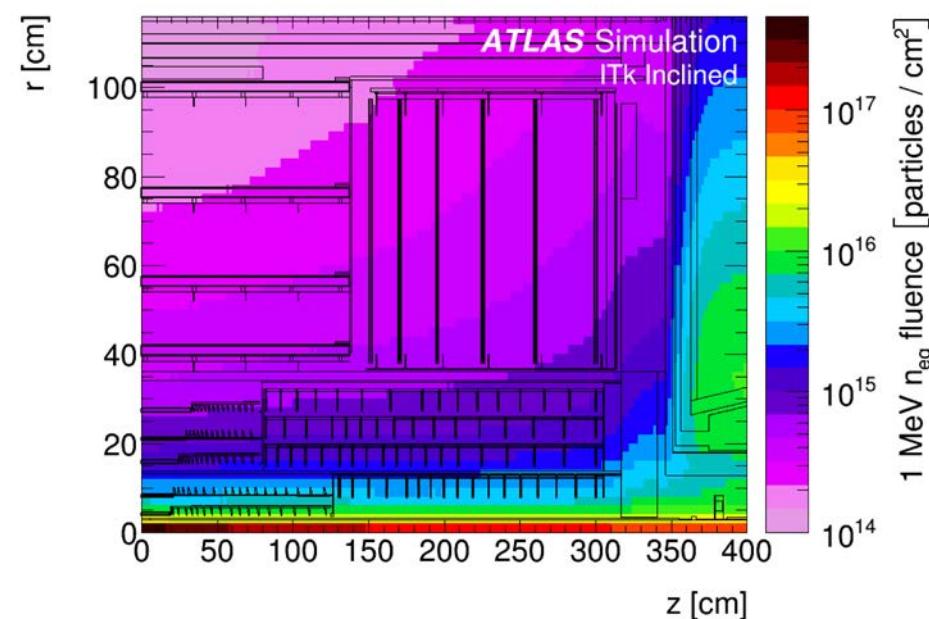
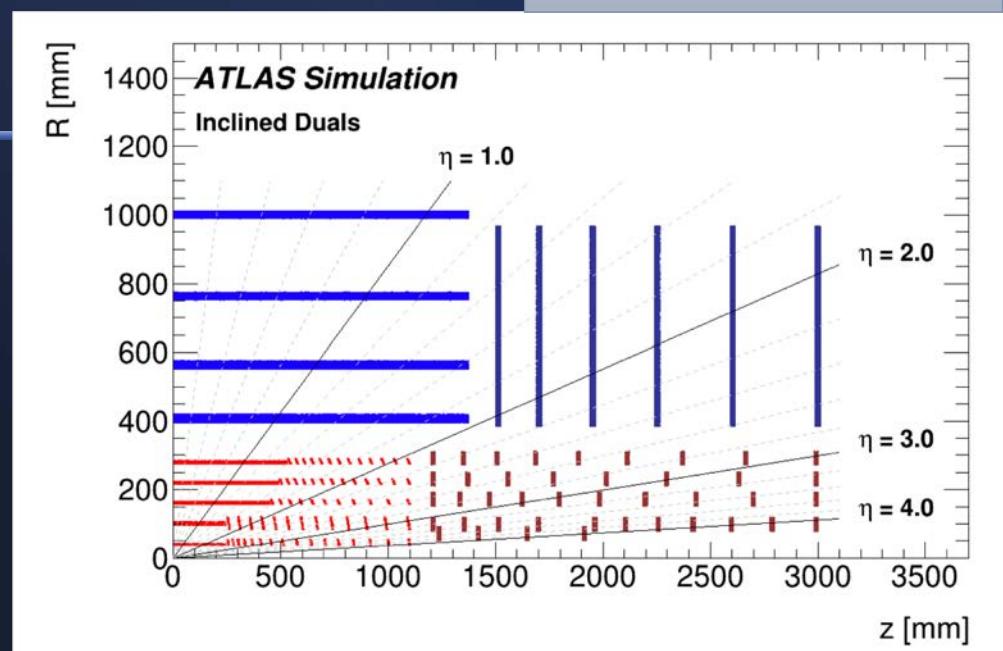
- Replacement of the inner tracking detector with the ITk (inner tracker) to cope with:
  - Increased average pile-up of ~200 proton-proton interactions per bunch crossing. (*factor* ~7-8)
  - Instantaneous luminosity:  $7.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$  (*factor* ~5-7)
  - Particle fluences of  $2 \times 10^{16} \text{ n}_{\text{eq}}/\text{cm}^2$  (*factor* ~10)
- 4000  $\text{fb}^{-1}$  integrated luminosity to be recorded



# New All Silicon Tracker

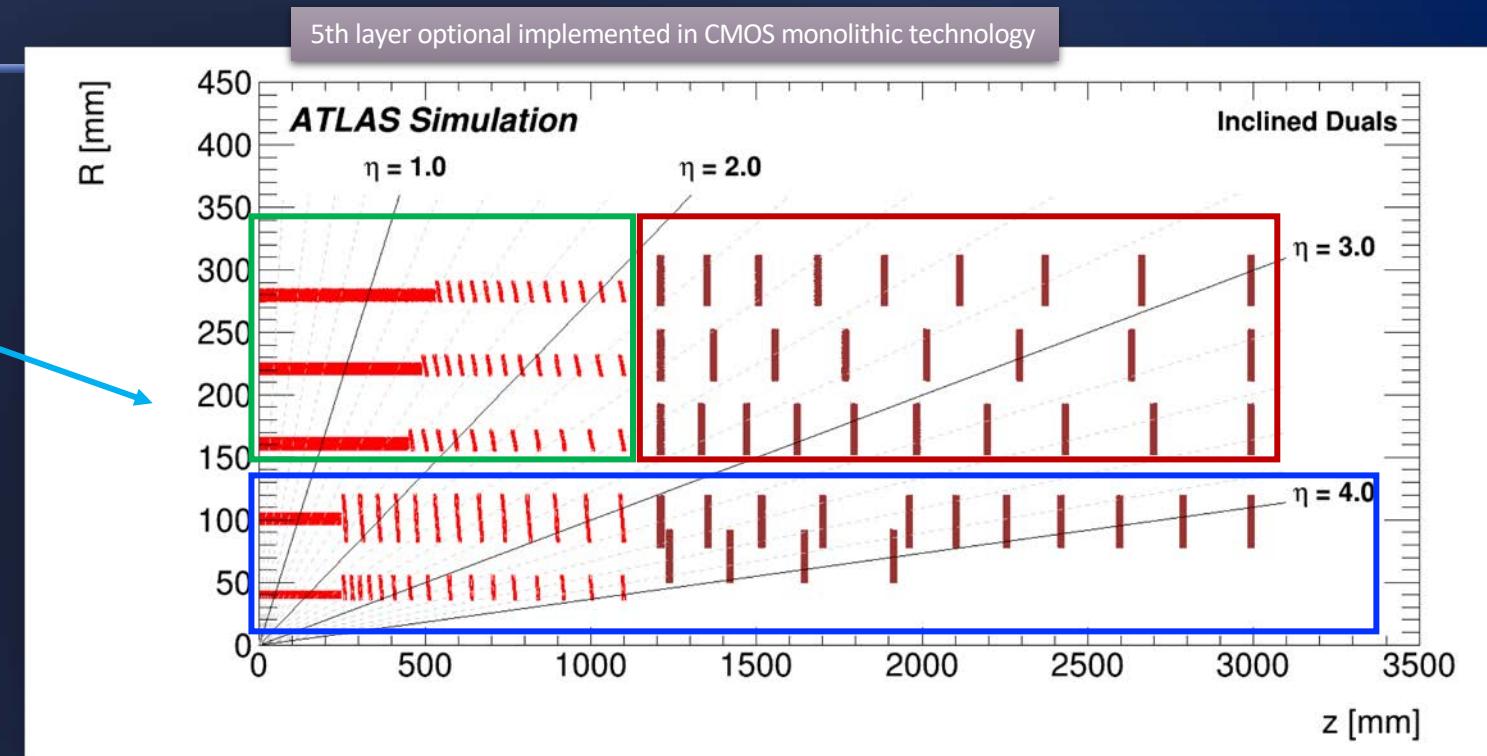
- New Inner Tracker: ITk
  - 5 **pixel** layers (barrel + rings)
  - 4 **strip** barrel (double-)layers + 6 disks per side
- 13 hits per crossing particle up to  $\eta=4$
- Low material budget
- Radiation levels up to 10 MGy for the innermost layer

	Pixel	Strips
Silicon area	$13 \text{ m}^2$	$160 \text{ m}^2$
Channels	$\sim 5 \text{ billions}$	$\sim 50 \text{ millions}$



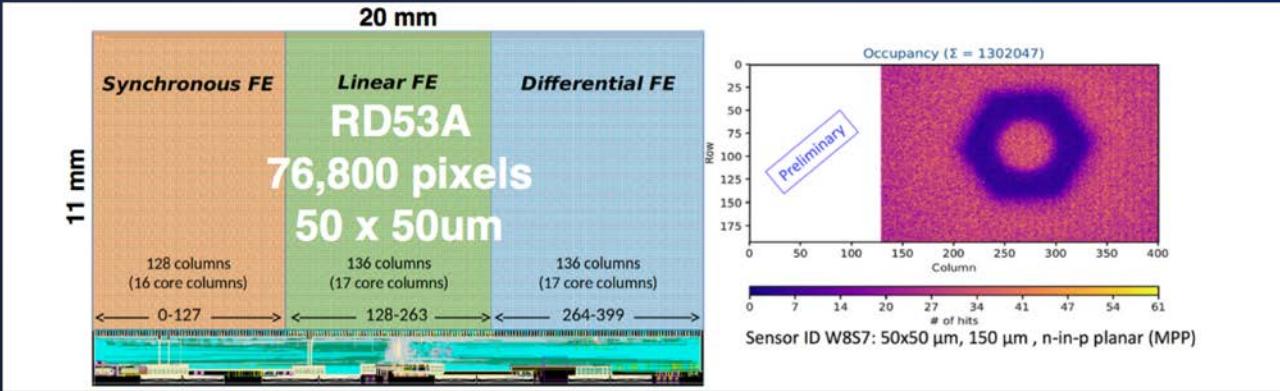
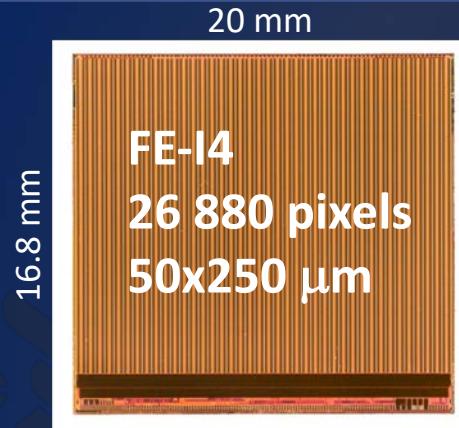
# New ATLAS ITk Pixel Detector

- 3 parts:
  - Inner system (replaceable)
  - Outer barrel
  - Outer endcap
- Different sensor types:
  - Planar silicon sensors (100 and 150  $\mu\text{m}$  thickness)
  - 3D silicon sensors (only innermost layer)
  - Pixel size 50  $\mu\text{m} \times 50 \mu\text{m}$  or 25  $\mu\text{m} \times 100 \mu\text{m}$
- Fast readout: up to 4 MHz trigger rate
- Data transmission using 4 x 1.28 Gb/s per front-end chip
- Serial powered detector modules
- CO<sub>2</sub> cooling



~ 35 000 ASICs  
~ 10 000 modules

# Front-End Chip Development



- FE-I4 done in 130 nm technology
- Radiation hardness up to 2.5 MGy
- Integrated shuntLDO (old design)
  - Not used in detector operation
- Lots of R&D activity ongoing with FE-I4 chips
  - Sensor testing
  - Module assembly (Bump-bonding)
  - Serial powering demonstrators

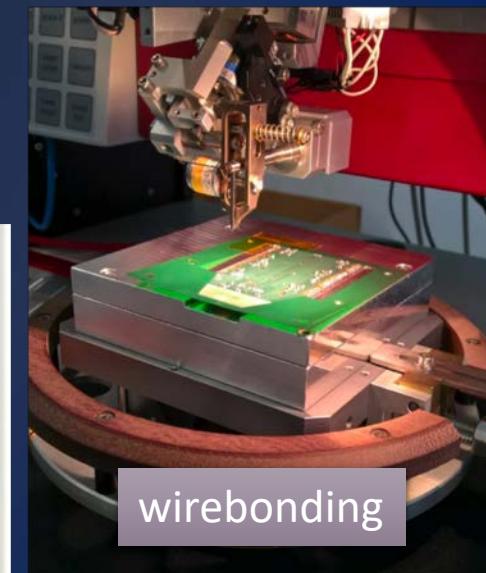
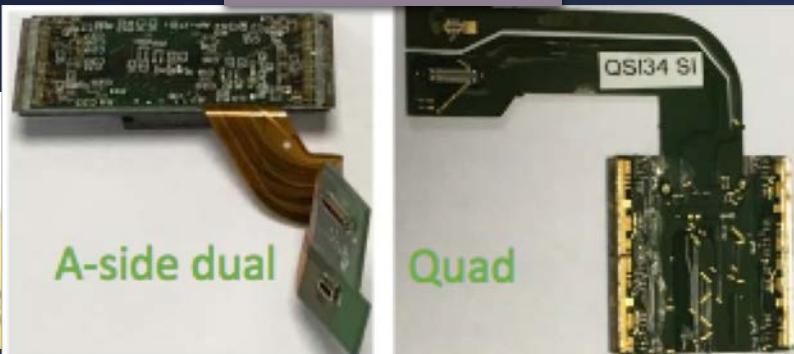
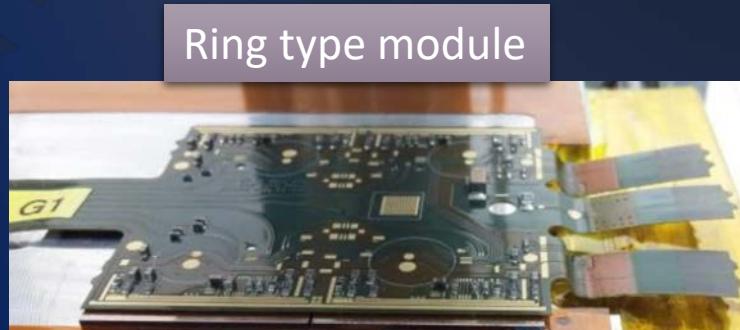
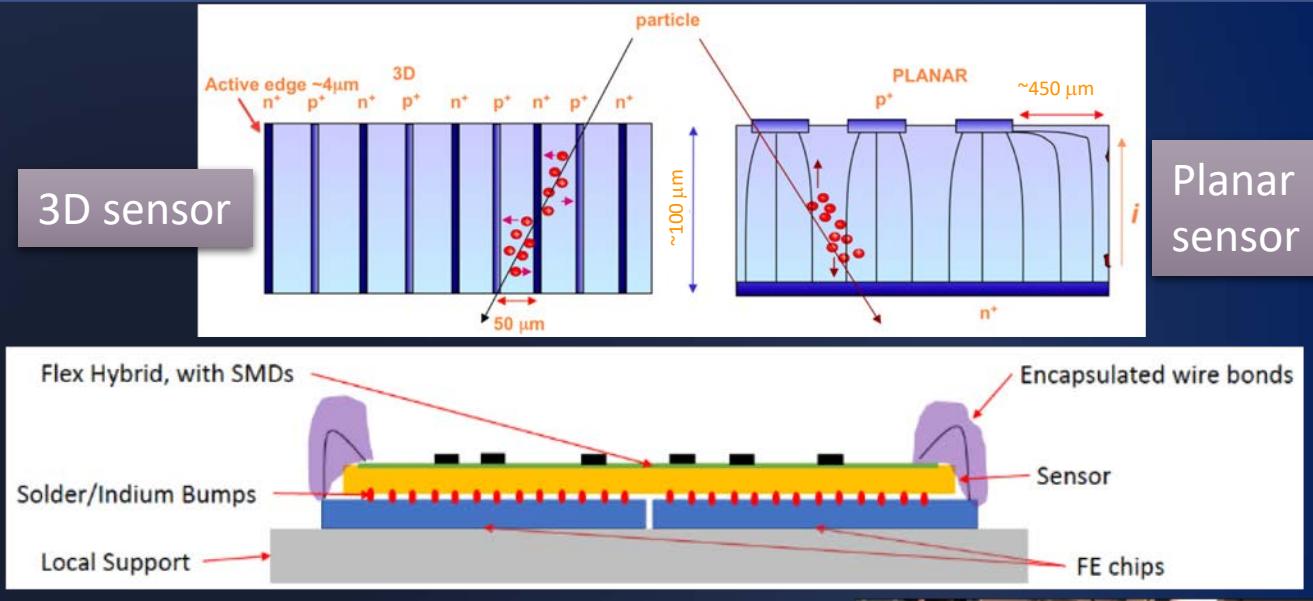
FE-I4: M. Garcia-Sciveres, NIM A636 (2011) 155  
RD53: M. Garcia-Sciveres, CERN-RD53-PUB-17-001

- RD53A is first prototype of the final readout ASIC
  - Done in 65 nm TSMC technology in collaboration between ATLAS and CMS
  - 4 data links at 1.28 Gb/s per chip
  - 50 μm x 50 μm (25 μm x 100 μm)
  - RD53A is 50% of final chip size (pixel matrix)
  - Integrated shunt LDO
- Module become available now
- Analog FE choice is due now
- **RD53B to be submitted mid of 2019**

See A. Dimitrievska's  
Talk tomorrow  
morning

# Sensor and Module Construction

- Hybrid modules consisting of silicon sensor and readout front-end ASIC
- Quad-chip modules prototyped with existing FE-I4 readout ASIC
  - 4 FE chips bump bonded to sensor (planar)
  - Wire bonds from ASICs to flex circuit board (encapsulated)
- Different types of modules for several prototype structures



# Serial Powering

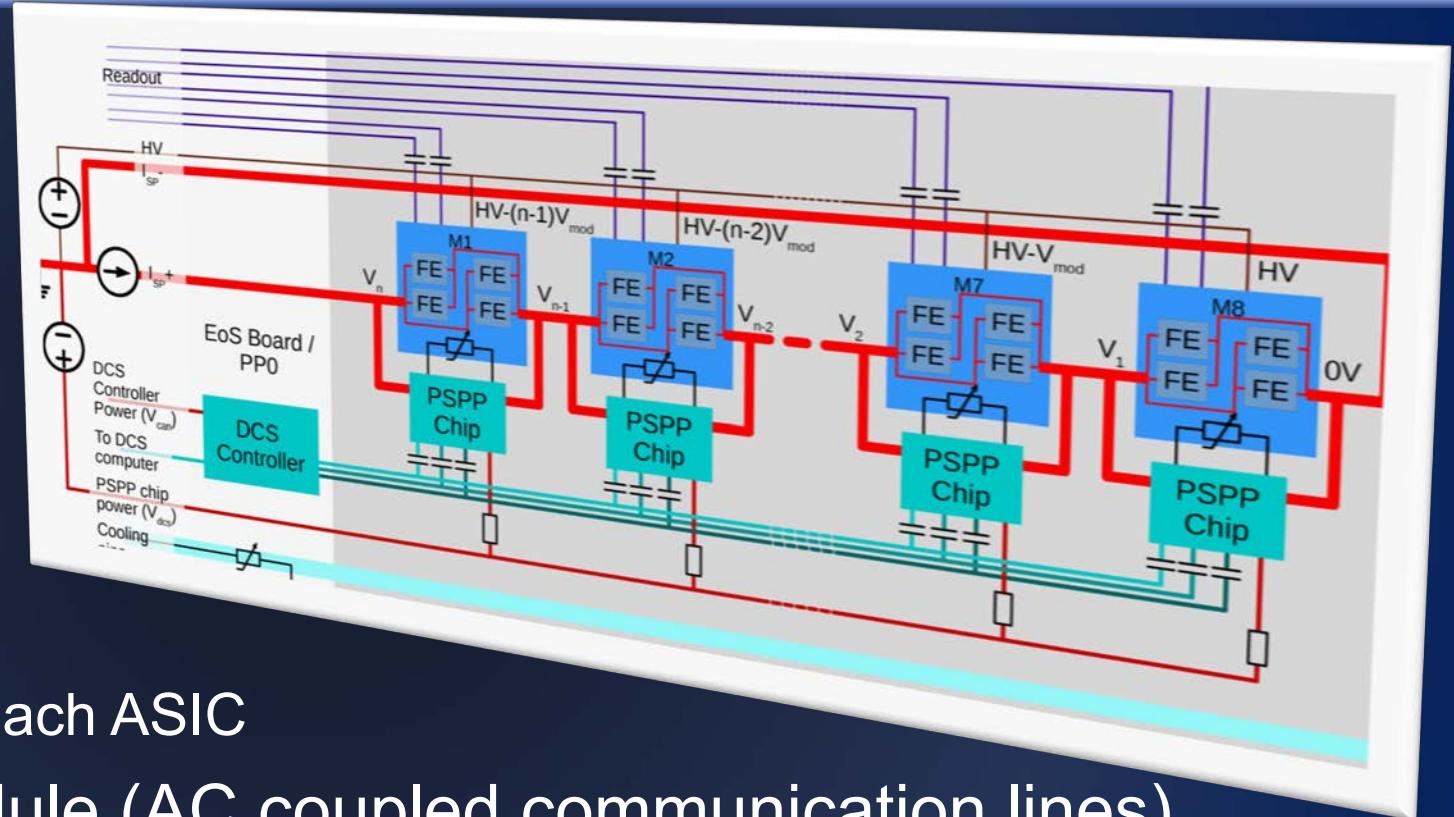
Serial powering:

T. Stockmanns et al., NIM A511 (2003) 174-179

D. Bao et al., NIM A557 (2006), 445-459

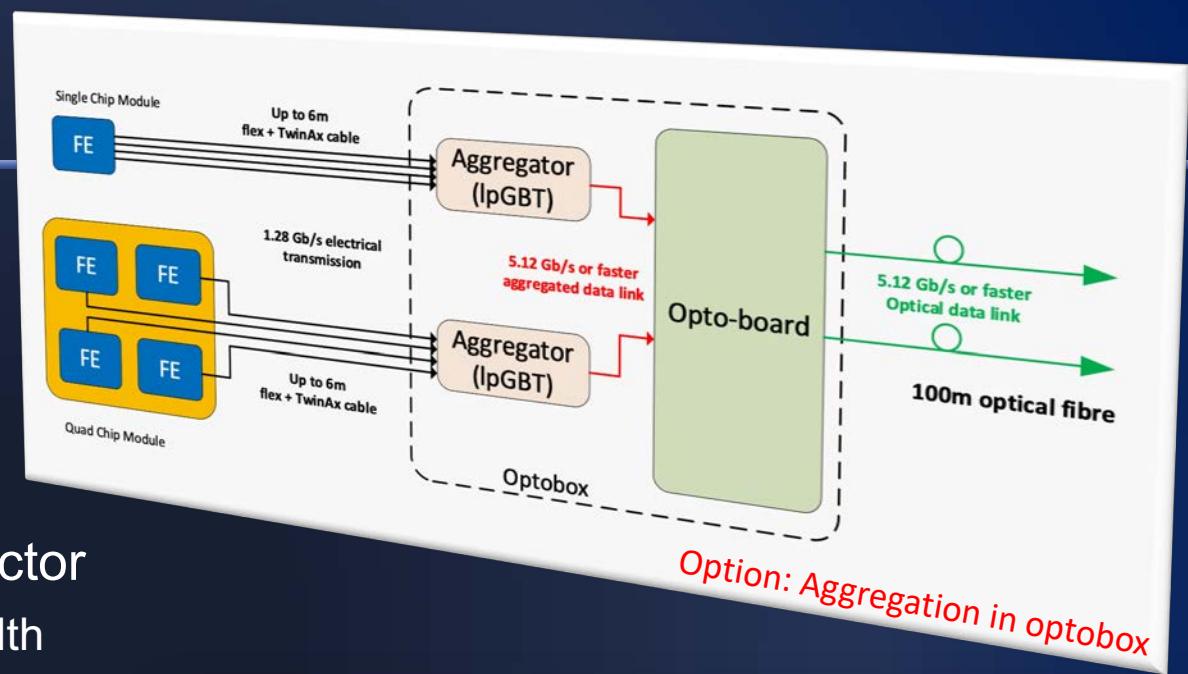
L Gonella et al., JINST 5 (2010) C12002

- Chains of modules powered in series
- Up to 14 modules per chain
- Reduced number of supply lines
- Efficient power distribution
- Voltage regulation on chip
  - radiation hard shuntLDO in each ASIC
- Different potentials per module (AC coupled communication lines)
- Sensors supplied by several HV lines per chain
- Protection and monitoring ASIC under test and risk evaluation

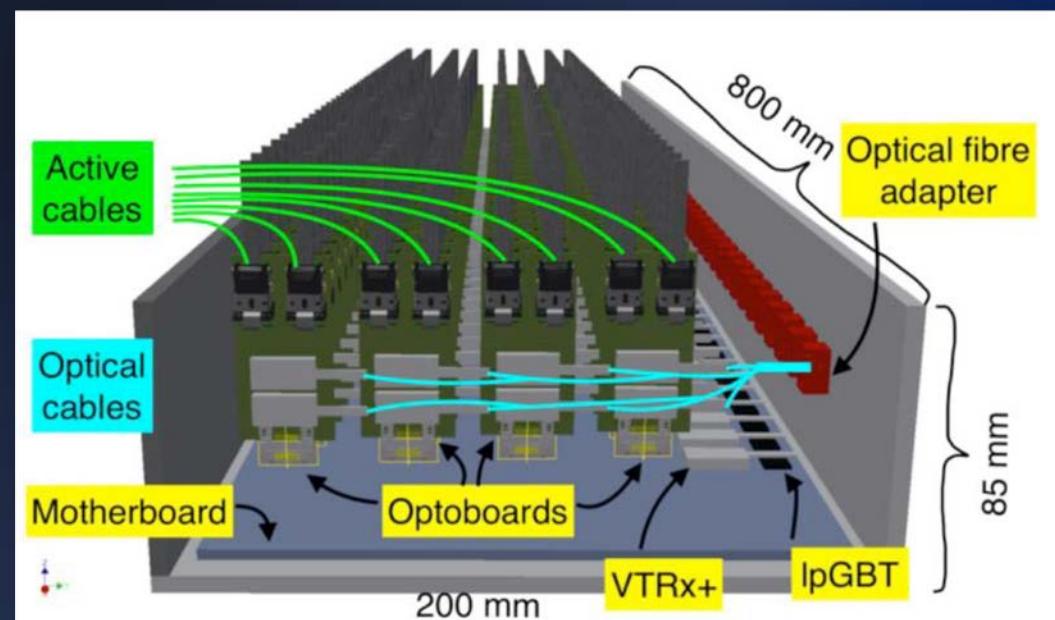


# Data Transmission

- Higher bandwidth needed to read out all the accumulated hits
  - $160 \text{ Mb/s} \rightarrow 5.12 \text{ Gb/s}$  per FE chip
- FE chip runs up to 4 lanes at 1.28 Gb/s
- Number of lines depends on the position in detector
  - Outer layers have less occupancy  $\rightarrow$  lower bandwidth needed
- Electrically connected to an optoboard
- Data aggregation to save lines
  - Close to module or inside optobox
- Electrical / optical conversion
- Long optical fibres up to the readout electronics

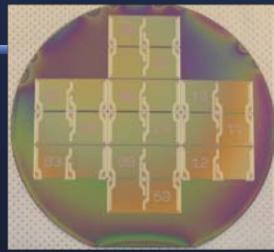


*Option: Aggregation in optobox*



# Thermal Prototype

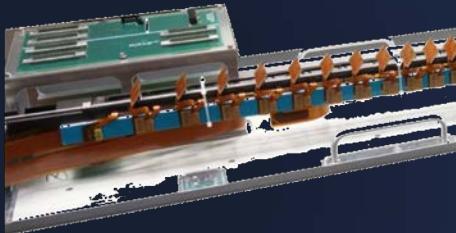
- Thermal prototypes to test thermal integrity with silicon heaters
- CO<sub>2</sub> cooling at -10 °C
- Heaters powered in steps: 0.1-0.7 W/cm<sup>2</sup>
- **Evaluation of test results ongoing**
- **First results show thermal performance within specifications**



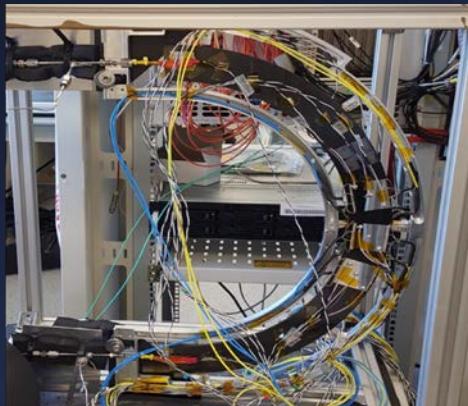
Wafer of heaters



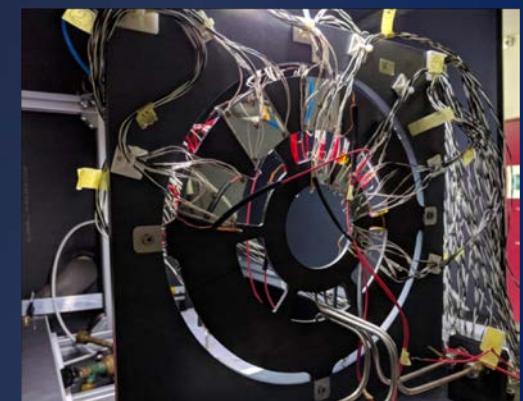
Quad heater with flex



Outer barrel: structure (longeron) with 44 silicon heaters



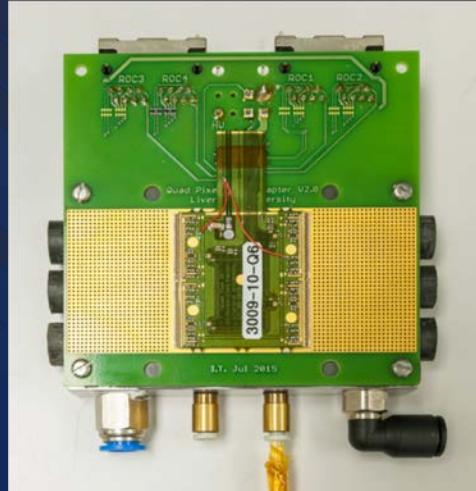
Outer endcap: half ring with temperature sensors on silicon



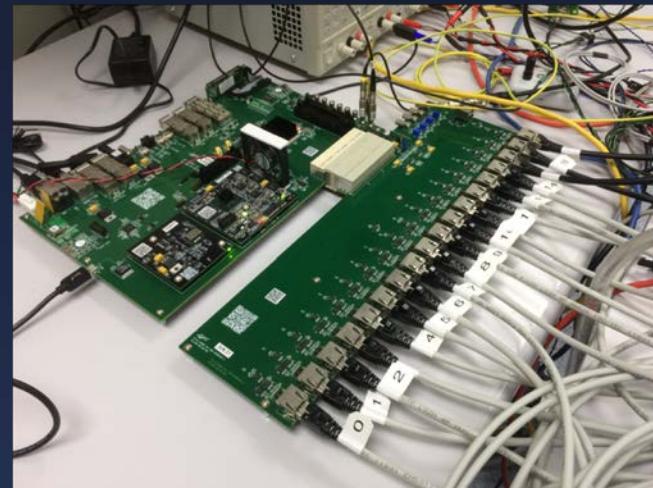
Inner system: ring with temperature sensors on silicon

# FE-I4 based prototypes: Endcap

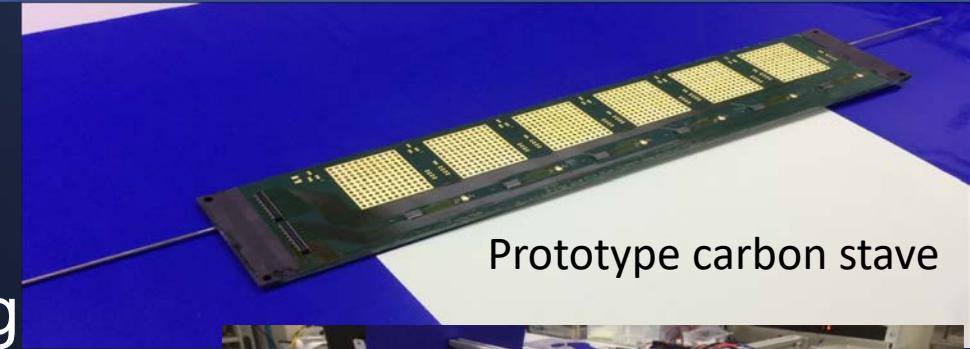
- Endcap prototype stave: double sided CF stave with 12 quad modules (6 / side)
- Modules qualified before loading
- Tapes for connection to allow serial powering
  - 2 chains of 6 modules or 1 chain of 12 modules
  - 13 module can be added on jig



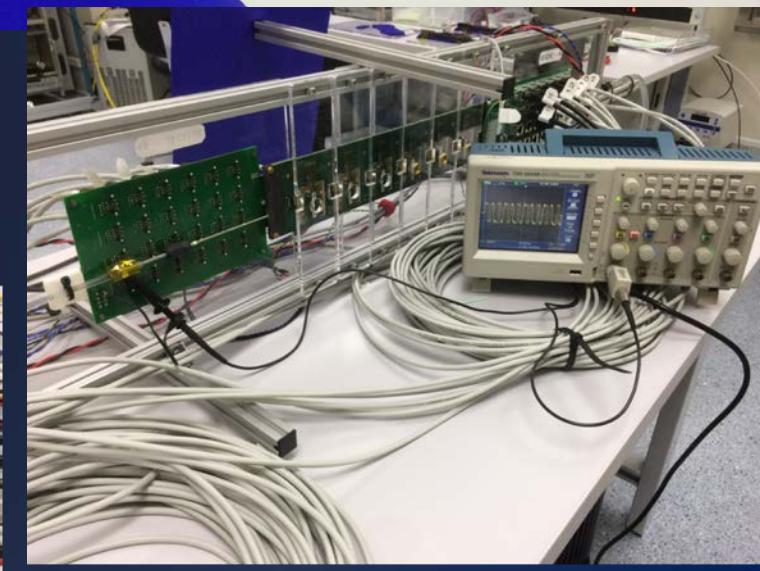
Module testing jig



RCE based readout system



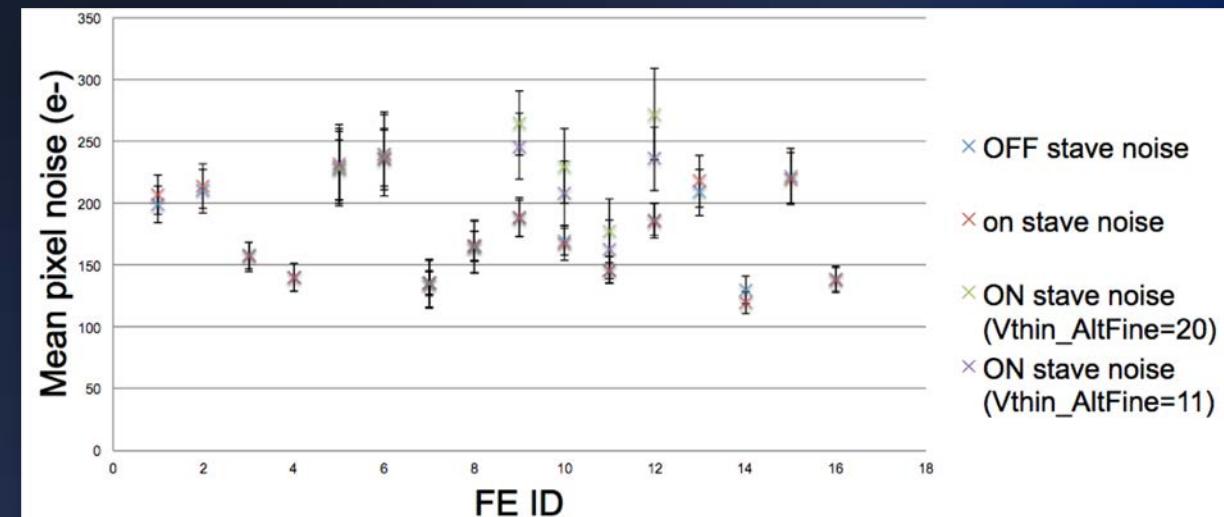
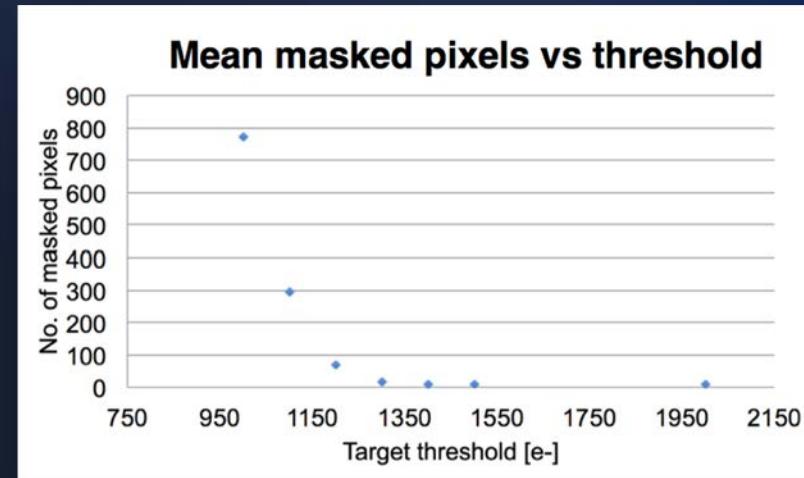
Prototype carbon stave



Fully mounted stave  
(CMD/CLK/data lines AC coupled)

# Results from Endcap Test-Stave

- Fully operational stave in SP chain configuration
  - Module behaviour in terms of threshold and noise performance does not show any additional effect
- SP chain operation smooth, not adding disturbances
- No additional noise due to stave mounting observed:
  - Threshold tuned to 1500 e<sup>-</sup>
  - Noise < 250 e<sup>-</sup>
  - Only few masked (noisy) pixels

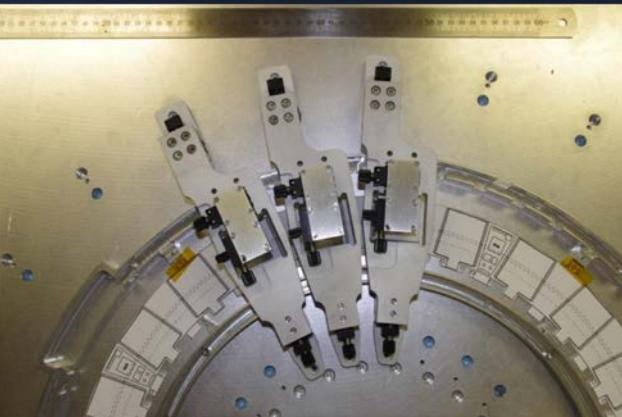


# FE-I4 based: Ring-0 Prototype

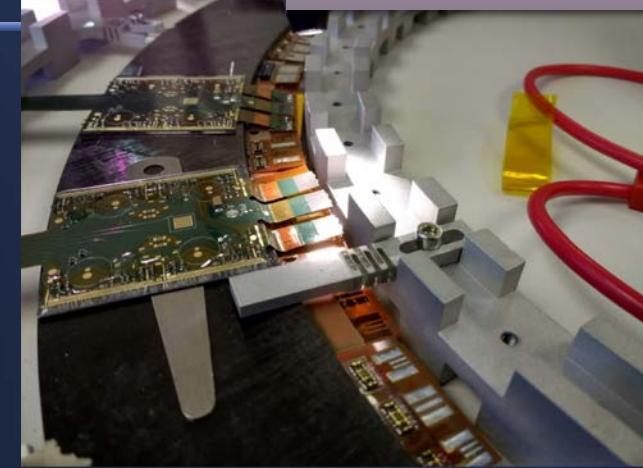
- 12 modules ring structure in preparation
- 2 SP-chains foreseen
- Modules from 3 assembly sites being mounted (test of production flow)
- Test setup:
  - Cooling with cooled air ventilation
  - Interlock system in place
  - DAQ system for operating modules



Local support in transport frame



Loading geantry

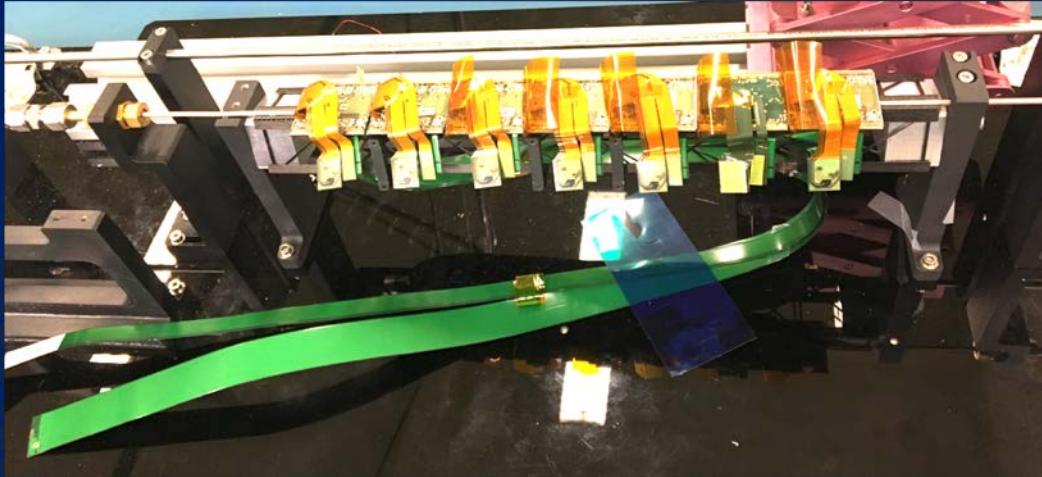


Loaded modules



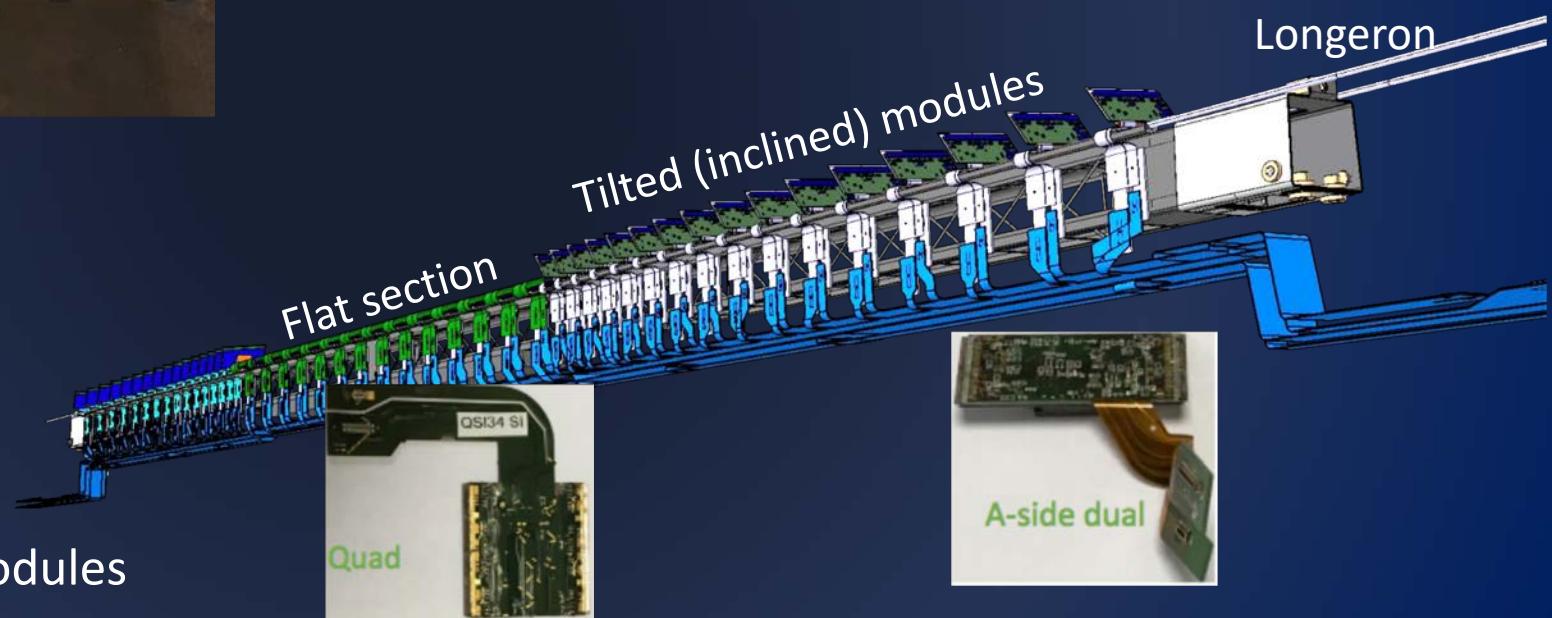
Test setup box: ring and fans

# FE-I4 based: Outer Barrel Stave Prototypes



## Full-size prototype:

- 1.6m long prototype structure
  - 6 serial powering chains
  - 4x8 dual modules and 2x7 quad modules
- 120 ASICs



## 7-cell structure:

Local support with 7 loaded FE-I4 quad modules,  
flex connections for power and readout

Fully working

## For final layout:

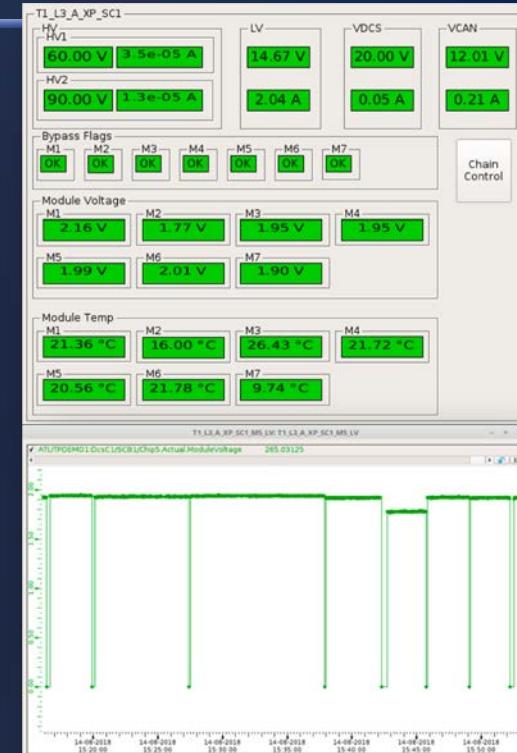
Inclined section is separated  
Quad modules instead of dual modules in inclined section

# 7-Cell Structure

Power  
Control  
Readout



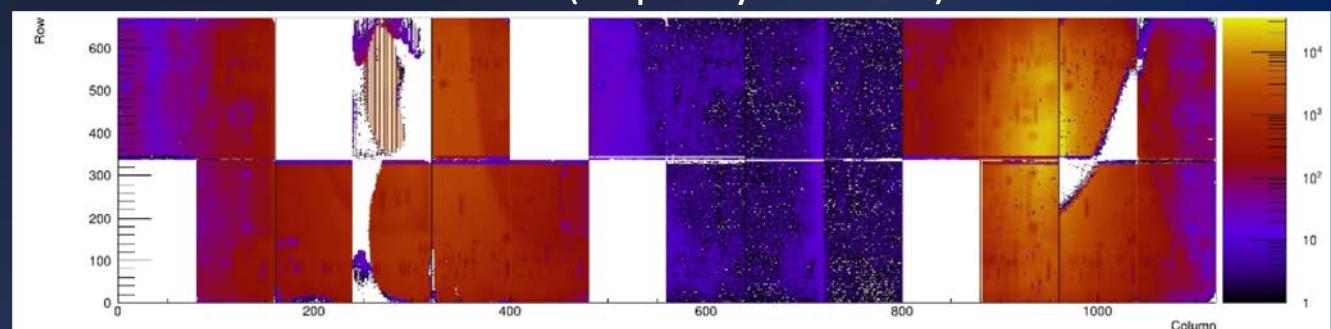
Detector Control



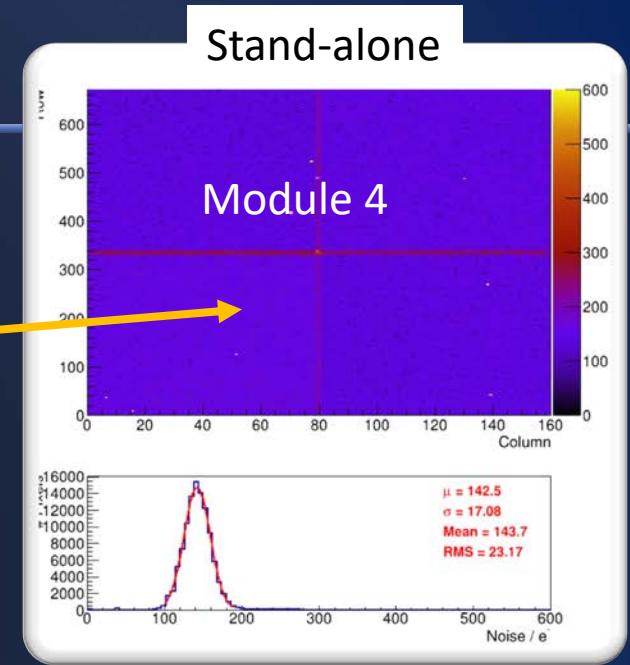
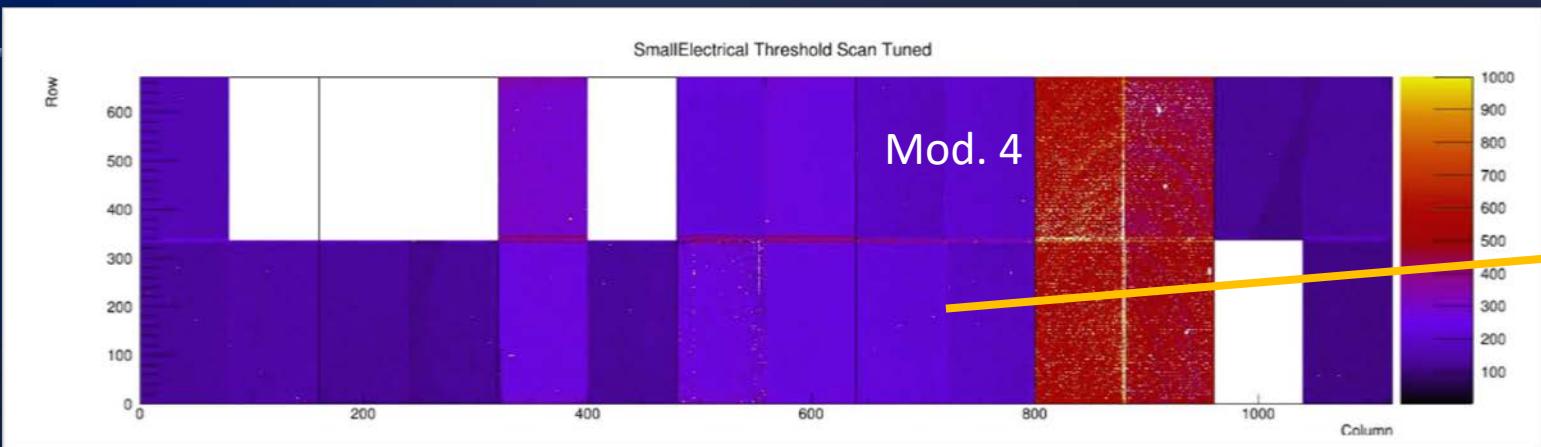
Fully electrical functional structure with 7 quad modules loaded  
Detector Control System (DCS) in place for controlling and monitoring

Serial powering with 2A per chain and 2V per module  
Two separate HV groups with common return

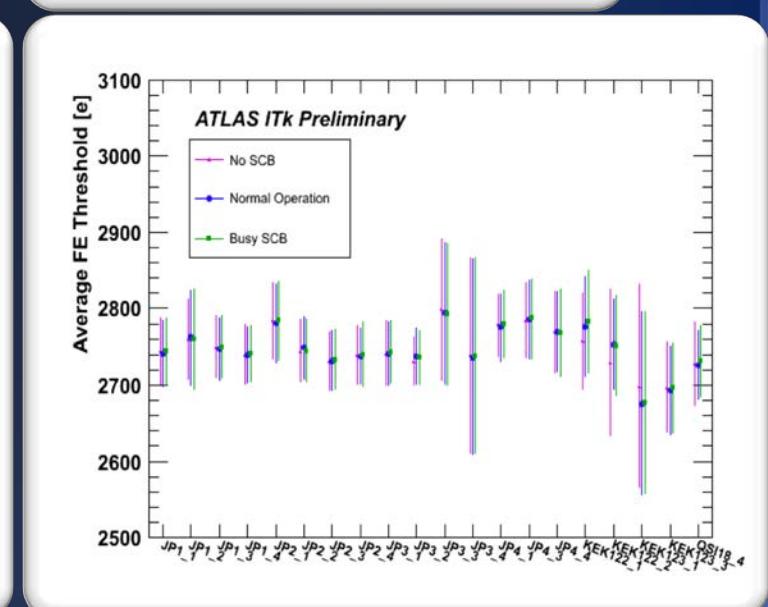
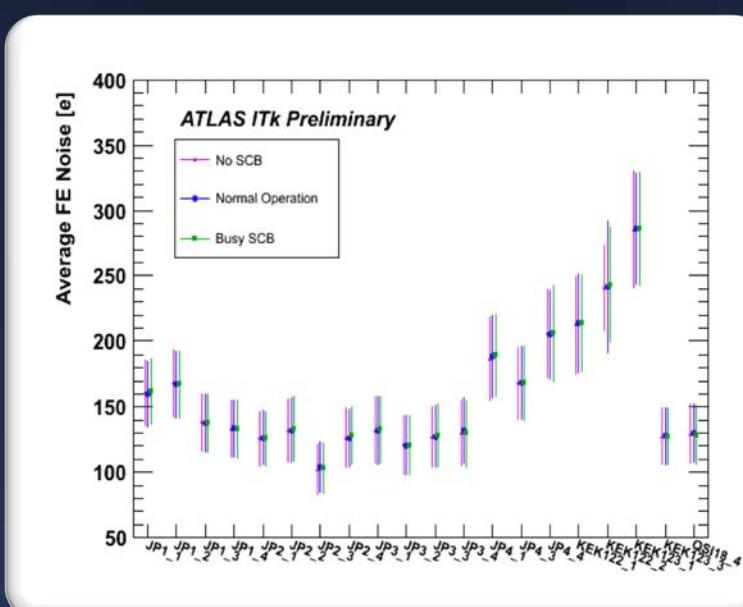
Sr90 source scan (B-quality modules)



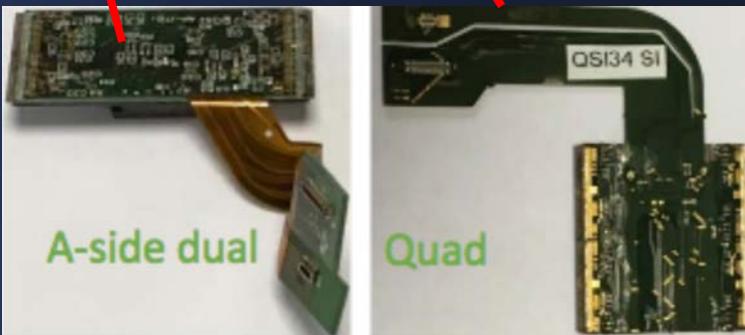
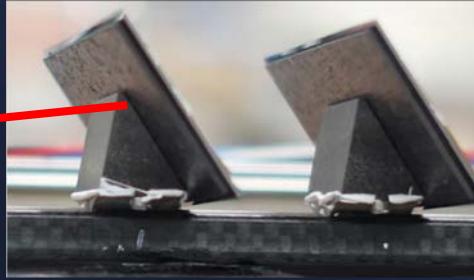
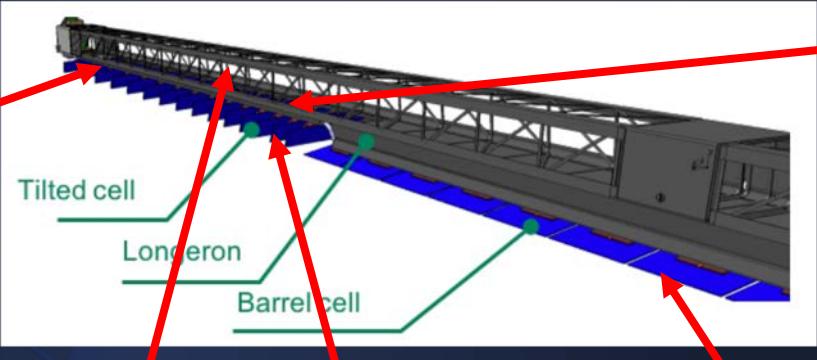
# 7-Cell Structure Results



- Test with several readout systems
- Serial powering protection chip connected to each module (connected via slow control bus, 200 kHz, 100 kb/s)
- Modules operate similar as in stand-alone
- No extra noise observable



# Full size Prototype Components



Assembly of full size prototype  
(1.6m long longeron, 120 ASICs)

Components prepared

Procedures well defined and  
exercised

Test of full production chain  
from module assembly and  
characterisation, local support  
production, loading, integration,  
and testing can be exercised.

Still FE-I4 modules, but  
mechanical procedures very  
similar if not the same.

# Conclusion

- New ATLAS pixel detector in preparation for the HL-LHC upgrade.
- Experience gained over the whole collaboration by building prototypes on small and larger scale
  - Module prototypes with currently existing FE-chip being done
  - Module assembly procedure defined
  - FE-I4 based prototypes have been constructed and tested for the outer endcap and barrel.  
Inner system prototype about to come.
    - Lots of experience gained.
    - QA/QC definition based on the experience gained.
  - New prototypes (ring-0, full size longeron) currently under construction to test logistics and full production chains.
  - Test setups using RD53A modules will be built up very soon too
    - Serial powering chain testing
    - RD53A demonstrator
- The collaboration is about to change over from R&D into production to deliver the ATLAS Pixel ITk by 2024 for installation