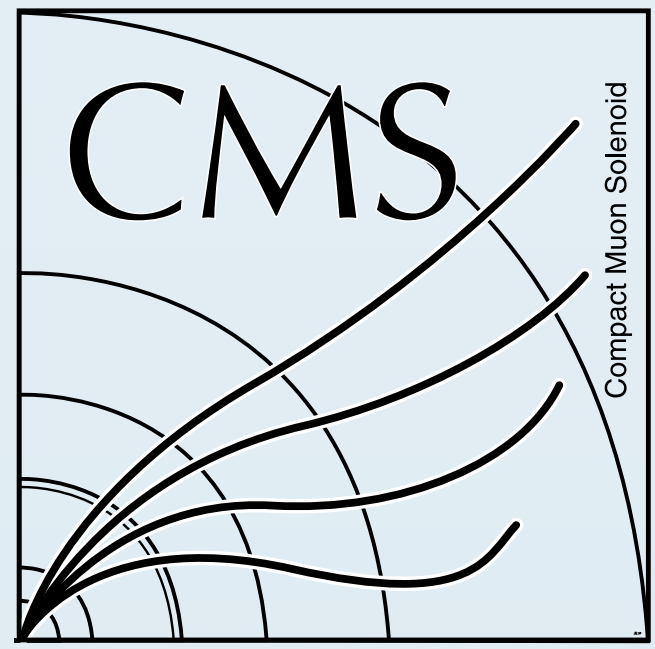


# Longevity studies and Phase 2 electronics upgrade for CMS Cathode Strip Chambers in preparation for HL-LHC



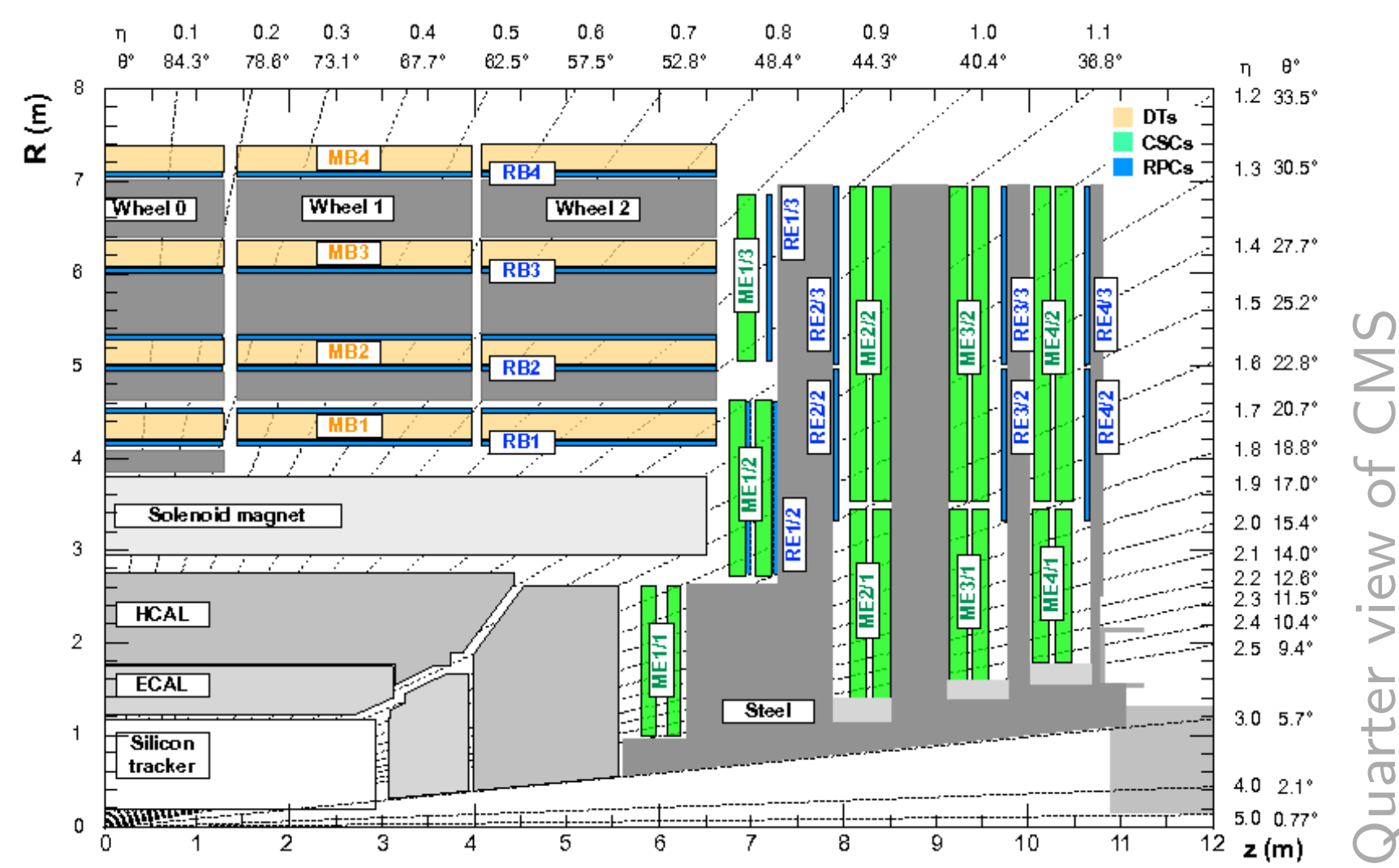
Bingran Wang (Northeastern University)

On behalf of the CMS Muon Group

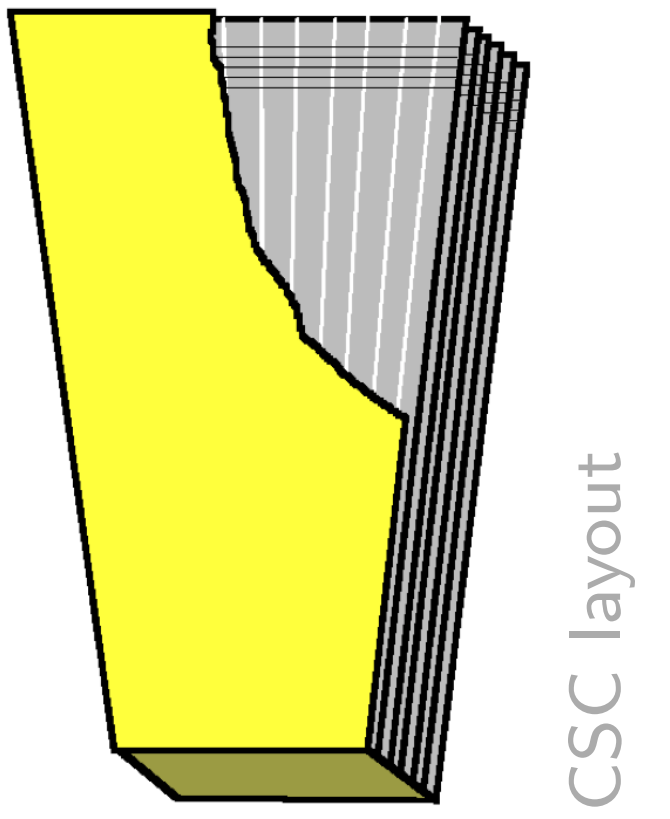
15th Vienna Conference on Instrumentation, 18-22 Feb 2019, Vienna (Austria)

## CMS CSCs (Cathode Strip Chambers)

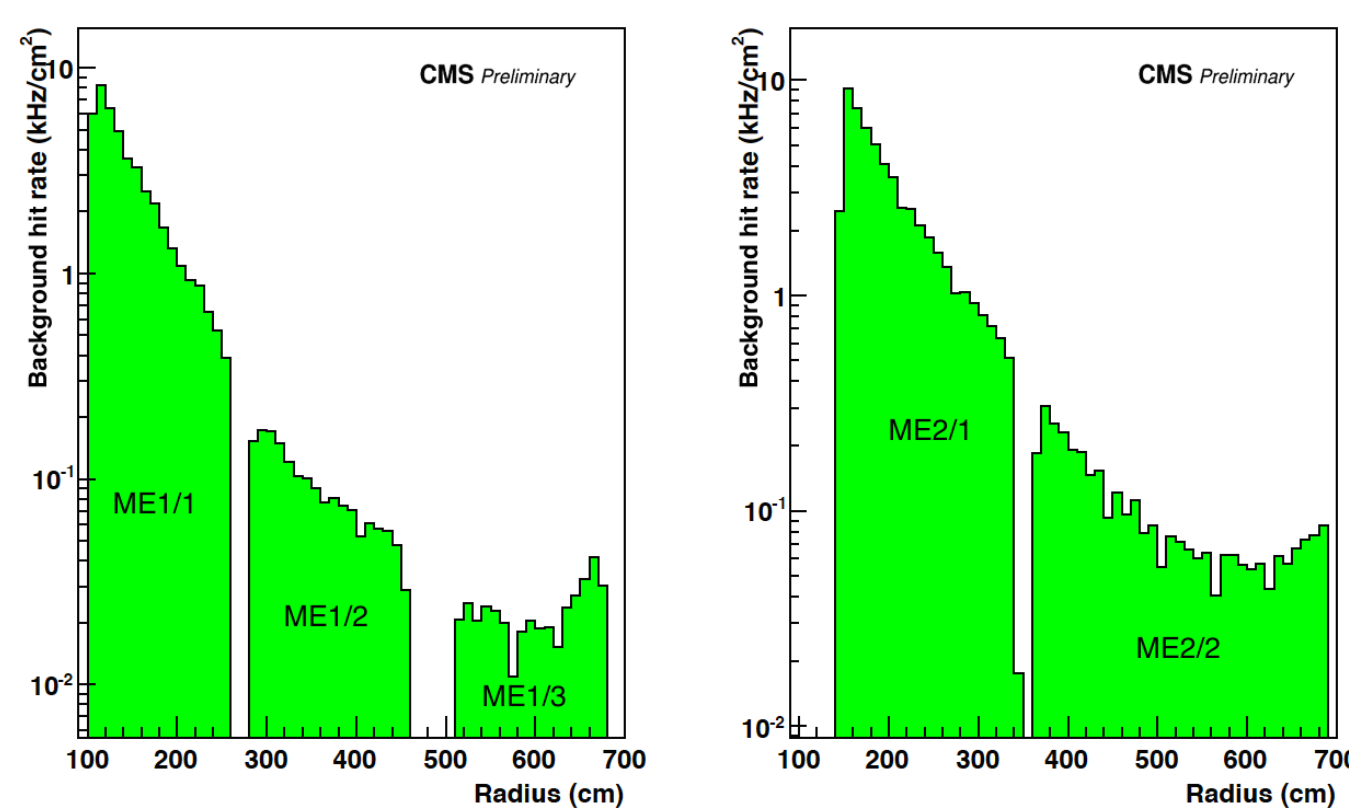
- 540 CSCs in total for muon identification, triggering and track reconstruction
- Each endcap of CMS has 4 stations of CSCs
- Each station has 2 or 3 rings of chambers



- Each CSC has 6 layers of anode wires and cathode strips to measure a muon track segment from 6 reconstructed hits
- CSC filled with 40% Ar, 50% CO<sub>2</sub>, and 10% CF<sub>4</sub> gas mixture
- Muon ionizes the gas mixture in chambers. A strong electric field creates a gas avalanche, which produces signals on strips and wires which provide a 2D muon hit position
- $\phi$  is precisely measured by strips, and  $r$  is measured by wires



## CSC under HL (High Luminosity) Conditions



Extrapolated HL-LHC background rate

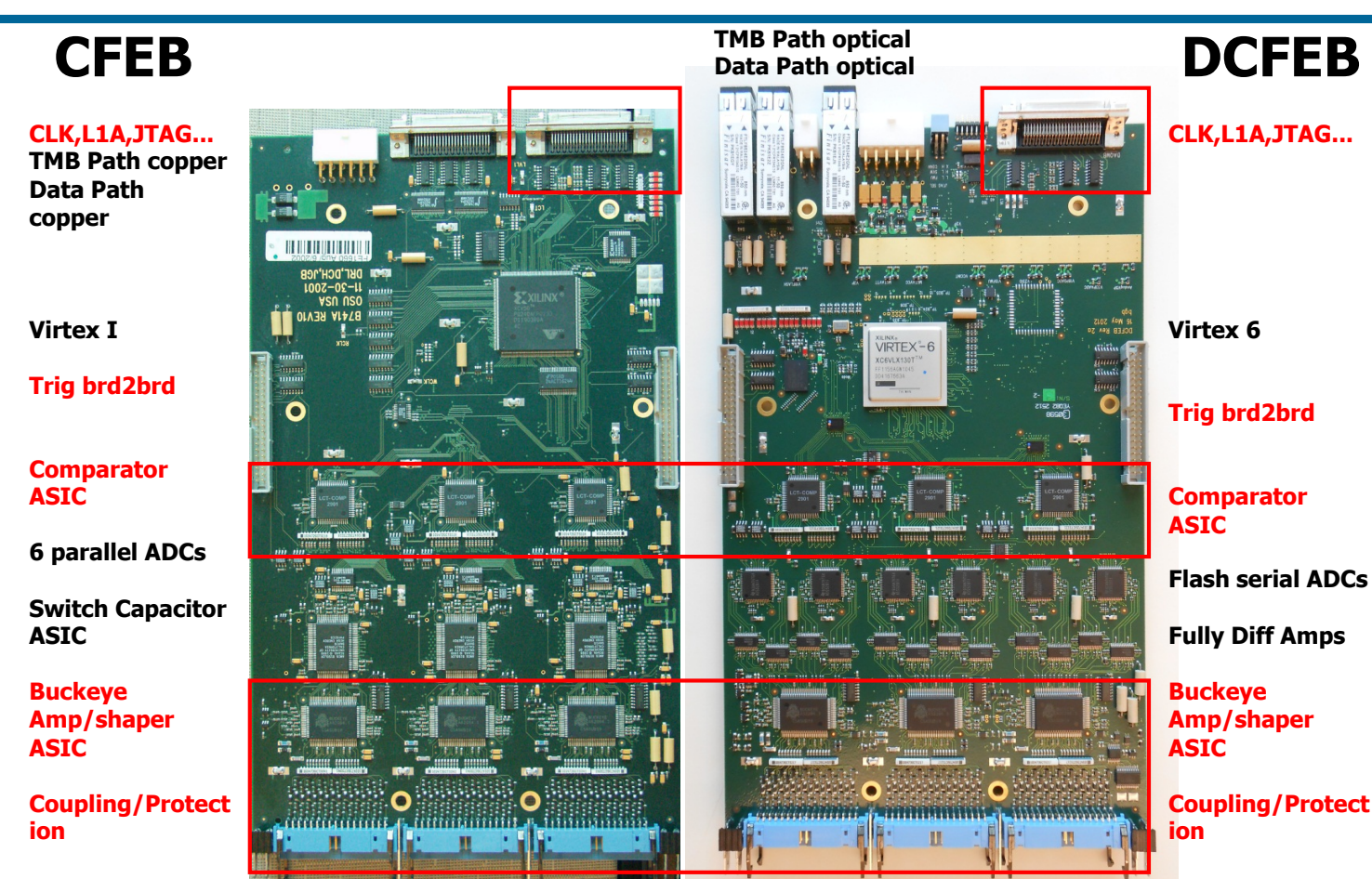
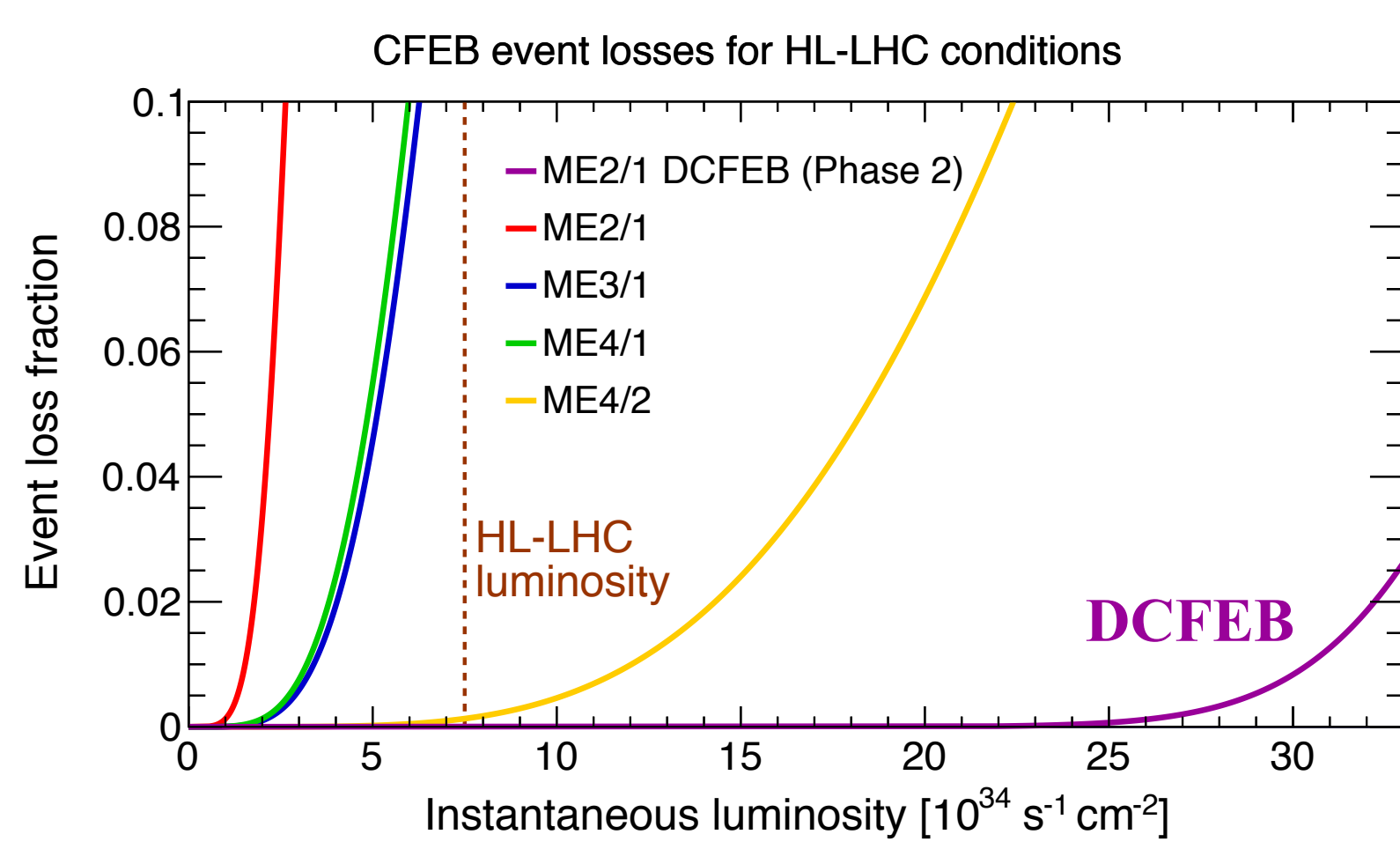
- The luminosity of HL-LHC could reach  $7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$  (7.5 times higher than original LHC design)
- The very forward CSCs (especially ME1/1 and ME2/1) will suffer large particle rates.

The increase in background and L1 trigger rate and latency pose two questions:

- Will CSC electronics operate reliably under much higher luminosity and pileup conditions? (Electronics Upgrades)
- Will CSC detector tolerate the much larger integrated charge expected at HL-LHC? (Longevity Study)

## Electronics Upgrades

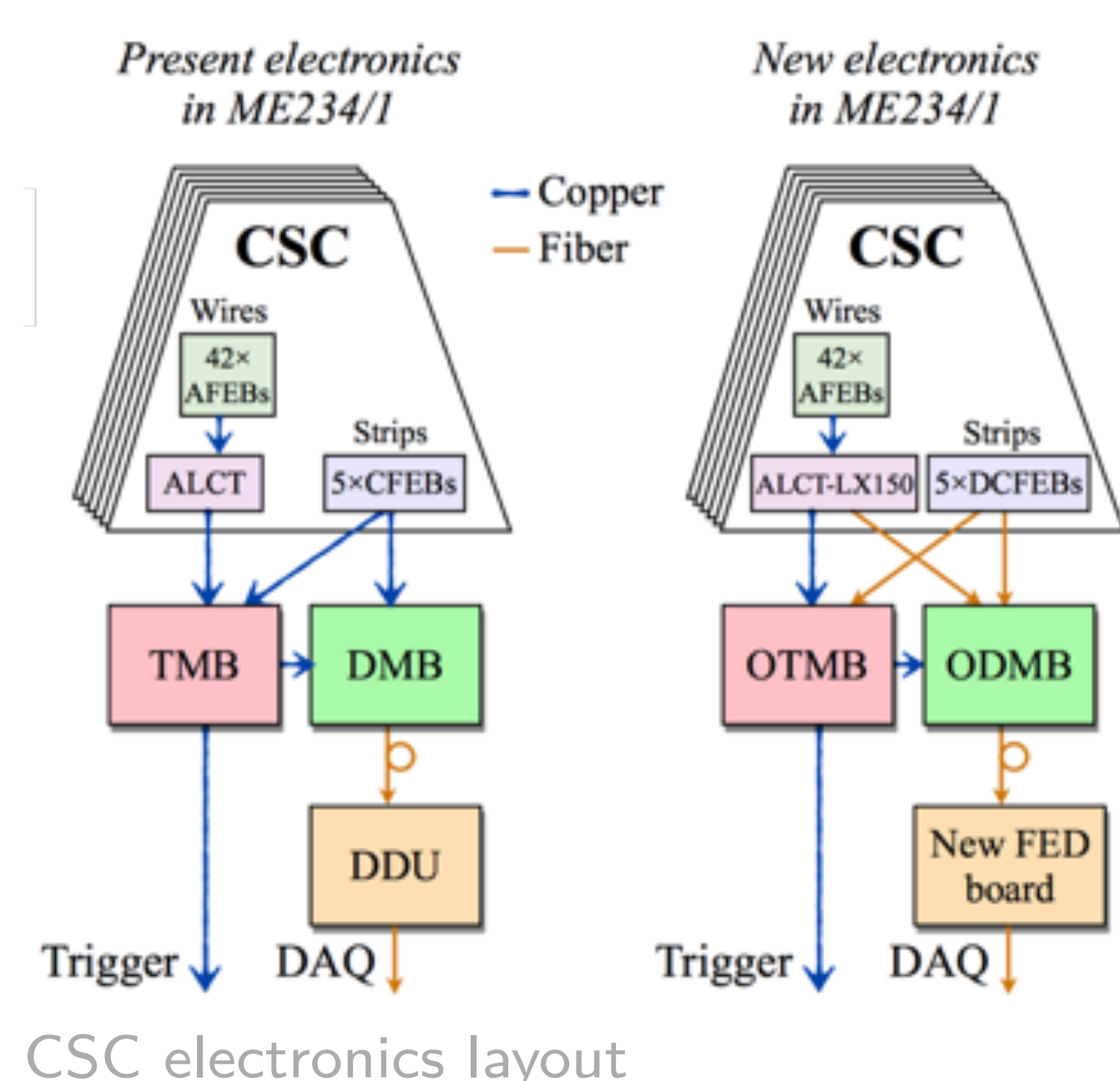
A CFEB (Cathode Front-End Board) stores analog signals from strips in SCA (switched capacitor array) for digitization. The expected number of events stored in SCA depends on the muon rate and the level-1 trigger latency, which will be nearly 3.5 times higher in HL-LHC. The limited storage of the SCA would lead to data losses at the HL-LHC data rates.



Comparison between CFEB and DCFEB

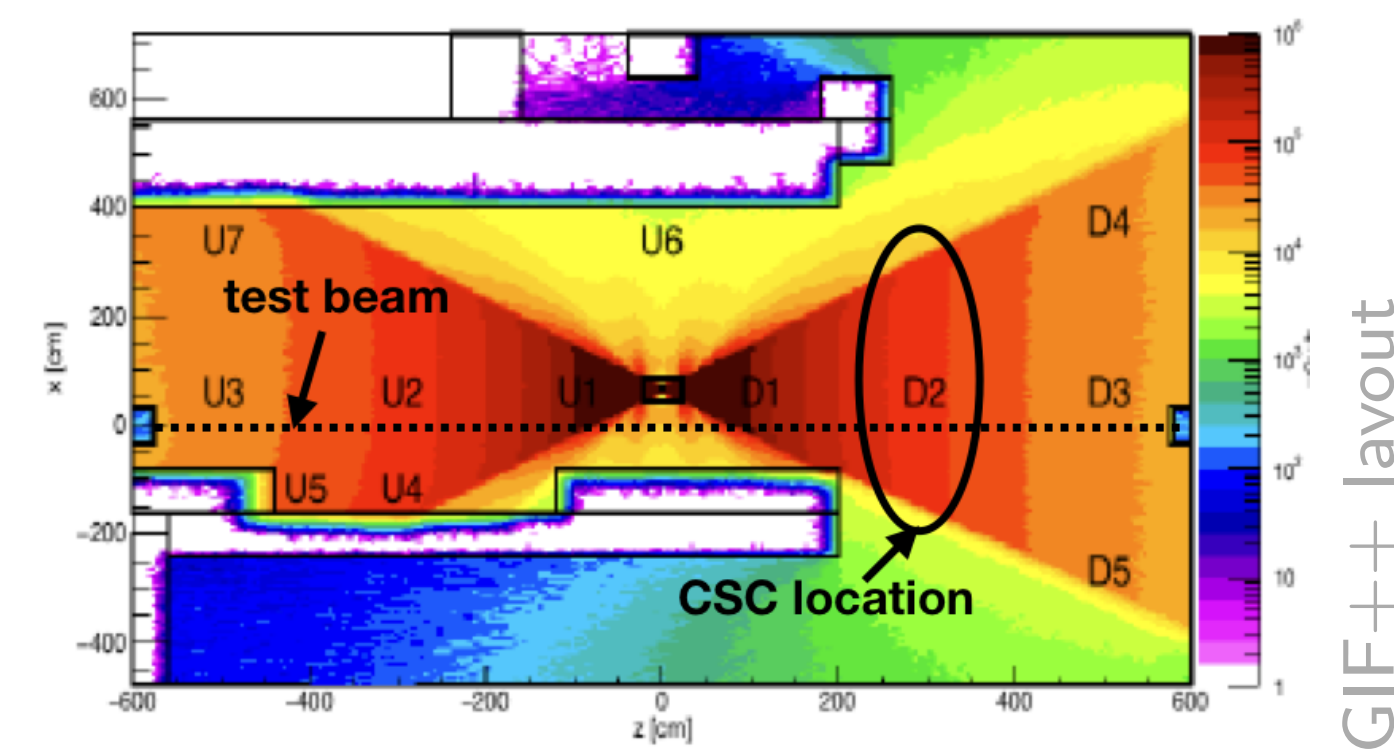
The data loss in HL-LHC can be solved by upgrading CFEB to DCFEB (D for digital), which uses Flash ADCs to continuously digitize and store into an infinitely deep pipeline the analog signal. The Virtex 6 FPGA is upgraded to a powerful Virtex 6, which stores the digitized signals from ADCs.

- The anode trigger board, ALCT, will be upgraded with Spartan 6 FPGA to cope with L1 trigger latency.
- ALCTs and DCFEBs in ME1/1 will be equipped with a fast optical programming path via GBTx to recover EPROM failure from radiation. New DCFEB is named xDCFEB.
- To accommodate higher rate, inner ring chambers' copper readout will be upgraded to optical links.



CSC electronics layout

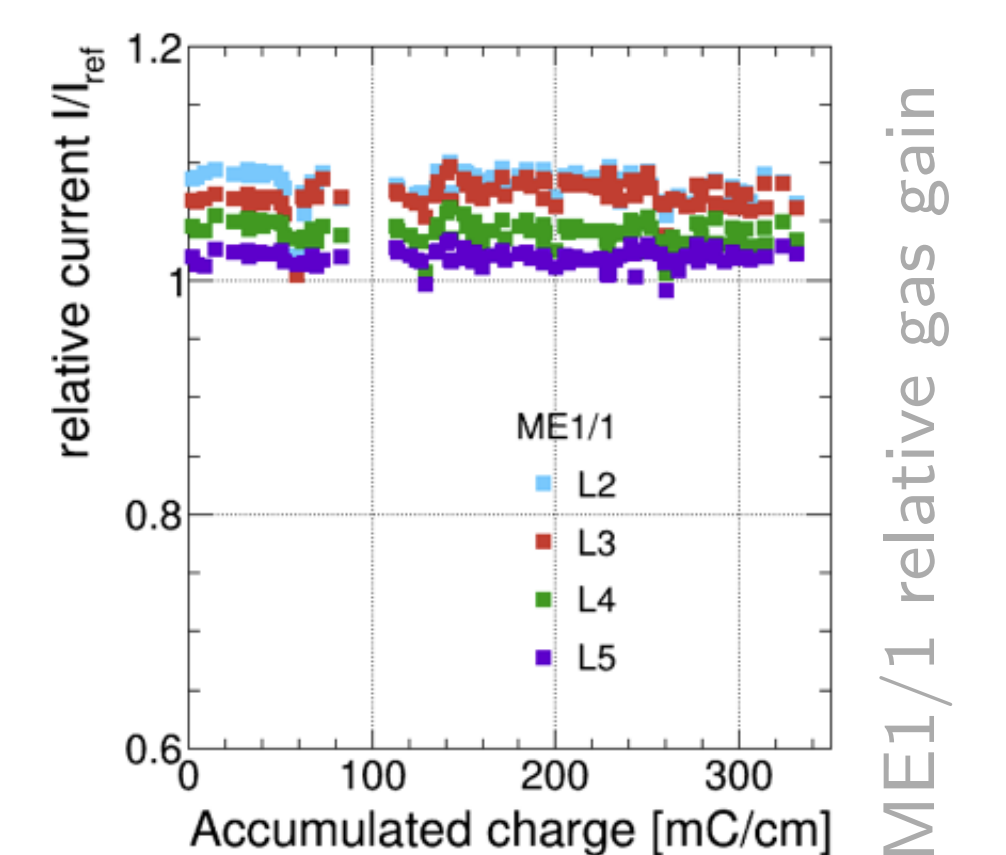
## Longevity Study



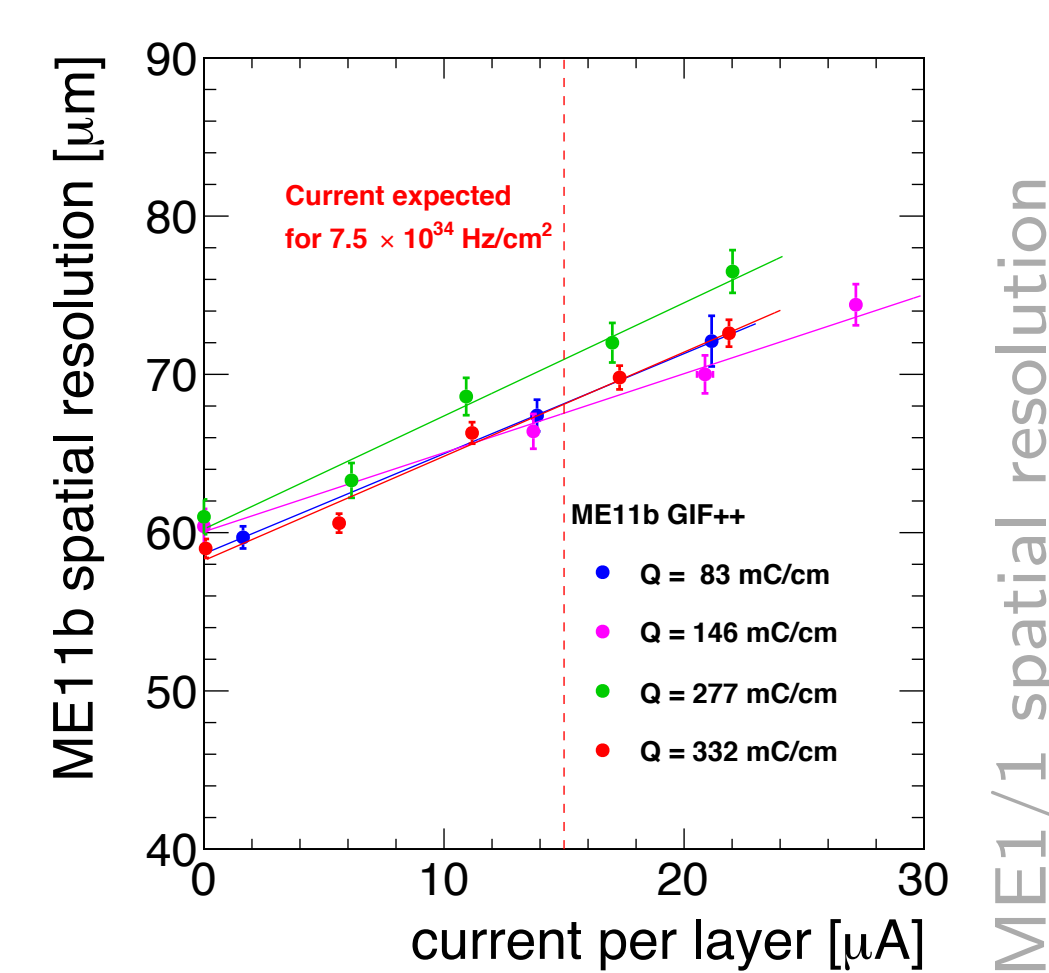
The high radiation doses of HL-LHC can cause CSC material aging thus preventing operation stability and deteriorating performance. Longevity tests of CSCs are being performed at the CERN GIF++ facility, which employs a 14 TBq <sup>137</sup>Cs source and a muon test beam.

CSC aging is studied by monitoring detector parameter stability during irradiation and measuring global performance using the muon beam.

Anode wire polymerization can increase wire diameter and cause a reduction in gas gain (a measure of avalanche size). Two CSCs (ME1/1 and ME2/1) have been irradiated up to a collected charge equivalent to 3 times that expected at the maximum HL-LHC integrated luminosity. All recorded parameters (gas gain, dark current, dark rate, etc.) were stable throughout the irradiation.



There is no evidence of significant chamber damage under HL-LHC conditions, but the high radiation dose may still degrade chamber performance. A muon test beam in GIF++ is used to monitor the performance throughout the period of chamber irradiation.



One characteristic of chamber performance is spatial resolution, defined as the deviation of predicted hit position from measured position. Study in GIF++ shows that increased instantaneous luminosity could cause a 10% deterioration in resolution, but it is stable up to an integrated luminosity equivalent to 3 times expectation for HL-LHC, so performance degradation will unlikely be an issue for HL-LHC.

## CSC upgrade history and plan

2013 -- 2014 LS1	2019 -- 2020 LS2	2024 -- 2025 LS3
<ul style="list-style-type: none"> <li>• CFEBs in ME1/1 replaced by DCFEBs</li> <li>• Addition of 72 ME4/2 chambers</li> <li>• Anode FPGA upgraded in ME1/1 and ME4/2</li> <li>• Optical data and trigger motherboards for DCFEB readout</li> </ul>	<ul style="list-style-type: none"> <li>• Replace DCFEBs in station 1 by xDCFEBs</li> <li>• Move old station 1 DCFEBs to stations 2-4</li> <li>• Anode trigger board upgrade with optical readout and more powerful FPGA</li> <li>• New optical trigger motherboard</li> </ul>	<ul style="list-style-type: none"> <li>• New optical data motherboard</li> <li>• New system of back end driver to accommodate higher input rate</li> </ul>