CMOS Active Pixel Sensors for High Energy Physics

Luciano Musa
Outline

① Prelude
  • Overview of CMOS Image Sensors

② First use of CMOS pixel sensors in HEP
  • STAR Heavy Flavor Tracker
  • ALICE Inner Tracking System

③ Novel Developments
  • Fully depleted sensors, wafer-scale integration, back-side processing

④ Some example of non HEP applications
Digital Imaging Revolution

Digital imaging began with the invention of the Charge-Coupled Device (CCD) in 1969

Start of the the digital imaging revolution

Boyle and Smith’s invention improved commercial and consumer products for decades and is one of the most important technological innovations of the past half-century

Since its inception, digital imaging has progressed through improvements in CCDs and with the emergence of Complementary Metal-Oxide Silicon (CMOS) Image Sensor technology

Since 10 years CMOS has become the leading imaging technology driving the second golden age ...

Nobel Prize in Physics 2009
Willard S. Boyle and George E. Smith  “for the invention of an imaging semiconductor circuit - the CCD sensor.”

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CMOS Image Sensor (CIS)

- Drive CMOS image sensors development and sales
- Cellular camera phones account for 62% of the sales
- 90% of the total image sensor sales in 2017 it was 74% in 2012, 54% in 2007

(Re)-invented in the early ‘90

- All-in-one: Electronic Camera On Chip
- Standard CMOS technology
  - lower production cost significantly
  - simpler integration of complex functionalities
- Very small pixels (today ~1µm, 40M pixel)
- Single low-supply and much lower power consumption
- Increased speed (column- or pixel- parallel processing)

Source: Olympus (optical microscopy)

Source: IC Insights
Structure of a CIS Pixel

absorption depth (visible light):
10nm – 5μm

Source: Olympus

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The photodiode usually occupies 20-30% of the pixel surface ... the rest if occupied by the in-pixel electronics.

“integration time” = “exposure time”, time between two consecutive reset pulses

Today, more complex structures (5T, 6T, ...) are also commonly used.
Typical CMOS Image sensors supports column- or pixel-parallel readout

Rolling Shutter or Global shutter

Global Shutter

Rolling Shutter

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CMOS Image Sensors (CIS)

Industry’s first 3-layer Stacked CMOS Image Sensor with DRAM for Smartphones (*presented at ISSCC, Feb 2017*)

Advanced 3D assembly techniques make distinction between hybrid (separate sensor and readout chip) and monolithic more vague

Source: Sony
Detection of charged particles in CMOS APS

In a standard CMOS image sensor (in the early days) the photodiode is implanted in low-resistivity silicon.

Depletion region is shallow, charge collection efficiency is low.

Moreover the detector element covers only a small fraction of the pixel area.

... not suitable for the measurement of single charged particles.

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Detection of charged particles in CMOS APS

Use of an epitaxial layer with doping few order of magnitude smaller than one of the p++ substrate

Potential barriers exist at its boundaries

\[ V_1 = \frac{kT}{q} \ln \frac{N_{\text{sub}}}{N_{\text{epi}}} \]

\[ V_2 = \frac{kT}{q} \ln \frac{N_{\text{PWELL}}}{N_{\text{epi}}} \]

which keep minority carriers confined in the epi-layer ....

... till they reach the depleted region underneath the NWELL collection electrode
Detection of charged particles in CMOS APS

Doping of epitaxial layer few order of magnitude smaller than that of the p-well or the p++ substrate

Potential barriers exist at its boundaries

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Detection of charged particles in CMOS APS

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Back-thinning to reduce material budget

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The inception of CMOS MAPS for charged particle tracking

A monolithic active pixel sensor for charged particle tracking and imaging using standard VLSI CMOS technology


*LEPSI, IN2P3/ULP, 25 rue du Loess, BP20, F-67037 Strasbourg, France
**IRcc, IN2P3/ULP, 25 rue du Loess, BP20, F-67037 Strasbourg, France

In a standard CMOS image sensor the photo diode is integrated in low-resistivity silicon:

- Standard CMOS substrate
- Depletion region is shallow, charge collection efficiency is low

Moreover the detector element covers only a small fraction of the pixel area

Integration of a sensor in 0.6μm CMOS process
- Twin (P and N) tubs
- Implanted in lightly doped (P⁺) epitaxial silicon layer
- Grown on top of the highly doped (P⁺⁺) substrate

The charge collection diode is made of the junction between the NWELL and the P-type epitaxial layer

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p-type crystalline epitaxial layer hosts n-well charge collector

Signal is generated in a high-resistivity (> 1 kΩcm) epi-layer ~20µm thick (larger values possible)

Early versions with thin and low resistivity epi-layer

R&D mostly with AMS 0.6µm and 0.35µm technology

Only one transistor type in the active area (NMOS)

→ 2T or 3T in-pixel circuit
→ Rolling shutter architecture for matrix analogue readout

epi-layer not fully depleted

→ Charge collected (mostly) by diffusion and drift
→ Typical charge collection time < 100ns

Sensitive to radiation induced displacement damage in the epi layer → ok for applications with up to ~ $10^{12}$ 1MeV $N_{eq}/cm^2$
The INMAPS Process

“Monolithic Active Pixel Sensors (MAPS) in a Quadruple Well Technology for Nearly 100% Fill Factor and Full CMOS Pixel”

R. Turchetta et al., Sensors 2008, 8, 5336-5351; DOI: 10.3390/s8095336

Standard CMOS with additional deep P-well implant Quadruple well technology
100% efficiency and CMOS electronics in the pixel

New generation of CMOS APS for scientific applications with complex CMOS circuitry inside the pixel (TowerJazz CIS 180nm)

TPAC - for ILC ECAL (CALICE)
PIMMS – for TOF mass spectroscopy
CHERWELL – Calorimetry/Tracking
ALPIDE – Tracking

50µm pixel
70µm pixel
48 µm x 96 µm pixel
27 µm x 29 µm pixel
Owing to the industrial development of CMOS imaging sensors and the intensive R&D by HEP community ...

... several experiments have selected CMOS APS (STAR, ALICE, CBM, NICA MPD, sPHENIX, Mu3e)

... and now intensive R&D ongoing for HL-LHC (ATLAS) and LC

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First use of CMOS APS in HEP - STAR Pixel Detector

- Ladder with 10 MAPS sensors (~ 2x2 cm² each)
- 2 layers (2.8cm and 8cm radii)
- 10 sectors total (in 2 halves)
- 4 ladders/sector

Radiation length (1st layer): x/X₀ = 0.39% (Al conductor cable)

20 to 90 kRad / year
2*10¹¹ to 10¹² 1MeV n_eq/cm²

- Full detector Jan 2014
- Physics Runs in 2015-216

356 M pixels on ~0.16 m² of Silicon

courtesy of STAR Collaboration

courtesy of STAR Collaboration

courtesy of STAR Collaboration

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**First use of CMOS APS in HEP - STAR Pixel Detector**

Process: AMS 0.35µm twin-well CMOS (NMOS only in pixel array)

- **20 µm high-resistivity p-epi layer (~ 800 Ω cm)**
- **Matrix**
  - pixel size: 20.7 µm x 20.7 µm
  - 928 rows x 960 columns ~ 1M pixel
  - in-pixel circuit: 2T structure
  - **Correlated Double Sampling**

Periphery

- end-of-column discriminators and zero suppression
- ping-pong memory for frame readout (1500 word)
- 2 LVDS output @160 MHz
- 185.6 µs integration time
- ~160 mW/cm² power dissipation
Detection efficiency and fake hit rate

**ULTIMATE-2** - epi 20 µm - 30°C

Detection efficiency vs fake hit rate:
- Sensor works with high detection efficiency and marginal contamination by noise fluctuations (fake hits).

**Single point resolution**:
- MIMOSA-26: $\sigma_{sp} \sim 3\,\mu$m
- ULTIMATE: $\sigma_{sp} \sim 3.5\,\mu$m

**Threshold** (mV)

- 4, 5, 6, 7, 8, 9, 10, 11

**Efficiency (%)**

- 94, 95, 96, 97, 98, 99, 100

**Average fake hit rate/pixel/event**

- $10^{-8}, 10^{-7}, 10^{-6}, 10^{-5}, 10^{-4}, 10^{-3}, 10^{-2}, 10^{-1}$

**Spatial Resolution**

**Resolution vs Threshold**

- Single point resolution ~ 3.7 µm

ENC ≤ 15 e⁻ at 30-35 °C

**First use of CMOS APS in HEP - STAR Pixel Detector**

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New ALICE ITS: closer to IP, thinner, higher position resolution

Closer to IP: 39mm ➞ 22mm
Thinner: ~1.14% ➞ ~ 0.3% (for inner layers)
Smaller pixels: 50µm x 425µm ➞ 27µm x 29µm
Increase granularity: 20 chan/cm³ ➞ 2k pixel/cm³
Faster readout: x 10² Pb-Pb, x 10³ pp
10 m² active silicon: 12.5 G-pixels, σ ≈ 5µm

ALPIDE (ALICE Pixel Detector) - Developed for the ALICE upgrade (ITS and MFT)
will be used for several other HEP detectors and non HEP applications

1.5 ≤ η ≤ 1.5

NICA MPD (@JINR)  sPHENIX (BNL)  proton CT (tracking)  CSES – HEPD2 ...

L. Musa (CERN) – VCI, Vienna, Feb 2019

Talk of Władysław Henryk Trzaska, Tue
Talk of Naomi Van Der Kolk, Tue
CMOS Pixel Sensor using TJ 0.18µm CMOS Imaging Process

- High-resistivity (> 1kΩ cm) p-type epitaxial layer (25µm) on p-type substrate
- Small n-well diode (2 µm diameter), ~100 times smaller than pixel => low capacitance (~fF)
- Reverse bias voltage (-6V < V_{BB} < 0V) to substrate (contact from the top) to increase depletion zone around NWELL collection diode
- Deep PWELL shields NWELL of PMOS transistors

Pixel capacitance ≈ 5 fF (@ V_{bb} = -3 V)

- Q_{in} (MIP) ≈ 1300 e \Rightarrow V \approx 40 mV
1. Overview

- ALICE experiment will fully replace its present Inner Tracking System (ITS) during the second long shutdown of the LHC in 2019/2020.
- New ITS will be fully equipped with monolithic CMOS pixel sensors.
- Development of dedicated pixel chip for the ITS upgrade – ALPIDE.
  - Fabricated in TowerJazz 180nm CMOS Imaging Sensor (CIS) process.
  - Chip development started end 2011, including 4 MPWs and 5 engineering runs, containing various small and full-scale prototypes.
- One of them: INVESTIGATOR.

Inner Barrel

- 7 layers, grouped into two barrels.
- Radial coverage 22mm - 406mm.
- ~10m² active area, ~25000 chips.
- ~12.5 Gigapixels with binary readout.

Outer Barrel

- Ø M. Mager: The Upgrade of the ALICE Inner Tracking System with the Monolithic Active Pixel Sensor ALPIDE, Session N12: High energy physics instrumentaFon I: Silicon, Monday, Oct. 31, 18:00.

ALPIDE

- 1024 pixel columns.
- 512 rows.
- 50µm thick.
- 130,000 pixels / cm² 27x29x25 µm³.
- Charge collection time < 30ns (Vbb = -3V).
- Max particle rate: 100 MHz/cm².
- Fake-hit rate: < 1 Hz/cm².
- Power: ≈300 nW/pixel (<40mW/cm²).

Signal processing circuitry integrated in pixel matrix.
Asynchronous matrix readout.

Matrix Layout

Pixel Layout

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ALICE Pixel DEtector (ALPIDE)

Large operational margin with only 10 masked pixels (0.002%), fake-hit rate < 2 \times 10^{-11} \text{ pixel/event}

Non irradiated and TID/NIEL chips similar performance

5 μm resolution @ 200 e^- threshold
Chip-to-chip negligible fluctuations
ALICE Pixel DEtector (ALPIDE)

Inner Barrel is built at CERN

E. Musa (CERN) – VCI, Vienna, Feb 2019
ALICE Pixel Detector (ALPIDE)

Layers – 0, 1 and 2

Outer Barrel Stave (1.5m long)

Material budget distribution

Layer-4

Layer-6

102 Million pixel, average noise uniform ~ 5e

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A process modification for CMOS Active Pixel Sensors (side activity of ALICE R&D)

A possible solution to achieve full depletion of the sensitive layer combined with a low capacitance electrode is to implement a planar junction separate from the collection electrode.

The process modification requires a single additional process mask with no changes on the sensor and circuit layout.

For details on process modification and experimental results: W. Snoeys et al. NIM, A 871C (2017) pp. 90-96

The ALICE test vehicle chip (investigator) and prototype ALPIDE chips exist with both flavors.
Fully depleted MAPS – small electrodes with TJ modified process

Signal and cluster distribution from a $^{55}$Fe source for standard and modified process

Modified Process 1 = higher dose, Modified Process = lower dose

Tests performed on investigator chip (same pixel as ALPIDE)
Pixel size: 28 x 28 $\mu$m$^2$, CE: 2 x 2 $\mu$m$^2$ centered in a 8 x 8 $\mu$m$^2$ opening, P-well & substrate @ -6V, CE @ 1V

- For a lower dose (MP1) a no sensor capacitance penalty
- For modified process, larger fraction of single pixel clusters (see also fraction of signal within the peak in A)

Note: chip output buffer limits the rise time to 10ns

(A) Seed signal  |  (B) cluster signal
TJ modified process – charge collection time

$^{90}$Sr measurements on modified process samples (different setup, different pixel w.r.t. before)

- Non-irradiated
- $1 \times 10^{14}$ 1MeV $n_{\text{eq}}$/cm$^2$ (NIEL) and 100krad (TID)
- $1 \times 10^{15}$ 1MeV $n_{\text{eq}}$/cm$^2$ (NIEL) and 1Mrad (TID)

Tests performed on investigator chip (different pixel w.r.t ALPIDE)  

Note: chip output buffer limits the rise time to 10ns

Pixel size: 50 x 50 $\mu$m$^2$,  

CE: 3 x 3 $\mu$m$^2$ centered in a 18 x 18 $\mu$m$^2$ opening, 25$\mu$m epi
New developments for ATLAS ITk L4

Outermost layer of ITk Pixel Barrel

- 2016 quad modules
- 3m²

For 4000 fb⁻¹

- TID = 80 Mrad
- NIEL = 1.5 x 10¹⁵ nₑ𝑞/cm²

Monolithic CMOS sensors are considered as option for the outermost layer

- Saves bump bonding for 45% of outer barrel system
- Cost reduction and reduce module assembly time

Three developments on three technologies

- Large CE: AMS ⇔ TSI (ATLASPix)
- Large CE: LFOUNDRY (Monopix)
- Small electrode: TJ modified process (MALTA, Monopix)
New developments for ATLAS ITk: small electrode TJ modified process

Analogue front-end optimized for timing, based on ALPIDE

Design of two large scale demonstrators
Collaboration CERN - Bonn

TJ MALTA (2018)
20 x 22 mm²
Asynchronous matrix readout

TJ MonoPix (2018)
20 x 10 mm²
Column drain readout

MALTA: Monolithic Pixel Detector from ALICE to ATLAS

- The 512 x 512 pixel – 8 sectors
- Front-end is a development from the ALPIDE one
- Design based on low-power analogue front-end and an asynchronous architecture to readout the pixel matrix

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MALTA – efficiency in test beam before and after irradiation

Decreasing threshold from ~600 e⁻ to ~250e⁻ (unirradiated) / ~350e⁻ (irrad.)

Unirradiated:
lowering the threshold gives the full efficiency

Could not reach
Lower threshold
(RTS + Making issues)

New prototypes that fix both problems are currently under test

Neutron irradiated
5x 10^{14} n_{eq}/cm²

Inefficiency in pixel corners due to low lateral electric field
Malta – efficiency in test beam before and after irradiation

Modified process (mp) – “standard”

Mp + additional p-implant

Mp + gap in n-layer

TJ modified process: E field minimum at pixel corners => charges pushed to the minimum before they propagate to CE

Additional p-implant or gap in n-layers: bend the field towards the CR, shorted drift path

Magdalena Munker (CERN), Pixel 2018 (Taipei - Dec 2018)
HV CMOS – developments for the Mu3e tracker and ATLAS

- Compatible with standard CMOS technology
- Triple well process on p-type substrate (20-1000 Ω cm)
- Prototypes with var CMOS processes (AMS, TSI, LFounfry)

I. Peric et al., NIM A 582 (2007) 872

- The collection diode occupies a large part of the pixel
- Electronic circuits inside deep n-well
- HV O(60 – 120V) contacts at the top side
- MUPIX8 pixel: 80x81 μm²

- Circuitry in the collection diode introduces additional sensor capacitance
- Keep pixel circuitry as simple as possible
- Confine digital circuitry at the periphery

courtesy of I. Peric and A. Schoening
MUPIX8 - a full-scale HV-CMOS prototype for the Mu3e tracker

Time resolution with timewalk correction

\[ \sigma_{\text{time}} = 6.4 \text{ ns} \]

Efficiency and fake hit rate
courtesy of I. Peric and A. Schoening
INFN projects SEED and ARCADIA: two phases of the same development

The SEED project successfully demonstrated a fully depleted, up to 300 µm thick MAPS sensor

- LFoundry 110nm CMOS process.
- Sensor nodes are n-type implantation (become insulated only with full substrate depletion)
- The high resistivity, floating zone n-type substrate is depleted by negative voltage at the p+ backside
- Deep pwell implantations allows implementing full CMOS gates

- Double-sided lithography was used for the processing of the backside layers (5 extra masks)
- The backside p+ implantation was done after thinning the substrate, and activated with laser annealing
- To avoid early breakdown, termination structures with floating guard rings have been added at the borders

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Photolithographic process defines wafer reticles size ⇒ Typical field of view $O(2 \times 2 \text{ cm}^2)$

Reticle is stepped across the wafers to create multiple identical images of the circuit(s)

A stepping process called “stitching” allows building sensors of arbitrary size, the only limit being the size of the wafer.

- Reticle made of blocks
- Printing only individual blocks at each step with a tiny well-defined overlap

These days, stitching is widely applied in the digital imaging industry (e.g. large flat panels for medical and dental X-rays)
Medical imaging can be further improved moving to Medical Tracking

The pCT works on the same principle as a “standard” x-rays CT: recording particles passing through the target from different angles to reconstruct a 3D image. Main difference is that, while photons are simply absorbed, protons also scatter.

At least $10^9$ proton tracks (energy loss, exit point & angle, entry point) have to be recorded to provide a detailed enough image. This leads to long exposure time (10s minutes) with current state of the art: limited to R&D only.
Medical tracking requires sensors which still DO NOT EXIST

- Fast (> 10 MHz cm\(^{-2}\)) proton tracking at low power in silicon (50 mW cm\(^{-2}\))
- Monolithic, thinned (≤ 50 µm) and large area (> 16 cm\(^2\)) device to minimize proton scattering.
- **No support structure behind the silicon**
- **Cost effective**, reliable, simplified commissioning & operations, commercial process (for large production)
- **Low voltage** for real clinical usage

ALPIDE is an excellent starting point, currently used by many groups for medical R&D

ALPIDE used to take a demonstrative proton radiography of a pen: metal, different plastic densities, air distinguishable

**Talk of Ganesh Tambav, Thu**

raw data of a single projection (4.5 x 10\(^5\) hits)
Concluding Remarks

Large area, monolithic, low power pixel sensors are enabling devices for many cutting-edge research field and practical application: HEP trackers, medical imaging, space-borne instruments, FEL imagers, etc...

The HEP community is in an unique position to bridge between different fields and drive for sensors advancement, leveraging on the last decades experience and acquired know-how!
Concluding Remarks

The HEP community is in an **unique position** to bridge between different fields and drive for sensors advancement, leveraging on the last decades experience and acquired know-how!

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X-ray detection in a sensor with std process

For X-ray absorption in sensors fabricated with the std process, three cases can be defined:

1. Absorption in depleted volume: charge collected by drift, no charge sharing, single pixel cluster
   - These events populate the calibration peak in the signal histogram
   - Charge collection time expected to be $<1\text{ns}$

2. Absorption in non-depleted volume of the epitaxial layer: charge partially collected by diffusion and then drift, charge sharing depending on position of X-Ray absorption
   - Charge collection time expected to be dependent on distance of X-Ray absorption from the depleted volume, and longer than events of case 1.

3. Absorption in substrate
   - Contribution depending on depth of X-Ray absorption, and charge carrier lifetime within substrate

$^{55}\text{Fe}$: two X-Ray emission modes:
1. $\text{K-}\alpha$: 5.9keV (1640 e/h in Si), rel. freq.: 89.5%, attenuation length in Si: 29$\mu$m
2. $\text{K-}\beta$: 6.5keV (1800 e/h in Si), rel. freq.: 10.5%, attenuation length in Si: 37$\mu$m

J. Van Hoorne NSS 2016
TJ standard process – charge collection time and seed signal

Tests performed on investigator chip (same pixel as ALPIDE) with analogue readout

Pixel size: 28 x 28 $\mu m^2$, CE: 2 x 2 $\mu m^2$ centered in a 8 x 8 $\mu m^2$ opening, P-well & substrate @ -6V, CE @ 1V

$V_{BB} = -1V$  
$V_{BB} = -3V$  
$V_{BB} = -6V$

Signal:

Calibration (drift) peaks
Blank Wafers QA at TMEC (SRP and XSEM measurements)

Resistivity : ITS5 run, T608519.1-6A1, 25 um epi

![Graph showing resistivity measurements with depth and resistivity values.](https://example.com/graph.png)

**Depth [µm]**

- 0
- 5
- 10
- 15
- 20
- 25
- 30

**Resistivity [Ohm.cm]**

- $10^{-5}$
- $10^{-4}$
- $10^{-3}$
- $10^{-2}$
- $10^{-1}$
- $10^0$
- $10^1$
- $10^2$
- $10^3$
- $10^4$
- $10^5$

Spec : 25 (meas. 19.30)

- 25 (19.17)
- 25 (19.01)
- 25 (19.01)
- 25 (19.49)

1 kΩcm

**Wafer thickness 97.22µm**

**High-res epi: 25.28µm**

**Epi layer thickness : 25.28 µm**

**Wafer thickness : 92.06 µm**

**XSEM : thickness 5. ITS5 run,**

**Wafer T608519.1-6A1 : Right-23/5,**

25 um epi, 100 um thick

**ALICE CMOS Pixel Sensor**

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Current pulse signal

Magdalena Munker (CERN), Pixel 2018 (Taipei - Dec 2018)

Significantly faster charge collection for design with additional p-implant and gap in n-layer

New prototypes with both type of further process modifications are presently being tested