CMOS Active Pixel Sensors
for High Energy Physics

Luciano Musa

15TH VIENNA CONFERENCE
ON INSTRUMENTATION

Outline
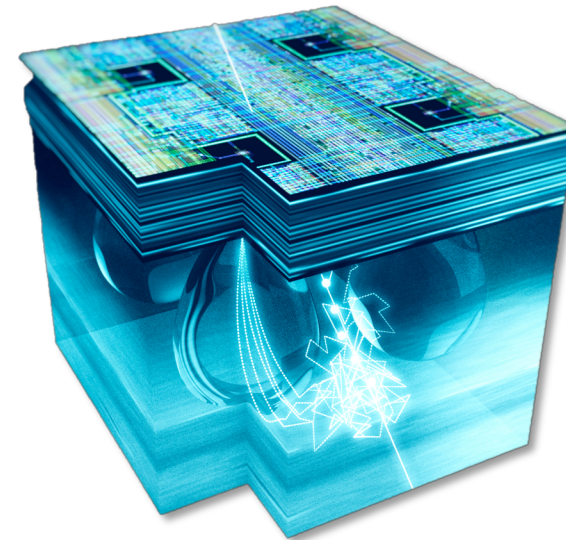
① **Prelude**

- Overview of CMOS Image Sensors

② **First use of CMOS pixel sensors in HEP**

- STAR Heavy Flavor Tracker
- ALICE Inner Tracking System

③ **Novel Developments**

- Fully depleted sensors, wafer-scale integration, back-side processing

④ **Some example of non HEP applications**

Digital imaging began with the invention of the Charge-Coupled Device (CCD) in 1969

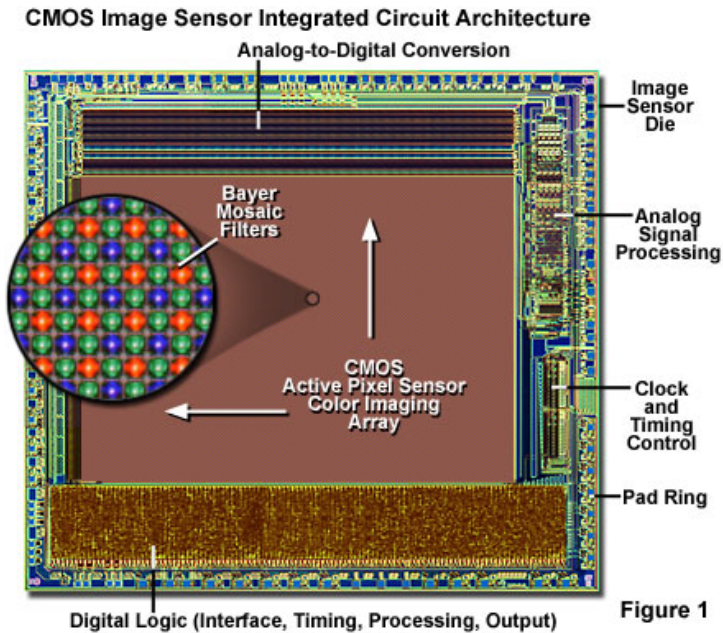Start of the the digital imaging revolution

Boyle and Smith's invention improved commercial and consumer products for decades and is one of the most important technological innovations of the past half-century

Since its inception, digital imaging has progressed through improvements in CCDs and with the emergence of Complementary Metal-Oxide Silicon (CMOS) Image Sensor technology

Since 10 years CMOS has become the leading imaging technology driving the second golden age …

Nobel Prize in Physics 2009
Willard S. Boyle and George E. Smith *"for the invention of an imaging semiconductor circuit - the CCD sensor."*

CMOS Image Sensor Integrated Circuit Architecture

Analog-to-Digital Conversion

Image Sensor Die

Bayer Mosaic Filters

Analog Signal Processing

CMOS Active Pixel Sensor Color Imaging Array

Clock and Timing Control

Pad Ring

Digital Logic (Interface, Timing, Processing, Output)

Figure 1

Source: Olympus (optical microscopy)

(Re)-invented in the early '90

- All-in-one: Electronic Camera On Chip
- Standard CMOS technology
    - ⇨ lower production cost significantly
    - ⇨ simpler integration of complex functionalities
- Very small pixels (today ~1µm, 40M pixel)
- Single low-supply and much lower power consumption
- Increased speed (column- or pixel- parallel processing)

camera phones, vehicles, machine vision, human recognition and security systems

⇨ drive CMOS image sensors development and sales

cellular camera phones account for 62% of the sales

90% of the total image sensor sales in 2017
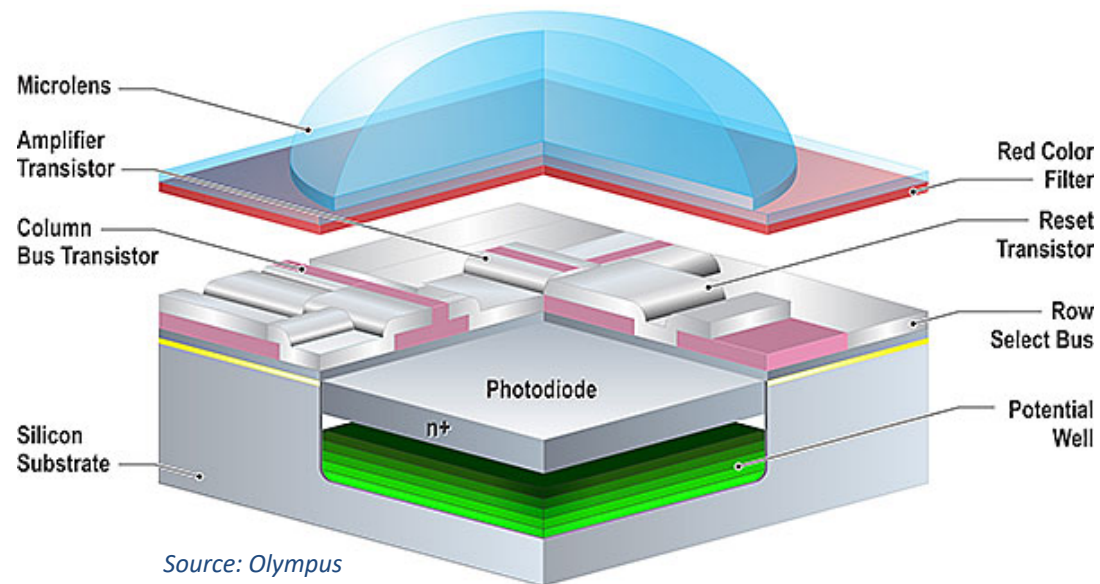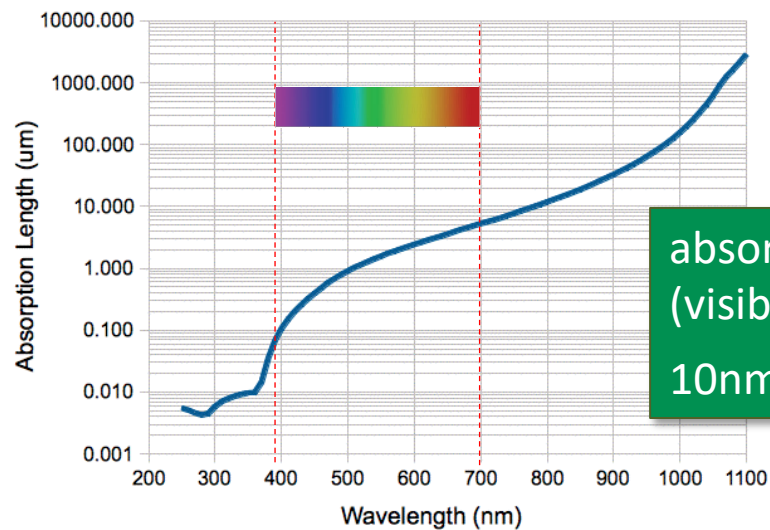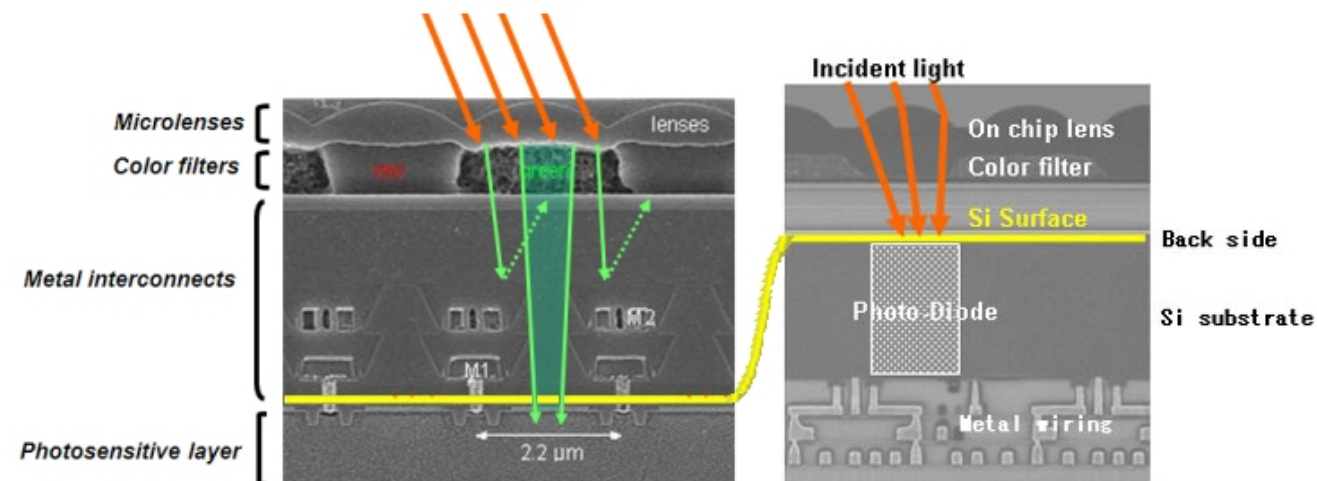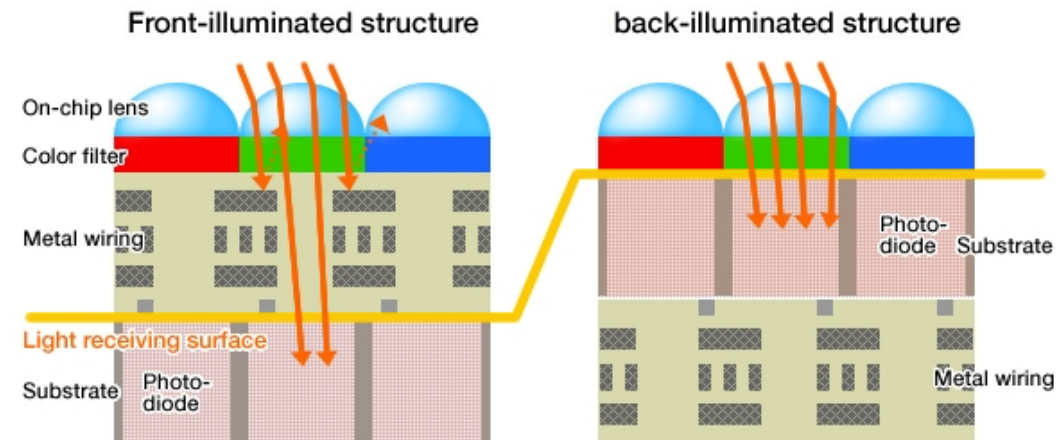it was 74% in 2012, 54% in 2007

CMOS Image Sensor Sales March Higher into Next Decade

Sales ($B)   Units (B)

2012-2017 CAGRs
Sales = 11.9% Units = 17.9%
2017-2022F CAGRs
Sales = 8.8% Units = 11.7%

$4.0 $7.1 $10.5 $12.5 $13.7 $19.0

Worldwide Market ($B)
Worldwide Unit Shipments (B)

07 08 09 10 11 12 13 14 15 16 17 18F 19F 20F 21F 22F
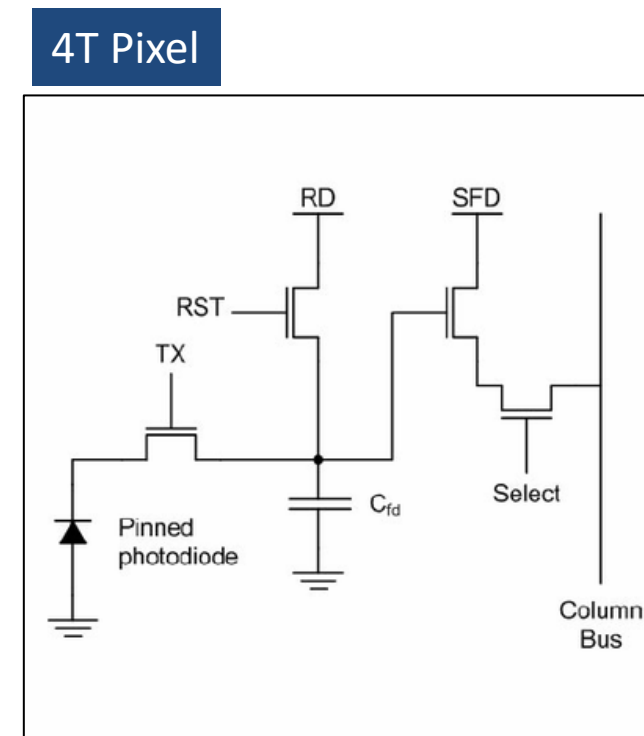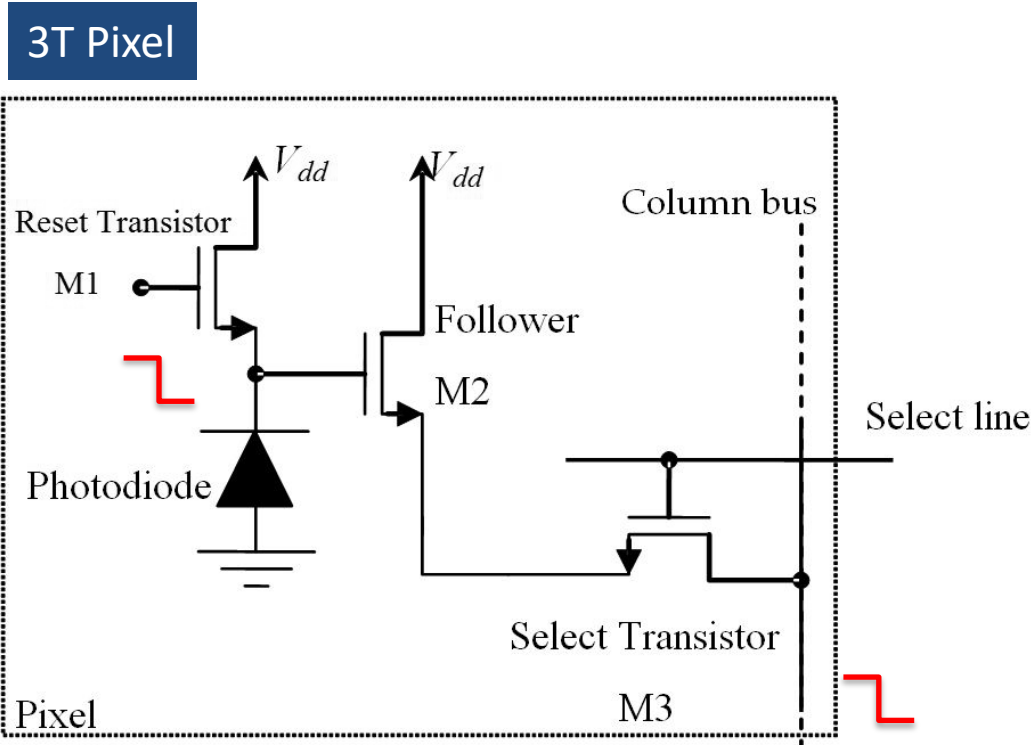
Source: IC Insights

Source: Olympus

absorption depth (visible light):

10nm – 5µm

The photodiode usually occupies 20-30% of the pixel surface … the rest if occupied by the in-pixel electronics
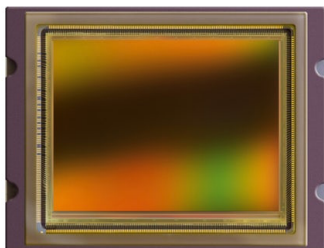
3T Pixel

4T Pixel

"integration time" = "exposure time", time between two consecutive reset pulses

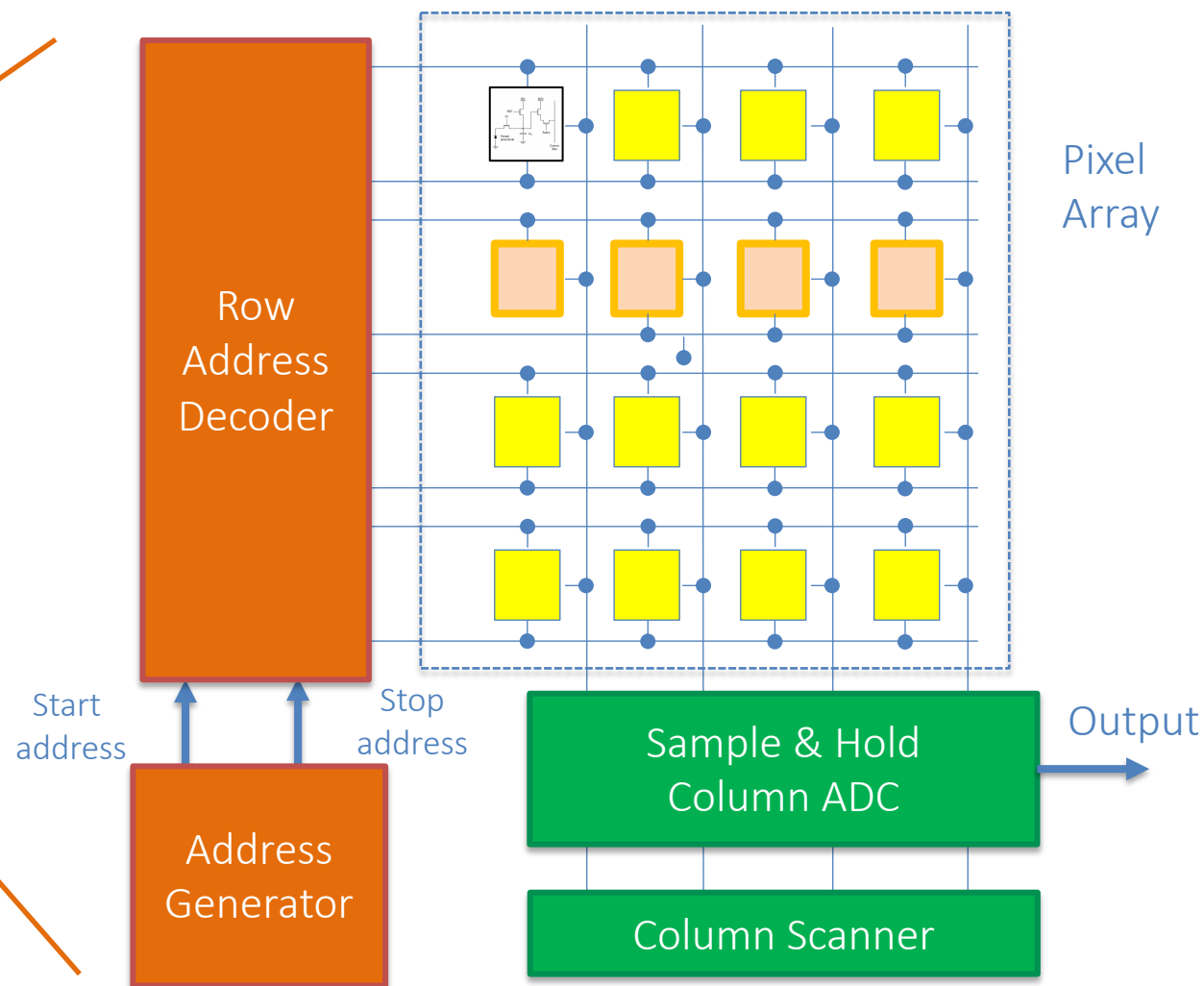Today, more complex structures (5T, 6T, …) are also commonly used

Rolling Shutter or Global shutter

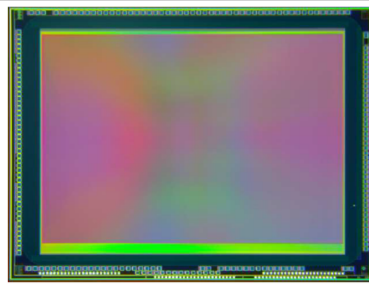Typical CMOS Image sensors supports column- or pixel-parallel readout

Pixel Array

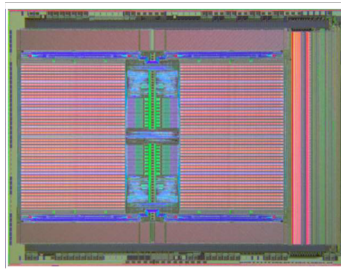Row Address Decoder

Start address

Stop address

Address Generator

Sample & Hold Column ADC

Output

Column Scanner

Global Shutter

Rolling Shutter

L. Musa (CERN) – VCI, Vienna, Feb 2019

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Industry's first 3-layer Stacked CMOS Image Sensor with DRAM for Smartphones *(presented at ISSCC, Feb 2017)*

Pixel array
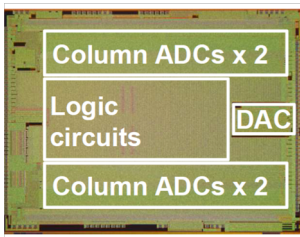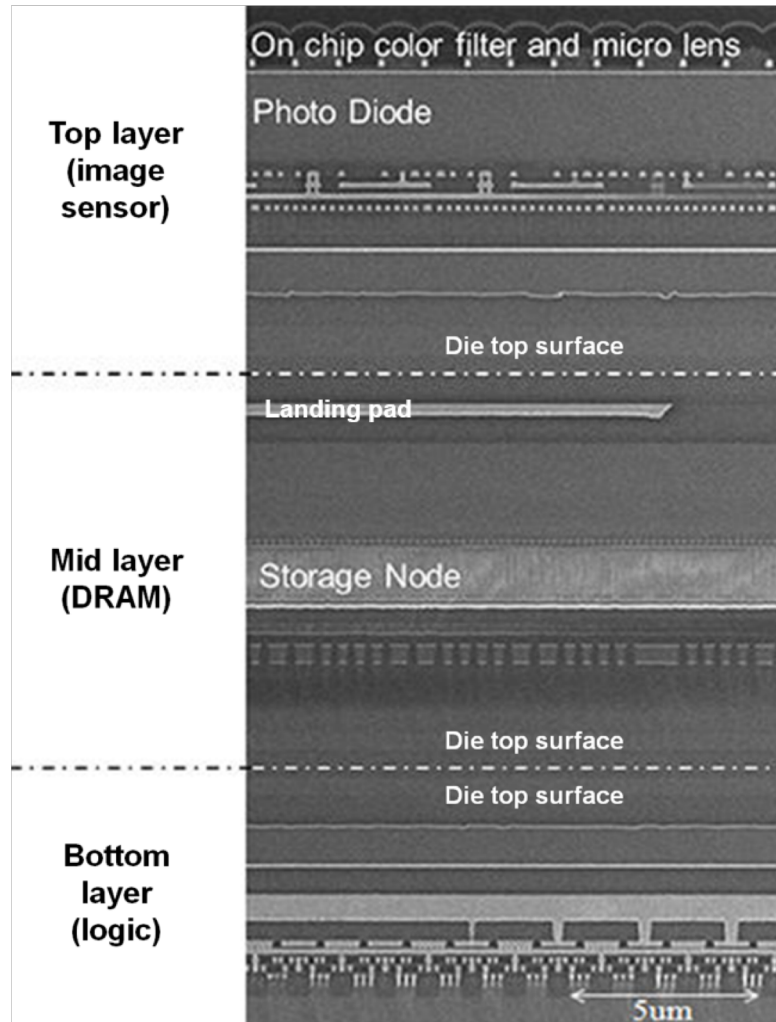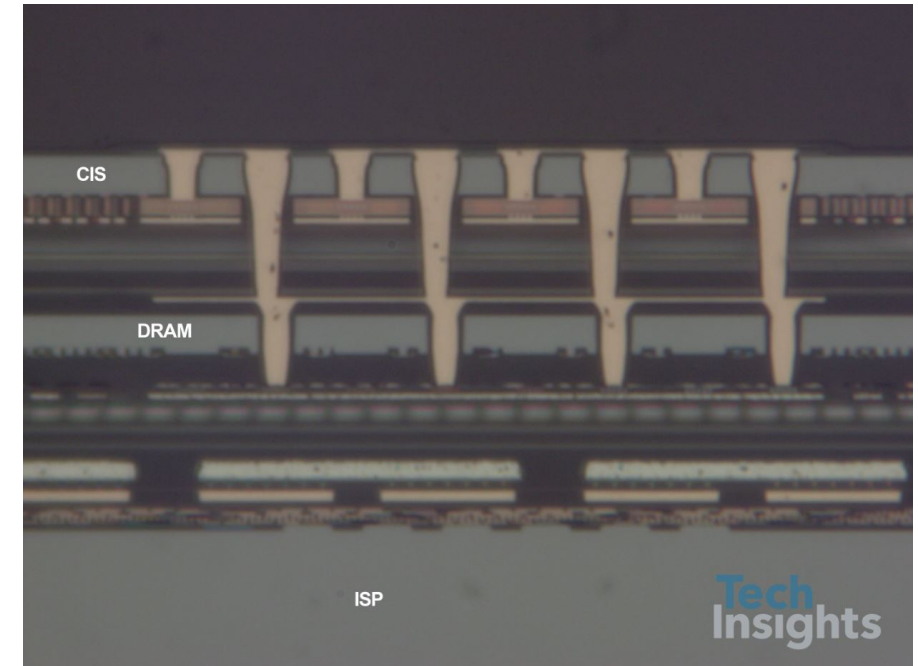
DRAM + row drivers

Source: Sony/ISSCC

Image processor

Column ADCs x 2

Logic circuits   DAC

Column ADCs x 2

On chip color filter and micro lens

Top layer (image sensor)

Photo Diode

Die top surface

Landing pad

Mid layer (DRAM)

Storage Node

Die top surface

Die top surface

Bottom layer (logic)

5um

Source: Sony
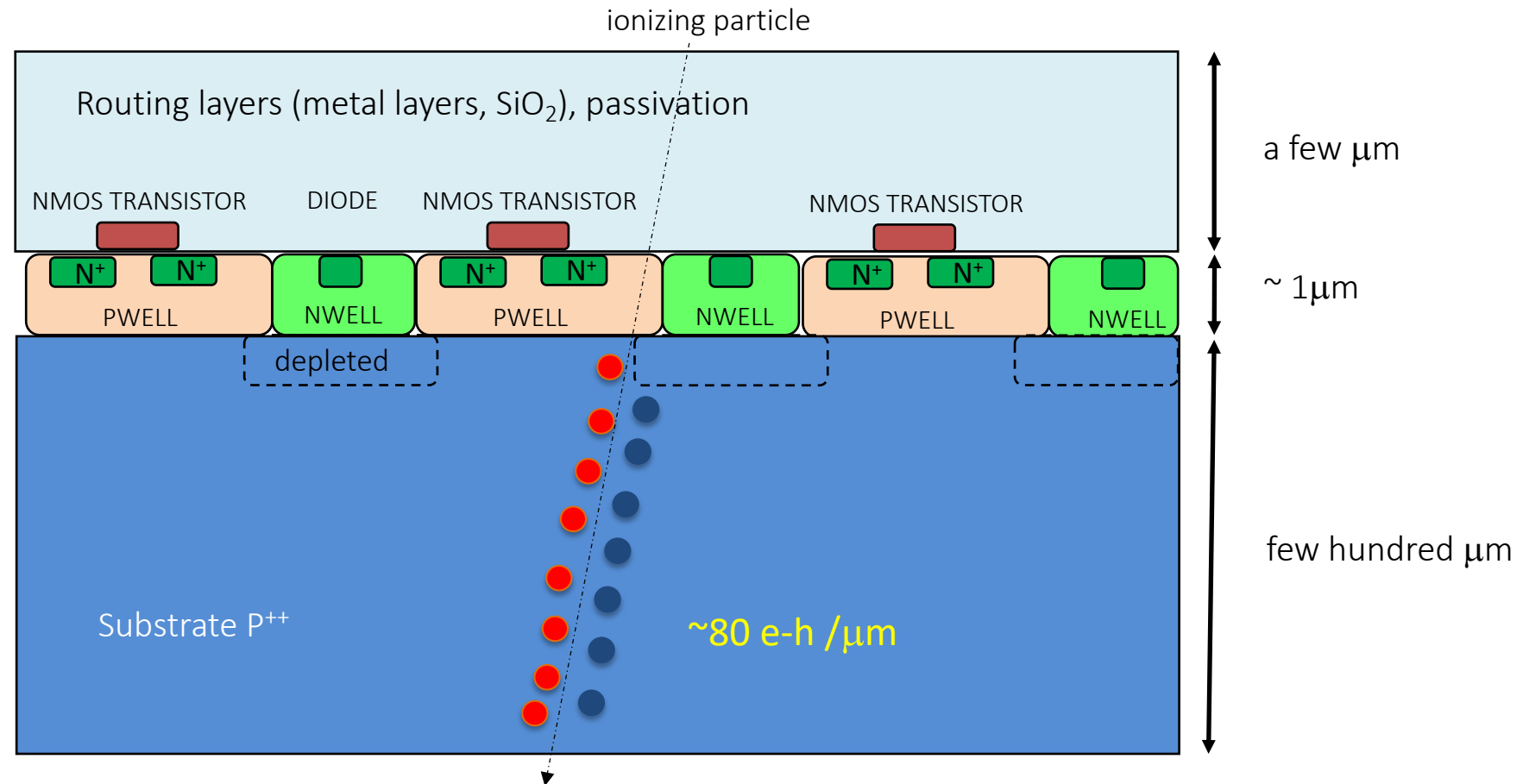
CIS

DRAM

ISP

Tech Insights

Advanced 3D assembly techniques make distinction between hybrid (separate sensor and readout chip) and monolithic more vague

In a standard CMOS image sensor (in the early days) the photodiode is implanted in low-resistivity silicon

Depletion region is shallow, charge collection efficiency is low

Moreover the detector element covers only a small fraction of the pixel area

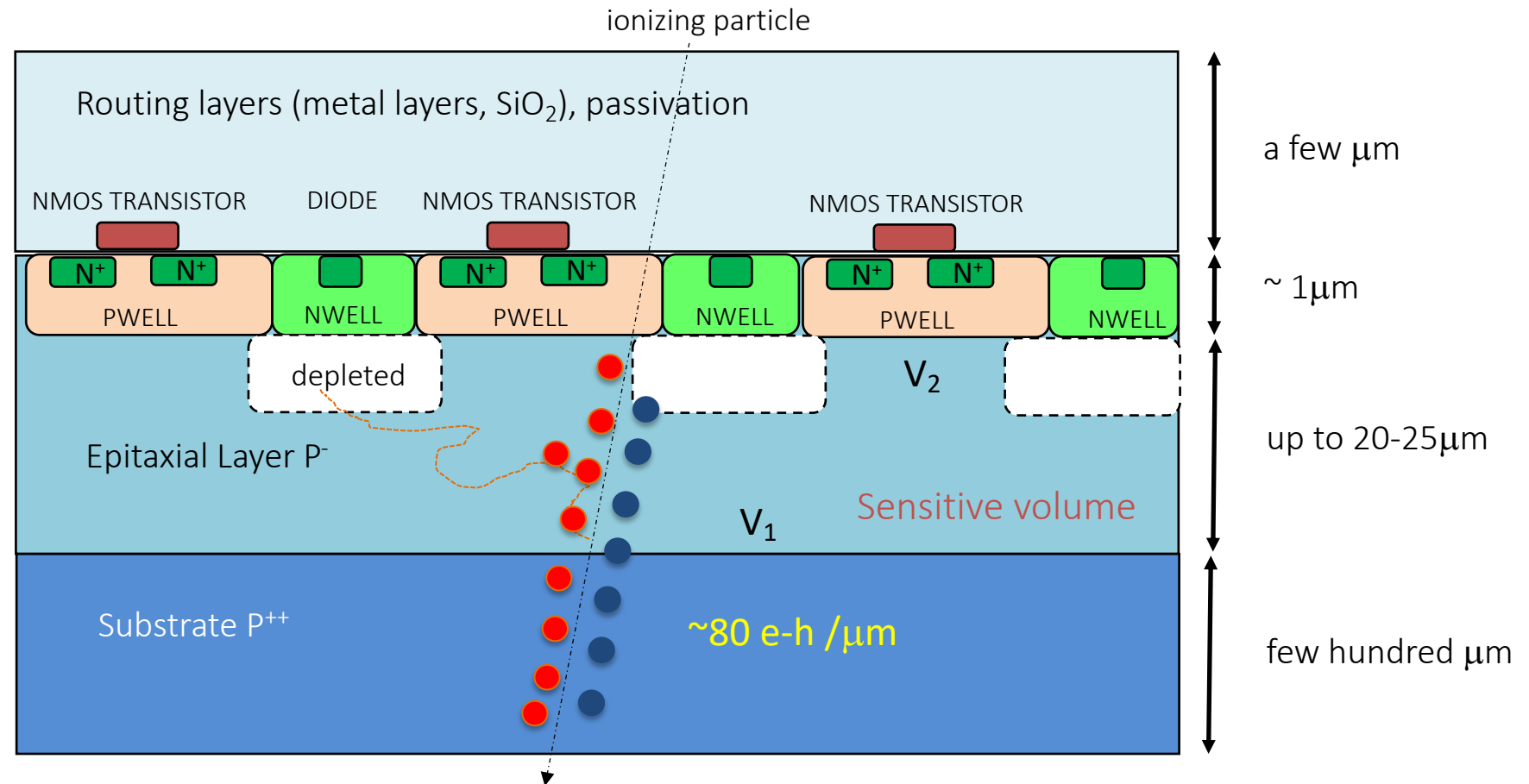... not suitable for the measurement of single charged particles

ionizing particle

Routing layers (metal layers, SiO_2), passivation

a few μm

NMOS TRANSISTOR   DIODE   NMOS TRANSISTOR   NMOS TRANSISTOR

N^+ N^+ N^+ N^+ N^+ N^+

PWELL   NWELL   PWELL   NWELL   PWELL   NWELL

~ 1μm
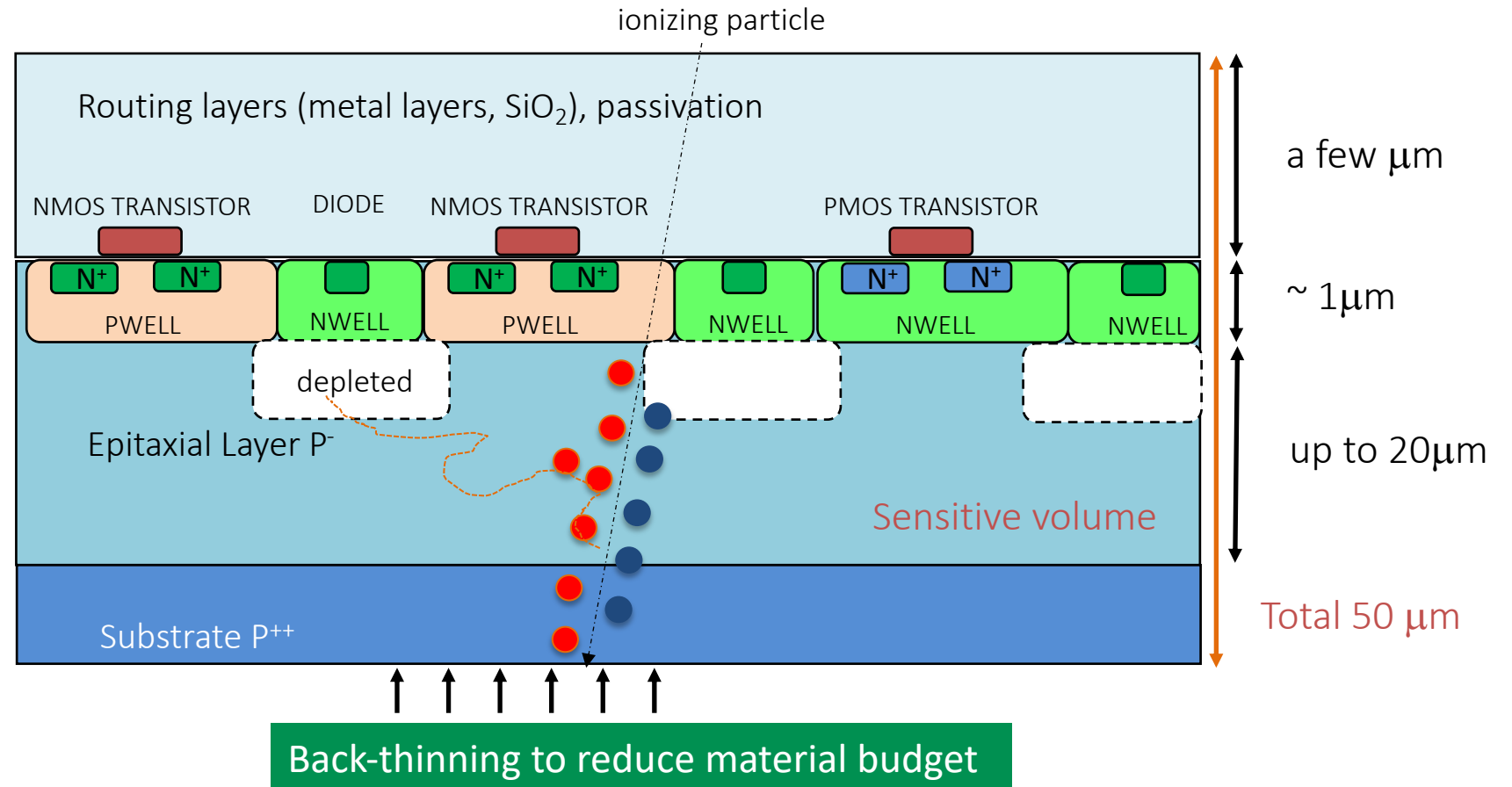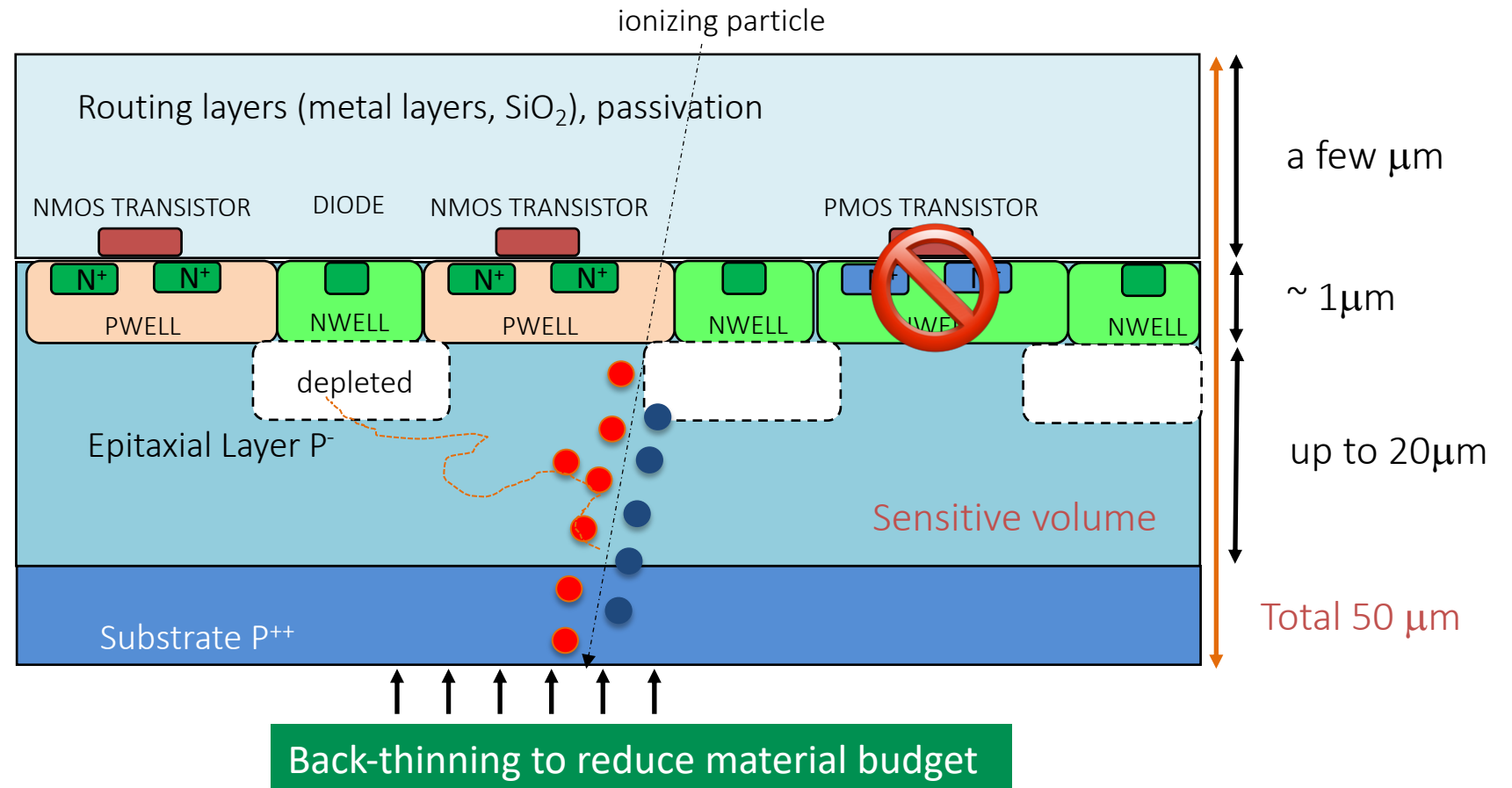
depleted

Substrate P^{++}

~80 e-h /μm

few hundred μm

Use of an epitaxial layer with doping few order of magnitude smaller than one of the p++ substrate

Potential barriers exist at its boundaries

$$V_1 = \frac{kT}{q} ln \frac{N_{sub}}{N_{epi}}$$

$$V_2 = \frac{kT}{q} ln \frac{N_{PWELL}}{N_{epi}}$$

which keep minority carriers confined in the epi-layer ....

ionizing particle

Routing layers (metal layers, SiO$_2$), passivation

a few μm

NMOS TRANSISTOR   DIODE   NMOS TRANSISTOR   NMOS TRANSISTOR

N$^+$ N$^+$ N$^+$ N$^+$ N$^+$ N$^+$

PWELL   NWELL   PWELL   NWELL   PWELL   NWELL

~ 1μm

depleted   V$_2$

Epitaxial Layer P$^-$ Sensitive volume   V$_1$

up to 20-25μm

Substrate P^{++} ~80 e-h /μm

few hundred μm

... till they reach the depleted region underneath the NWELL collection electrode

Doping of epitaxial layer few order of magnitude smaller than that of the p-well or the p++ substrate

Potential barriers exist at its boundaries

$$V_1 = \frac{kT}{q} \ln \frac{N_{sub}}{N_{epi}}$$

$$V_2 = \frac{kT}{q} \ln \frac{N_{PWELL}}{N_{epi}}$$

which keep minority carriers confined in the epi-layer ....

ionizing particle

Routing layers (metal layers, SiO$_2$), passivation — a few μm

NMOS TRANSISTOR   DIODE   NMOS TRANSISTOR   PMOS TRANSISTOR

N$^+$ N$^+$ PWELL   NWELL   N$^+$ N$^+$ PWELL   NWELL   N$^+$ N$^+$ NWELL   NWELL — ~ 1μm

depleted

Epitaxial Layer P$^-$

Sensitive volume — up to 20μm

Substrate P^{++} — Total 50 μm

Back-thinning to reduce material budget

... till they reach the depleted region underneath the NWELL collection electrode

Doping of epitaxial layer few order of magnitude smaller than that of the p-well or the p++ substrate

Potential barriers exist at its boundaries

$$V_1 = \frac{kT}{q} \ln \frac{N_{sub}}{N_{epi}}$$

$$V_2 = \frac{kT}{q} \ln \frac{N_{PWELL}}{N_{epi}}$$

which keep minority carriers confined in the epi-layer ....

ionizing particle

Routing layers (metal layers, SiO$_2$), passivation

a few µm

NMOS TRANSISTOR   DIODE   NMOS TRANSISTOR   PMOS TRANSISTOR

N$^+$ N$^+$ N$^+$ N$^+$

PWELL   NWELL   PWELL   NWELL   NWELL   NWELL

~ 1µm

depleted

Epitaxial Layer P$^-$

up to 20µm

Sensitive volume

Substrate P^{++}

Total 50 µm

Back-thinning to reduce material budget

... till they reach the depleted region underneath the NWELL collection electrode

A monolithic active pixel sensor for charged particle tracking and imaging using standard VLSI CMOS technology

R. Turchetta[a,*], J.D. Berst[a], B. Casadei[a], G. Claus[a], C. Colledani[a], W. Dulinski[a], Y. Hu[a], D. Husson[a], J.P. Le Normand[a], J.L. Riester[a], G. Deptuch[b,1], U. Goerlach[b], S. Higueret[b], M. Winter[b]

[a]LEPSI, IN2P3/ULP, 23 rue du Loess, BP20, F-67037 Strasbourg, France
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In a standard CMOS image sensor the photo diode is integrated in low-resistivity silicon:

⇨ Standard CMOS substrate

⇨ Depletion region is shallow, charge collection efficiency is low

Moreover the detector element covers only a small fraction of the pixel area
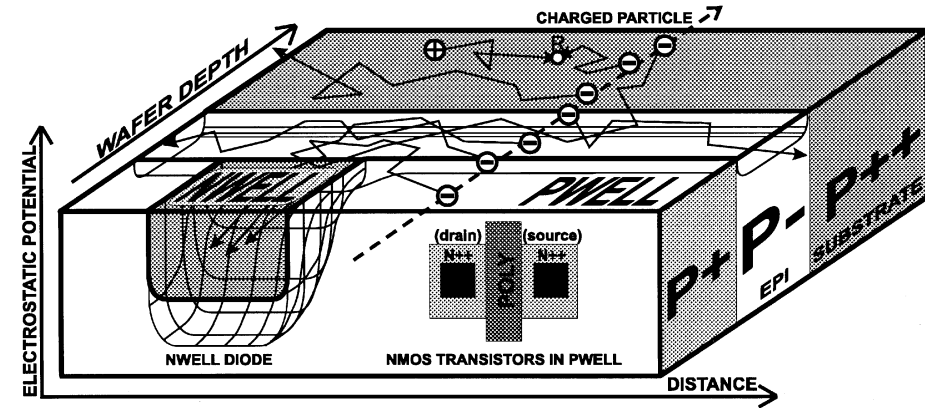
Integration of a sensor in 0.6μm CMOS process
- Twin (P and N) tubs
- Implanted in lightly doped (P⁻) epitaxial silicon layer
- Grown on top of the highly doped (P⁺⁺) substrate

The charge collection diode is made of the junction between the NWELL and the P-type epitaxial layer

p-type crystalline epitaxial layer hosts n-well charge collector

Signal is generated in a high-resistivity (> 1 kΩcm) epi-layer ~20μm thick (larger values possible)

Early versions with thin and low resistivity epi-layer

R&D mostly with AMS 0.6μm and 0.35μm technology

Only one transistor type in the active area (NMOS)

⇨ 2T or 3T in-pixel circuit

⇨ Rolling shutter architecture for matrix analogue readout

epi-layer not fully depleted

⇨ Charge collected (mostly) by diffusion and drift

⇨ Typical charge collection time < 100ns

Sensitive to radiation induced displacement damage in the epi layer ⇨ ok for applications with up to ~ 10^{12} 1MeV N_{eq}/cm^2

Rolling Shutter Architecture

rolling shutter

SUZE (Zero Suppression and Encoding)

The INMAPS Process
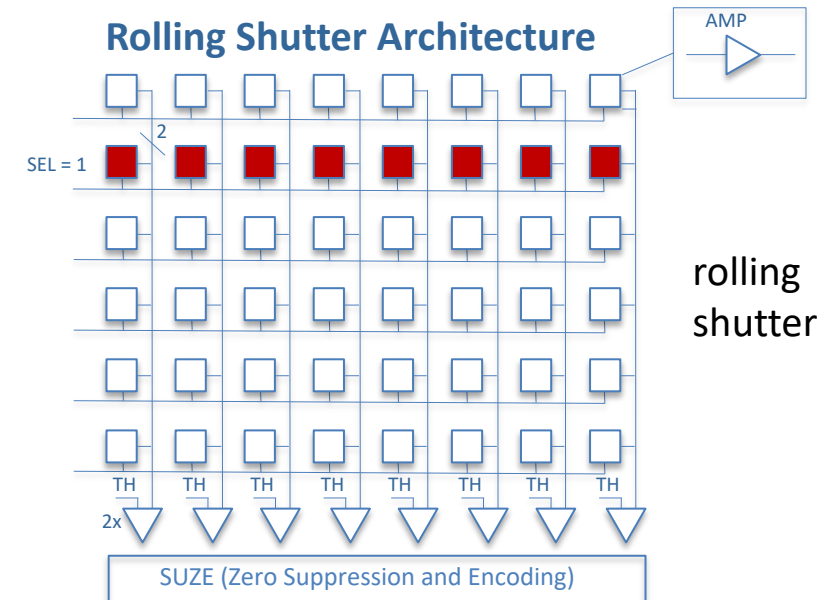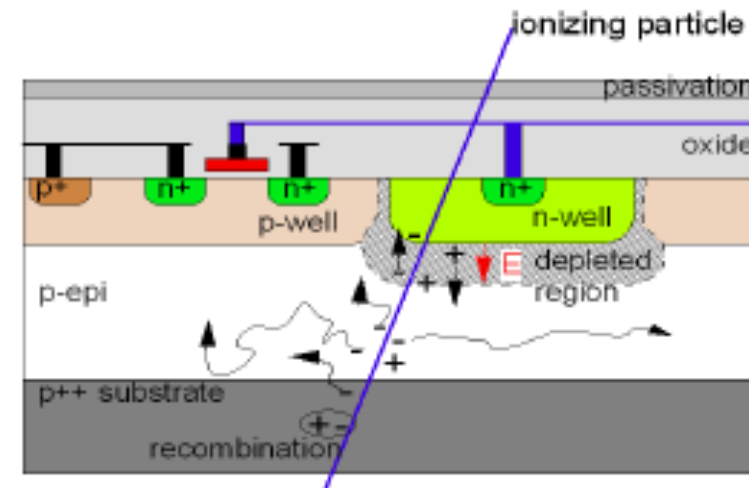
"Monolithic Active Pixel Sensors (MAPS) in a Quadruple Well Technology for Nearly 100% Fill Factor and Full CMOS Pixel"

R. Turchetta et al. , Sensors 2008, 8, 5336-5351; DOI: 10.3390/s8095336

Standard CMOS with additional deep P-well implant Quadruple well technology

100% efficiency and CMOS electronics in the pixel
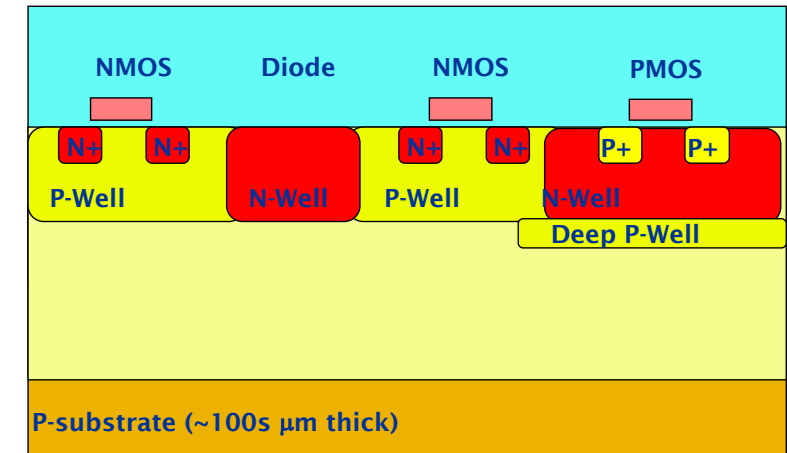
New generation of CMOS APS for scientific applications with complex CMOS circuitry inside the pixel (TowerJazz CIS 180nm)

TPAC - for ILC ECAL (CALICE)
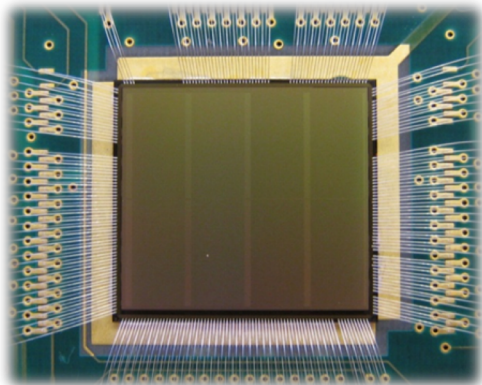
50μm pixel

PIMMS – for TOF mass spectroscopy
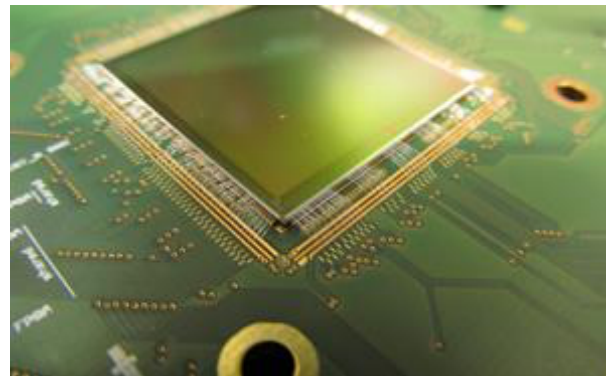
70μm pixel

CHERWELL – Calorimetry/Tracking
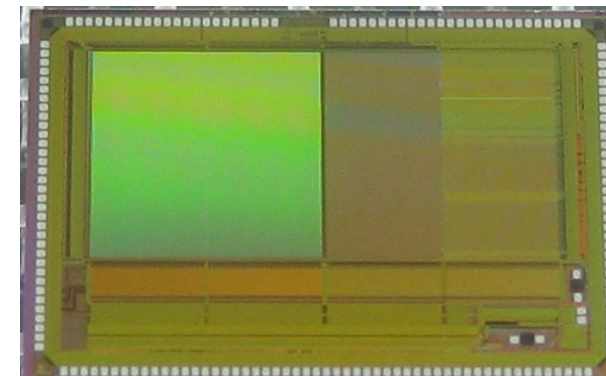
48 μm x 96 μm pixel

ALPIDE – Tracking

27 μm x 29 μm pixel

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Owing to the industrial development of CMOS imaging sensors and the intensive R&D by HEP community ...

Mimosa-1

Mimosa-2

Mimosa-3

...

Mimosa-26
2.7 cm^2
(EUDET Telescope)

Cherwell

ALPIDE
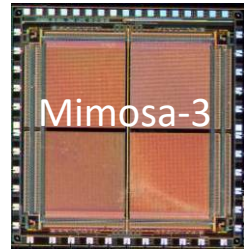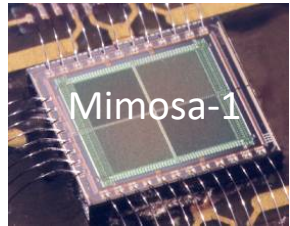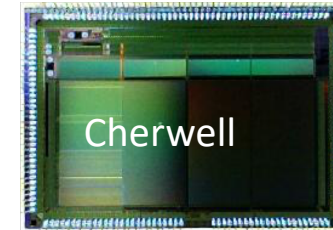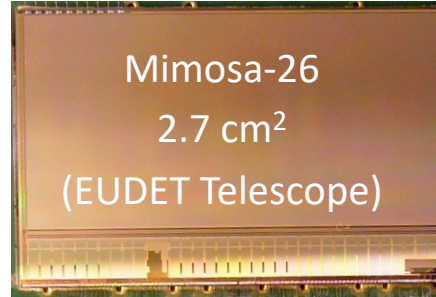
... several experiments have selected CMOS APS (STAR, ALICE, CBM, NICA MPD, sPHENIX, Mu3e)

... and now intensive R&D ongoing for HL-LHC (ATLAS) and LC

2014 - First CPS Detector
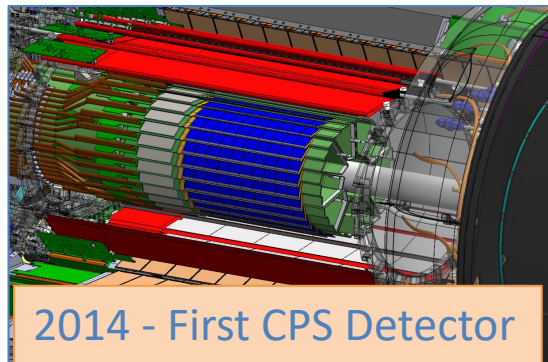
STAR HFT
0.16 m^2 – 356 M pixels
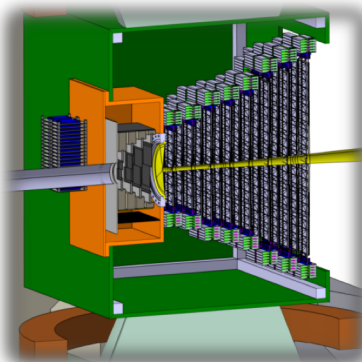
CBM MVD
0.08 m^2 – 146 M pixel
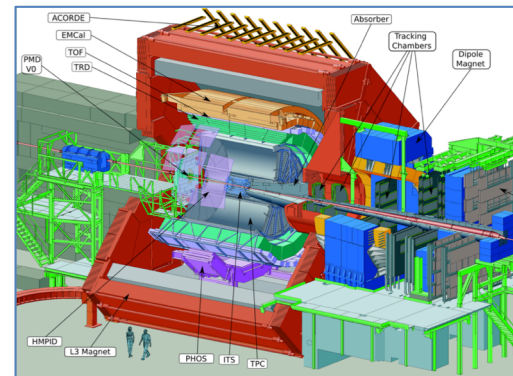
ALICE ITS Upgrade (and MFT)
10 m^2 – 12 G pixel
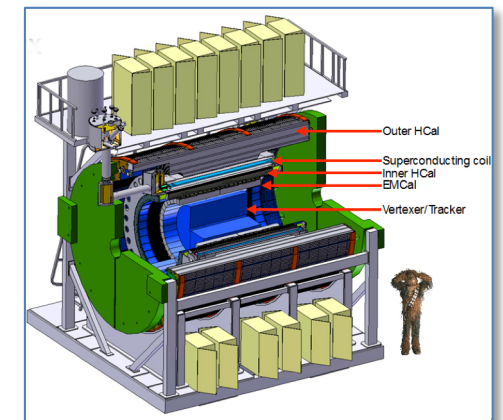
sPHENIX
0.2 m^2 – 251 M pixel
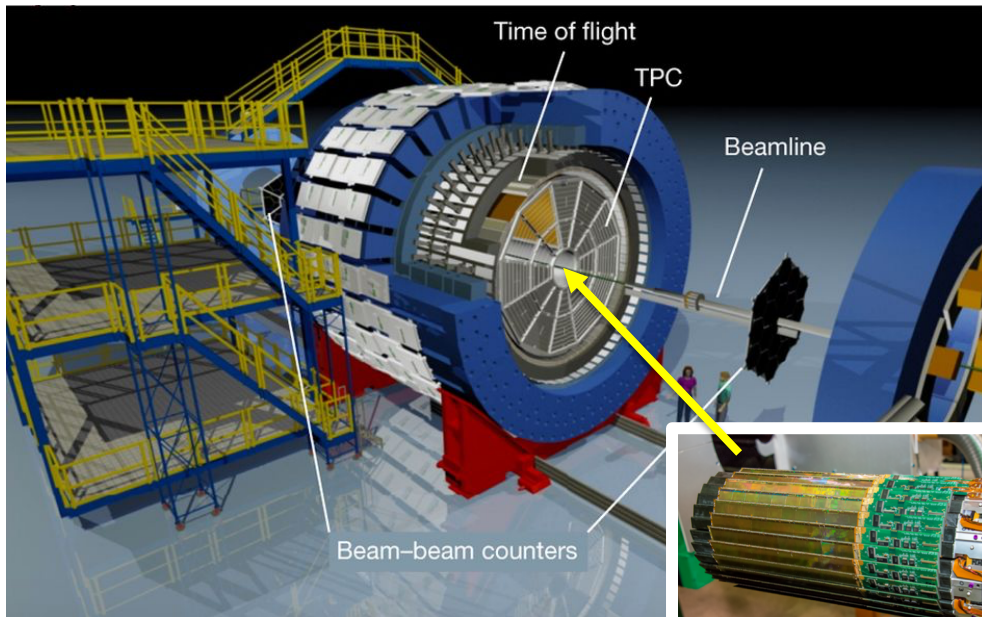
356 M pixels on ~0.16 m² of Silicon

- Full detector Jan 2014
- Physics Runs in 2015-216

- 2 layers (2.8cm and 8cm radii)
- 10 sectors total (in 2 halves)
- 4 ladders/sector

20 to 90 kRad / year
$2*10^{11}$ to 10^{12} 1MeV n_{eq}/cm^2

Ladder with 10 MAPS sensors (~ 2×2 cm² each)

courtesy of STAR Collaboration

2-layer kapton flex cable with Al traces
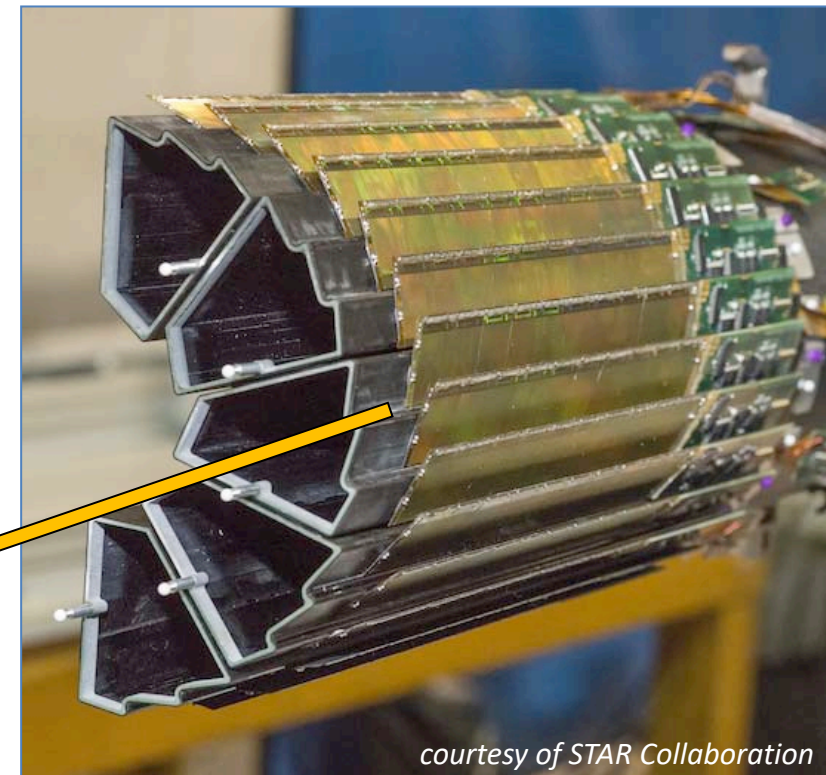
courtesy of STAR Collaboration

Radiation length (1st layer):
$x/X_0 = 0.39\%$ (Al conductor cable)

Process: AMS 0.35μm twin-well CMOS
(NMOS only in pixel array)

courtesy of PICSEL group (IPHC)

Rolling Shutter Architecture

SUZE (Zero Suppression and Encoding)

ULTIMATE (MIMOSA 28)

22.710 mm

3.280 mm

22.240 mm
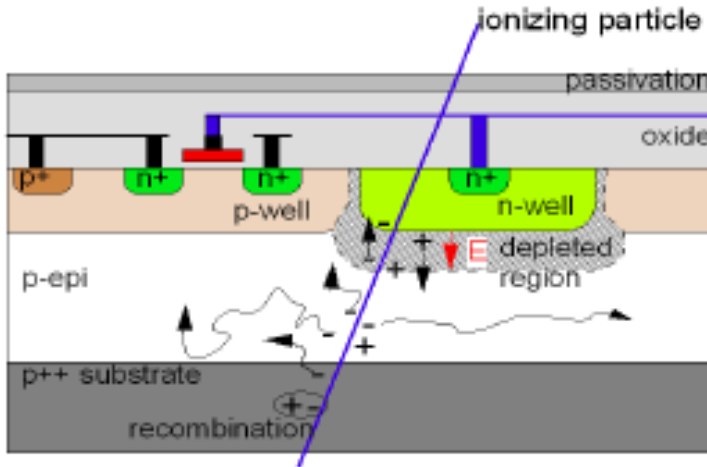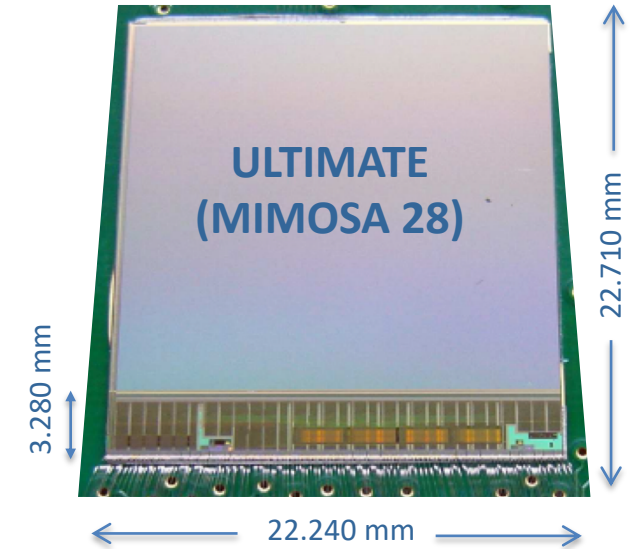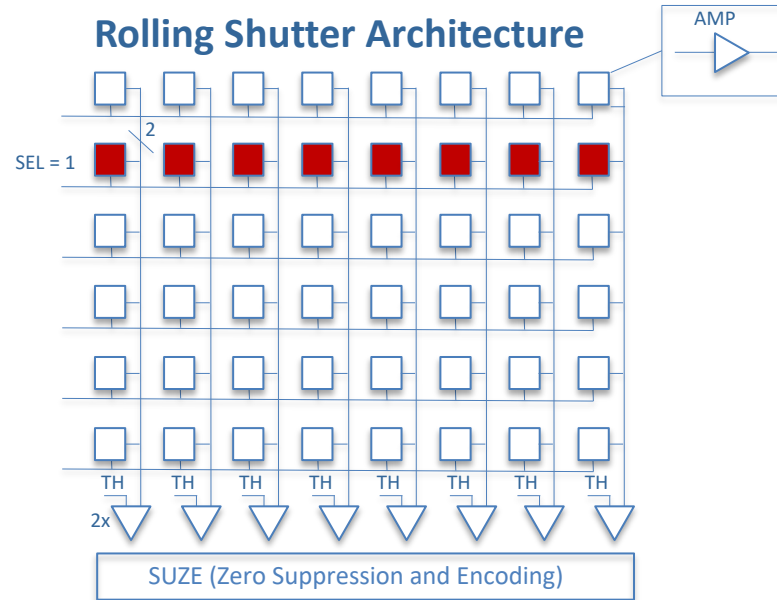
courtesy of PICSEL group (IPHC)

20 μm high-resistivity p-epi layer (~ 800 Ω cm)

Matrix

- pixel size: 20.7 μm x 20.7 μm
- 928 rows x 960 columns ~ 1M pixel
- in-pixel circuit: 2T structure
- Correlated Double Sampling

Periphery

- end-of-column discriminators and zero suppression
- ping-pong memory for frame readout (1500 word)
- 2 LVDS output @160 MHz
- 185.6 μs integration time
- ~160 mW/cm^2 power dissipation

Detection efficiency and fake hit rate
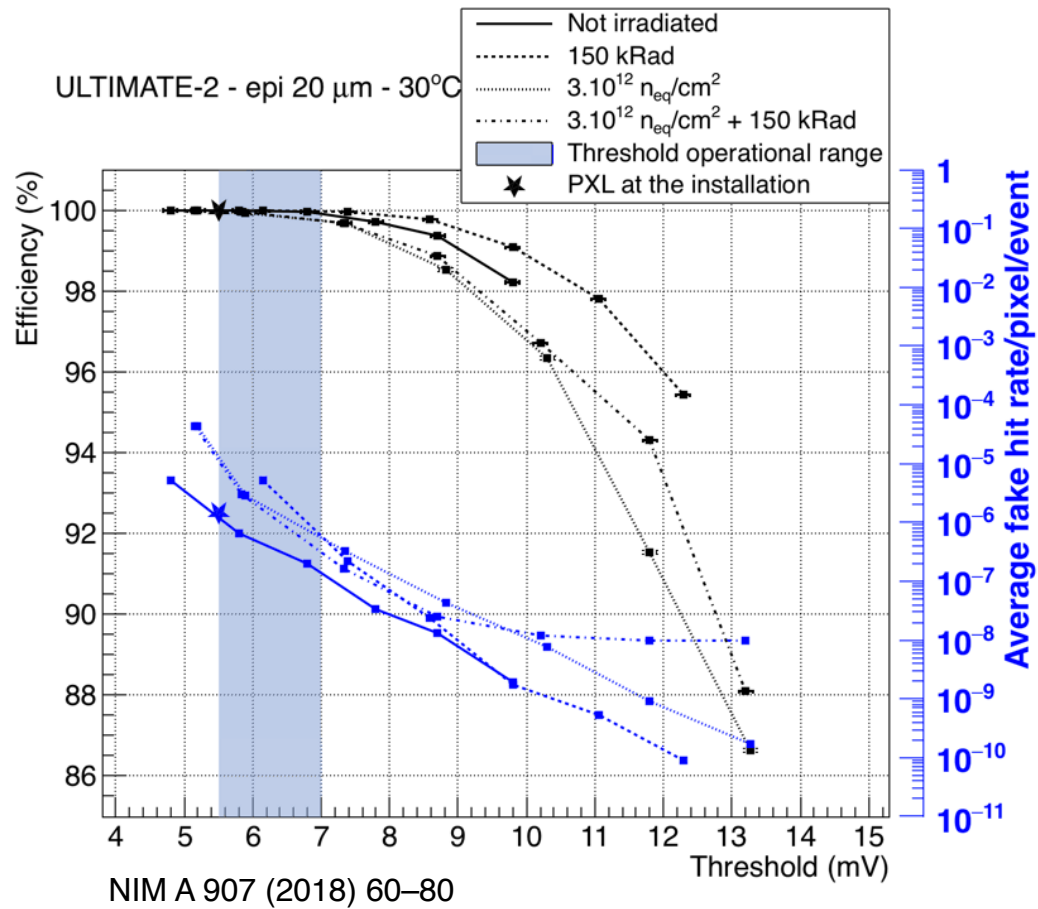
ENC $\leq$ 15 e$^-$ at 30-35 ^{o}C

Spatial Resolution
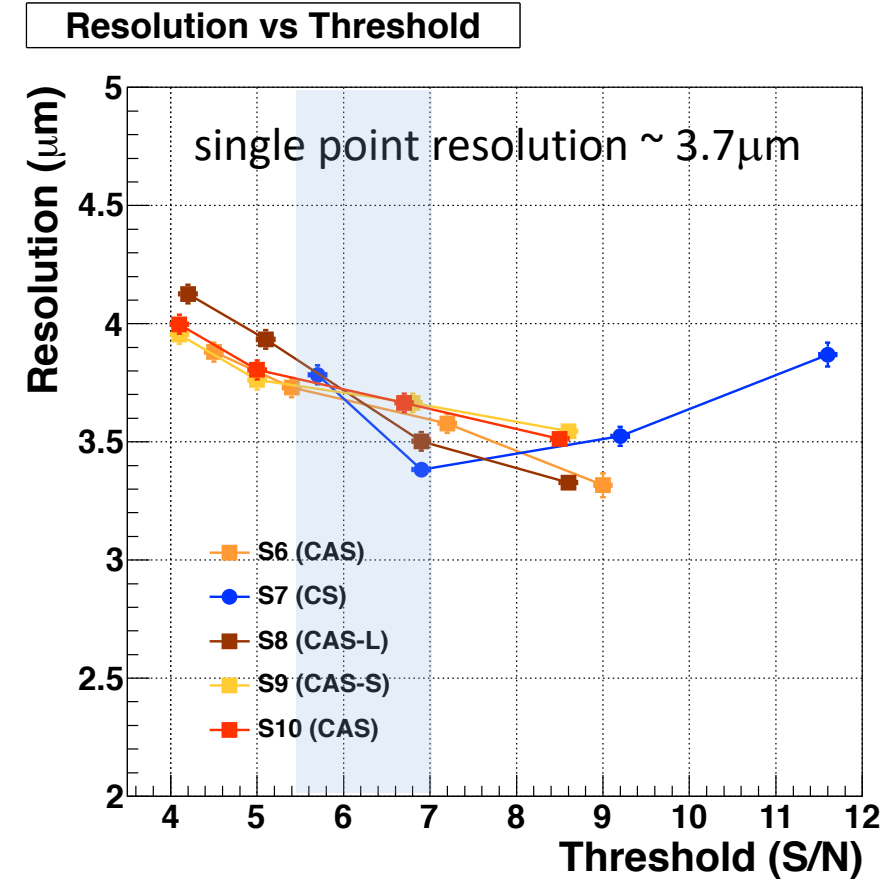
Single point resolution $\approx$ 3.7μm

Beam pipe

40cm

Inner Barrel

Outer Barrel

147 cm
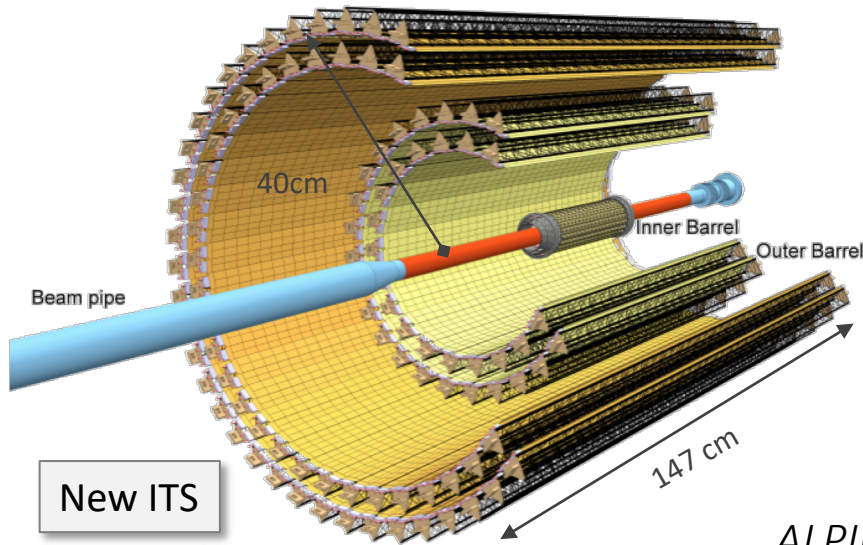
New ITS

$1.5 \leq \eta \leq 1.5$

Closer to IP:	39mm ➡ 22mm
Thinner:	~1.14% ➡ ~ 0.3% (for inner layers)
Smaller pixels:	50μm x 425μm ➡ 27μm x 29μm
Increase granularity:	20 chan/cm^3 ➡ 2k pixel/cm^3
Faster readout:	x 10^2 Pb-Pb, x 10^3 pp
10 m^2 active silicon:	12.5 G-pixels, σ ≈ 5μm

ALPIDE (ALICE Pixel Detector) - Developed for the ALICE upgrade (ITS and MFT)

will be used for several other HEP detectors and non HEP applications

NICA MPD (@JINR)
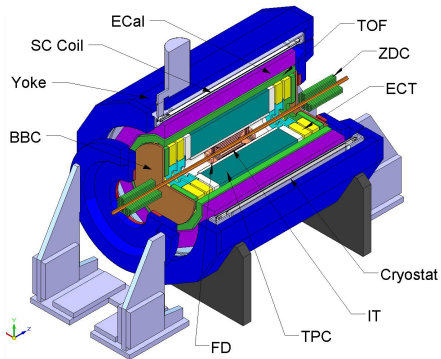
sPHENIX (BNL)
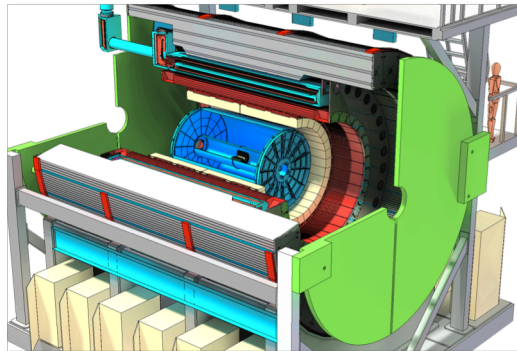
proton CT (tracking)

CSES – HEPD2 ...

Talk of Wladyslaw Henryk Trzaska, Tue

Talk of Naomi Van Der Kolk, Tue
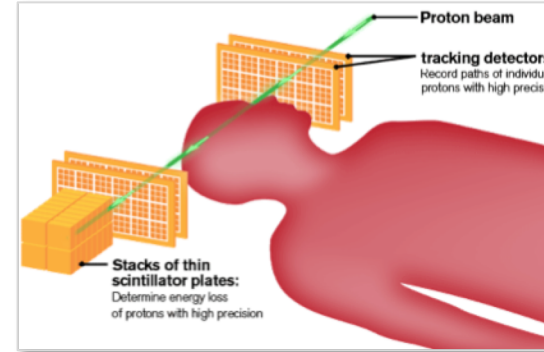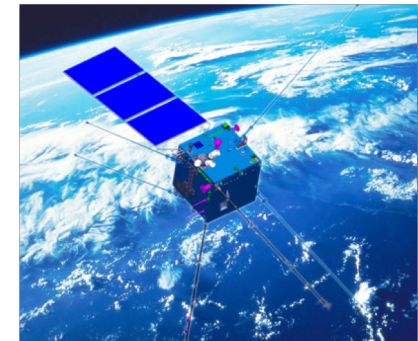
CMOS Pixel Sensor using TJ 0.18μm CMOS Imaging Process

NWELL DIODE

NMOS TRANSISTOR

PMOS TRANSISTOR

collection electrode

28 μm

PWELL

PWELL

NWELL

$N_A \sim 10^{16}$

DEEP PWELL

$N_A \sim 10^{13}$

h

e

e

h

h

e

e

h

Epitaxial Layer P-

Substrate P++

$N_A \sim 10^{18}$
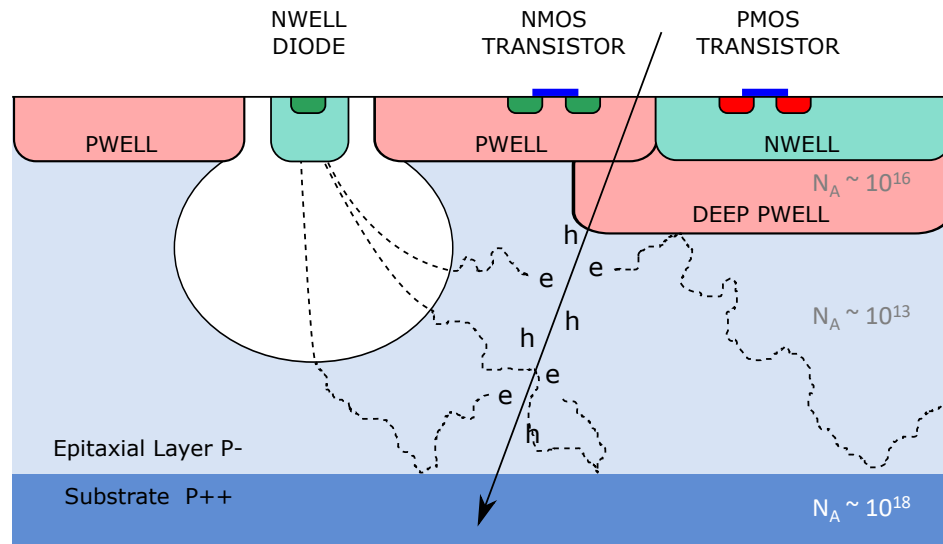
pixel capacitance ≈5 fF (@ V_bb = -3 V)

2 x 2 pixel volume

Artistic view of a SEM picture of ALPIDE cross section

$C_{in} \approx 5\ fF$

Q_{in} (MIP) ≈ 1300 e ⇨ V ≈ 40mV

▶ High-resistivity (> 1kΩ cm) p-type epitaxial layer (25μm) on p-type substrate

▶ Small n-well diode (2 μm diameter), ~100 times smaller than pixel => low capacitance (~fF)

▶ Reverse bias voltage (-6V < V_{BB} < 0V) to substrate (contact from the top) to increase depletion zone around NWELL collection diode

▶ Deep PWELL shields NWELL of PMOS transistors

➡ full CMOS circuitry within active area

ALICE PIxel DEtector (ALPIDE)

1024 pixel columns

AMP COMP
THR

512 rows

zero suppression

Bias, Data Buffering, Interface

signal processing circuitry integrated in pixel matrix

Asynchronous matrix readout
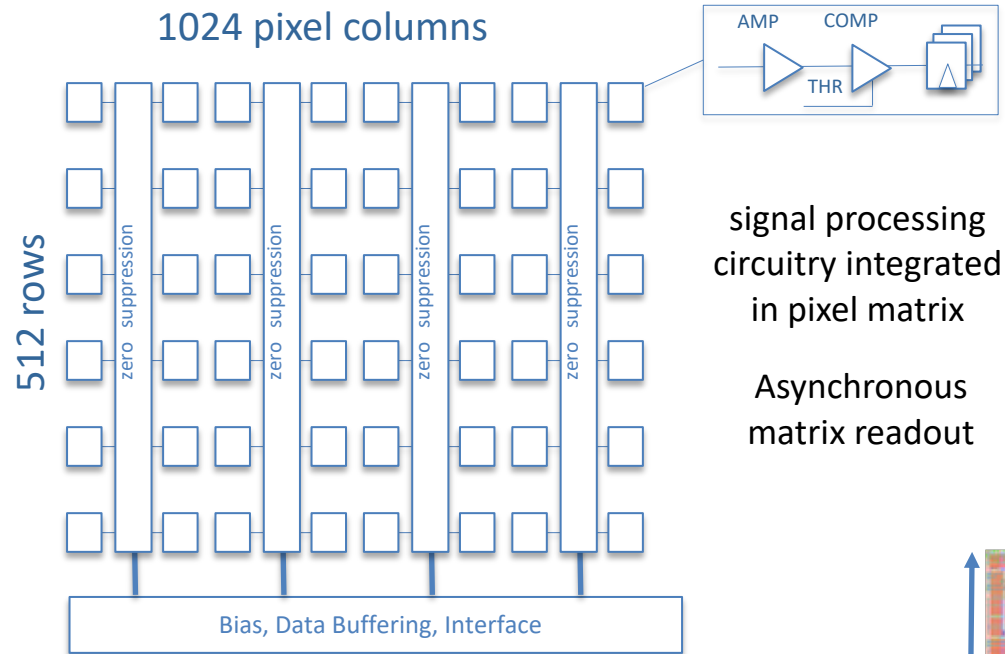
130,000 pixels / cm² 27x29x25 μm³

charge collection time <30ns (V_{bb} = -3V)

Max particle rate: 100 MHz/cm²

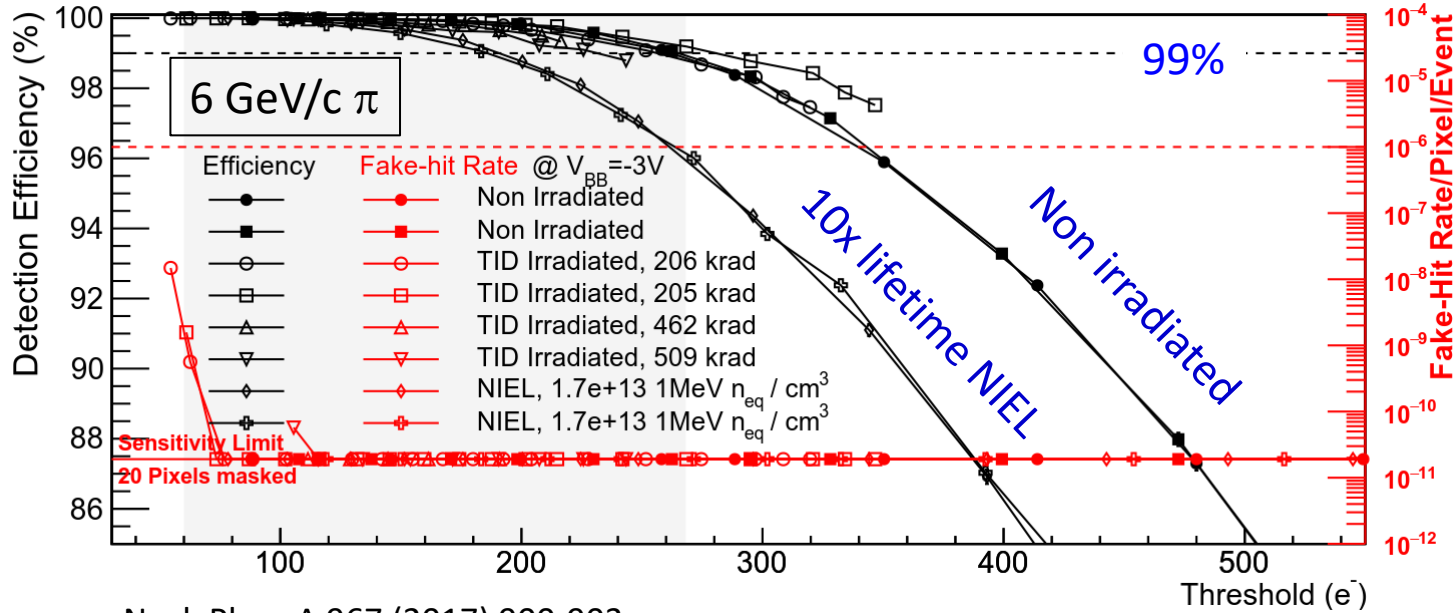fake-hit rate: < 1 Hz/ cm²

power : ≈300 nW /pixel (<40mW/cm²)

50μm thick

ALPIDE

30mm

pads over matrix

pixel matrix

15mm

periphery

Matrix Layout

4 pixels

Priority encoder

Pixel double column

Priority encoder

4 pixels

Pixel Layout

Collection Diode

Priority encoder

Front End

Digital Pixel Section

26.88 μm

9.66μm   19.58 μm

22

6 GeV/c π
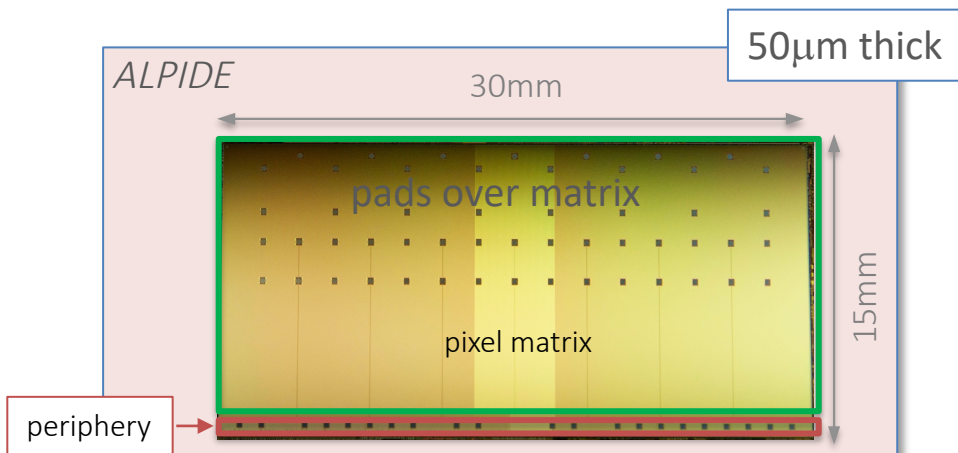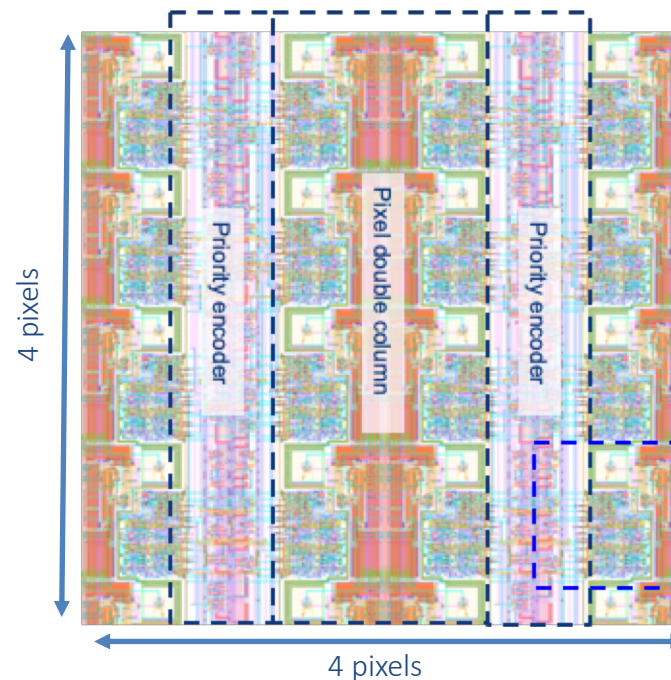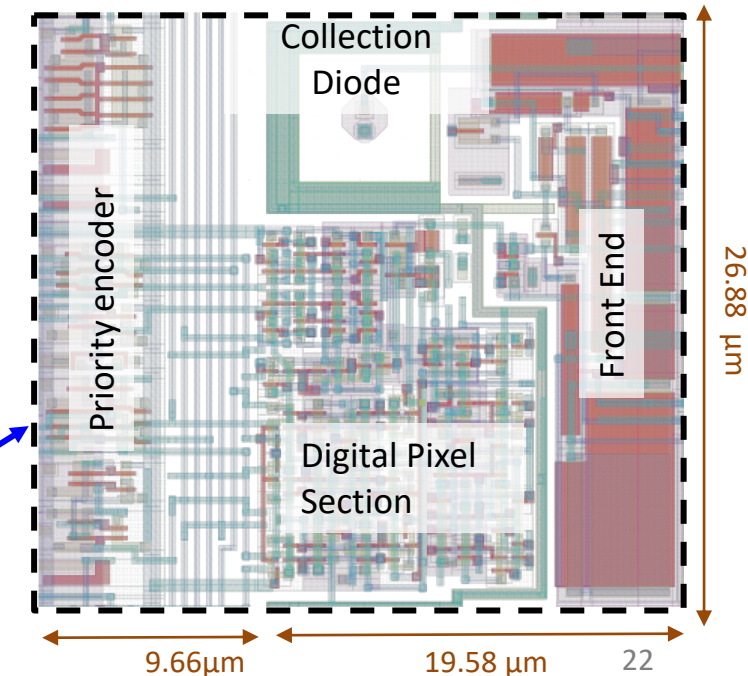
Nucl. Phys. A 967 (2017) 900-903

Large operational margin with only 10 masked pixels (0.002%), fake-hit rate < 2 x 10⁻¹¹ pixel/event

Non irradiated and TID/NIEL chips similar performance

Nucl. Phys. A 967 (2017) 900-903

5 μm resolution @ 200 e⁻ threshold

Chip-to-chip negligible fluctuations

6 GeV/c π
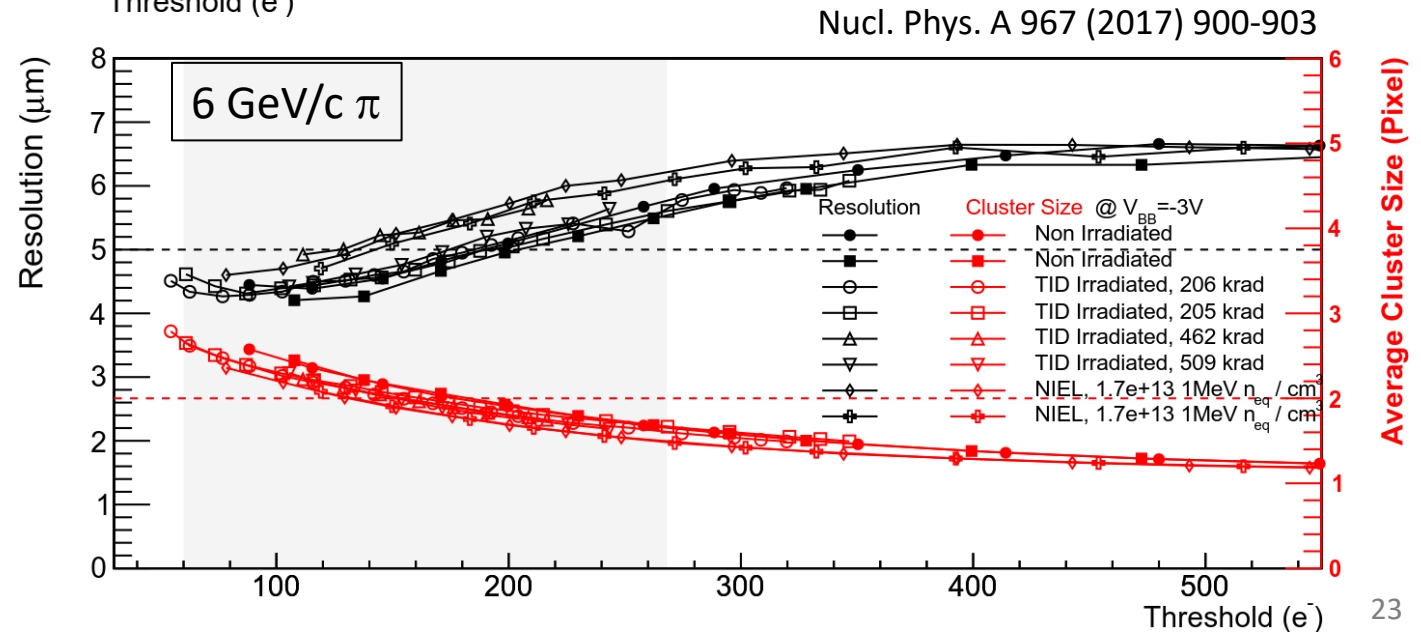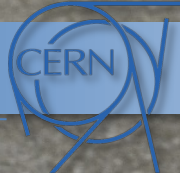
Inner Barrel is
built at CERN

Sensors

150 µm

100 µm

pixel matrix

pixel matrix
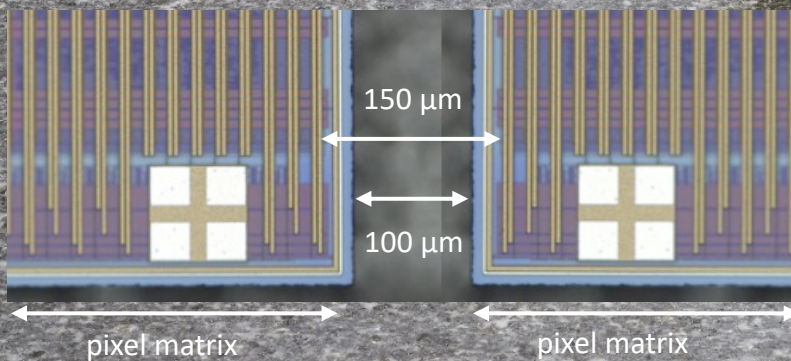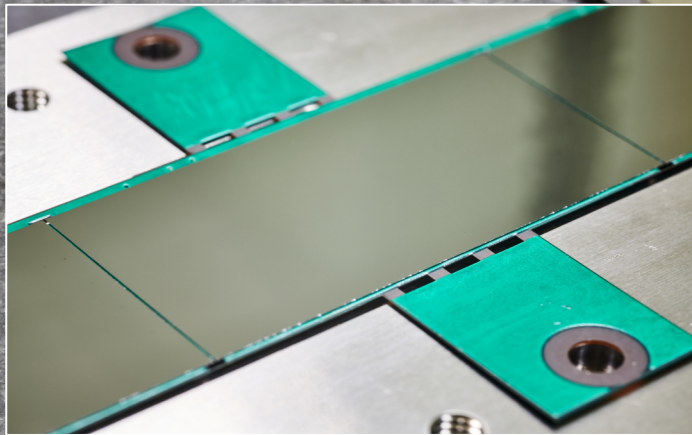
ALICE PIxel DEtector (ALPIDE)

Layers – 0, 1 and 2

Outer Barrel Stave (1.5mlong)
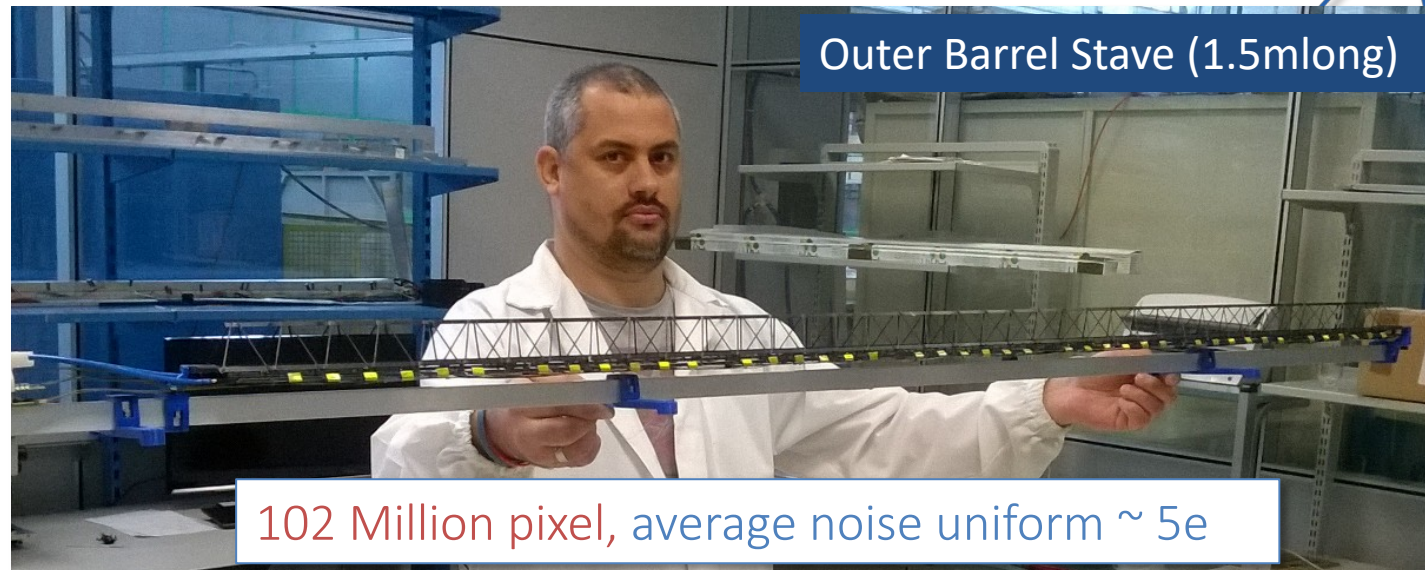
102 Million pixel, average noise uniform ~ 5e

Material budget distribution
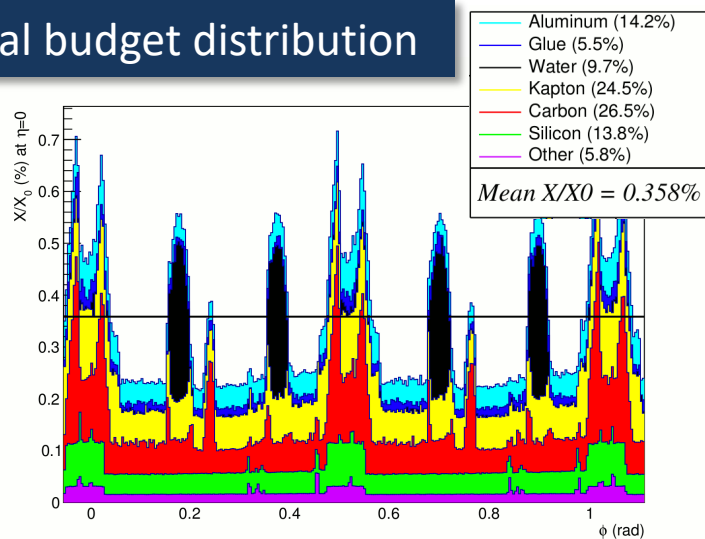
- Aluminum (14.2%)
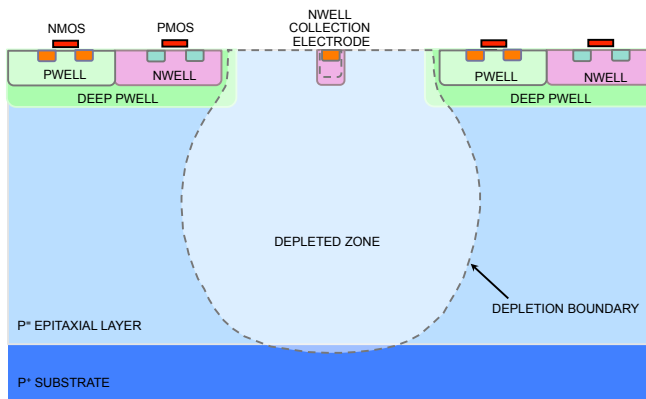- Glue (5.5%)
- Water (9.7%)
- Kapton (24.5%)
- Carbon (26.5%)
- Silicon (13.8%)
- Other (5.8%)

Mean X/X0 = 0.358%
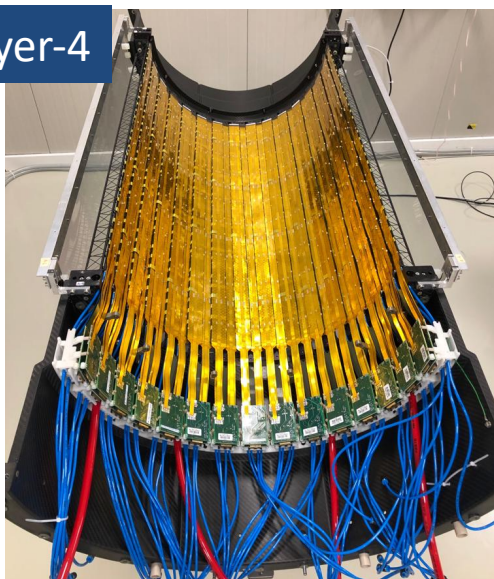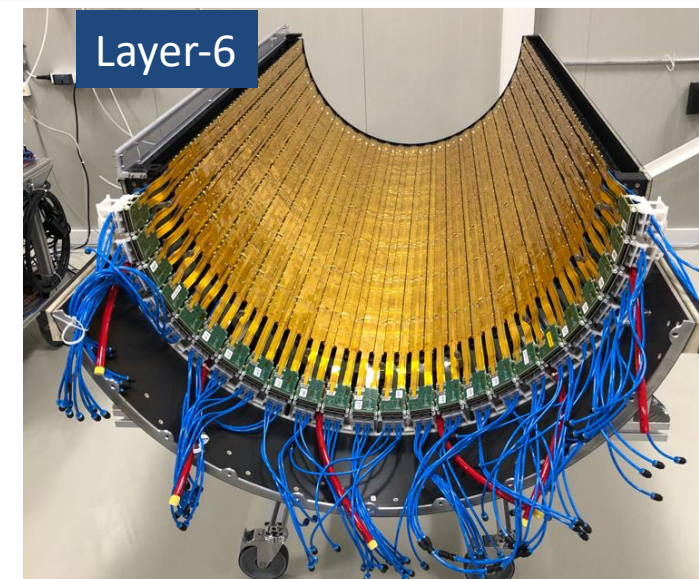
Layer-4

Layer-6

A process modification for CMOS Active Pixel Sensors (side activity of ALICE R&D)

A possible solution to achieve full depletion of the sensitive layer combined with a low capacitance electrode is to implement a planar junction separate from the collection electrode
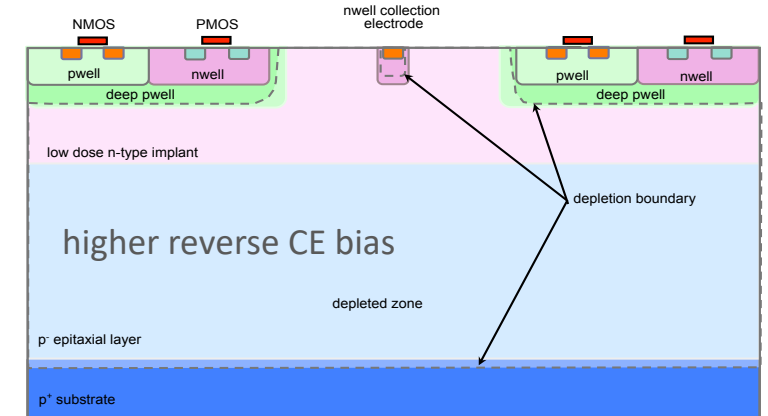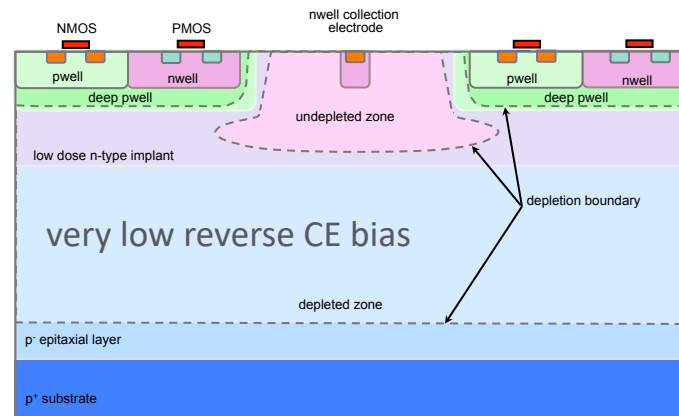
Standard Process (+DEEP PWELL)   Modified Process with low-dose n-type implant (+DEEP PWELL)

The process modification requires a single additional process mask with no changes on the sensor and circuit layout

For details on process modification and experimental results: *W. Snoeys et al. NIM, A 871C (2017) pp. 90-96*

The ALICE test vehicle chip (investigator) and prototype ALPIDE chips exist with both flavors

Signal and cluster distribution from a ^{55}Fe source for standard and modified process

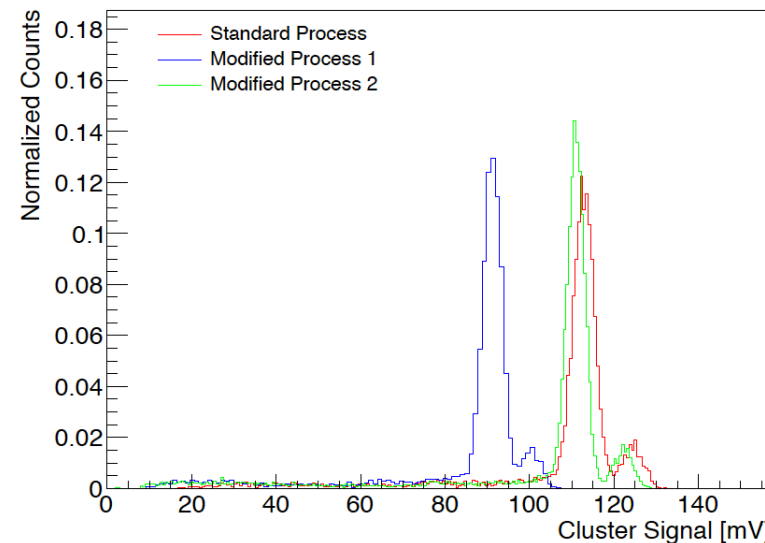Modified Process 1 = higher dose, Modified Process = lower dose

J. Van Hoorne et al., NSS 2016

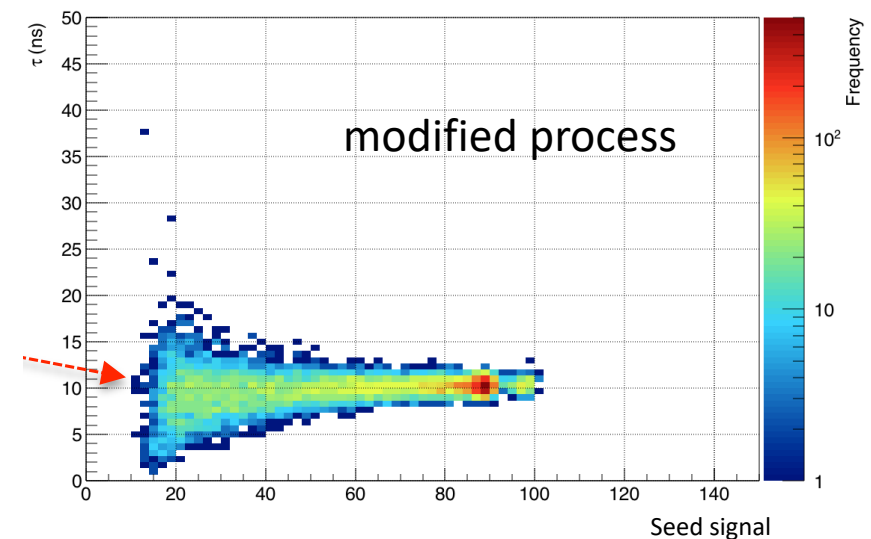*Tests performed on investigator chip (same pixel as ALPIDE)*

Pixel size: 28 x 28 μm^2,   CE: 2 x 2 μm^2 centered in a 8 x 8 μm^2 opening,   P-well & substrate @ -6V, CE @ 1V
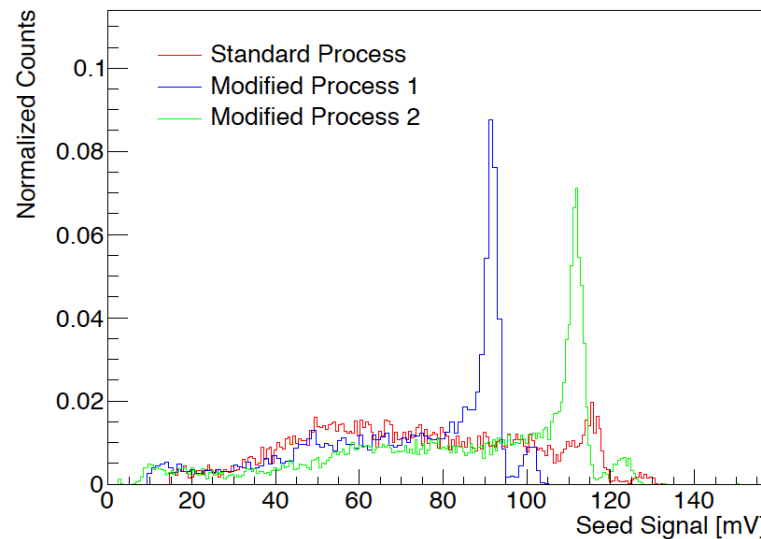

(A) Seed signal

(B) cluster signal

Note: chip output buffer limits the rise time to 10ns

- For a lower dose (MP1) a no sensor capacitance penalty

- For modified process, larger fraction of single pixel clusters (see also fraction of signal within the peak in A)

^{90}Sr measurements on modified process samples (different setup, different pixel w.r.t. before)

- Non-irradiated

- 1×10^{14} 1MeV n_{eq}/cm^2 (NIEL) and 100krad (TID)

- 1×10^{15} 1MeV n_{eq}/cm^2 (NIEL) and 1Mrad (TID)

H. Pernegger et al 2017 JINST 12 P06008
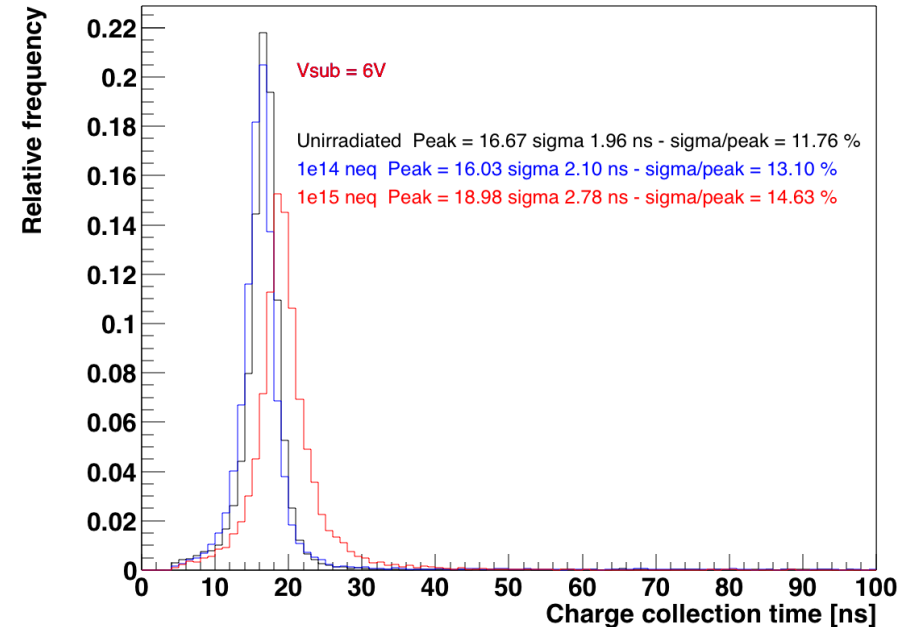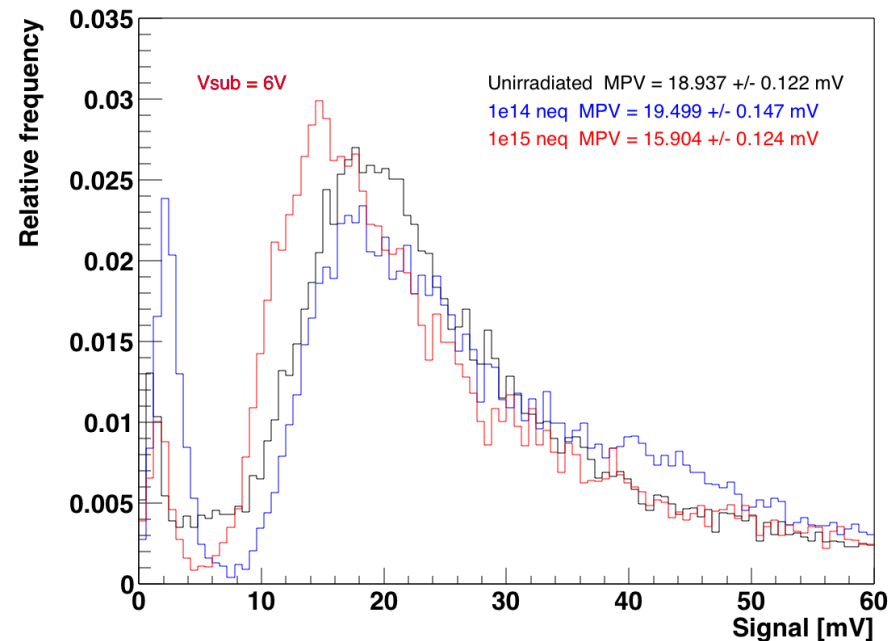
Tests performed on investigator chip (different pixel wrt to ALPIDE) *Note: chip output buffer limits the rise time to 10ns*
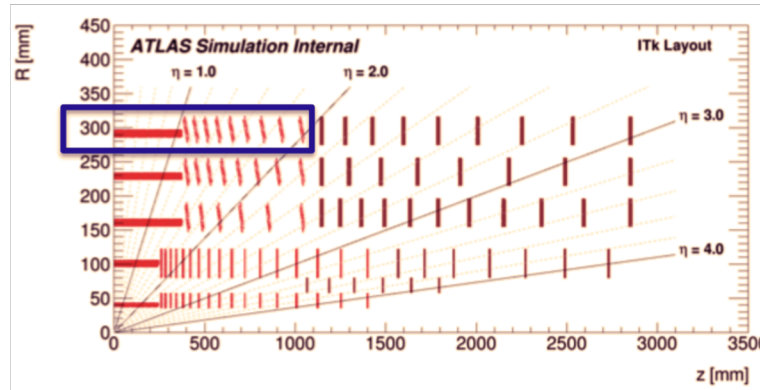
Pixel size: 50 x 50 μm^2,   CE: 3 x 3 μm^2 centered in a 18 x 18 μm^2 opening, 25μm epi

Outermost layer of ITk Pixel Barrel

- 2016 quad modules
- 3m^2

For 4000 fb^{-1}

- TID = 80 Mrad
- NIEL = 1.5 x 10^{15} n$_{eq}$/cm^2

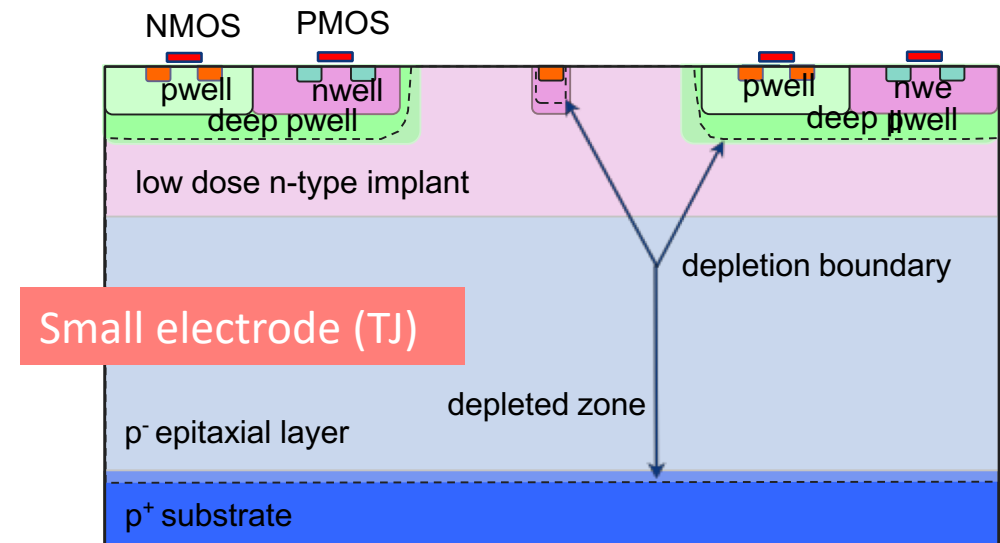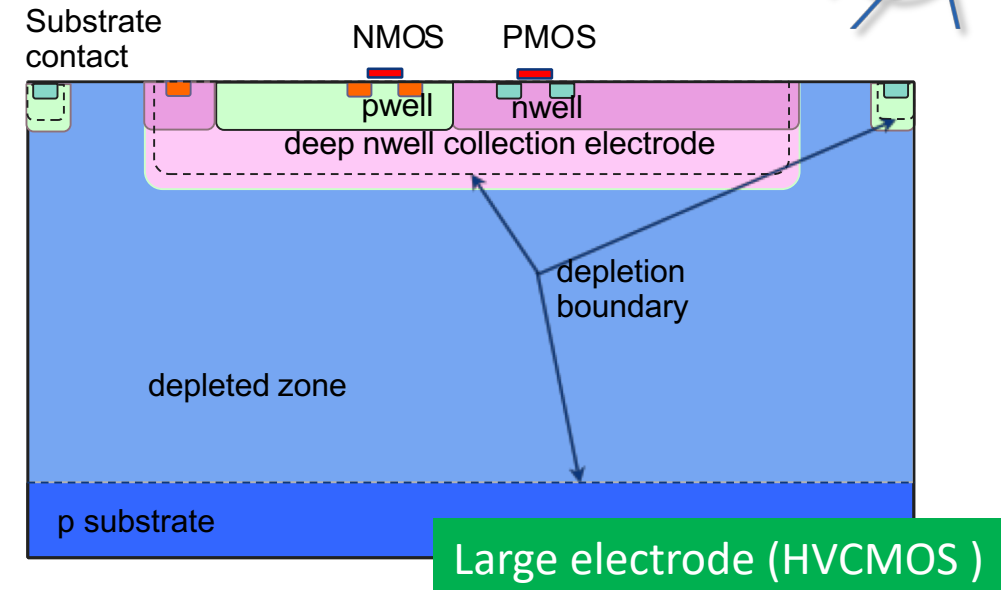## Monolithic CMOS sensors are considered as option for the outermost layer

- Saves bump bonding for 45% of outer barrel system
- Cost reduction and reduce module assembly time

Three developments on three technologies

- Large CE: AMS ⇨ TSI (ATLASPix)
- Large CE: LFOUNDRY (Monopix)   *Toko Hirono, Thu*
- Small electrode: TJ modified process (MALTA, Monopix)
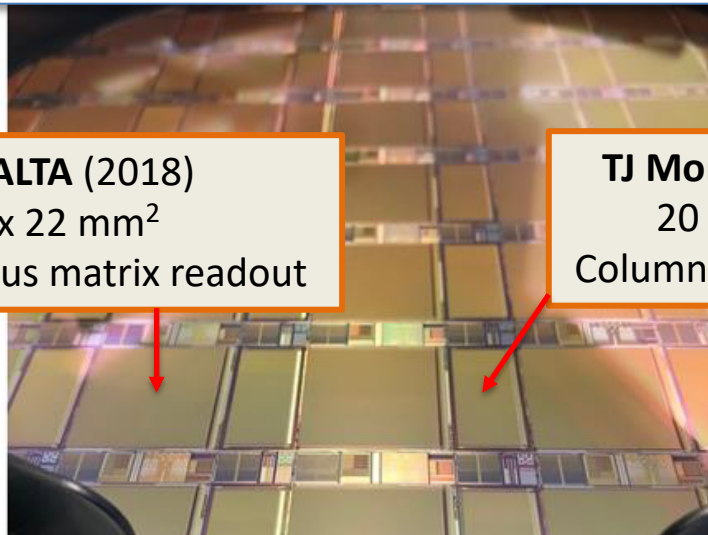
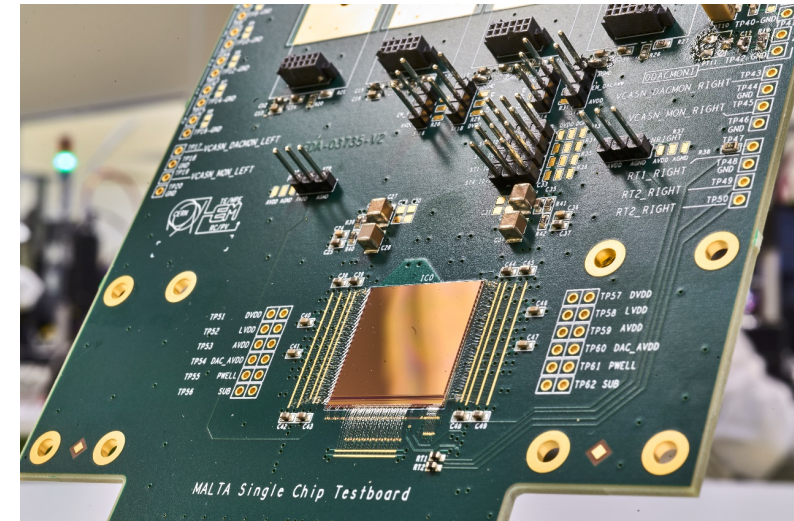 *Enrico Junior Schioppa, Thu*

Analogue front-end optimized for timing, based on ALPIDE

Design of two large scale demonstrators
Collaboration CERN - Bonn

TJ MALTA (2018)
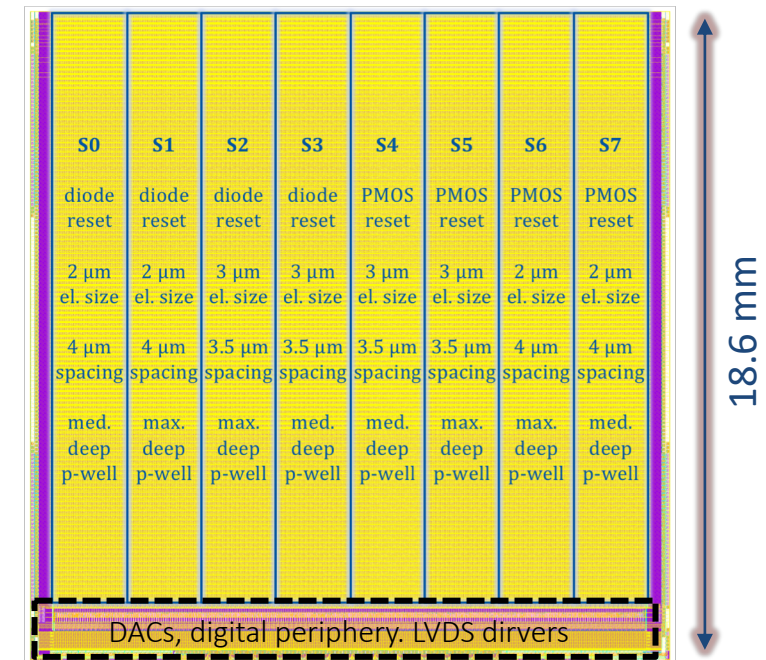20 x 22 mm^2
Asynchronous matrix readout

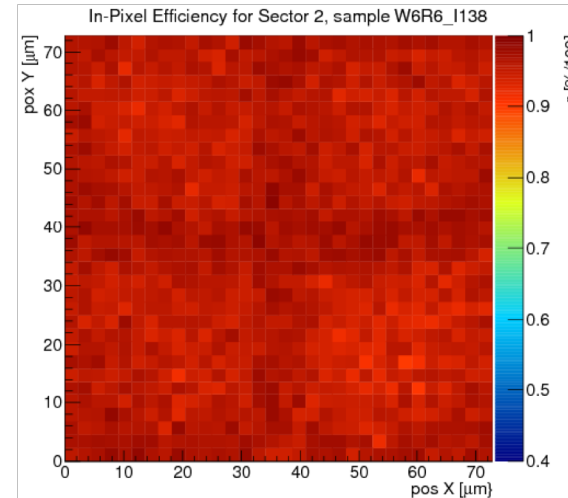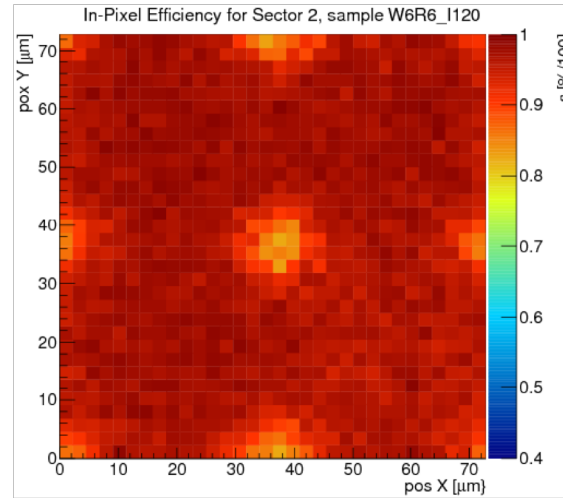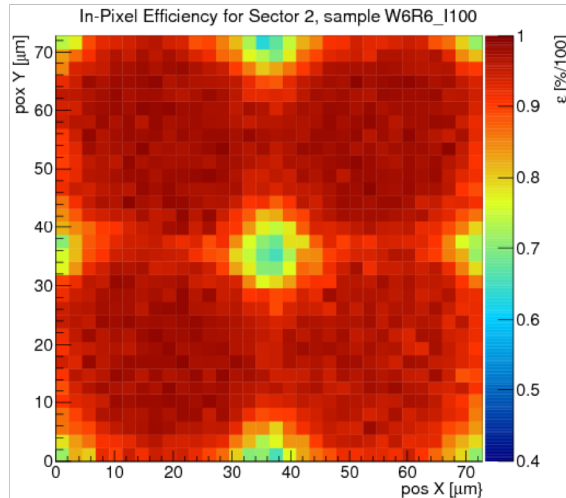**TJ MonoPix** (2018)
20 x 10 mm^2
Column drain readout

MALTA: Monolithic Pixel Detector from ALICE to ATLAS

- The 512 x 512 pixel – 8 sectors
- Front-end is a development from the ALPIDE one
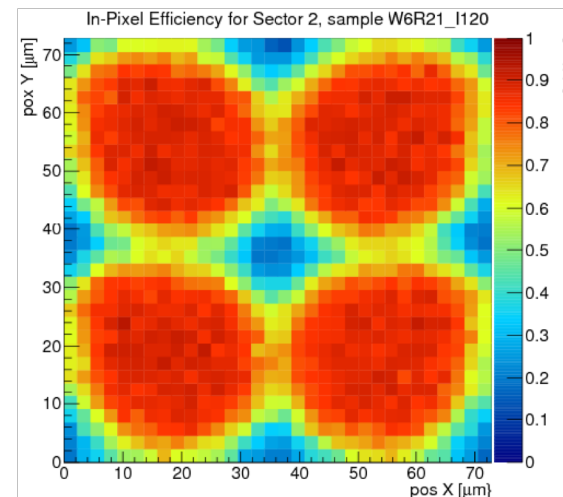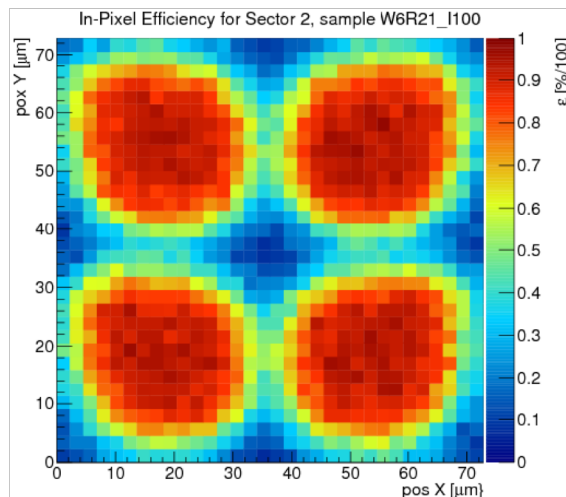- Design based on low-power analogue front-end and an asynchronous architecture to readout the pixel matrix

MALTA Single Chip Testboard

S0	S1	S2	S3	S4	S5	S6	S7
diode reset	diode reset	diode reset	diode reset	PMOS reset	PMOS reset	PMOS reset	PMOS reset
2 μm el. size	2 μm el. size	3 μm el. size	3 μm el. size	3 μm el. size	3 μm el. size	2 μm el. size	2 μm el. size
4 μm spacing	4 μm spacing	3.5 μm spacing	3.5 μm spacing	3.5 μm spacing	3.5 μm spacing	4 μm spacing	4 μm spacing
med. deep p-well	max. deep p-well	max. deep p-well	med. deep p-well	med. deep p-well	max. deep p-well	max. deep p-well	med. deep p-well

18.6 mm

DACs, digital periphery. LVDS dirvers

30

In-Pixel Efficiency for Sector 2, sample W6R6_I100

In-Pixel Efficiency for Sector 2, sample W6R6_I120

In-Pixel Efficiency for Sector 2, sample W6R6_I138

Decreasing threshold from ~600 e⁻ to ~250e- (unirradiated) / ~350e⁻ (irrad.)

In-Pixel Efficiency for Sector 2, sample W6R21_I100

In-Pixel Efficiency for Sector 2, sample W6R21_I120

Could not reach
Lower threshold
(RTS + Making issues)

New prototypes that fix
both problems are
currently under test

Unirradiated:
lowering the threshold
gives the full efficiency

Neutron irradiated
$5x\ 10^{14}\ n_{eq}/cm^2$

Inefficiency in pixel
corners due to low
lateral electric field

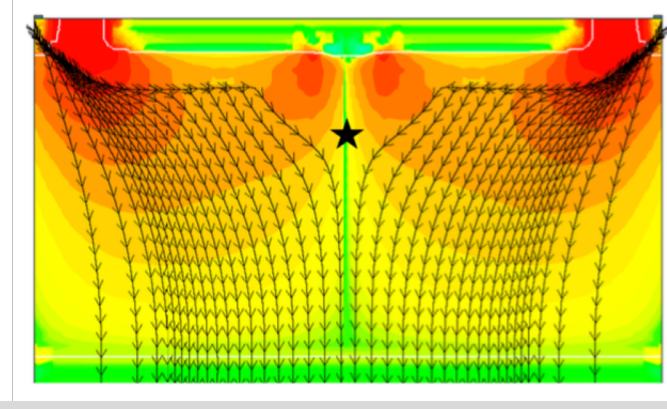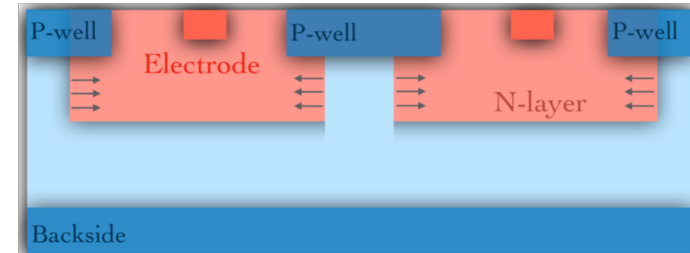*L. Musa (CERN) – VCI, Vienna, Feb 2019*

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modified process (mp) – "standard"
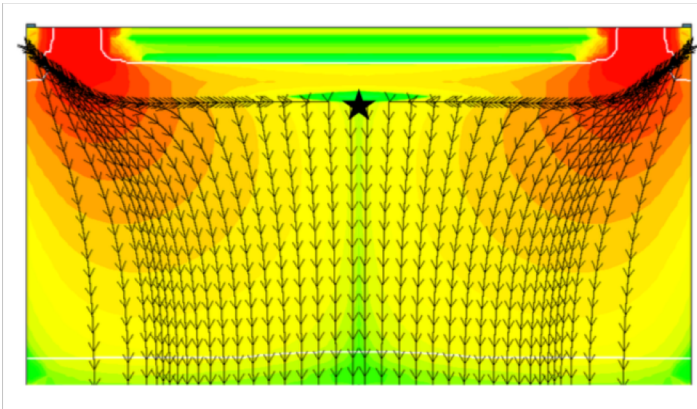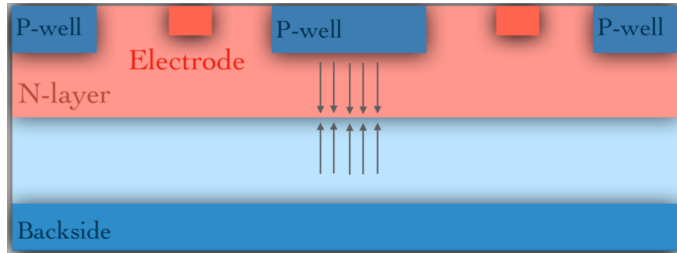
mp + additional p-implant
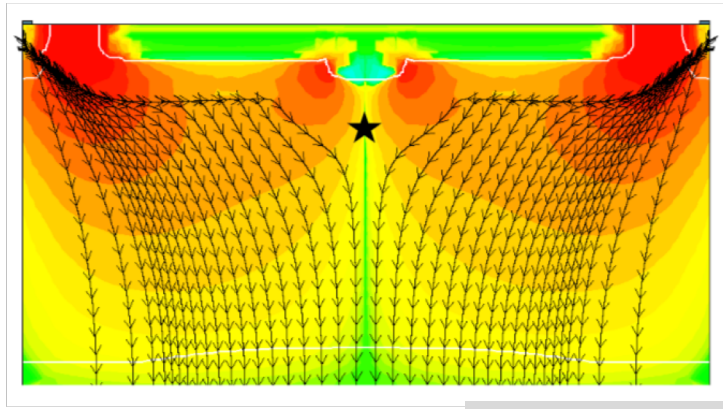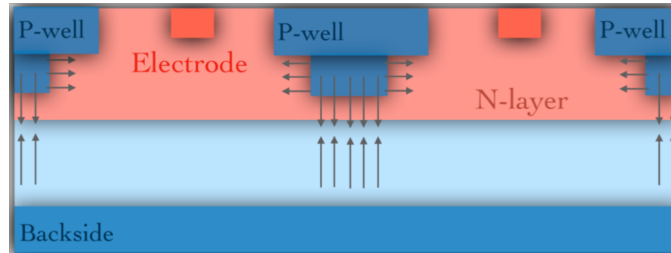
mp + gap in n-layer

Magdalena Munker (CERN), Pixel 2018 (Taipei - Dec 2018)

TJ modified process: E field minimum at pixel corners => charges pushed to the minimum before they propagate to CE

Additional p-implant or gap in n-layers: bend the field towards the CR, shorted drift path

- Compatible with standard CMOS technology

- Triple well process on p-type substrate (20- 1000 Ω cm)

- Prototypes with var CMOS processes (AMS, TSI, LFounfry)

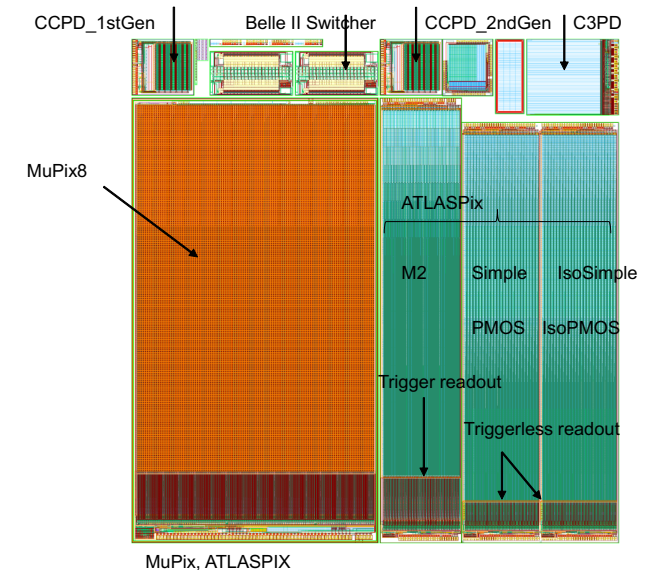*The HV CMOS Collaboration*

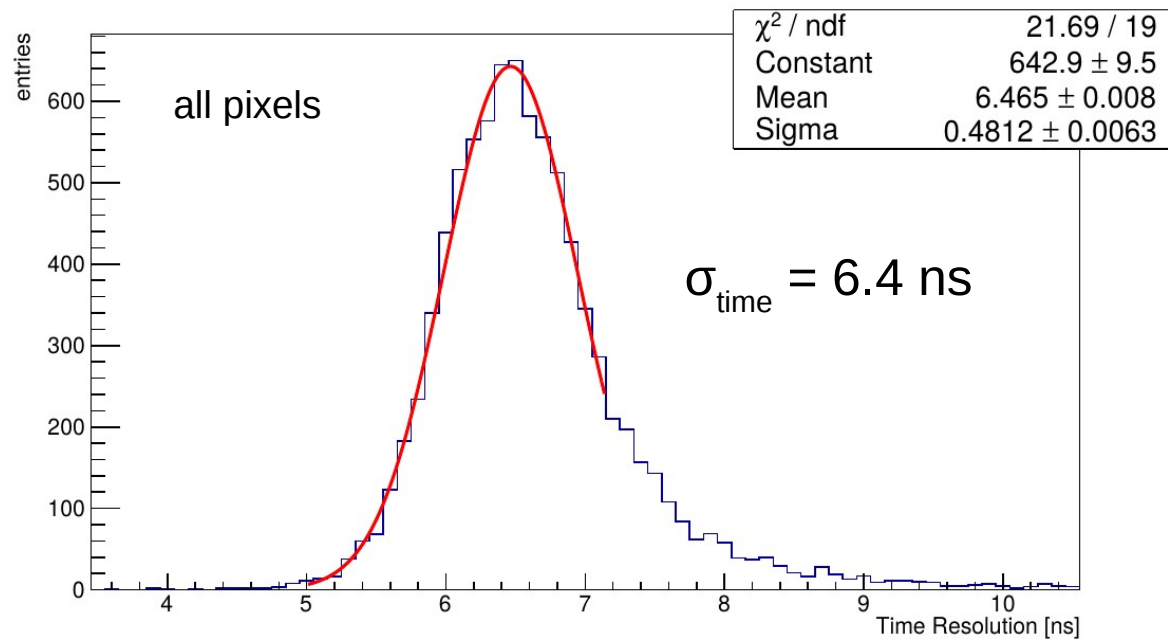MUPIX8

I. Peric et al., NIM A 582 (2007) 872
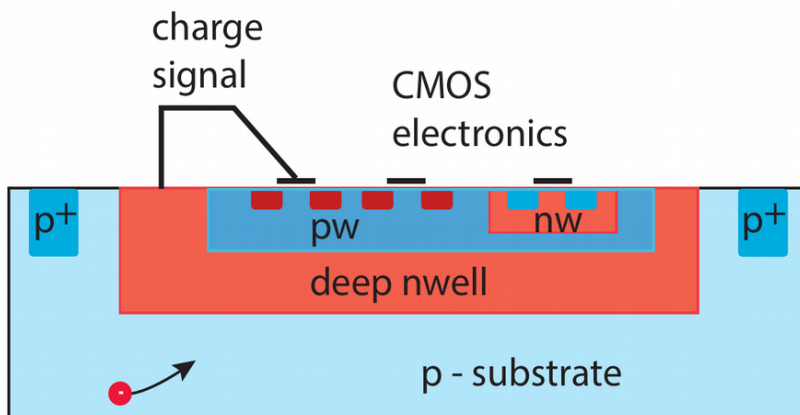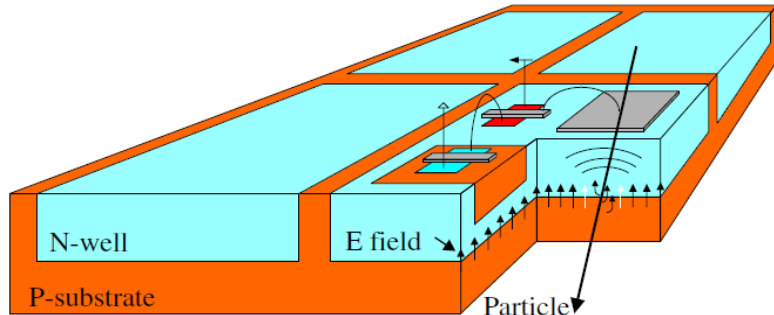
- The collection diode occupies a large part of the pixel

- Electronic circuits inside deep n-well

- HV O$(60 - 120V)$ contacts at the top side
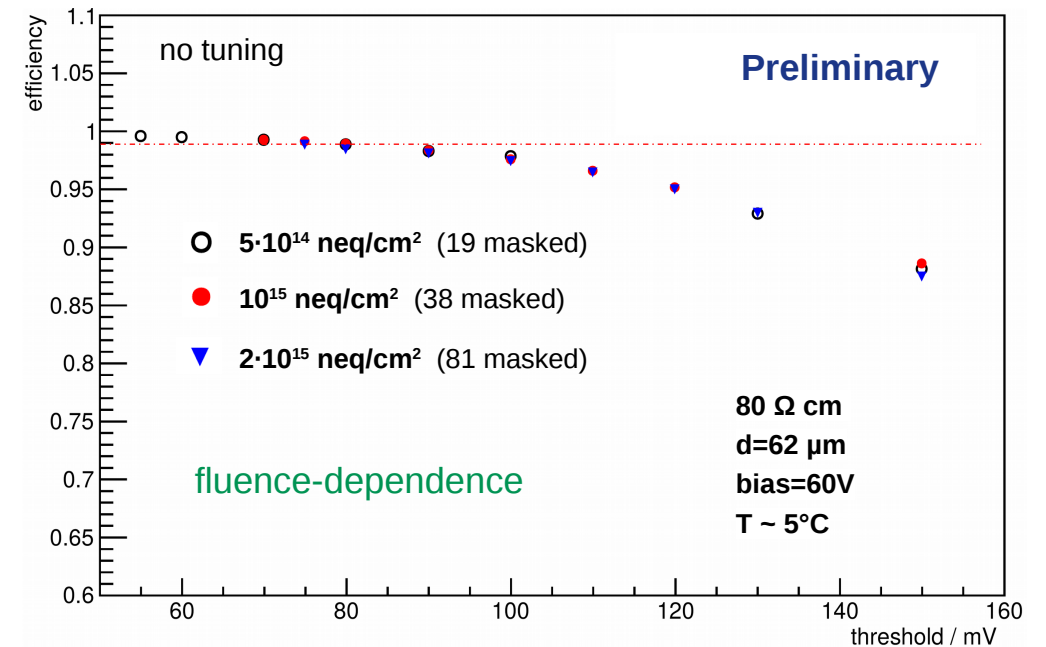
- MUPIX8 pixel: $80 \times 81 \ \mu m^2$

- Circuitry in the collection diode introduces additional sensor capacitance

- Keep pixel circuitry as simple as possible

- Confine digital circuitry at the periphery

courtesy of I. Peric and A. Schoening

Time resolution with timewalk correction

Efficiency and fake hit rate

all pixels

χ^2 / ndf	21.69 / 19
Constant	642.9 ± 9.5
Mean	6.465 ± 0.008
Sigma	0.4812 ± 0.0063

σ_{time} = 6.4 ns

entries

Time Resolution [ns]

no tuning

Preliminary

efficiency

- O $5 \cdot 10^{14}$ neq/cm² (19 masked)
- ● 10^{15} neq/cm² (38 masked)
- ▼ $2 \cdot 10^{15}$ neq/cm² (81 masked)

80 Ω cm
d=62 μm
bias=60V
T ~ 5°C

fluence-dependence

threshold / mV

courtesy of I. Peric and A. Schoening

INFN projects SEED and ARCADIA: two phases of the same development

The SEED project successfully demonstrated a fully depleted, up to 300 μm thick MAPS sensor

- LFoundry 110nm CMOS process.

- Sensor nodes are n-type implantation (become insulated only with full substrate depletion)

- The high resistivity, floating zone n-type substrate is depleted by negative voltage at the p+ backside

- Deep pwell implantations allows implementing full CMOS gates

- Double-sided lithography was used for the processing of the backside layers (5 extra masks)

- The backside p+ implantation was done after thinning the substrate, and activated with laser annealing

- To avoid early breakdown, termination structures with floating guard rings have been added at the borders

Collection n+/n implants
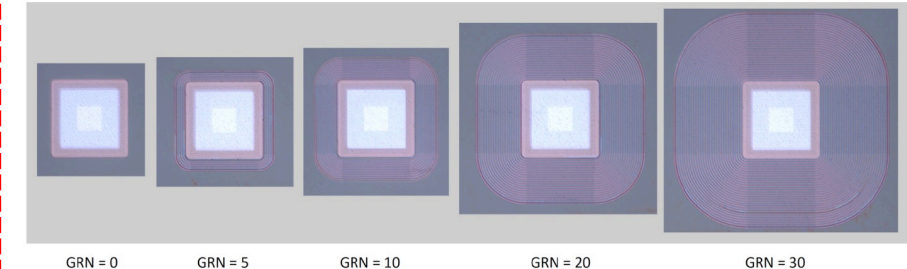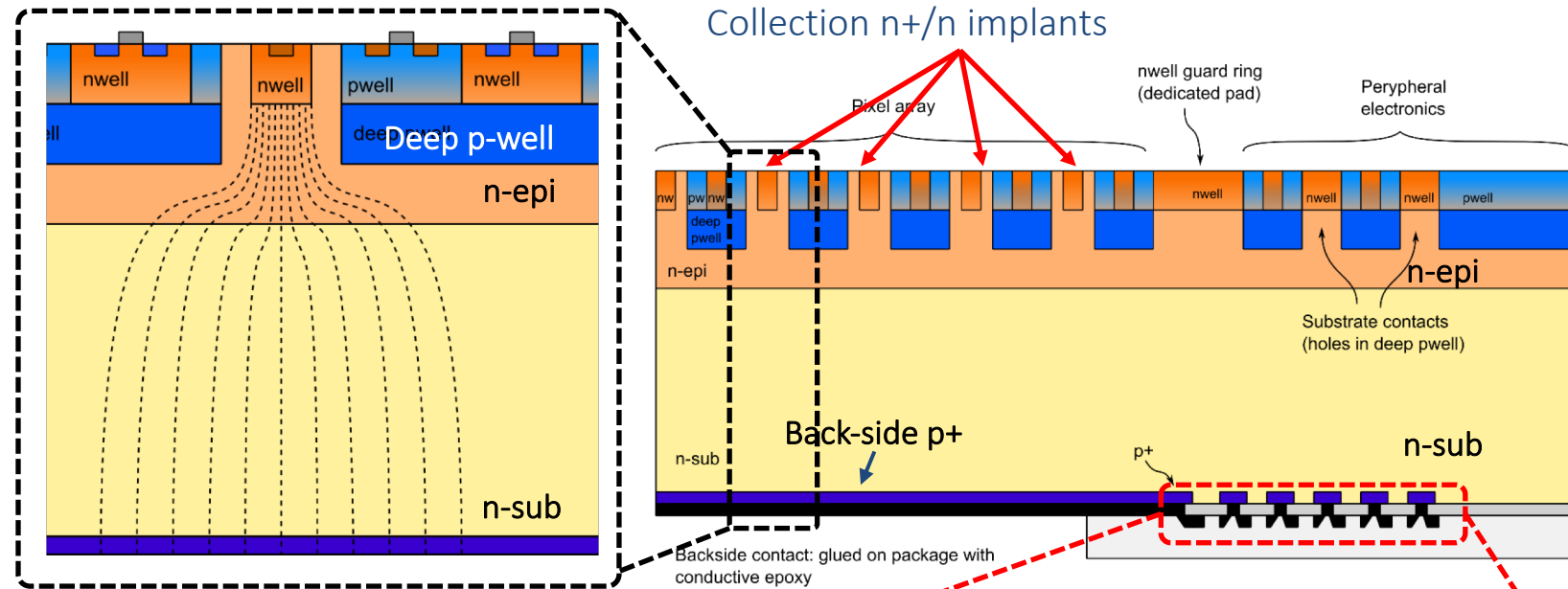
Different guard-rings on the backside diodes

L. Musa (CERN) – VCI, Vienna, Feb 2019

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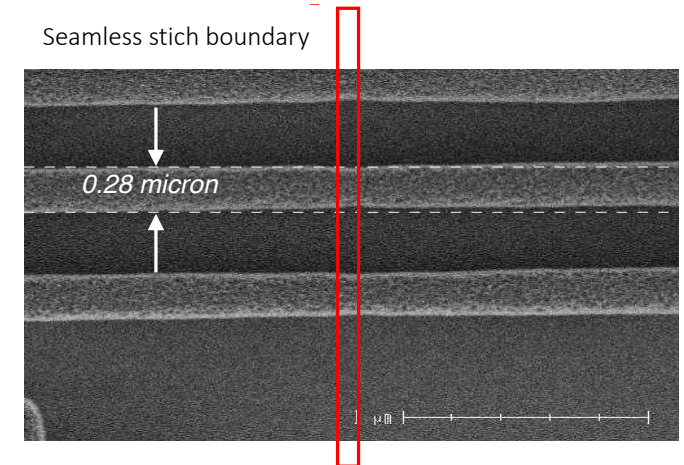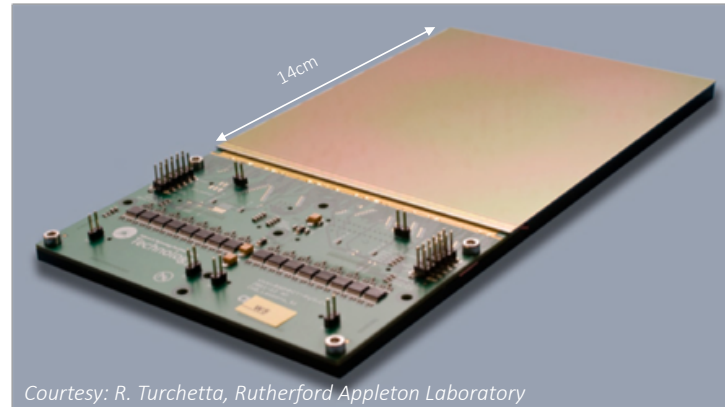
Photolithographic process defines wafer reticles size ⇨ Typical field of view O(2 x 2 cm^2)

Reticle is stepped across the wafers to create multiple identical images of the circuit(s)
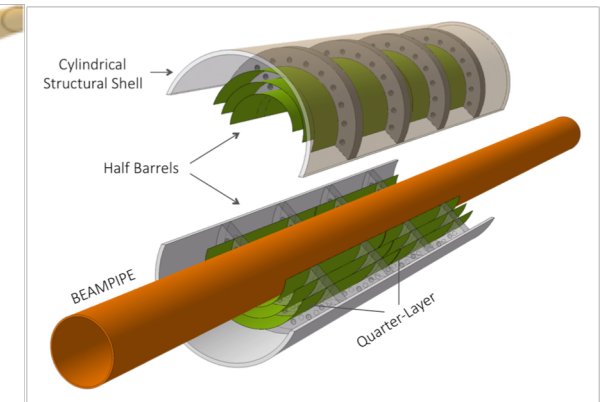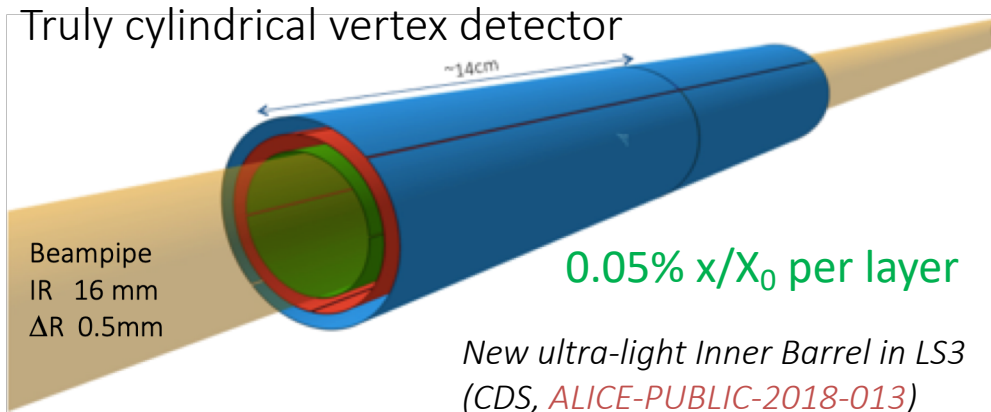
A stepping process called "stitching" allows building sensors of arbitrary size, the only limit being the size of the wafer.

- Reticle made of blocks
- Printing only individual blocks at each step with a tiny well-defined overlap

These days, stitching is widely applied in the digital imaging industry (e.g. large flat panels for medical and dental X-rays)

14cm

Courtesy: R. Turchetta, Rutherford Appleton Laboratory

Seamless stich boundary

0.28 micron

Silicon Genesis: 20 micron thick wafer

Ultra-thin chip (<50 um): flexible with good stability

Truly cylindrical vertex detector

~14cm

Beampipe
IR   16 mm
ΔR 0.5mm

0.05% x/X$_0$ per layer

New ultra-light Inner Barrel in LS3 (CDS, ALICE-PUBLIC-2018-013)

Cylindrical Structural Shell

Half Barrels

BEAMPIPE

Quarter-Layer

The pCT works on the same principle as a "standard" x-rays CT: recording particles passing through the target from different angles to reconstruct a 3D image. Main difference is that, while photons are simply absorbed, protons also scatter

Proton true trajectory

Energy measurement

p'

L

p

L'

Med Phys **40** (2013) 031103

Proton beam

tracking detectors:
Record paths of individual protons with high precision

360°

Stacks of thin scintillator plates:
Determine energy loss of protons with high precision

X-Rays
Protons
Protons – different reconstruction

NIM A **699** (2013) 205–210
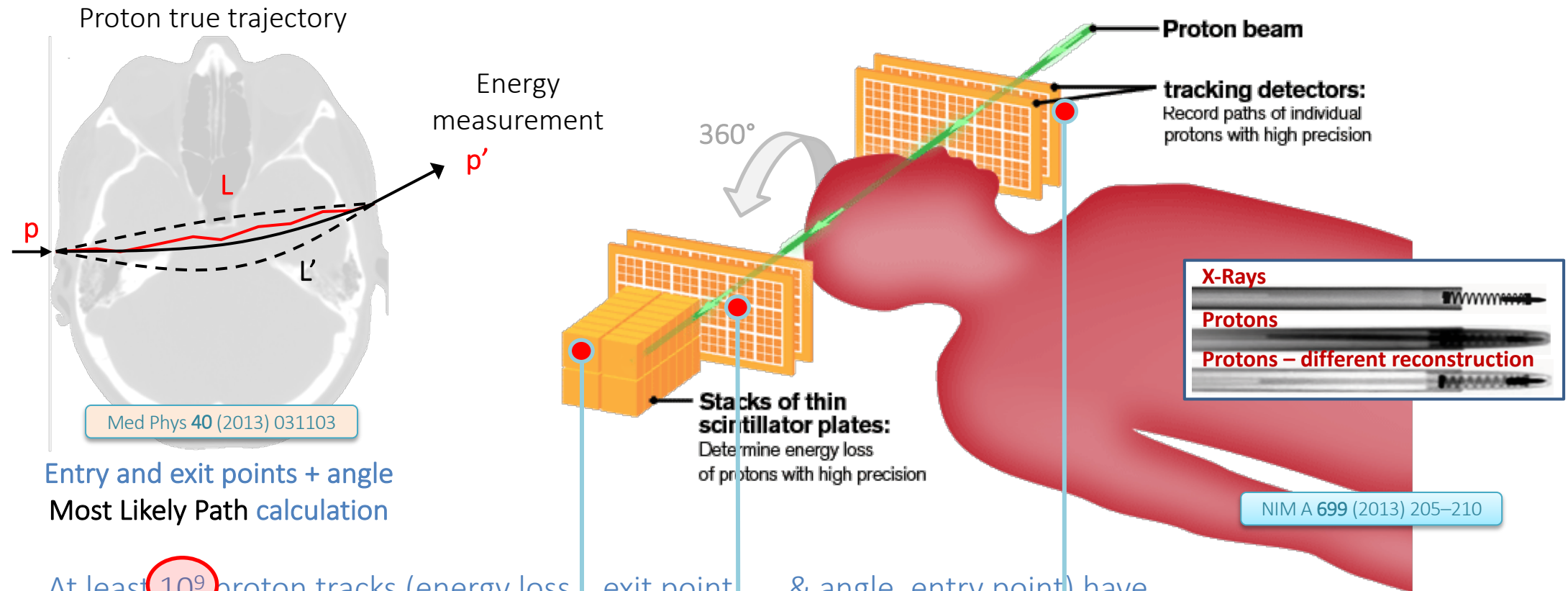
Entry and exit points + angle
Most Likely Path calculation

At least 10^9 proton tracks (energy loss, exit point & angle, entry point) have to be recorded to provide a detailed enough image. This leads to long exposure time (10s minutes) with current state of the art: limited to R&D only.

Talk of Alexander Burker, Thu

- Fast (> 10 MHz cm^{-2}) proton tracking at low power in silicon (**50 mW cm^{-2}**)

- Monolithic, thinned (≤ 50 μm) and large area (**> 16 cm^2**) device to minimize proton scattering.

- No support structure behind the silicon

- **Cost effective**, reliable, simplified commissioning & operations, commercial process (for large production)

- **Low voltage** for real clinical usage

ALPIDE is an excellent starting point, currently used by many groups for medical R&D

iMPACT *pen image w/ Alpide monolithic pixel sensor*   70 MeV protons / TIFPA beamline at APSS Trento
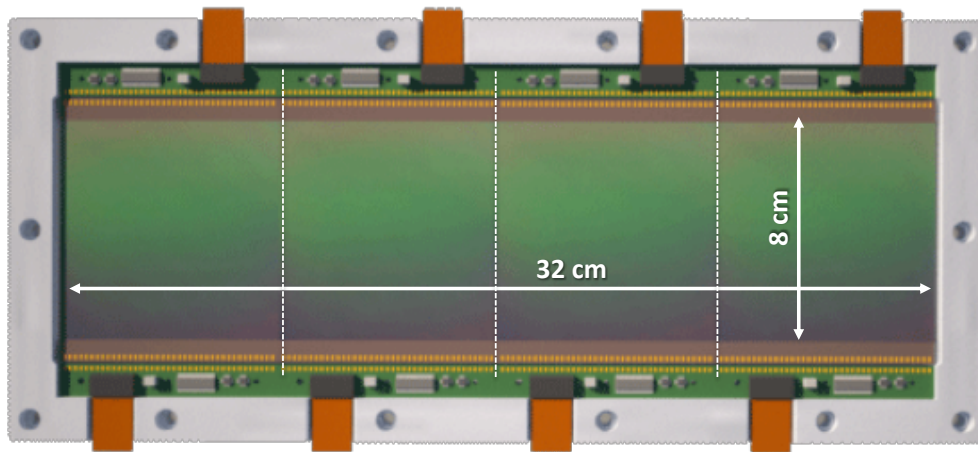
ALPIDE used to take a demonstrative proton radiography of a pen:
metal, different plastic densities, air distinguishable

Talk of Ganesh Tambav, Thu
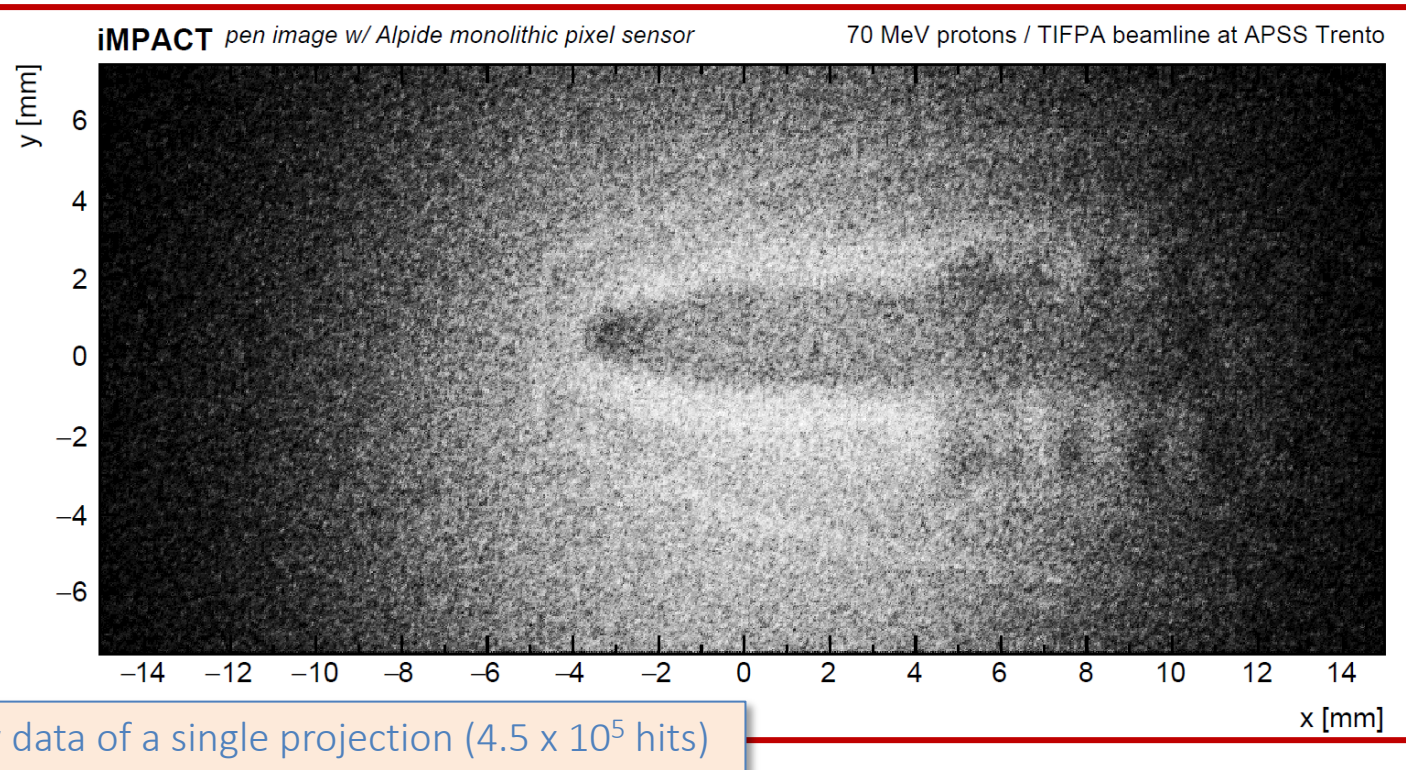
raw data of a single projection (4.5 x 10^5 hits)

Large area, monolithic, low power pixel sensors are enabling devices for many cutting-edge research field and practical application: HEP trackers, medical imaging, space-borne instruments, FEL imagers, etc...
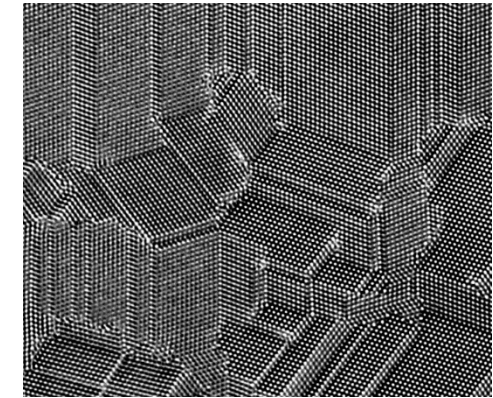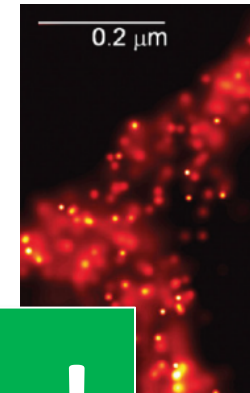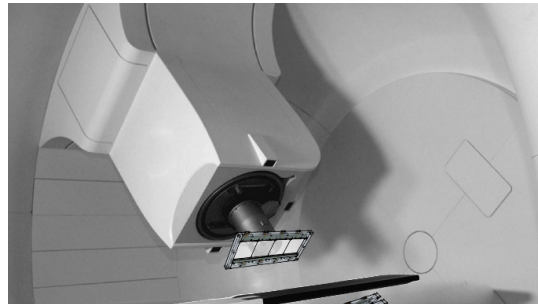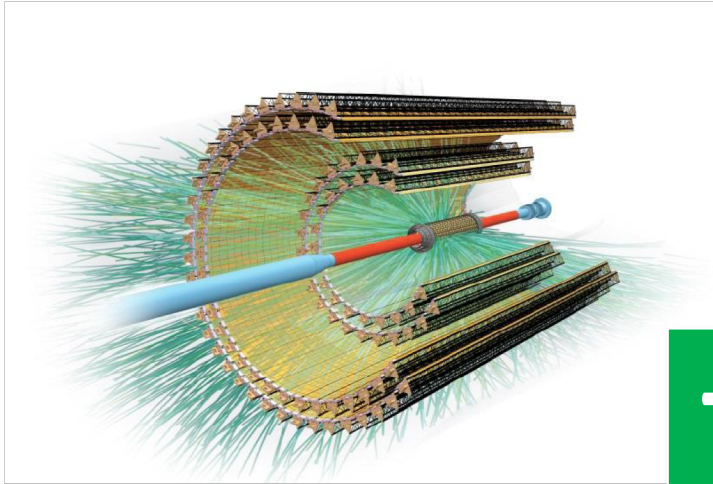

The HEP community is in an **unique position** to bridge between different fields and drive for sensors advancement, leveraging on the last decades experience and acquired know-how !
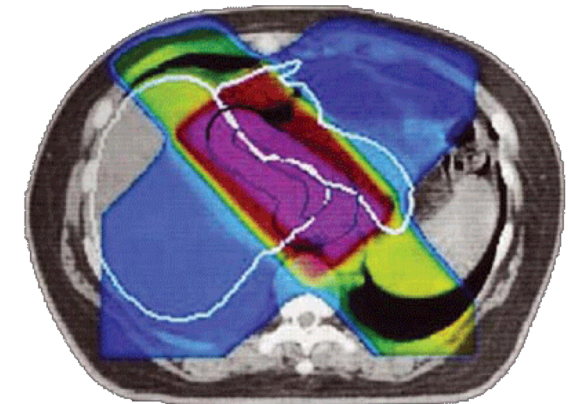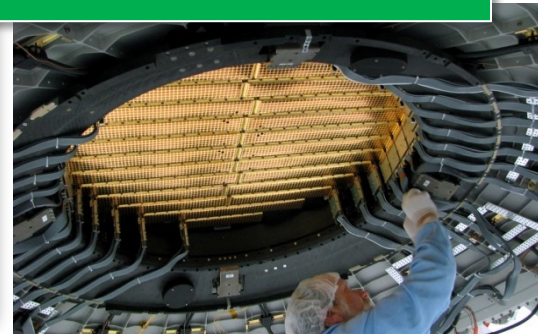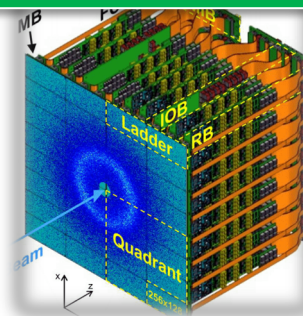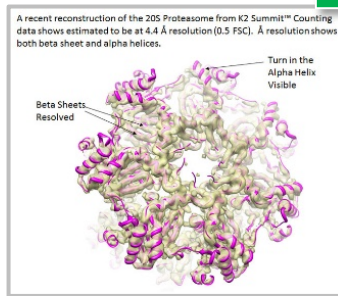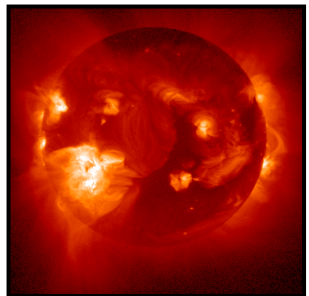
Large area, monolithic, low power pixel sensors are enabling devices for many cutting-edge research field and practical application: HEP trackers, medical imaging, space-borne instruments, FEL imagers, etc...
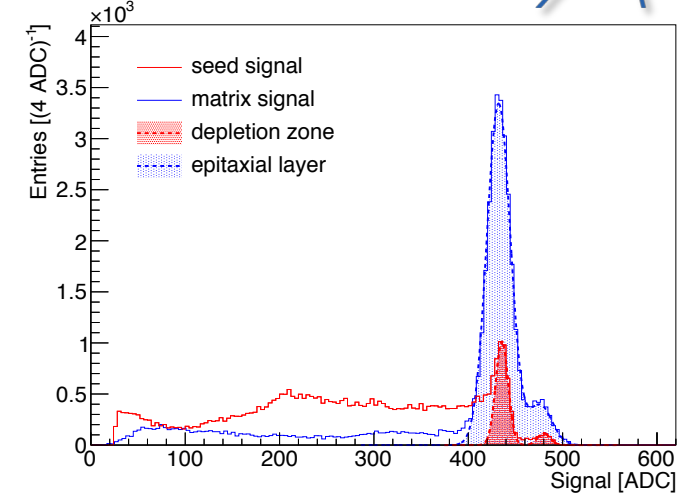

Thank You!

The HEP community is in an **unique position** to bridge between different fields and drive for sensors advancement, leveraging on the last decades experience and acquired know-how !
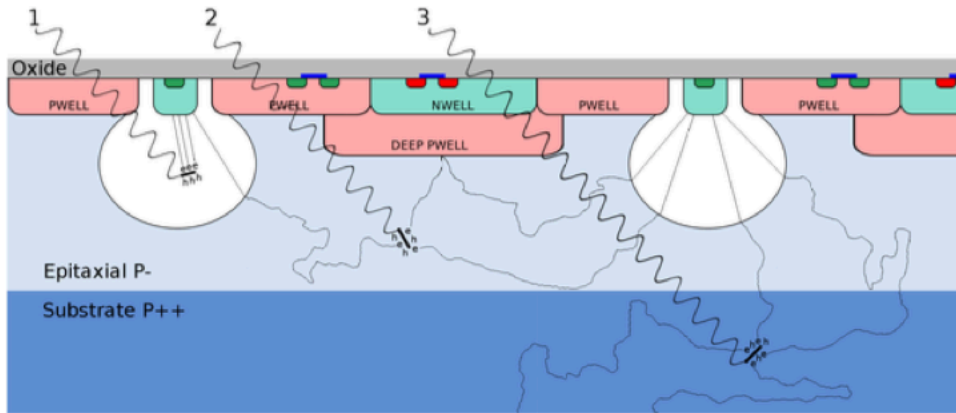
^{55}Fe: two X-Ray emission modes:

1. K-α: 5.9keV (1640 e/h in Si), rel. freq.: 89.5%, attenuation length in Si: 29μm

2. K-β: 6.5keV (1800 e/h in Si), rel. freq.: 10.5%, attenuation length in Si: 37μm

For X-ray absorption in sensors fabricated with the std process, three cases can be defined

1. **Absorption in depleted volume**: charge collected by drift, no charge sharing, single pixel cluster   *J. Van Hoorne NSS 2016*
   - These events populate the calibration peak in the signal histogram
   - Charge collection time expected to be <1ns

2. **Absorption in non depleted volume of the epitaxial layer**: charge partially collected by diffusion and then drift, charge sharing depending on position of X-Ray absorption
   - Charge collection time expected to be dependent on distance of X-Ray absorption from the depleted volume, and longer than events of case 1.

3. **Absorption in substrate**
   - Contribution depending on depth of X-Ray absorption, and charge carrier lifetime within substrate
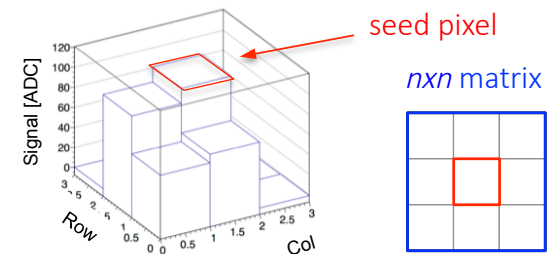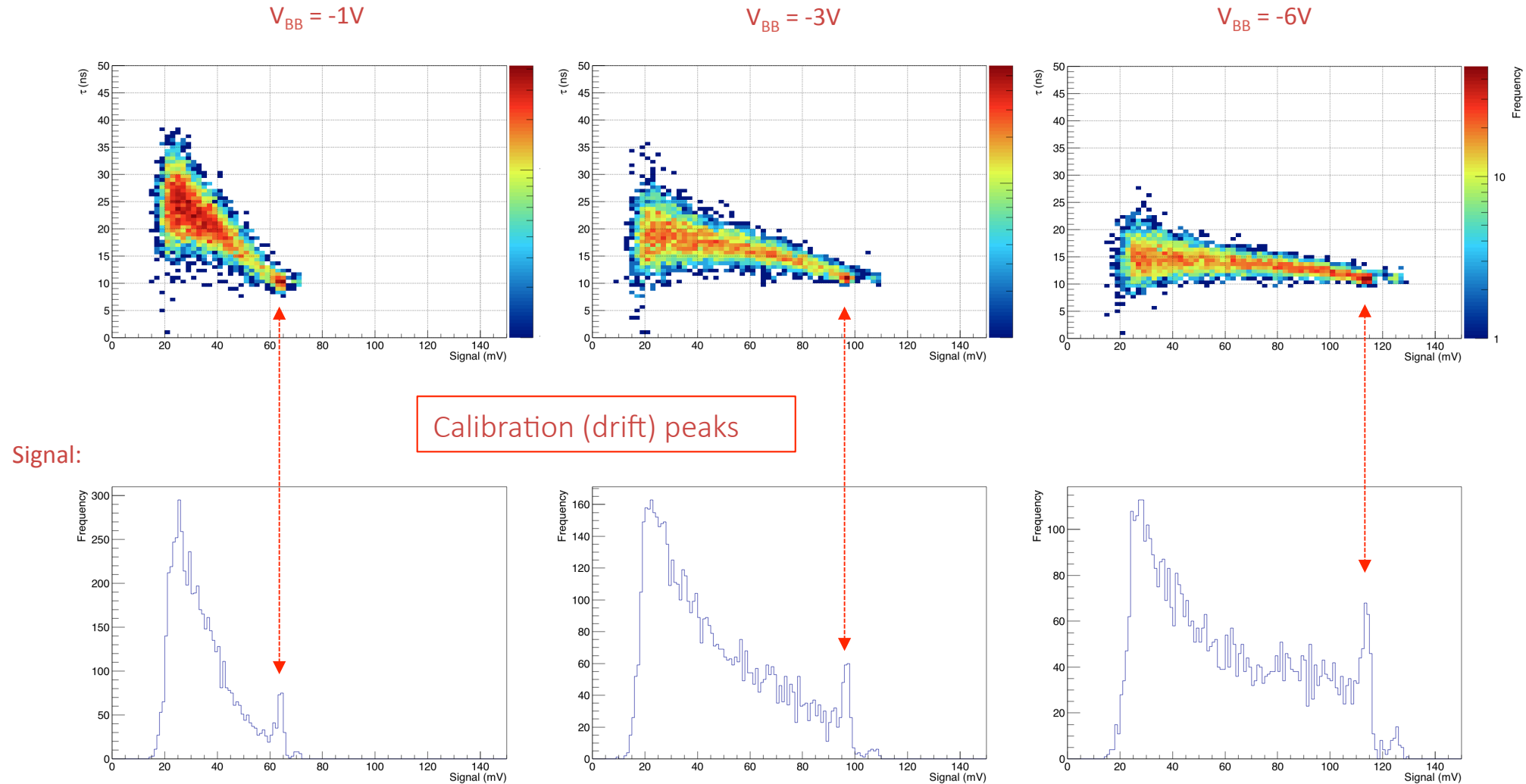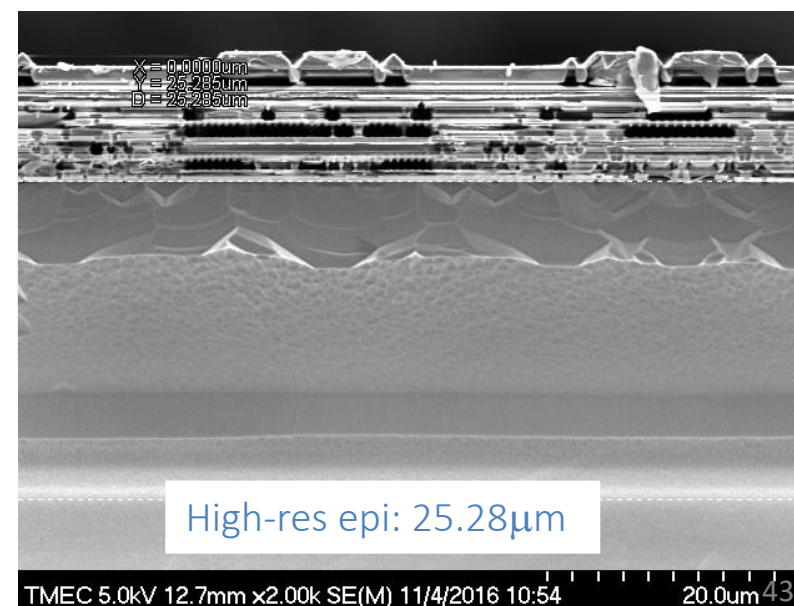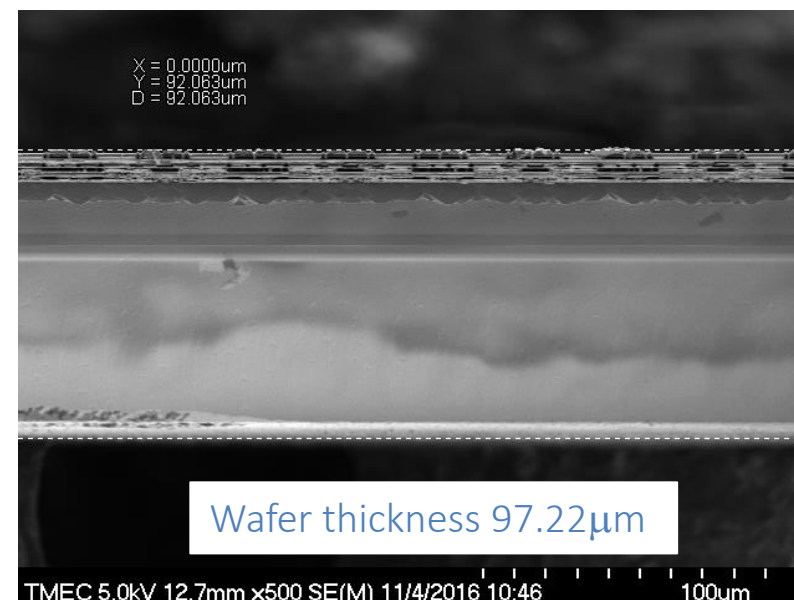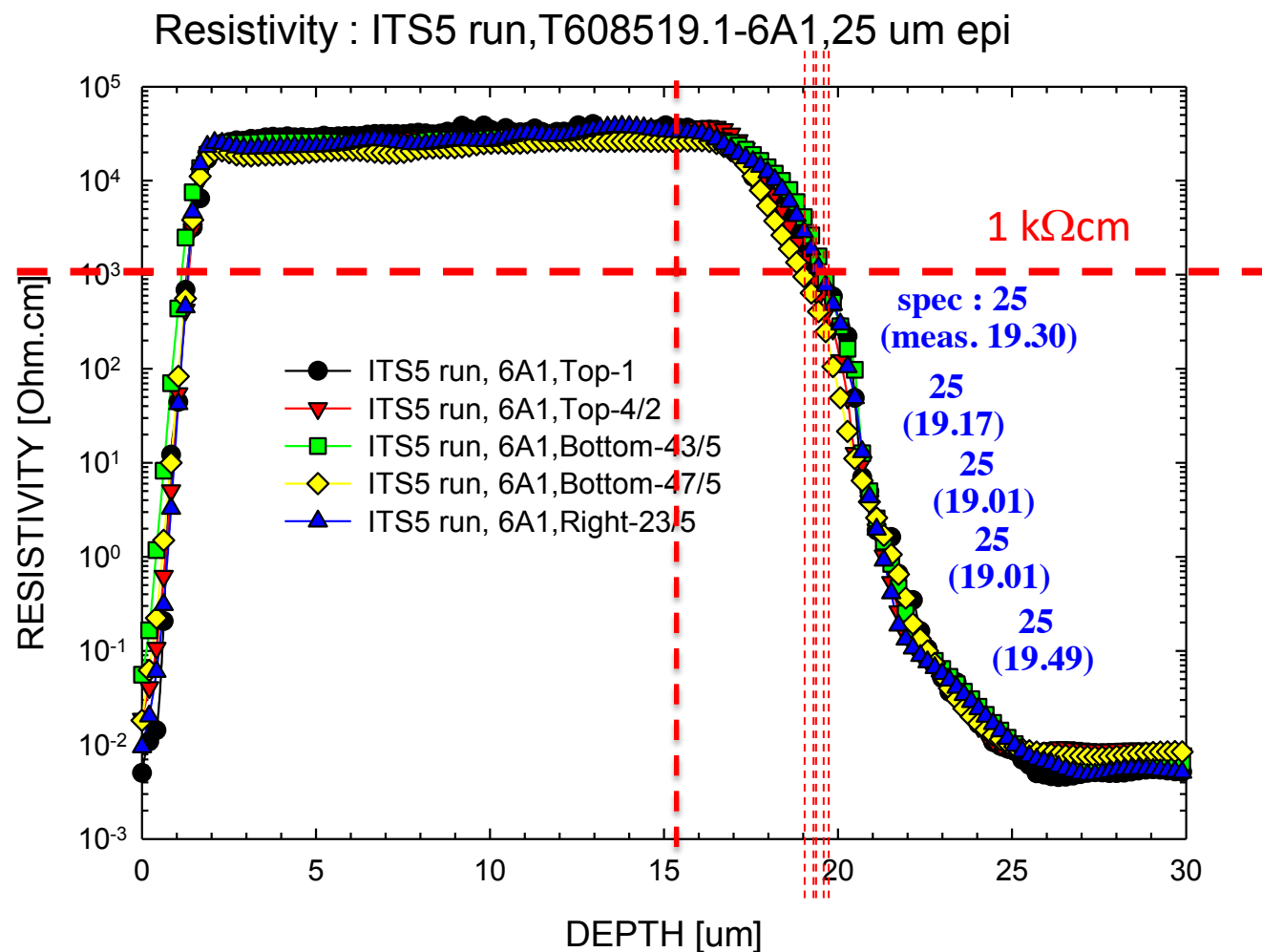
Tests performed on investigator chip (same pixel as ALPIDE) with analogue readout

Pixel size: 28 x 28 μm^2,   CE: 2 x 2 μm^2 centered in a 8 x 8 μm^2 opening,   P-well & substrate @ -6V, CE @ 1V

V_{BB} = -1V V_{BB} = -3V V_{BB} = -6V

Calibration (drift) peaks

Signal:

ALICE CMOS Pixel Sensor

Blank Wafers QA at TMEC (SRP and XSEM measurements)

Resistivity : ITS5 run,T608519.1-6A1,25 um epi

1 kΩcm

spec : 25
(meas. 19.30)
25
(19.17)
25
(19.01)
25
(19.01)
25
(19.49)

Legend:
- ITS5 run, 6A1,Top-1
- ITS5 run, 6A1,Top-4/2
- ITS5 run, 6A1,Bottom-43/5
- ITS5 run, 6A1,Bottom-47/5
- ITS5 run, 6A1,Right-23/5

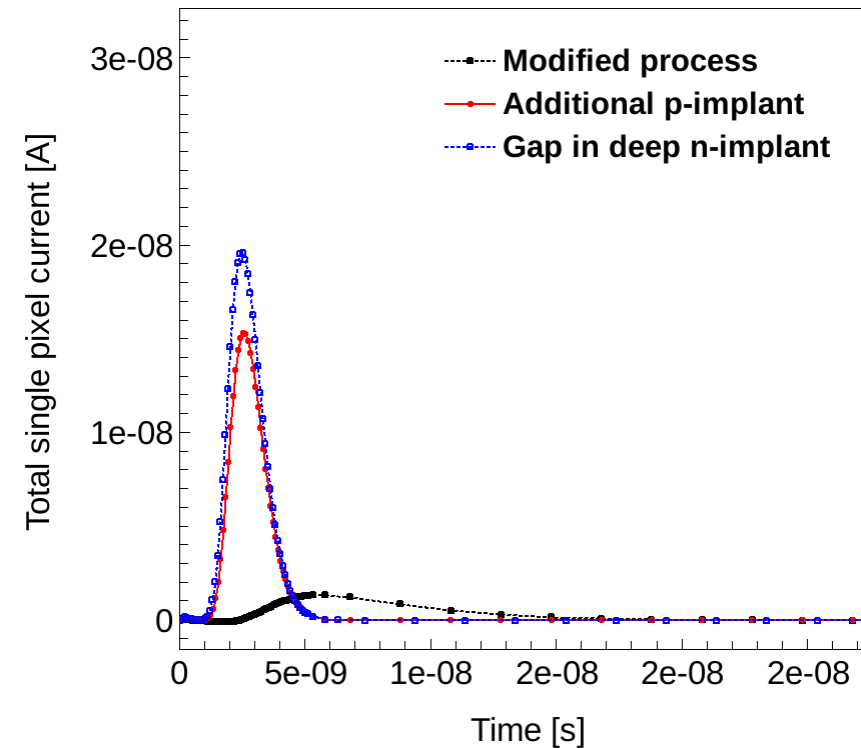Wafer thickness 97.22µm

High-res epi: 25.28µm

Current pulse signal

Magdalena Munker (CERN), Pixel 2018 (Taipei - Dec 2018)

Before Irradiation
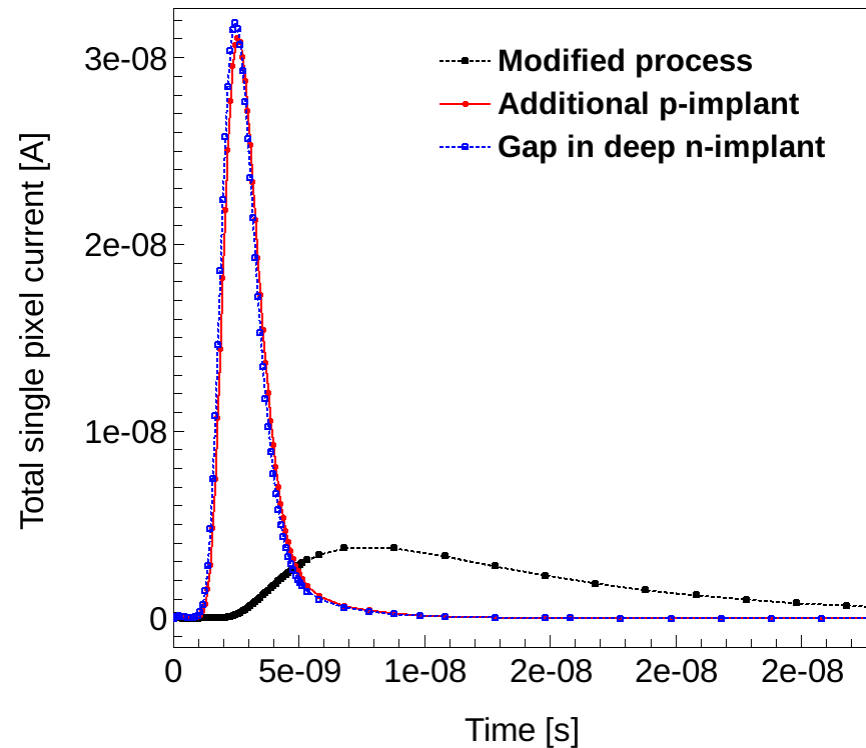
After Irradiation

Significantly faster charge collection for design with additional p-implant and gap in n-layer

New prototypes with both type of further process modifications are presently being tested