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Deep Machine Learning on FPGAs for L1 trigger and Data Acquisition

Machine learning is becoming ubiquitous across HEP. There is great potential to improve trigger and DAQ performances with it. However, the exploration of such techniques within the field in low latency/power FPGAs has just begun. We present HLS4ML, a user-friendly software, based on High-Level Synthesis (HLS), designed to deploy network architectures on FPGAs. As a case study, we use HLS4ML for boosted-jet tagging with deep networks at the LHC. We map out resource usage and latency versus network architectures, to identify the typical problem complexity that HLS4ML could deal with. We discuss possible applications in current and future HEP experiments.

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