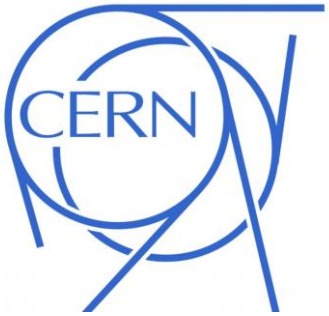
# FCC Radiation Environment: An Unprecedented Challenge For MOS Transistors

GIULIO BORGHELLO
giulio.borghello@cern.ch




| RADIATION EFFECTS | IONIZING | NON-IONIZING |
|---|---|---|
| CUMULATIVE | TOTAL IONIZING DOSE (TID) | DISPLACEMENT DAMAGE |
| STOCHASTIC | ~~SINGLE EVENT EFFECTS~~ | ---------- |

Cumulative: The higher the dose, the larger the damage.

SI unit of measure for TID:

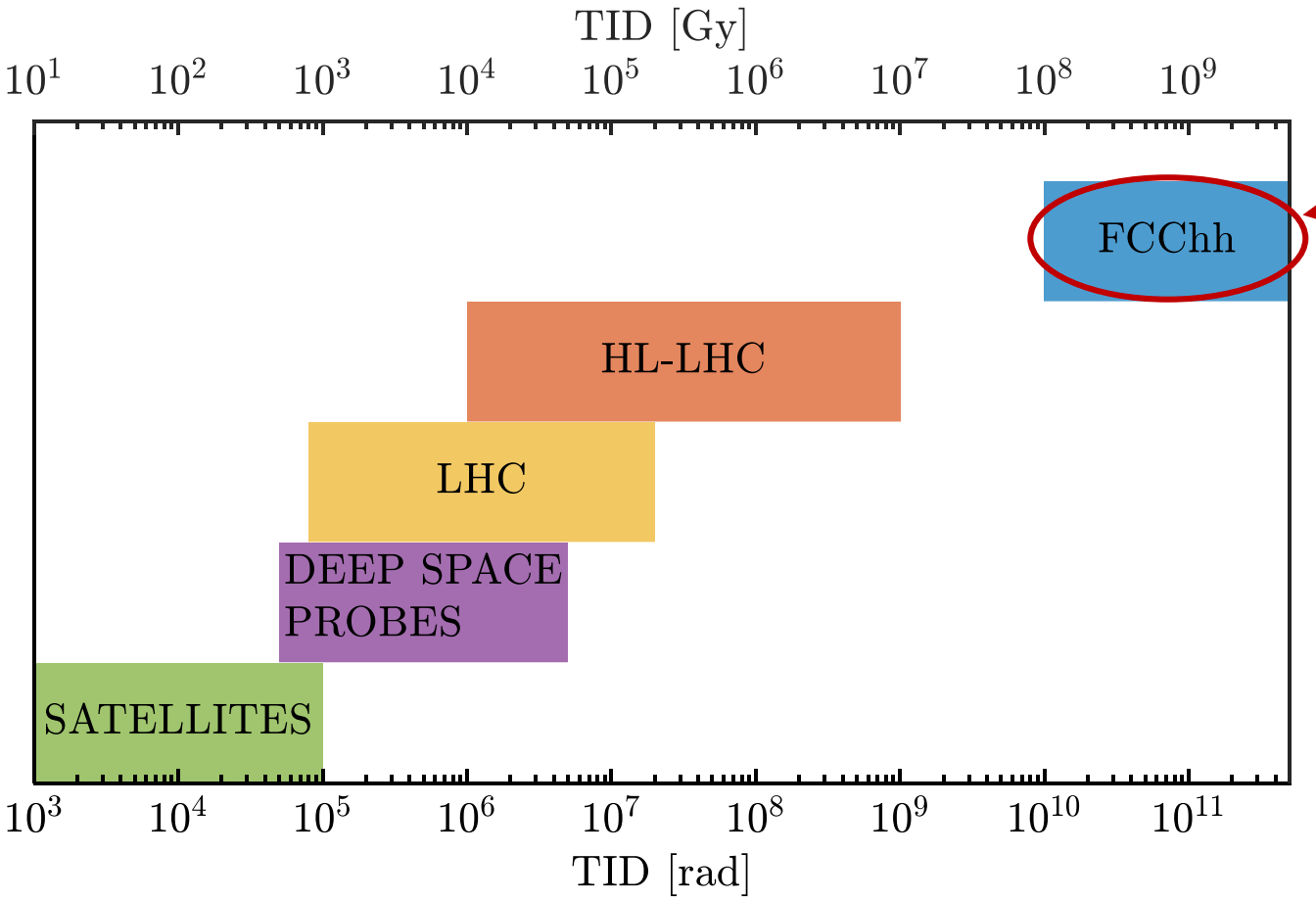
**Gy (*gray*); 1 Gy = 1 J/Kg**

Often used:

**rad *(radiation absorbed dose)*; 1 rad = 100 erg/g**

Therefore:

**1 Gy = 100 rad**




0.1-5 GGy
=
10-500 Grad

Huge TID!

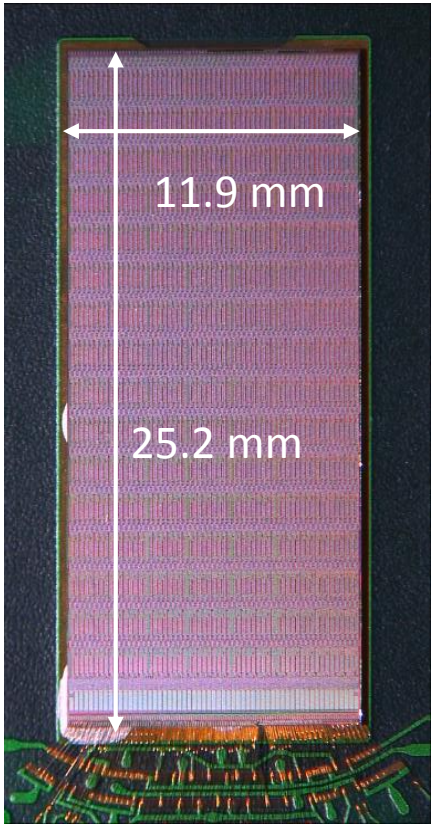
How MOS transistors respond to TID?

Why should we care about it?

| Processor | N. Transistor | Year | Designer |
|---|---|---|---|
| Apple A11 Bionic (hexa-core ARM64 "mobile SoC") | 4,300,000,000 | 2017 | Apple |
| 8-core Ryzen | 4,800,000,000 | 2017 | AMD |
| IBM z14 | 6,100,000,000 | 2017 | IBM |
| Xbox One X (Project Scorpio) main SoC | 7,000,000,000 | 2017 | Microsoft/AMD |
| Centriq 2400 | 18,000,000,000 | 2017 | Qualcomm |

Source: *https://en.wikipedia.org/wiki/Transistor_count*

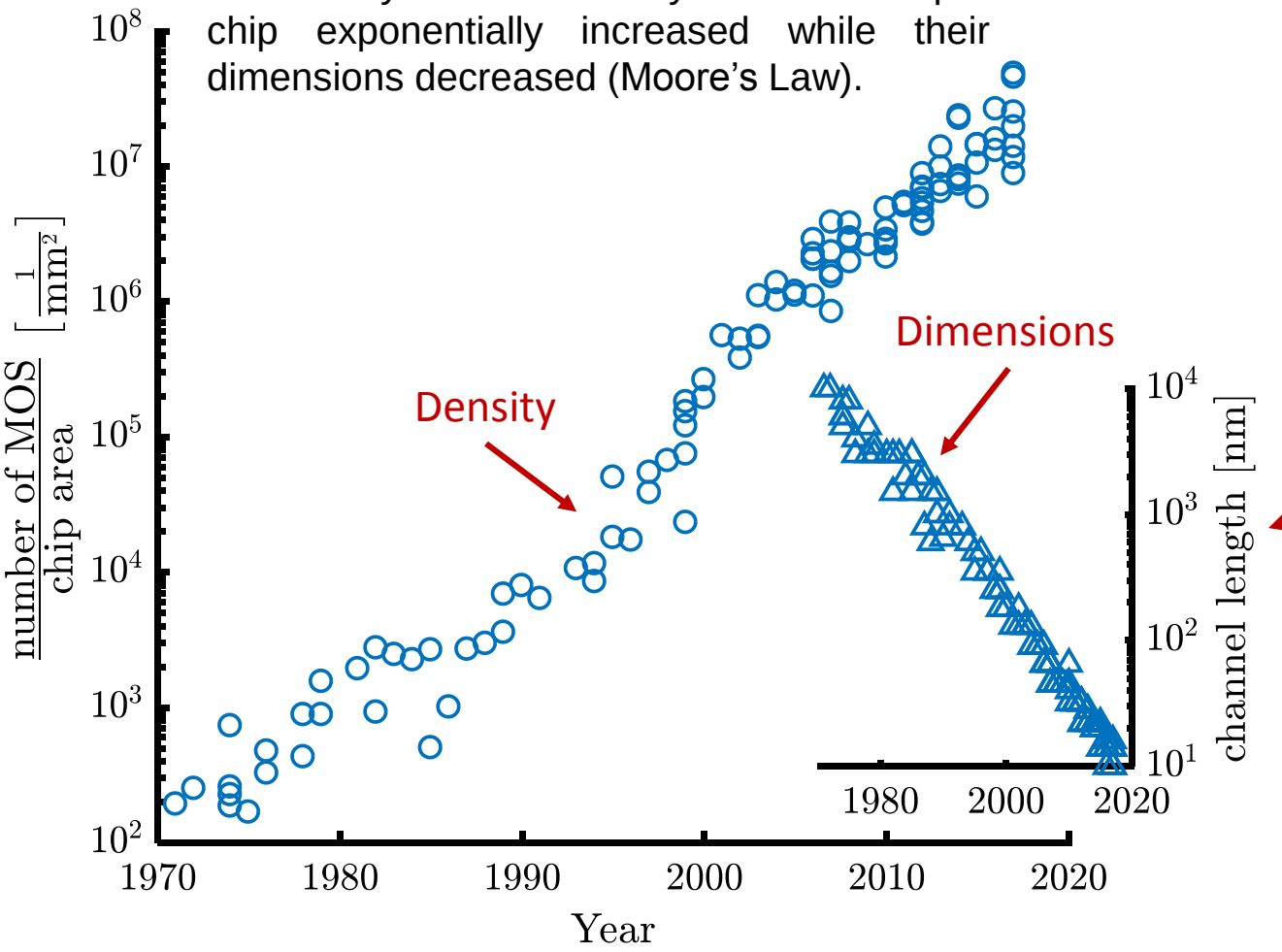
Example:
**MPA** (Macro Pixel ASIC)
For **CMS** outer tracker:
**~1.5M of transistors**




Courtesy of Davide Ceresa,
CERN (EP-ESE-ME section)

Billions of transistors
for each experiment!

Over the years the density of MOSFET per chip exponentially increased while their dimensions decreased (Moore's Law).



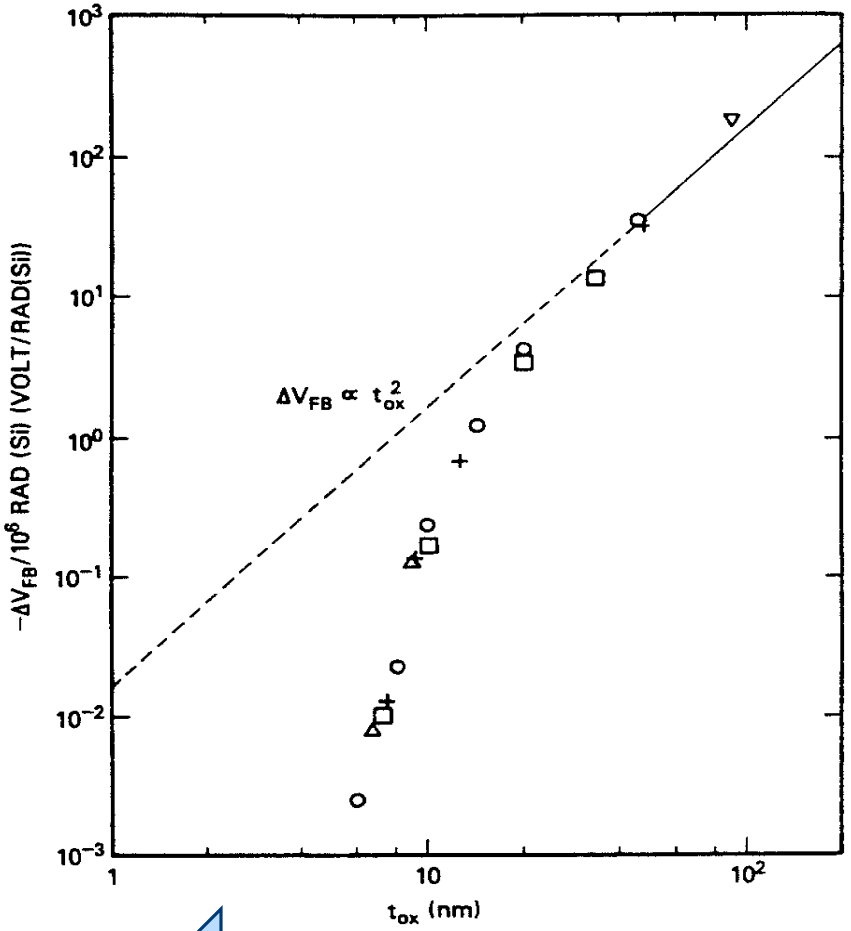

Source: *https://en.wikipedia.org/wiki/Transistor_count*

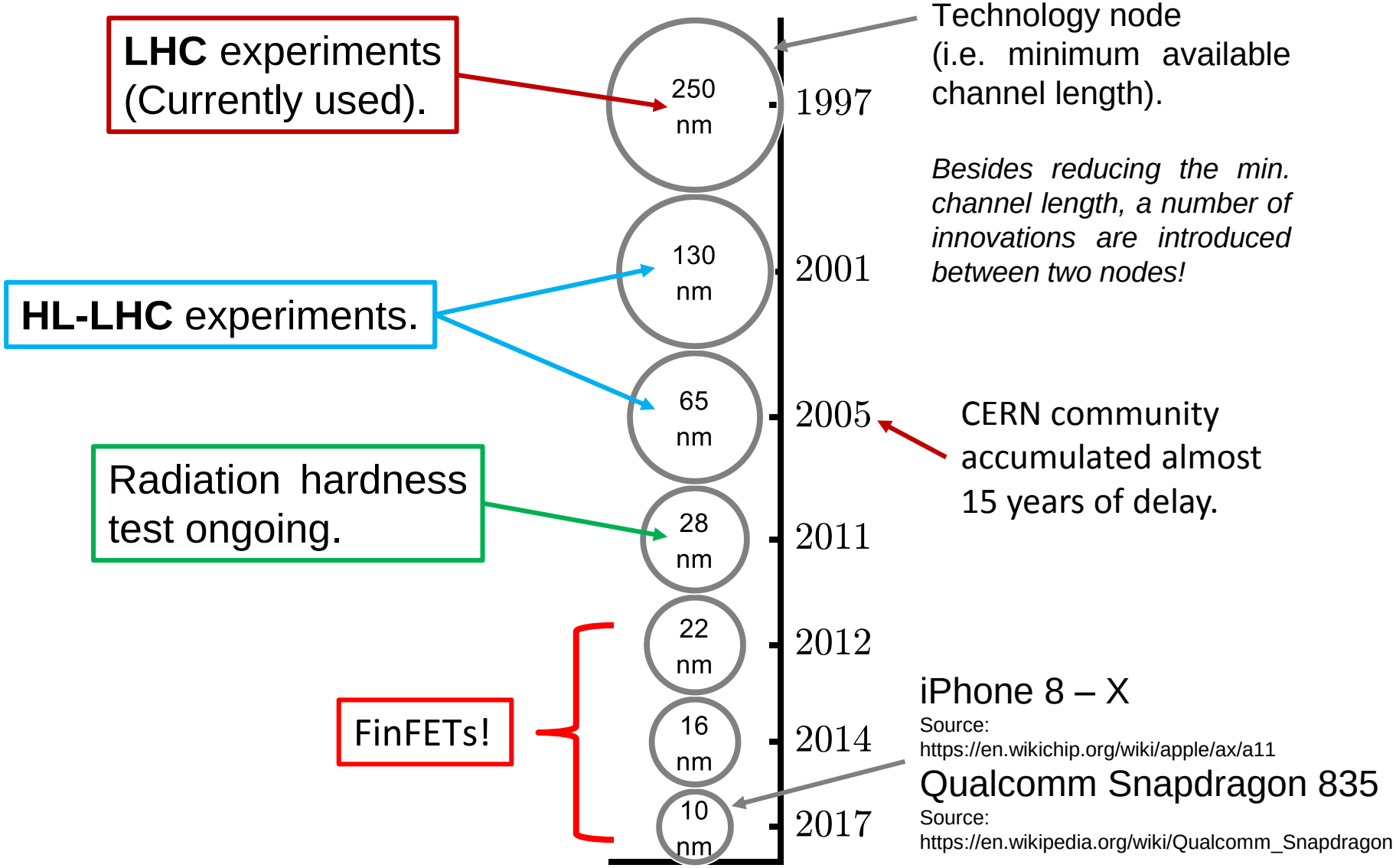
Minimum available channel length (i.e. technology node).

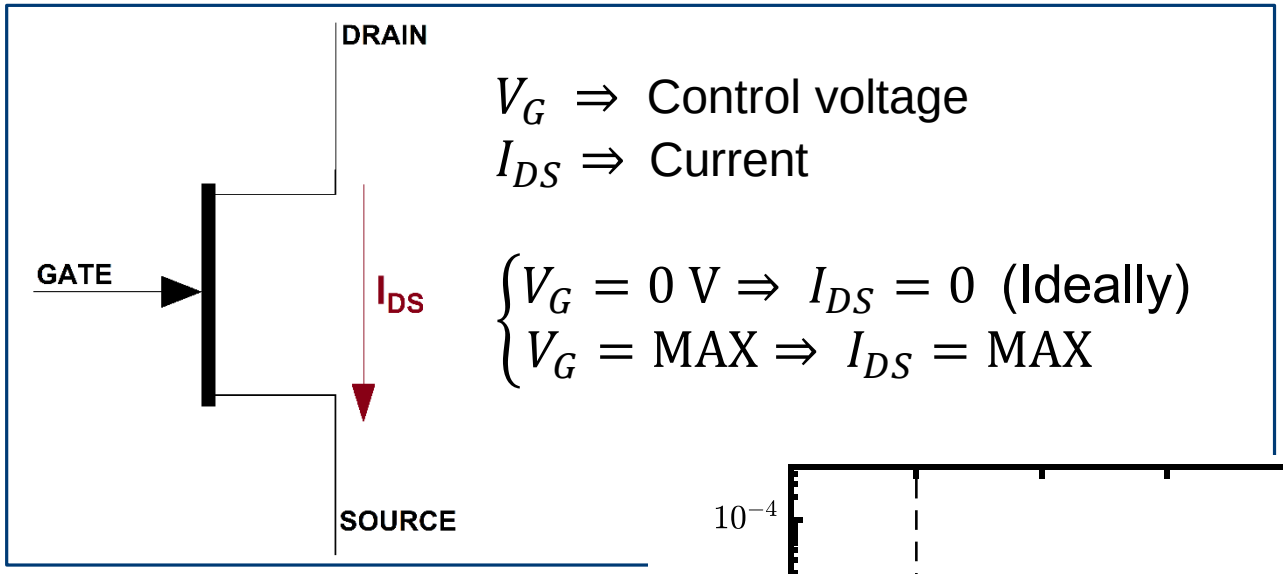
*Besides reducing the min. channel length, a number of innovations are introduced between two nodes!*

***Some aspects*** of MOS radiation response improve with scaling.

Saks, N. S., et al. IEEE Trans. on Nucl. Sci. 31.6 (1984): 1249-1255.




**LHC** experiments (Currently used).
**HL-LHC** experiments.
Radiation hardness test ongoing.
FinFETs!
250 nm
130 nm
65 nm
28 nm
22 nm
16 nm
10 nm
1997
2001
2005
2011
2012
2014
2017
Technology node (i.e. minimum available channel length).
*Besides reducing the min. channel length, a number of innovations are introduced between two nodes!*
CERN community accumulated almost 15 years of delay.
iPhone 8 – X
Source: https://en.wikichip.org/wiki/apple/ax/a11
Qualcomm Snapdragon 835
Source: https://en.wikipedia.org/wiki/Qualcomm_Snapdragon



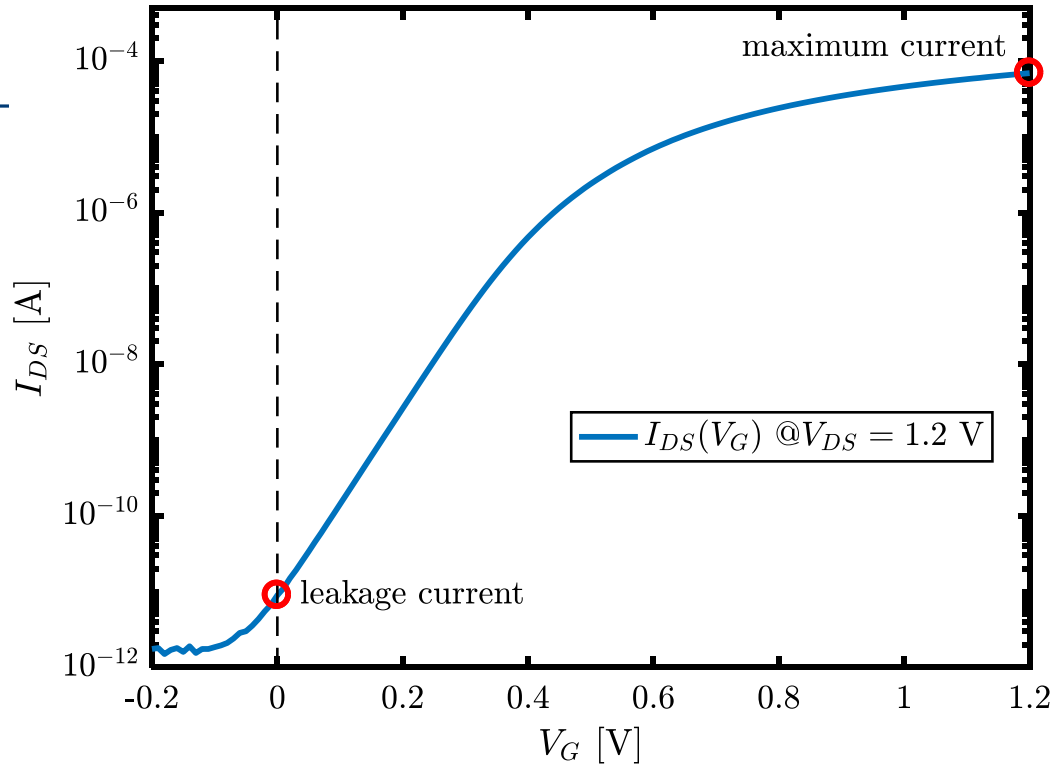

$V_G \Rightarrow$ Control voltage

$I_{DS} \Rightarrow$ Current

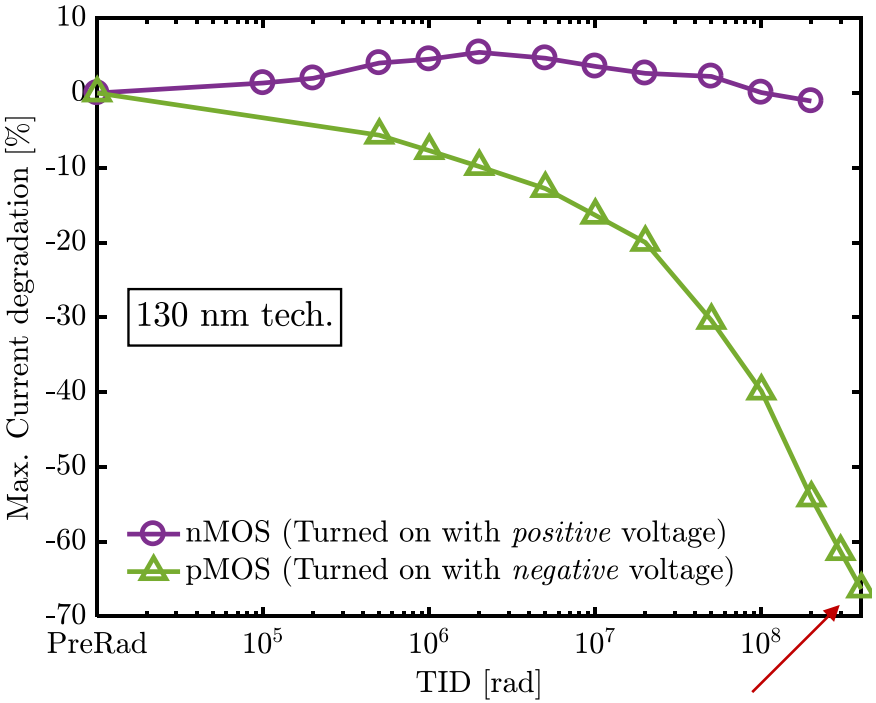
$$\begin{cases} V_G = 0\ \text{V} \Rightarrow\ I_{DS} = 0\ \text{(Ideally)} \\ V_G = \text{MAX} \Rightarrow\ I_{DS} = \text{MAX} \end{cases}$$

We want:

- **High** maximum current.
- **Low** leakage current.



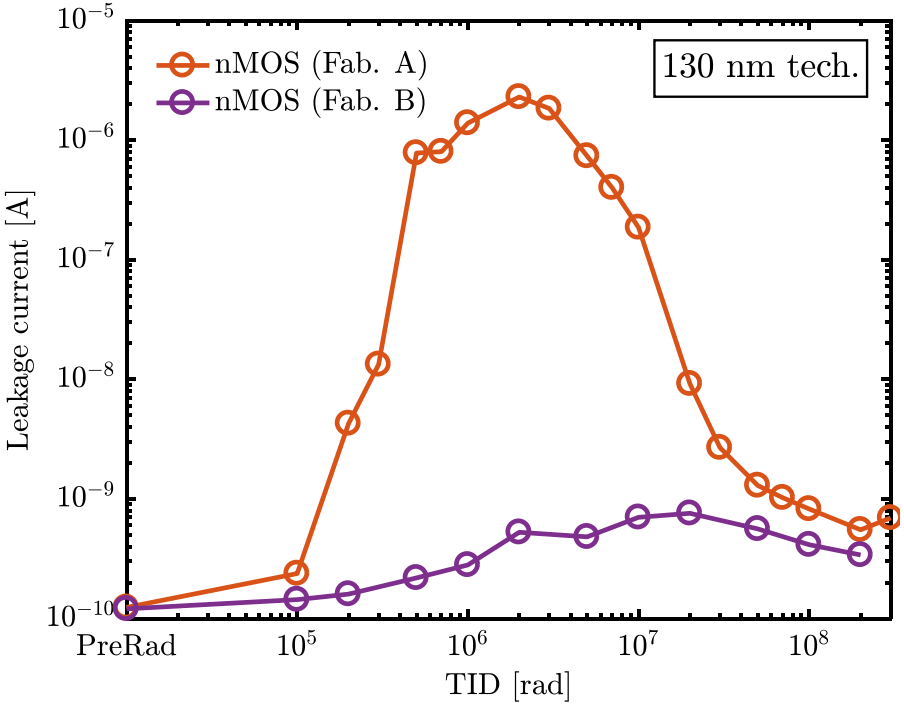
# 130 nm



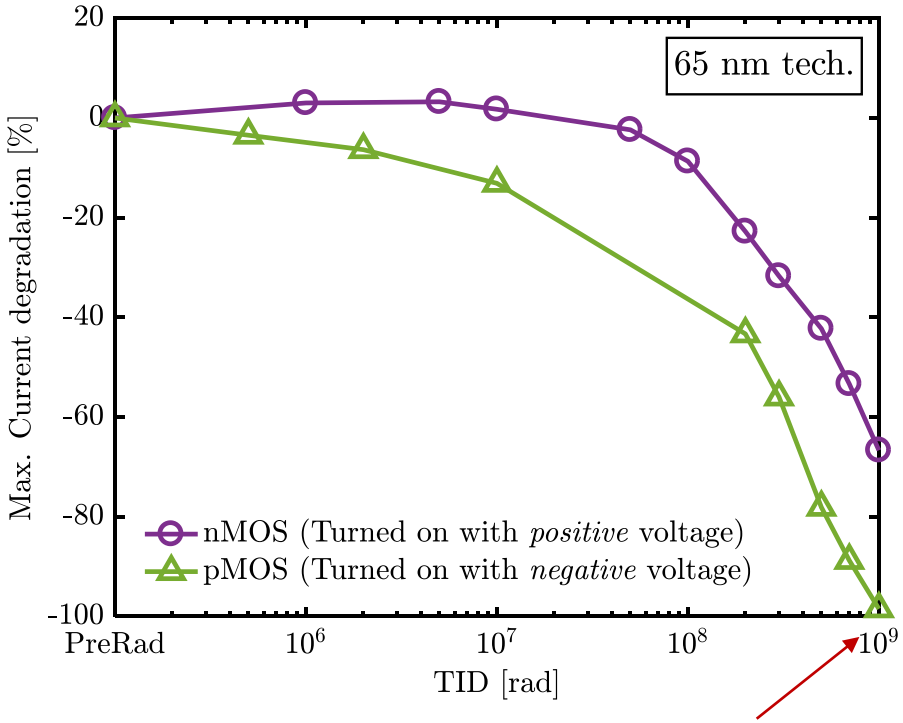

Severe maximum current degradation for pMOS.

~-70% @400 Mrad

- Large increase of leakage current.
- Peak around 1~3 Mrad.
- Extremely process-dependent.



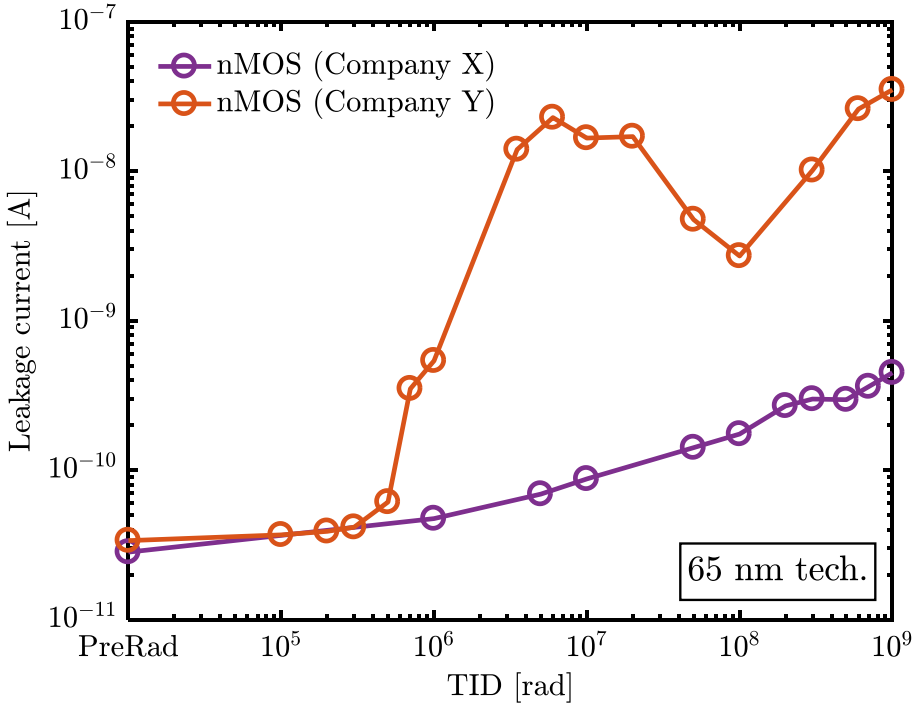
65 nm




Severe maximum current degradation.

~-100% @1 Grad

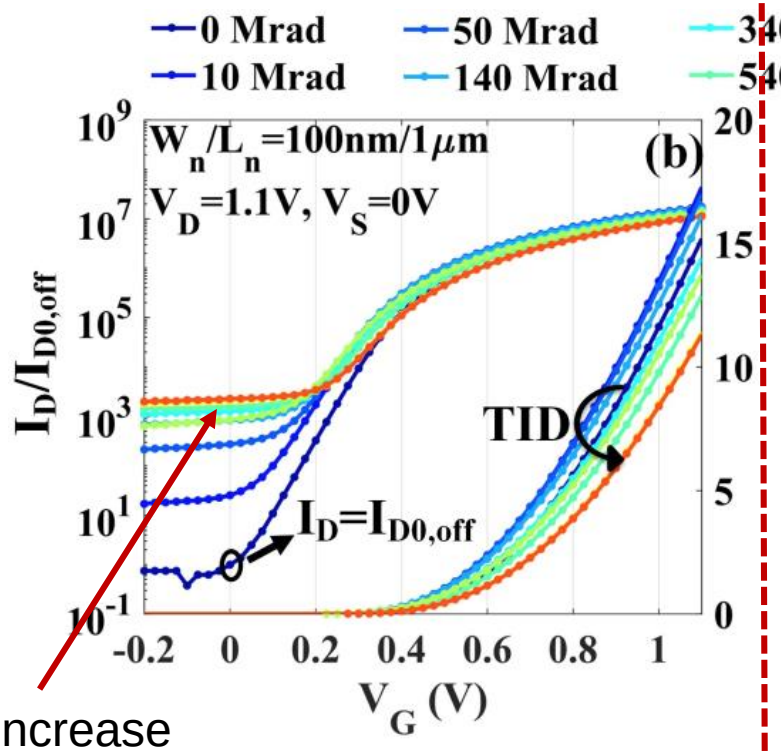
Large increase of leakage current in some manufacturers.



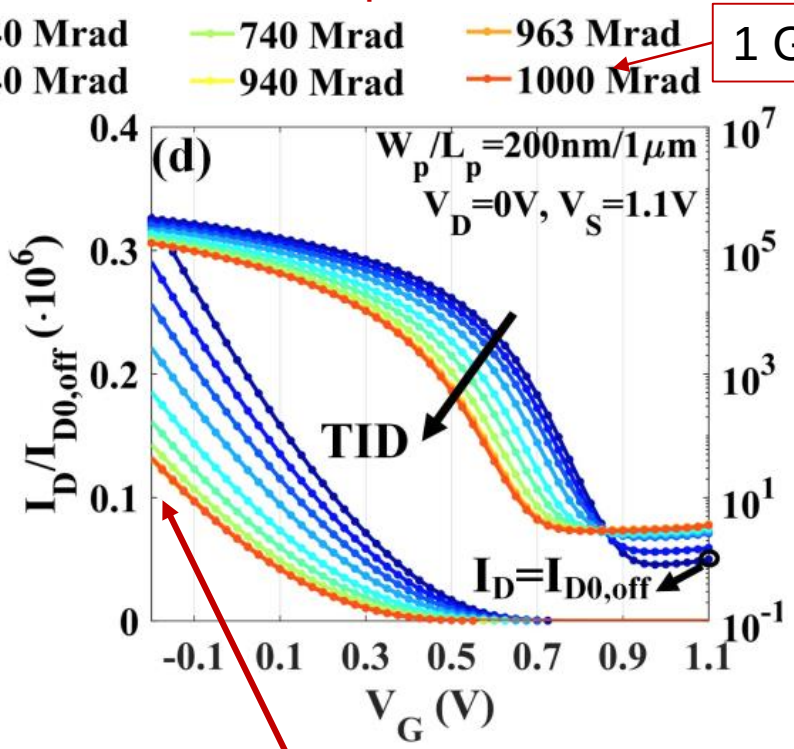
Results obtained in the context of the *Scaltech28* (INFN) and *GigaRadMOST* (SNSF) projects.

28 nm

nMOS




pMOS




1 Grad

Large increase of leakage current in nMOS.

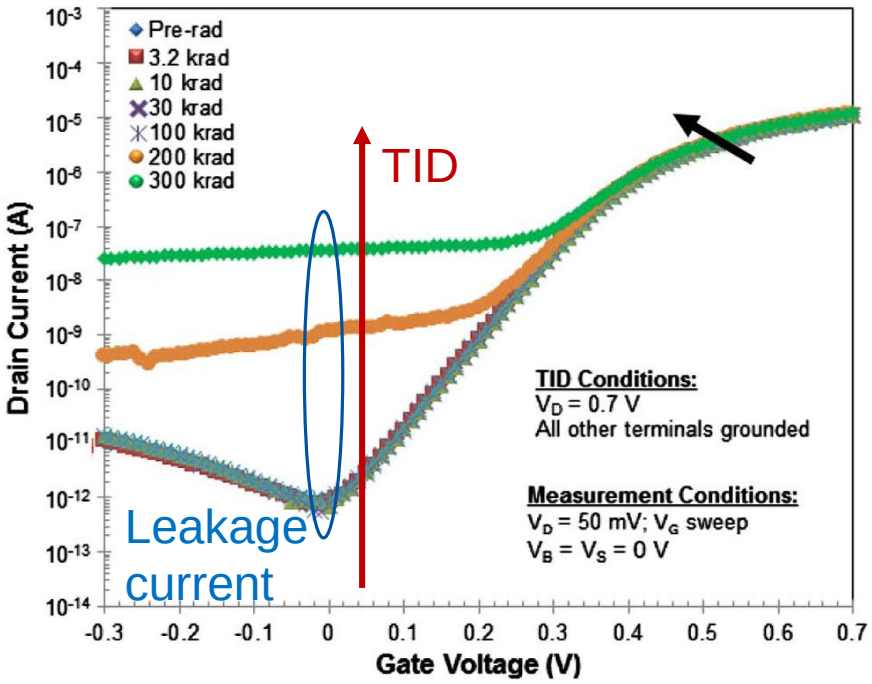
Severe maximum current degradation in pMOS.

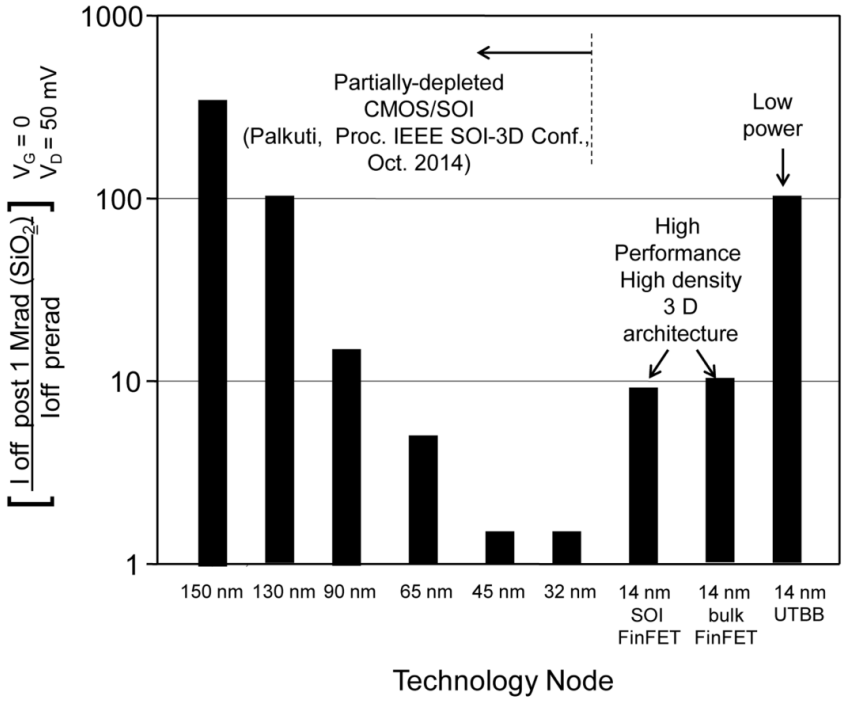
*After* C.Zhang et al., "Characterization of GigaRad Total Ionizing Dose and Annealing Effects on 28 nm Bulk MOSFETs", IEEE TNS 64, n.10, Oct.2017.

Below 28 nm:
**Planar MOSFETs → FinFETs**

FinFETs ≤22 nm

Large increase of leakage current!



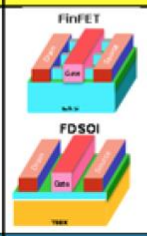
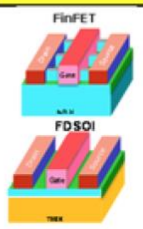
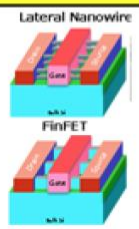
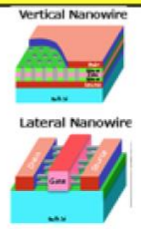
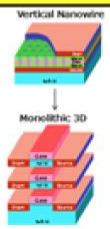
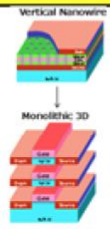
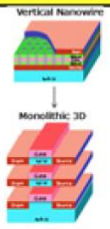



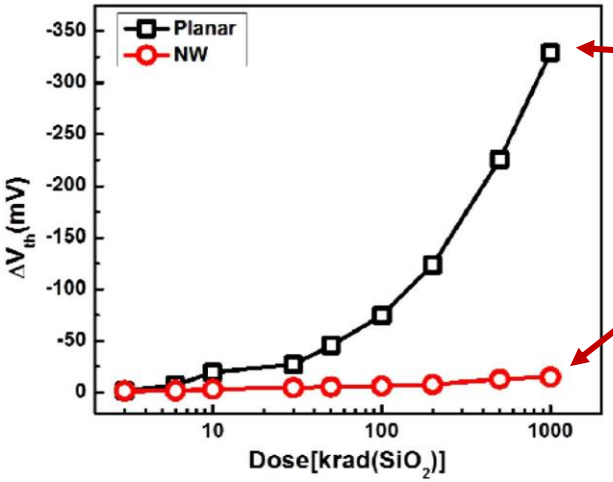

*After* I.Chatterjee et al., “Bias Dependence of Total-Dose Effects in Bulk FinFETs”, IEEE TNS 60, n.6, 2013

*After* H. Hughes *et al.*, "Total Ionizing Dose Radiation Effects on 14 nm FinFET and SOI UTBB Technologies," *2015 IEEE Radiation Effects Data Workshop (REDW)*, Boston, MA, 2015, pp. 1-6.

# Future technologies (likable)

Source: *International roadmap for devices and systems - 2016 edition - more moore white paper "https://irds.ieee.org/images/files/pdf/2016_MM.pdf"*

| YEAR OF PRODUCTION | 2015 | 2017 | 2019 | 2021 | 2024 | 2027 | 2030 |
|---|---|---|---|---|---|---|---|
| Logic device technology naming | P70M56 | P54M36 | P42M24 | P32M20 | P24M12G1 | P24M12G2 | P24M12G3 |
| Logic industry "Node Range" Labeling (nm) | "16/14" | "11/10" | "8/7" | "6/5" | "4/3" | "3/2.5" | "2/1.5" |
| Logic device structure options | finFET FDSOI | finFET FDSOI | finFET LGAA | finFET LGAA VGAA | VGAA, M3D | VGAA, M3D | VGAA, M3D |
| |   |   |   |   |   |   |   |




"Standard" MOSFET

Gate All Around (GAA) nanowire

*After* S. Ren *et al.*, in *IEEE Transactions on Nuclear Science*, vol. 62, no. 6, pp. 2888-2893, Dec. 2015.

New technologies could be more rad-hard, but:

- Very small literature on TID effects.
- We are very far from commercial products.

Expected TID in FCC-hh:

10 – 500 Grad

X-ray irradiation facility at CERN can provide (MAX):

~10 Mrad/h

To perform TID experiments:

~40 days – 5+ years

# Displacement Damage

MOSFET are usually not sensitive to DD.

However in FCC-hh fluence can be two order of magnitude higher than in the HL-LHC!

Has to be tested!

# CONCLUSIONS

- Huge expected TID.
- Planar MOSFET technology currently used cannot withstand this TID.
- Radiation response of FinFETs does not seem to be promising.
- Too early to tell if new commercial technologies will be more rad-hard (at the expected ultra-high TID levels).
- Ways to perform high-TID experiments within a reasonable time have to be found.
- DD may lead to additional failure mechanisms.