



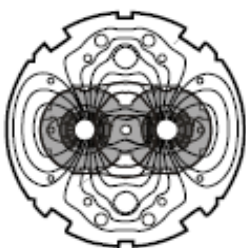
LHC Hardware Commissioning

Documentation on Powering Tests

**MPP, kick-off meeting
Sept 21st 2006**

frm

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AB/AT/TS

EDMS Document No.

477145

Date: 2004-09-29

Engineering Specification

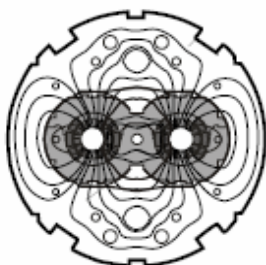
RELEASED

GENERAL PROCEDURE FOR THE COMMISSIONING OF THE ELECTRICAL CIRCUITS OF A SECTOR

Abstract

This document describes the sequence of the steps which lead to the commissioning of the electrical circuits of each sector. It gives the backbone of the general procedures and refers to more detailed documents which in turn describe the individual system tests and hardware commissioning procedures.

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Hardware Commissioning Procedure

THE COMMISSIONING OF THE HARDWARE IN THE LHC SECTORS

POWERING OF THE SUPERCONDUCTING CIRCUITS OF A SECTOR UP TO NOMINAL CURRENT

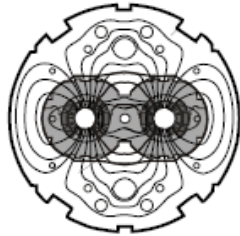
Abstract

This document describes the sequence of the steps which lead to the powering of the superconducting circuits of a sector to nominal current. It covers the phases after the connection of the power cables to the current leads up to the powering in unison of all the circuits of a sector to nominal current.

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	PIC2	PLI1							PLI2						PLI3				P L I 4	PNO						P A C						
		1	2	3	4	5	6	7	1	2	3	4	5	6	1	2	3	4		1	2	3	4	5	6							
13kA Main																																
IP Q&D																																
600A EE																																
600A no EE crowbar																																
600A no EE																																
80-120A																																
60A																																

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TS

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758068

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Hardware Commissioning Procedure

THE COMMISSIONING OF THE HARDWARE IN THE LHC SECTORS

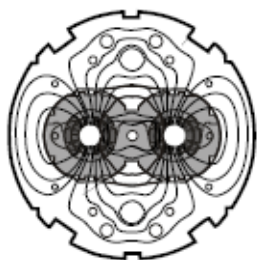
POWERING STRATEGIES FOR THE COMMISSIONING OF THE SUPERCONDUCTING CIRCUITS IN SECTORS 7-8 AND 8-1

IN WORK

Abstract

The present document describes the schedule of the activities which lead to the powering of the superconducting circuits of the LHC sectors 7-8 and 8-1. After specifying the superconducting electrical circuits present in sectors 7-8 and 8-1 together with the commissioning procedures required by each one, the commissioning strategy is defined and the detailed schedule (sets of the day) presented taking into consideration the constraints given by the different subsystem responsible (e.g. power converters, magnets, DFBs, etc.).

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531773

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Hardware Commissioning Procedure

THE COMMISSIONING OF THE HARDWARE IN THE LHC SECTORS

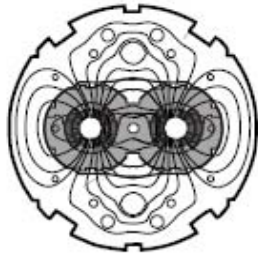
THE COMMISSIONING OF THE INNER TRIPLER REGION

Abstract

This document describes the sequence of the steps which lead to the commissioning of **the complete inner triplet**. It gives the backbone of the general procedures and refers to more detailed documents associated to the different systems, which in turn describe the individual system tests and the hardware commissioning procedures.

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AB/AT/TS

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573115

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Test Procedure

THE COMMISSIONING OF THE HARDWARE IN THE LHC SECTORS

GENERAL PROCEDURE FOR THE COMMISSIONING OF THE WARM ELECTRICAL CIRCUITS

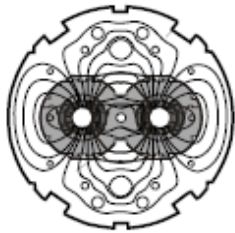
Abstract

This document describes the set of tests which will be carried-out to condition and validate for operation all **the components of the electrical circuits for the normal conducting magnets.**

These tests also include the commissioning of the controls, the timing and interlock system (WIC).

IN WORK

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EDMS Document No.

766220

Date: 2006-08-11

Hardware Commissioning Procedure

THE COMMISSIONING OF THE HARDWARE IN THE LHC SECTORS

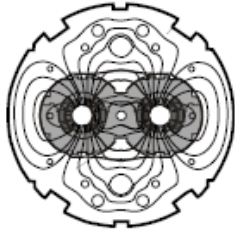
SPECIFICATIONS OF THE POST-MORTEM ANALYSIS TOOLS FOR THE MAIN EQUIPMENT OF THE LHC SUPERCONDUCTING CIRCUITS

IN WORK

Abstract

This document describes the tools required by the power converters, the powering interlock and the quench protection systems for managing and analysing the post-mortem data.

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EDMS Document No.

766988

Date: 2006-08-16

Hardware Commissioning Procedure

THE COMMISSIONING OF THE HARDWARE IN THE LHC SECTORS

SPECIFICATION OF THE POST-MORTEM GLOBAL ANALYSIS TOOLS FOR THE LHC SUPERCONDUCTING CIRCUITS

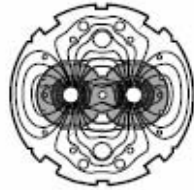
IN WORK

Abstract

After a failure during the operation or the commissioning of the LHC, as well as following every test carried out during the so-called powering tests of the superconducting circuits, a coherent set of post-mortem information will be required from the various sub-systems involved in the event to analyse the causes of the failure or to evaluate the results of the test.

As a prolongation of the document [1] describing the specifications for the Post-Mortem analysis tools necessary to each main system alone (i.e. quench protection, power converters and PIC), this document describes the specifications for the post-mortem tool needed for the so-called global analysis of the superconducting circuits.

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Engineering Specification

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**THE COMMISSIONING OF THE HARDWARE IN THE LHC
SECTORS**

FAILURE SCENARIOS FOR THE ELECTRICAL CIRCUITS

Abstract

This document describes the failure scenarios for the Electrical Circuits which are relevant during the Hardware Commissioning. The objective is to identify show stoppers and define the strategies to repair, recover or do with them.

Documents existing at present

□ Powering

- General procedure
- Powering to nominal of sc magnet circuits
- Powering to nominal of resistive magnet circuits
- Strategies (for optimizing durations)
- Inner triplets

□ Post-Mortem specifications

- Per system (QPS, PIC, converters)
- Global Analysis

□ Failure scenarios

- Electrical circuits (DC)