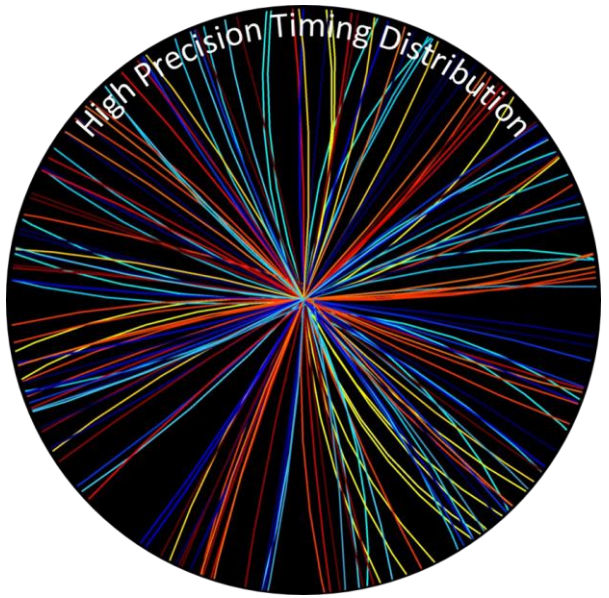
Xilinx FPGA transceiver study

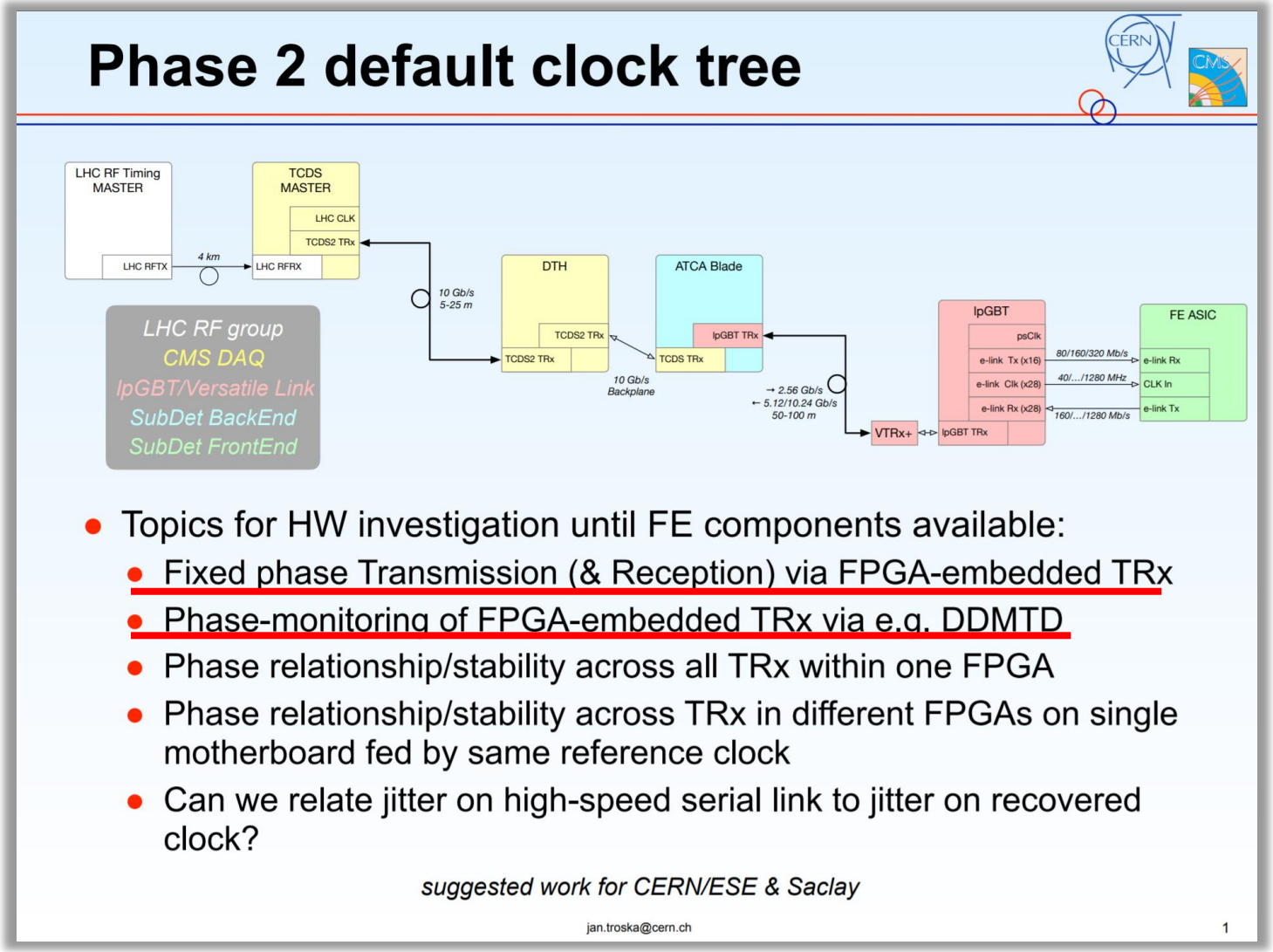


Eduardo Mendes
On behalf of the HPTD team (E. Mendes, S. Baron)

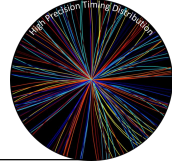
… many thanks to Jan Troska (CERN) and Paolo Novellini (Xilinx)

Motivation

- Investigation triggered by first CMS High Precision meeting
- Interesting to all LHC experiments
- Targeted Ultrascale+ GTH/GTY transceivers

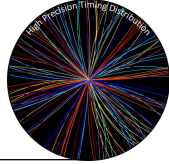


Outline



- Fixed and deterministic phase?
- Transmitter path
- Receiver path
- Phase monitoring aspects
- Conclusions

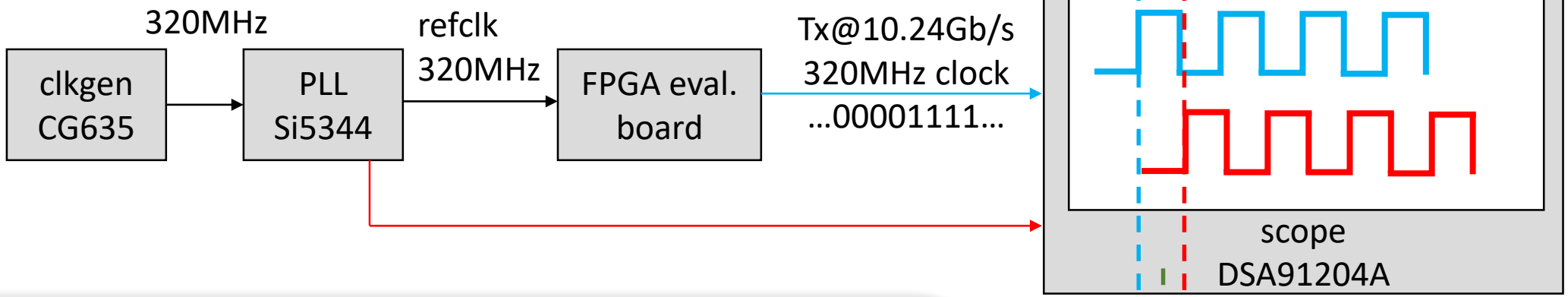
Fixed and deterministic phase?



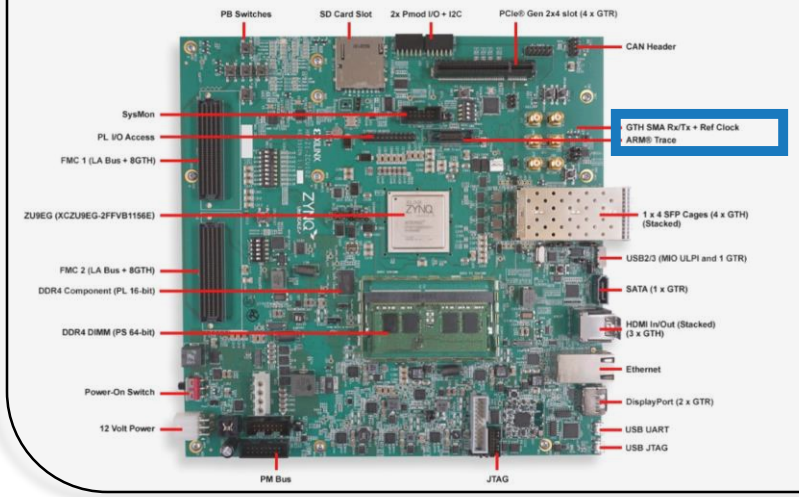
- Phase of a transceiver changes with reset
  - What can we achieve nowadays with the techniques learnt from the experience of developing ‘fixed-phase’ FPGA transceiver cores (e.g. GBT-FPGA, TTC-PON)?
- A device potentially impacted by many other factors (temperature, voltage, fabric logic utilization/activity)
- Is it relevant? How ‘fixed’ a ‘fixed phase’ has to be?
  - Physics phase monitoring based on collision monitoring
    - Aspects to be considered: accuracy, ‘refresh-rate’?
  - System-level impact?

Transmitter path

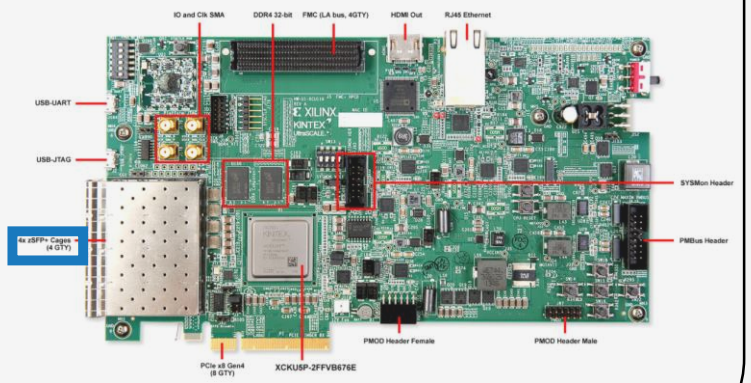
- Test setup

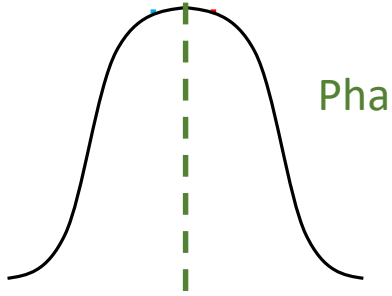


GTH tests with Zynq-Ultrascale+
ZCU102



GTY tests with Kintex-Ultrascale+
KCU116





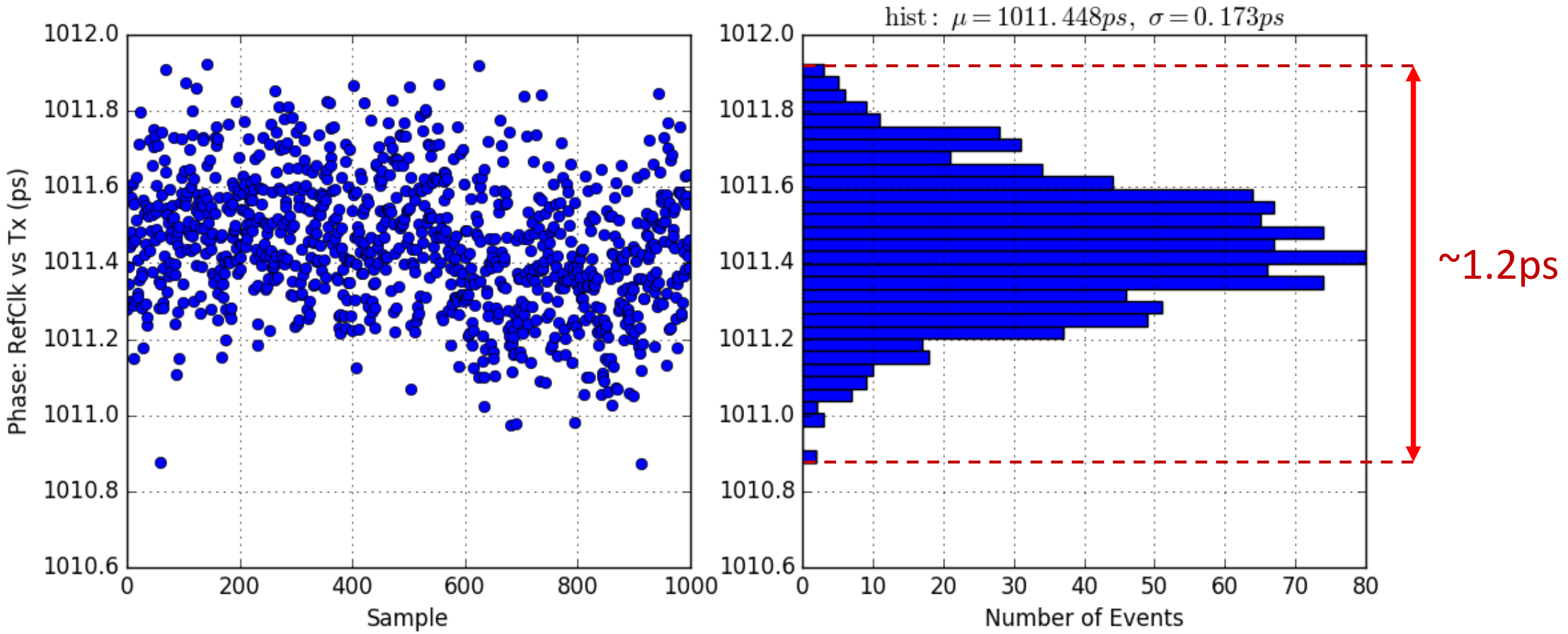
Phase (Delta time):
RefClk vs Tx

~600k samples
single shot - 2ms acquisition window

- parameters:
  - standard deviation (TIE rms)
  - average

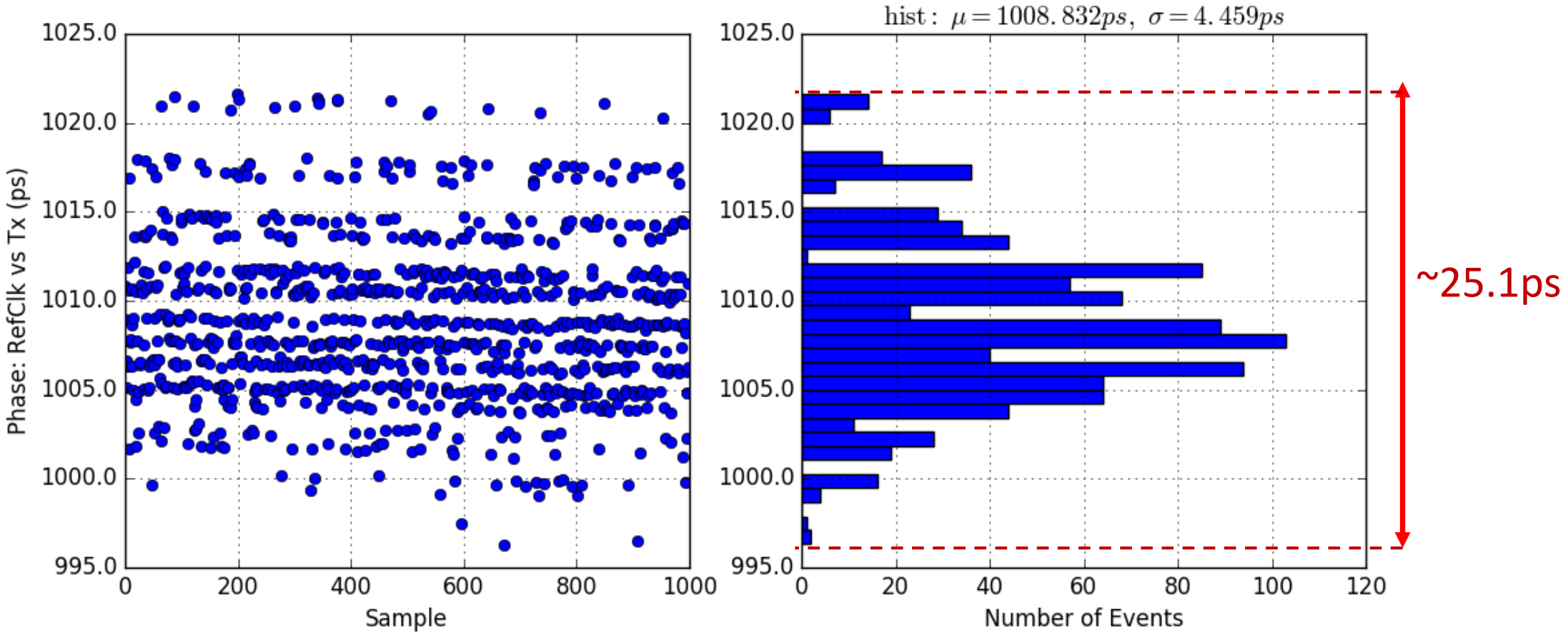
Transmitter path (no reset)

- Average: no reset - stable measurement



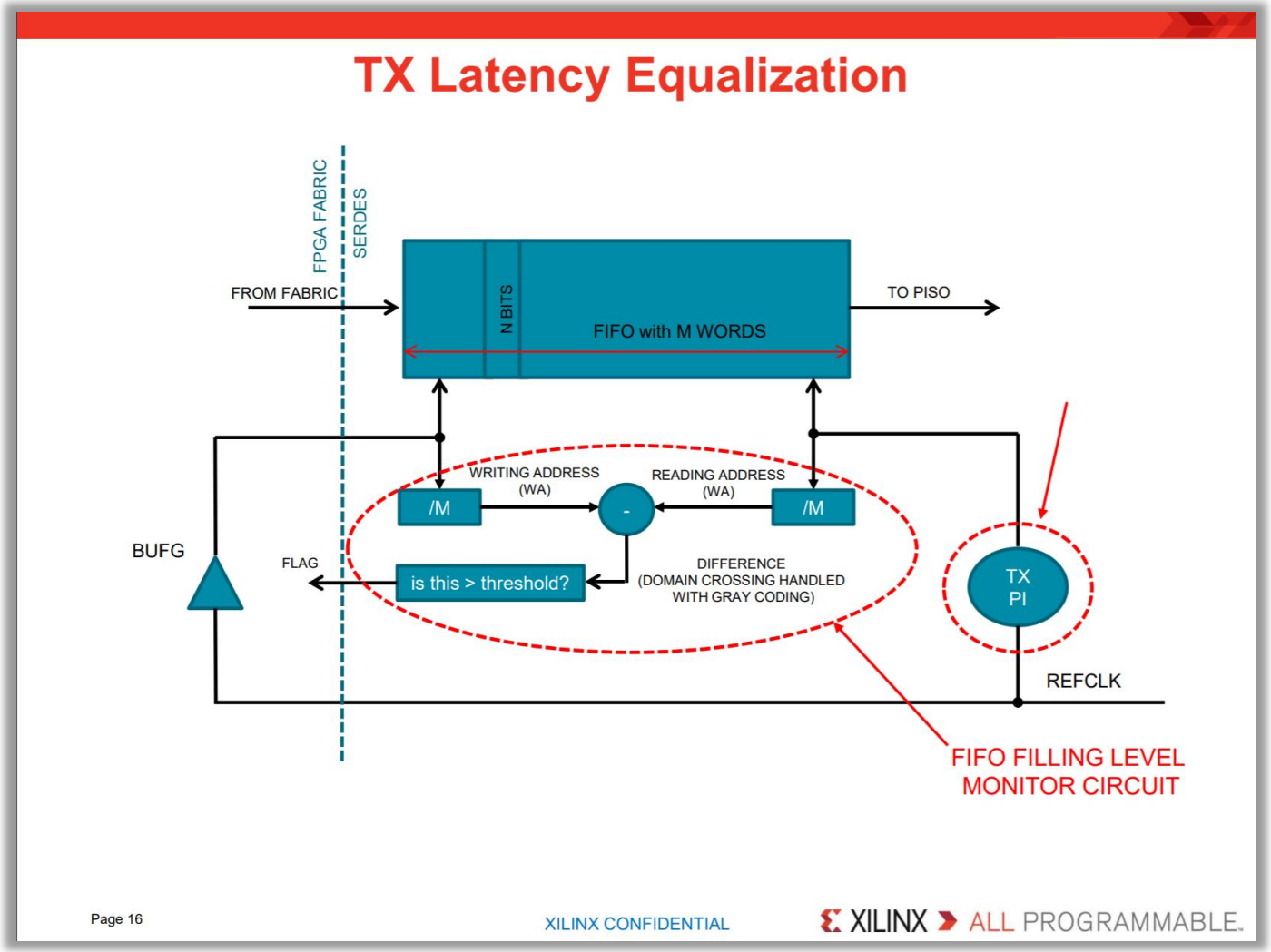
Transmitter path (reset at every acquisition)

- Buffer-Bypass: a.k.a. fixed latency (technique used for GBT-FPGA, TTC-PON)
- Average: reset at every acquisition



Transmitter path – (solution?)

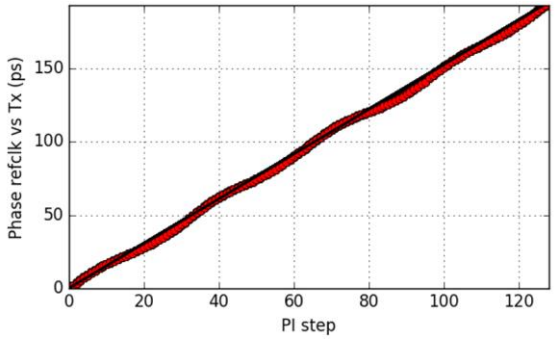
- Solution based on advanced proprietary features of Ultrascale+ GTH/GTY transceivers:

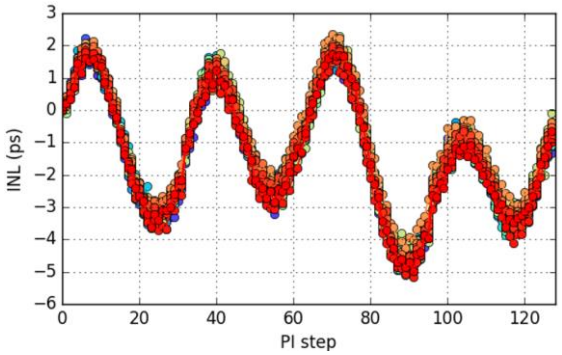


source: https://indico.cern.ch/event/598467/attachments/1475212/2284761/CERN_June_13_v_1_3.pdf

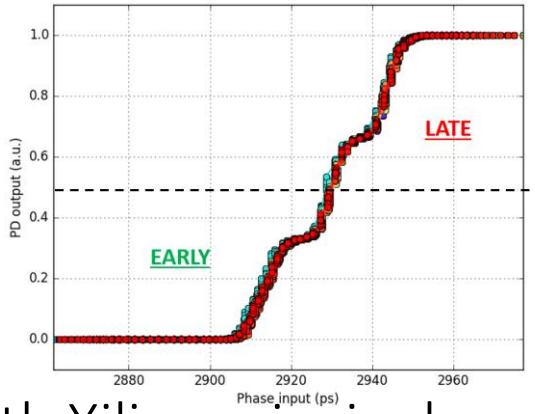
Transmitter path – (solution?)

- Solution based on advanced proprietary features of Ultrascale+ GTH/GTY transceivers:
  - Phase-interpolator control





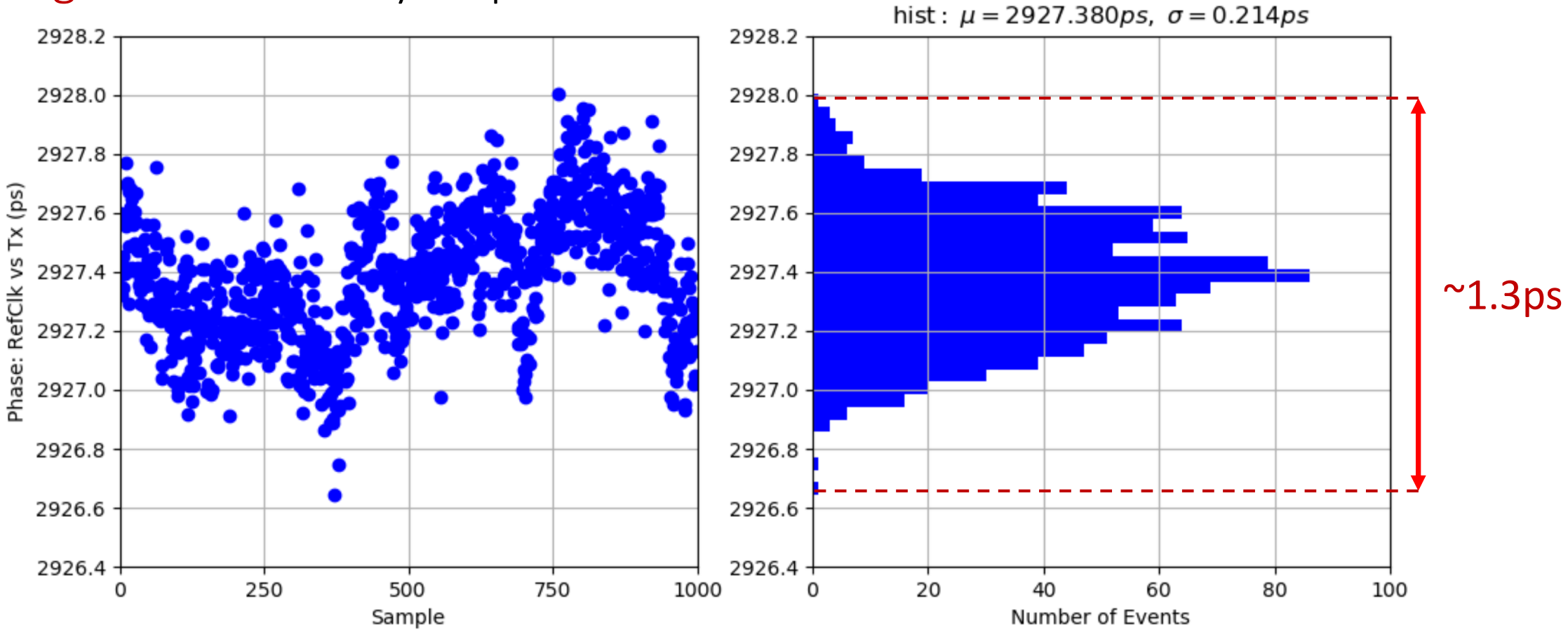
  - FIFO filling-level



- Concept and close collaboration with Xilinx principal engineer (Paolo Novellini)
  - First implementation in software: time to reset ~ 1s
  - Hardware: expected very light FPGA core (most of the blocks are inside transceiver) and fast (~few ms)
- Many flavours possible (and other techniques)
  - Will be discussed in a report and delivered as a core in GIT (see ACES18 Sophie's talk)

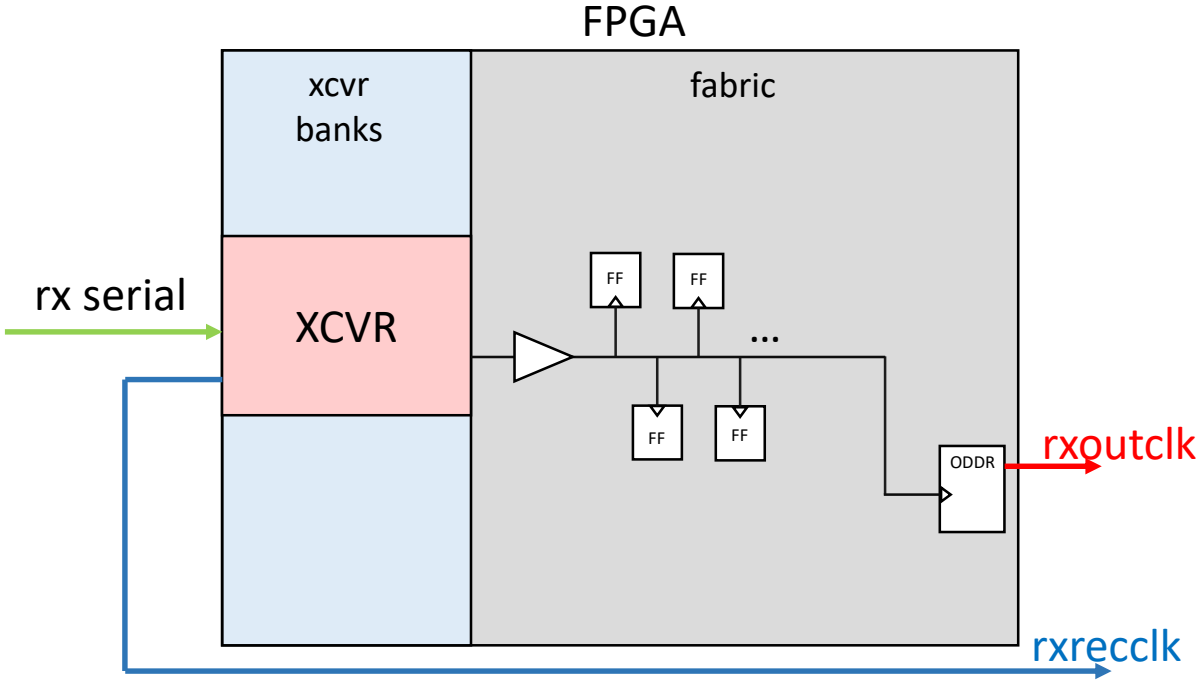
Transmitter path – (reset at every acquisition)

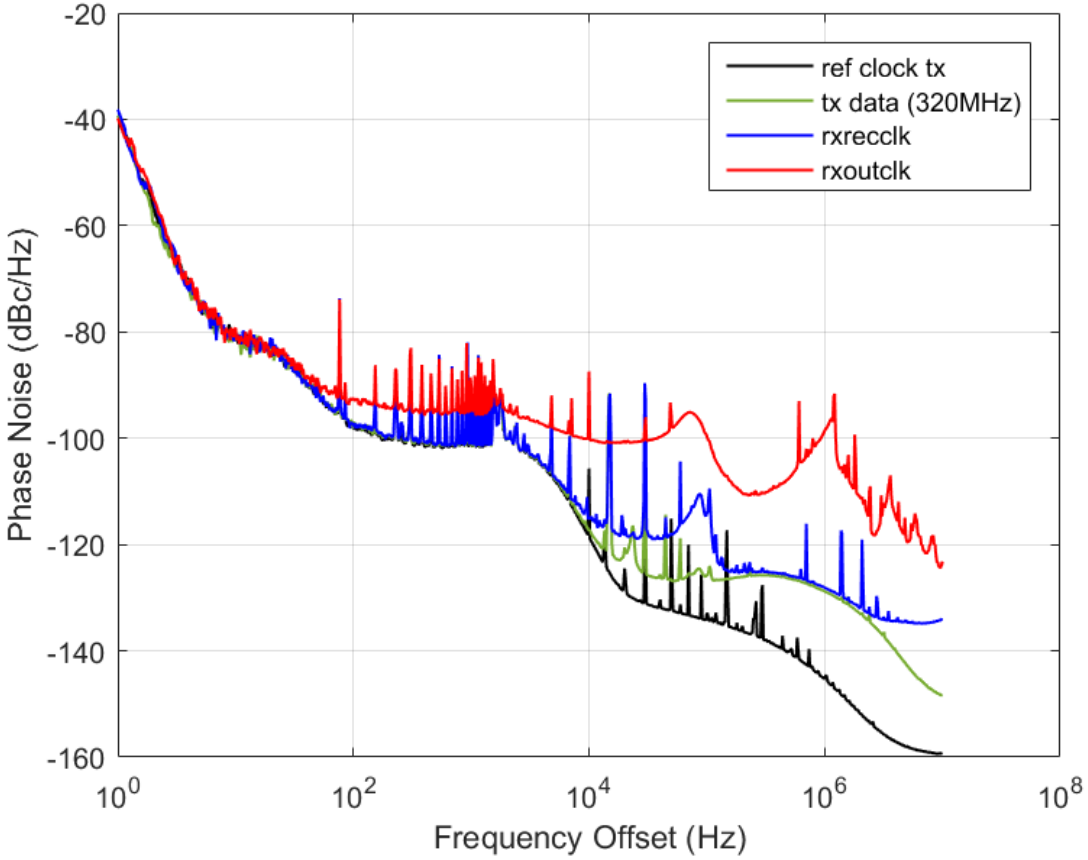
- Results for first implementation (UI compensation):
  - Promising results which will be further verified for more channels/devices
- Average: reset at every acquisition



Receiver path

- Recovered clock?

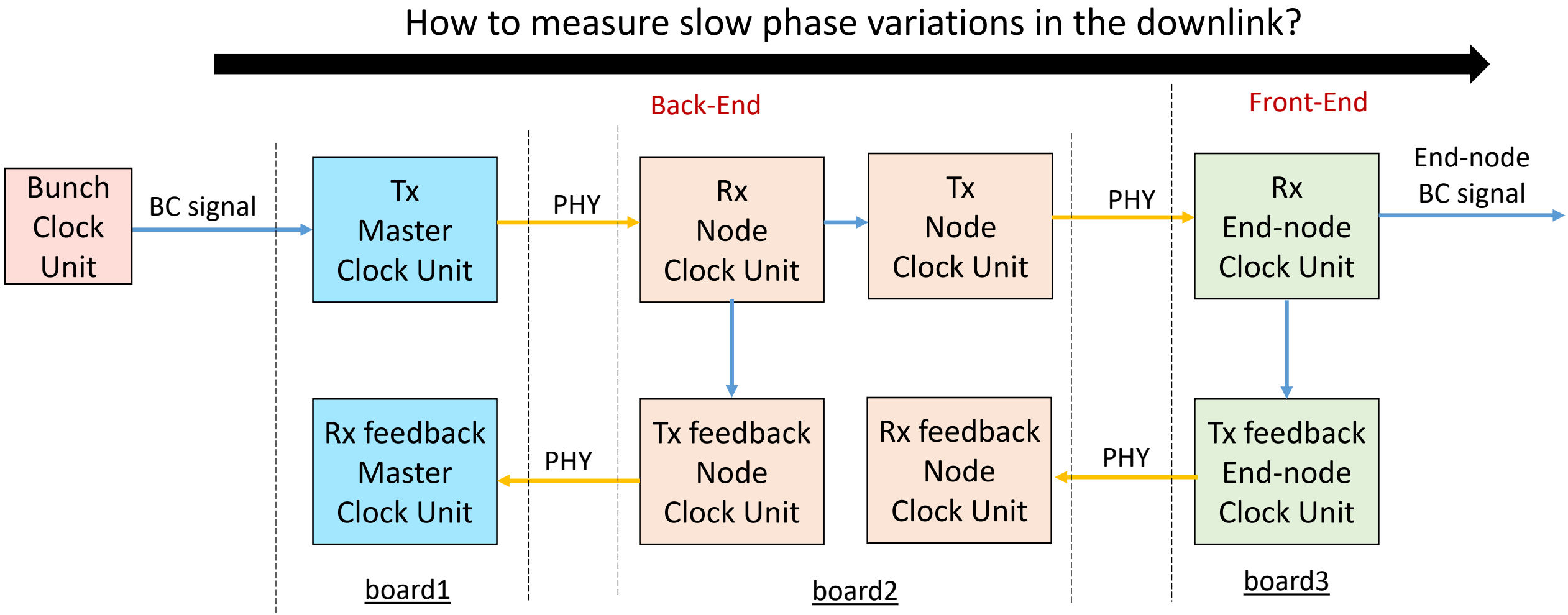




- Does it matter if it is cleaned by a PLL with 1kHz bandwidth?
- Repeatability in a programmable device?
- On-going study for fixed-phase

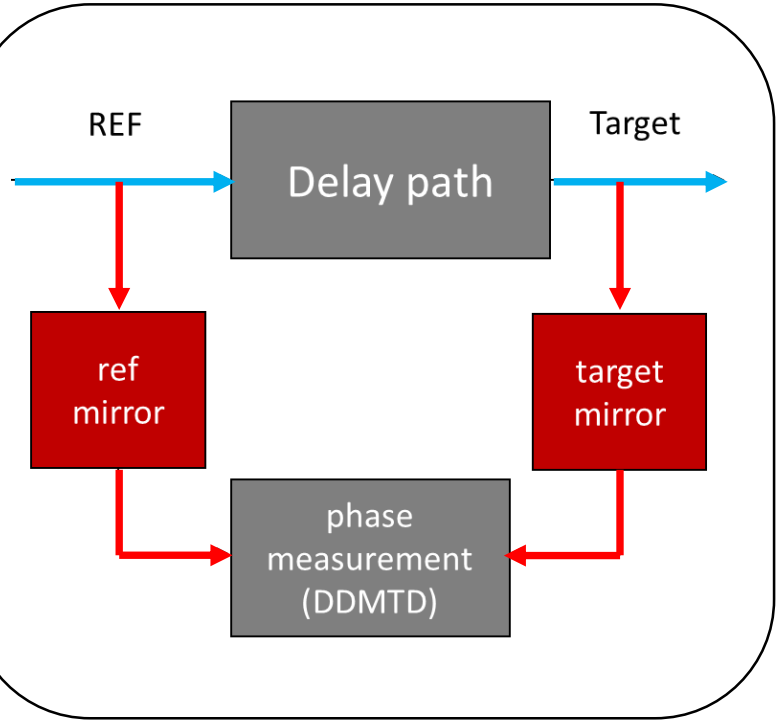
ref clock tx	tx data (320MHz)	rxrecclk	rxoutclk	Integration Band
3.4ps	3.5ps	3.6ps	3.9ps	1Hz - 1kHz (rms rnd)
0.6ps	0.8ps	1.2ps	9.1ps	1kHz – 10MHz (rms rnd)

Phase monitoring aspects

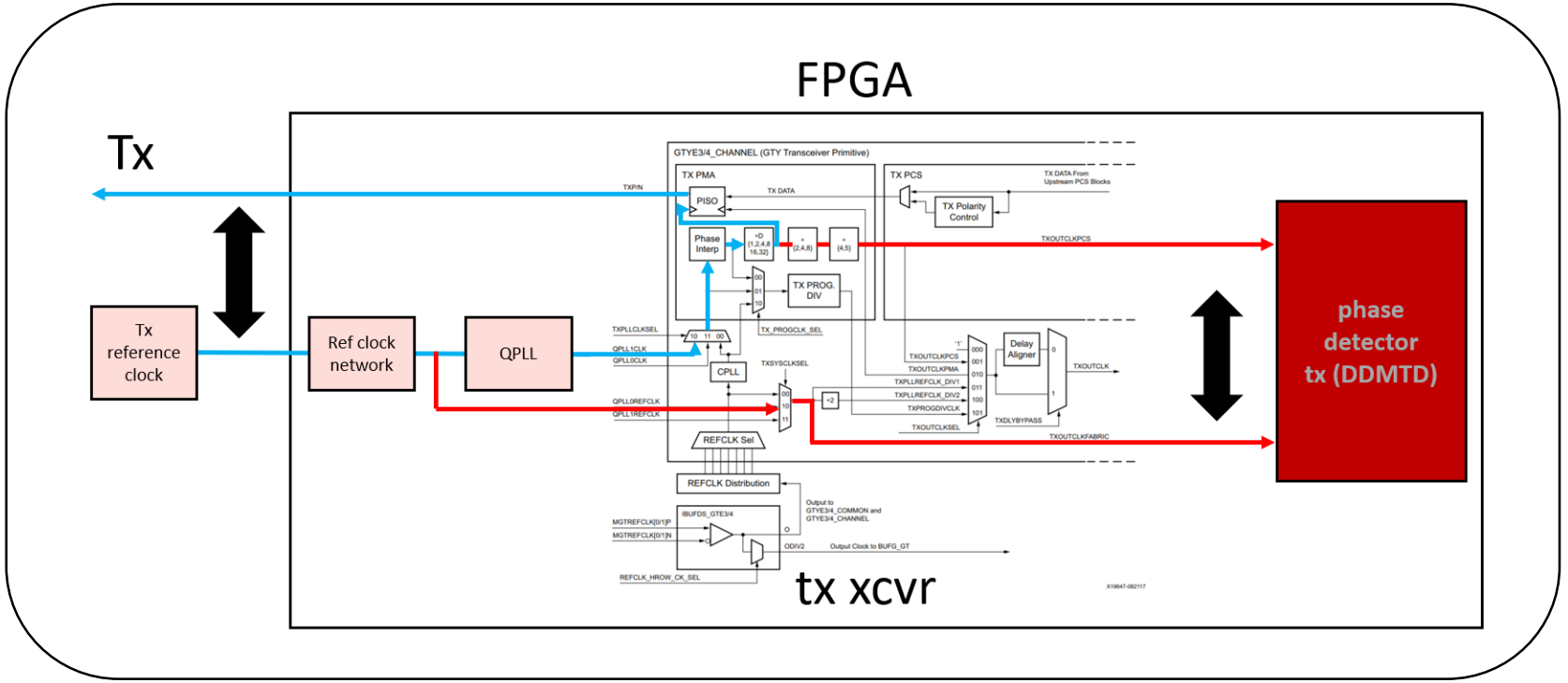


Phase monitoring aspects

- SerDes phase variations monitoring based on a clock-mirroring (on-going!)



concept



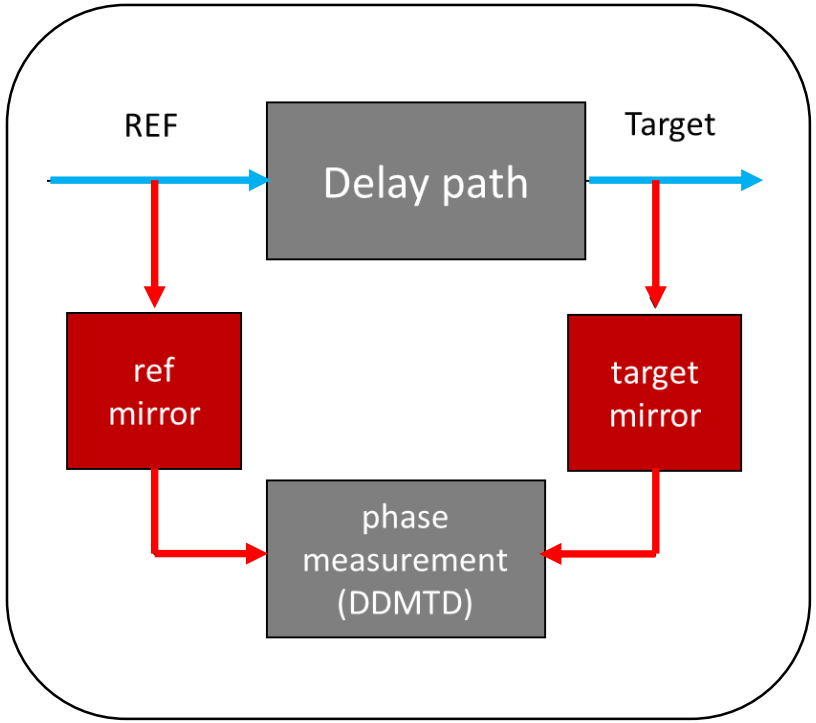
example Tx path

→ mirror paths are micro-paths inside the FPGA which will impact the measurement

→ DDMTD: https://www.ohwr.org/projects/white-rabbit

Phase monitoring aspects

- SerDes phase variations monitoring based on a clock-mirroring (on-going!)

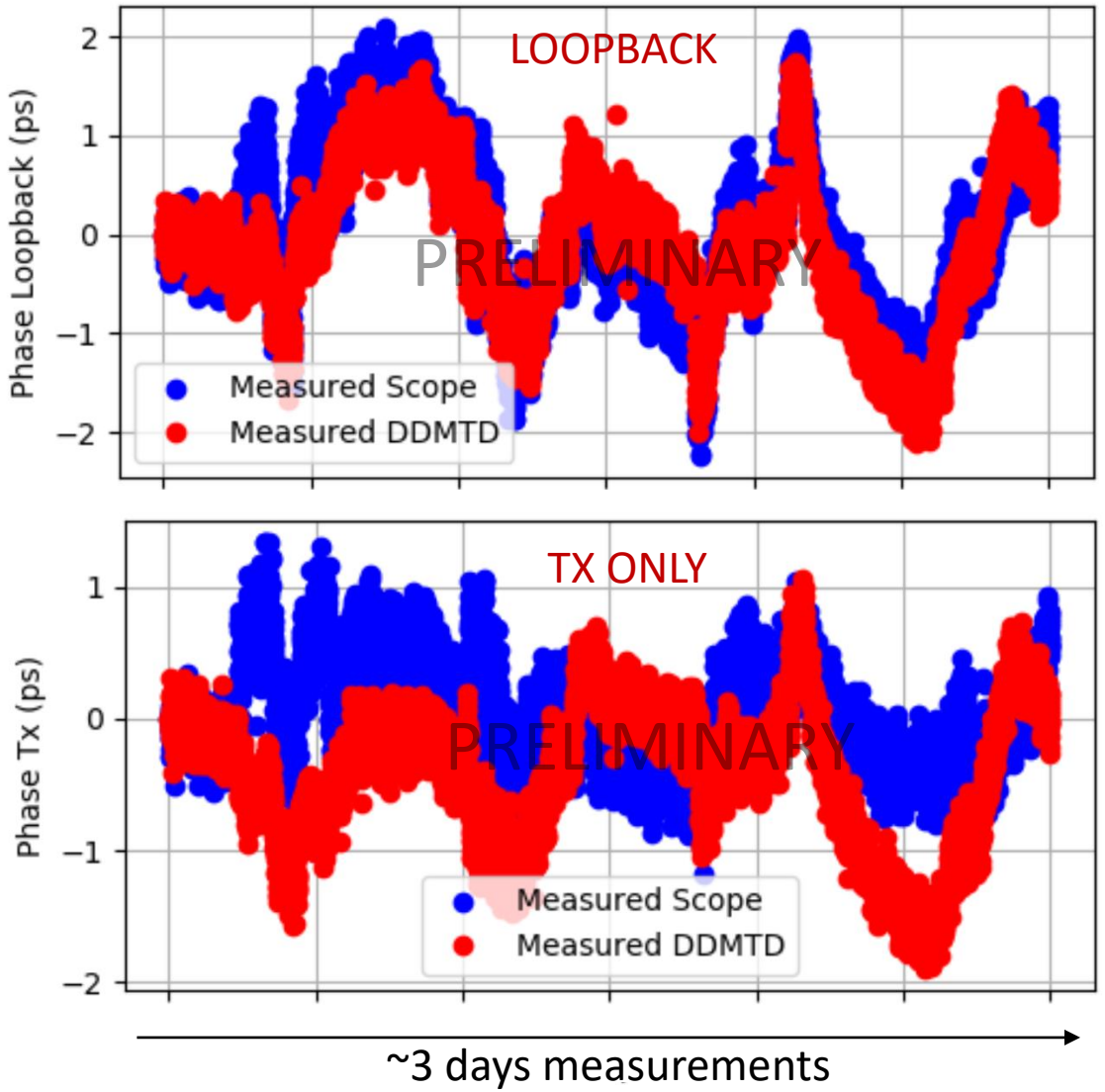


concept

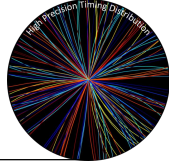
→ mirror paths are micro-paths inside the FPGA which will impact the measurement

→ DDMTD: https://www.ohwr.org/projects/white-rabbit

→ On-going work



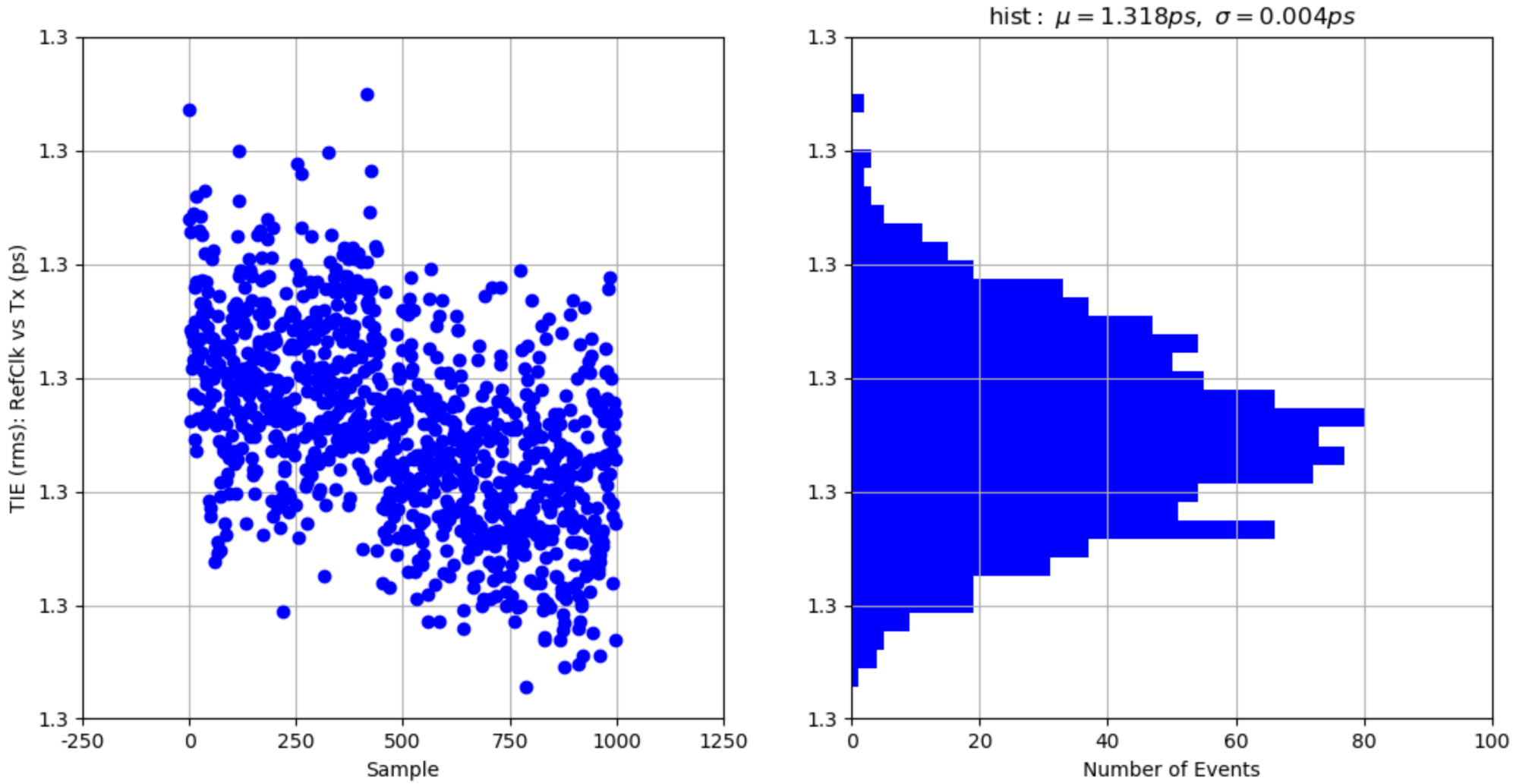
Conclusions



- We have a implemented a promising method (~25ps -> ~2ps pk-pk) for achieving a more stable phase over resets on Xilinx Ultrascale+ transceiver transmitters
  - To be further tested with more channels, devices
  - Is it relevant? How ‘fixed’ a ‘fixed phase’ has to be?
    - Physics phase monitoring based on collision monitoring
    - Aspects to be considered: accuracy, ‘refresh-rate’?
    - System-level impact?
- Work in progress for the receiver path
- Investigating phase monitoring aspects on serial links

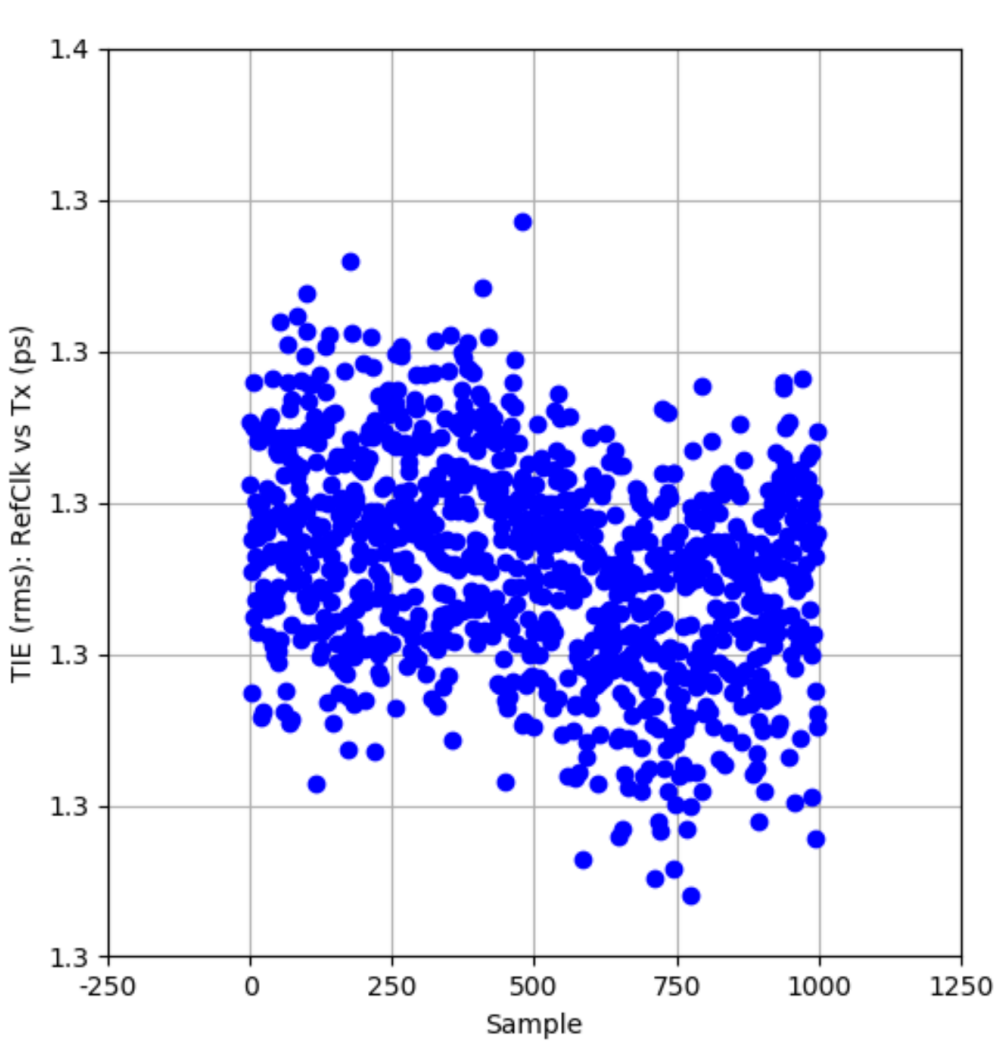
Transmitter path (no reset)

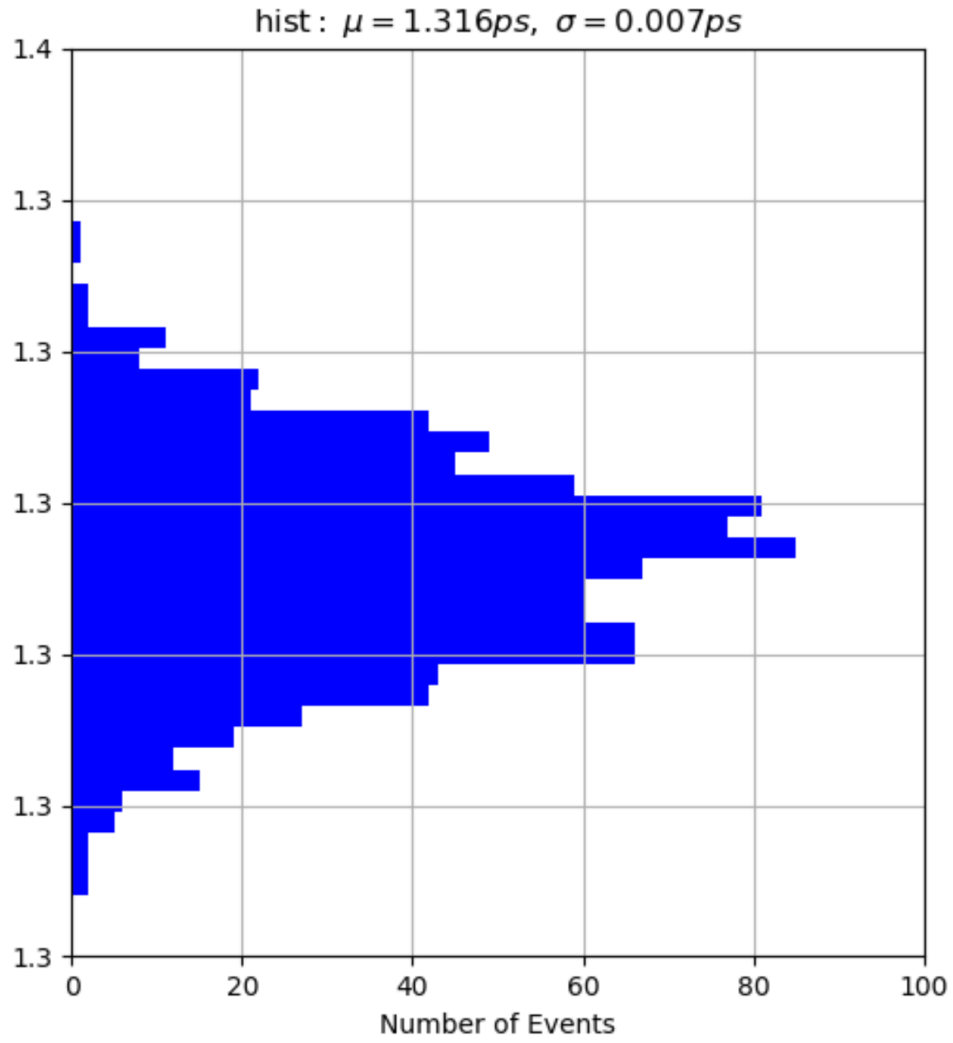
- Standard deviation: no reset - stable measurement



Transmitter path (reset at every acquisition)

- Standard deviation: reset at every acquisition - stable measurement





Transmitter path (GTY Ultrascale+)

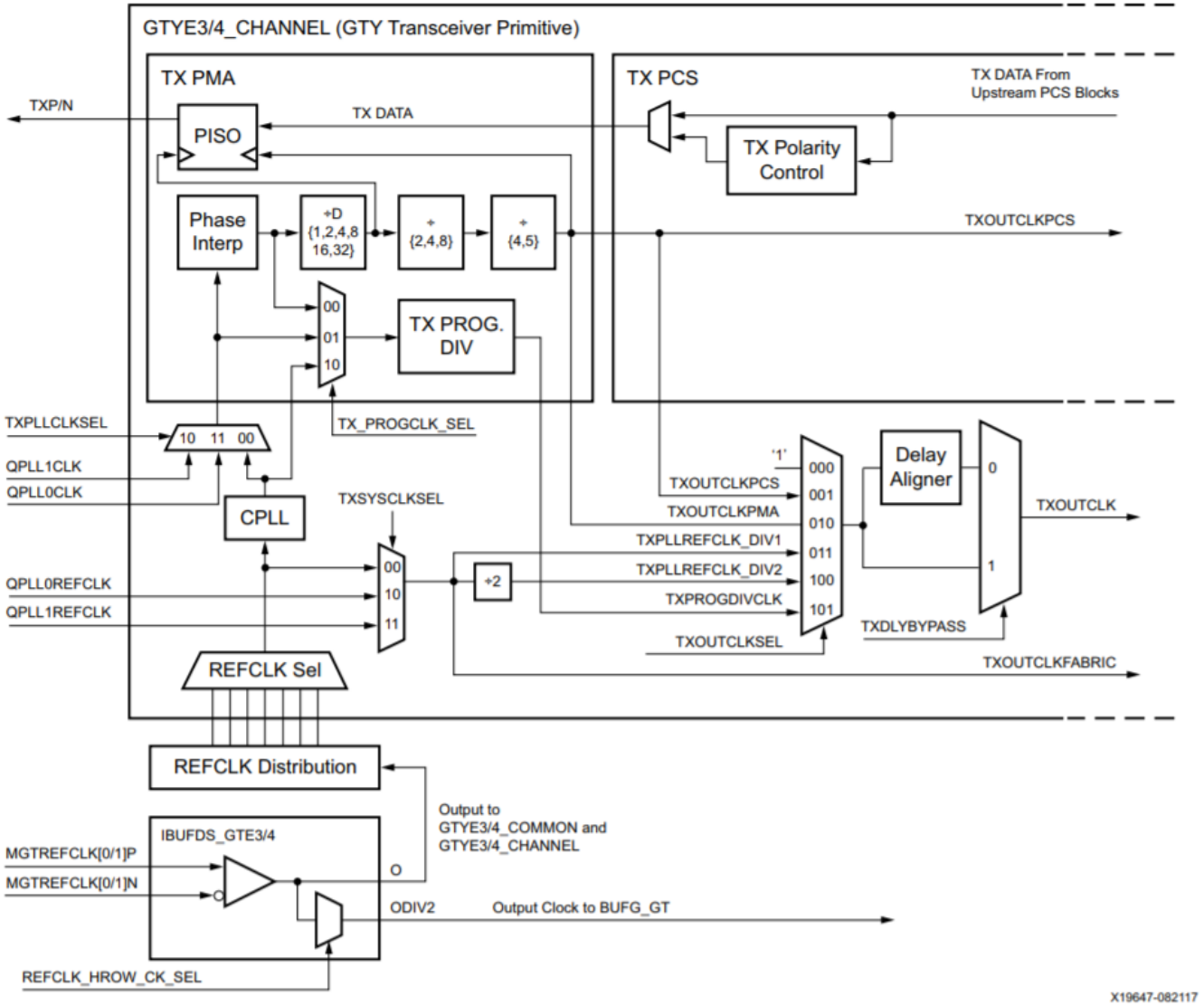


Figure 3-30: **TX Serial and Parallel Clock Divider**

Receiver path (GTY Ultrascale+)

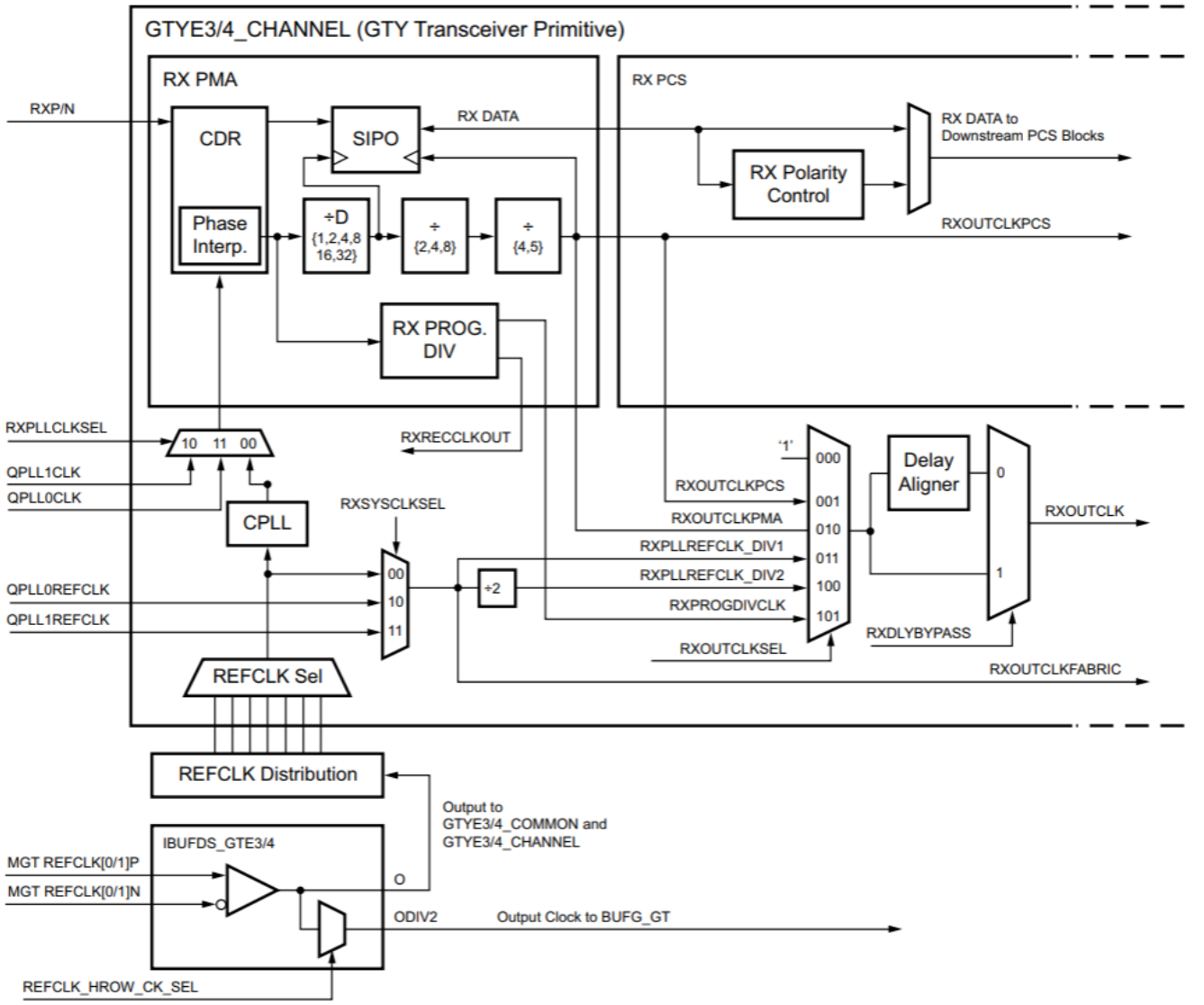


Figure 4-16: **RX Serial and Parallel Clock Divider**