Vertex and Tracker Technologies

CLICdp Advisory Board

Dominik Dannheim (CERN)
on behalf of the CLICdp collaboration

Outline

- Vertex- and tracking-detector requirements
- Sensor and readout technologies
- Simulations and DAQ
- Detector integration studies
- Conclusions

CLIC vertex- and tracking detector requirements

Vertex detector:

- efficient tagging of heavy quarks through precise determination of displaced vertices:
  - → good single point resolution: σ_{SP}~3 µm
    - → small pixels <~25x25 µm^2, analog readout
  - → low material budget: ≲ 0.2% X_0 / layer
    - → low-power ASICs + air cooling (~50 mW/cm^2)

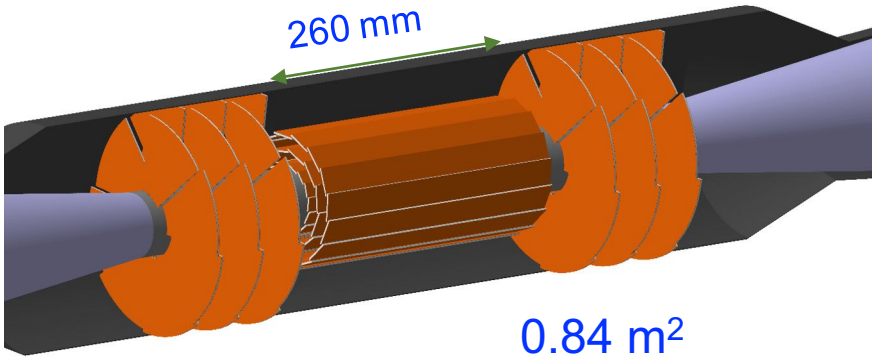
Tracker:

- Good momentum resolution: $\sigma(p_T) / p_T^2 \sim 2 \times 10^{-5}$ GeV^{-1}
  - → 7 µm single-point resolution (~30-50 µm pitch in Rφ)
  - → many layers, large outer radius (~140 m^2 surface)
  - → ~1-2% X0 per layer
    - → low-mass supports + services

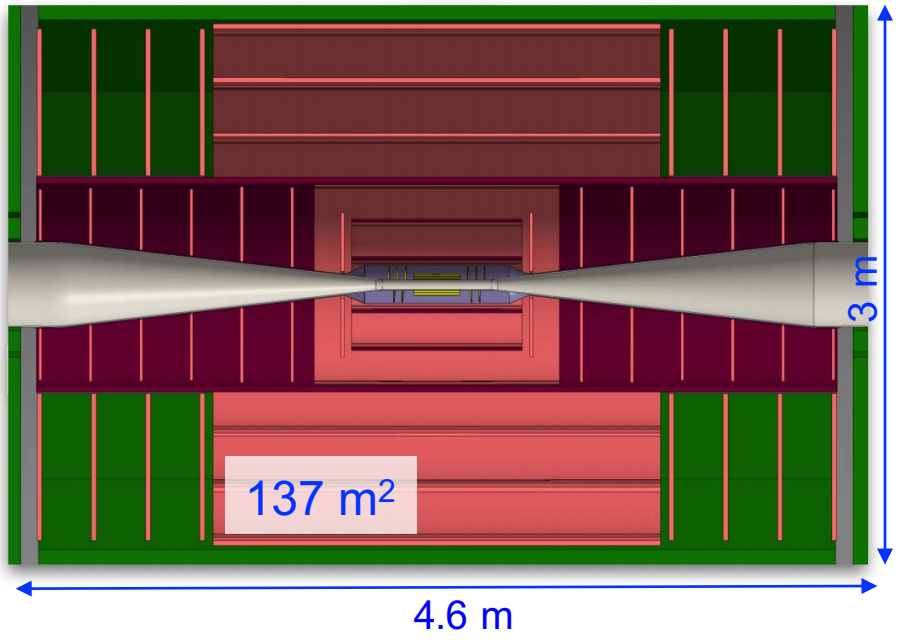
Both:

- 20 ms gaps between bunch trains
  - → trigger-less readout, pulsed powering
- few % maximum occupancy from beam backgrounds
  - → sets inner radius and limits cell sizes
  - → time stamping with ~5 ns accuracy
    - → depleted sensors (high resistivity / high voltage)
- moderate radiation exposure (~10^4 below LHC!):
  - NIEL: < 10^{11} n_{eq}/cm^2/y
  - TID: < 1 kGy / year

Vertex-detector simulation geometry



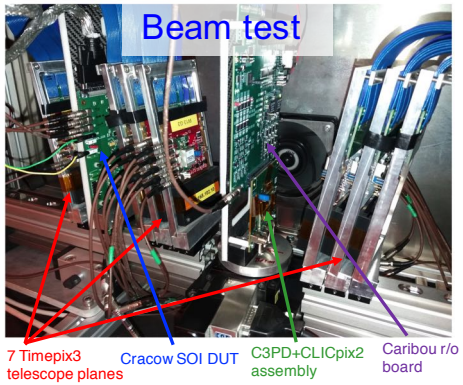
Tracker simulation geometry

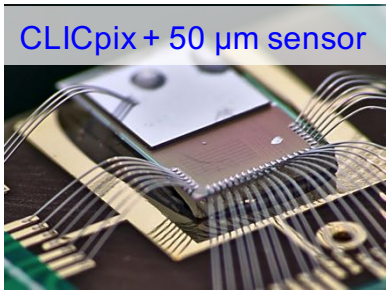


CLIC pixel-detector technology R&D

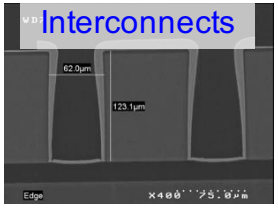
Sensor + readout technologies

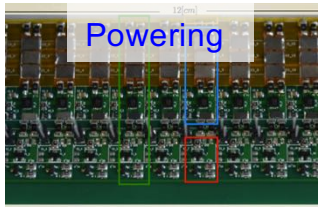
Sensor + readout technology	Currently considered for
Bump-bonded Hybrid planar sensors	Vertex
Capacitively coupled HV-CMOS sensors	Vertex
Monolithic HV-CMOS sensors	Tracker
Monolithic HR-CMOS sensor	Tracker
Monolithic SOI sensors	Vertex, Tracker

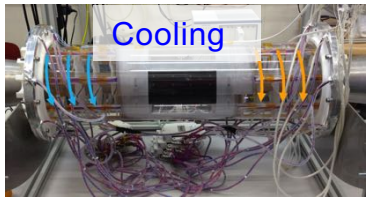


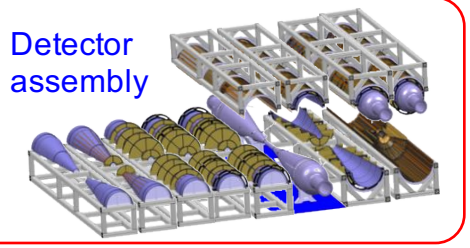


Detector integration studies







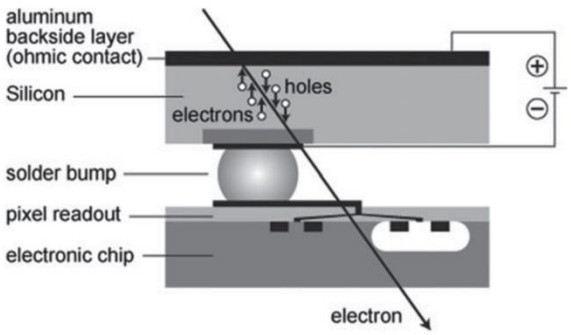


- Challenging requirements lead to extensive detector R&D program
- ~10 institutes active in vertex/tracker R&D
- Collaboration with ATLAS, ALICE, LHCb, RD53, AIDA-2020

Hybrid planar sensor technology

- Planar pixel sensors bump-bonded to r/o ASICs
- Considered for vertex detector

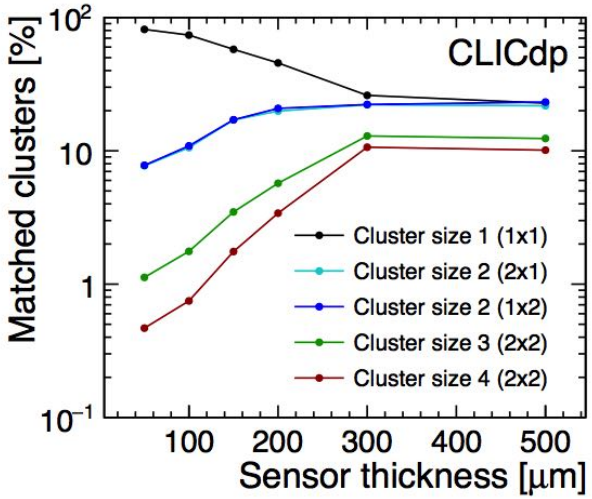
Hybrid pixel detector



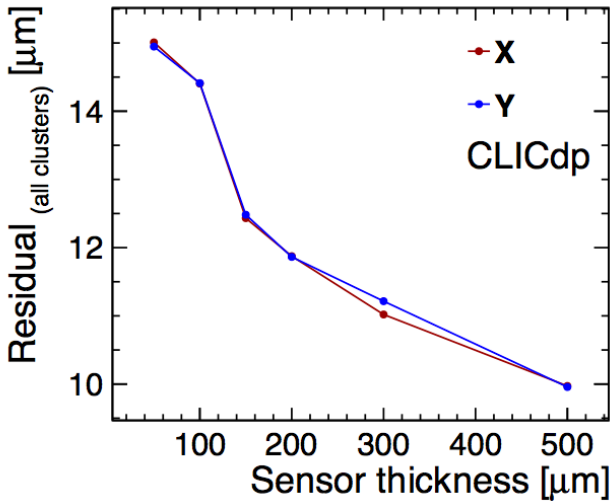
Status:

- Comprehensive thin-sensor studies with slim-edge and active-edge sensors (50-300 µm thickness) on Timepix/Timepix3 readout ASICs (55 µm pitch)

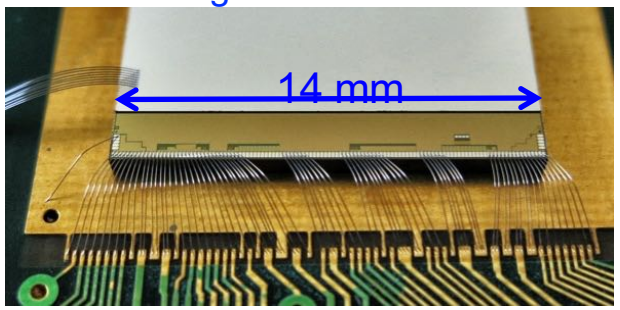
Cluster sizes vs. thickness

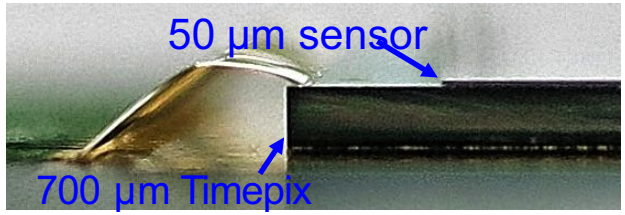


Track residuals vs. thickness



Timepix with 50 µm active-edge sensor





- Achievable resolution limited by fraction of 2-hit clusters
  → Not enough charge sharing in ultra-thin sensors

CLICdp-Note-2016-001

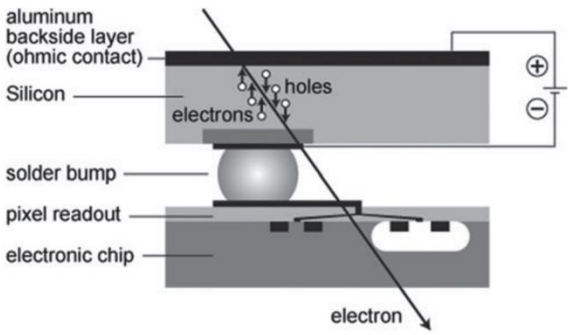
Hybrid planar sensor technology

- Planar pixel sensors bump-bonded to r/o ASICs
- Considered for vertex detector

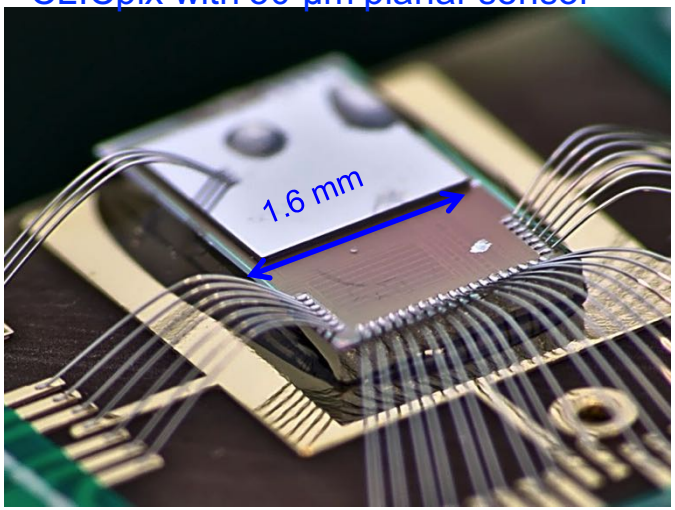
Status:

- Comprehensive thin-sensor studies with slim-edge and active-edge sensors (50-300 µm thickness) on Timepix/Timepix3 readout ASICs
- CLICpix/CLICpix2 prototype r/o ASICs with in-pixel time and energy measurement, 25x25 µm^2 pitch, implemented in 65 nm TSMC process, including full 12" wafer from RD53 prototype run
- Single-chip bump-bonding with 25 µm pitch
- ~100% efficiency, few ns timing, σ_{SP}~7 µm

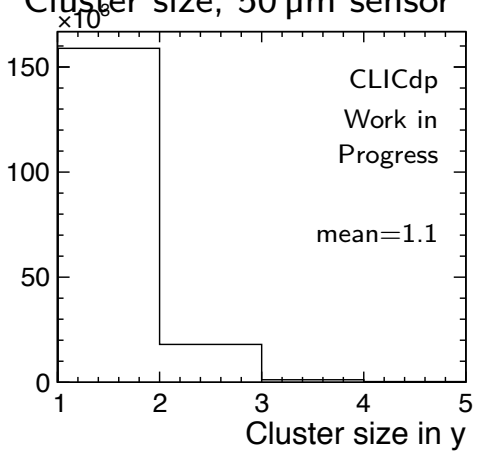
Hybrid pixel detector



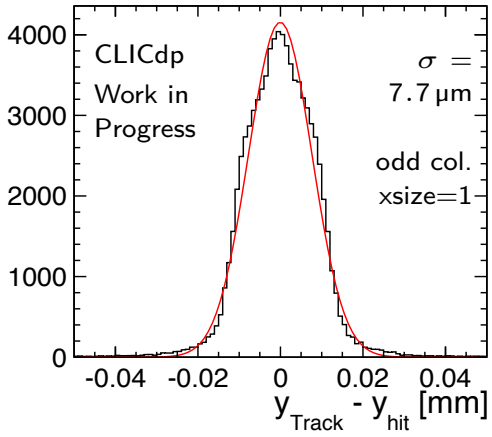
CLICpix with 50 µm planar sensor



Cluster size, 50 µm sensor



Residual, 50 µm sensor



CLICdp-Conf-2017-010

Hybrid planar sensor technology

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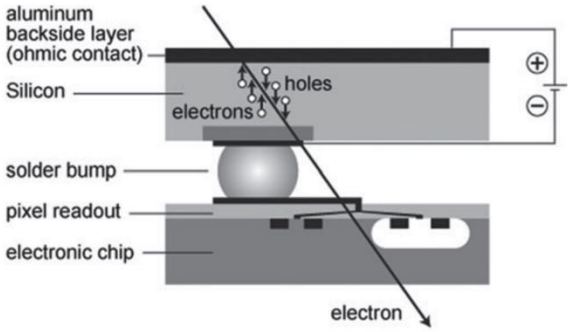
- Considered for vertex detector

Hybrid pixel detector



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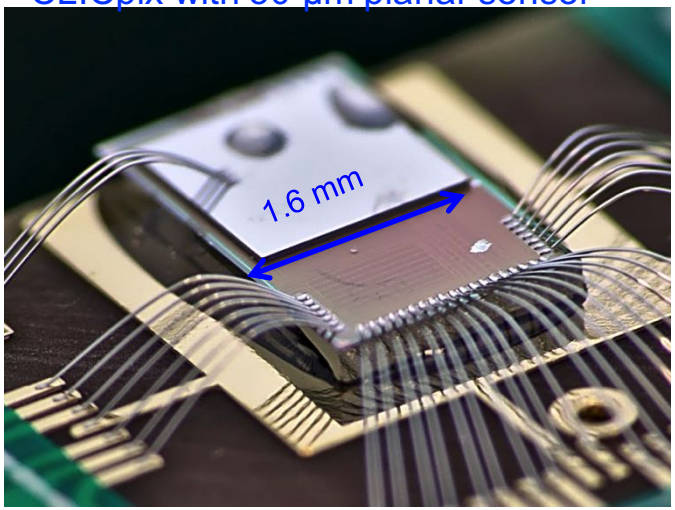
CLICpix with 50 µm planar sensor



Ongoing work:

- Validation of new single-chip bump-bonding process
- Beam tests for CLICpix2 planar-sensor assemblies
- Reduce σ_{SP}: ELAD sensors with enhanced charge sharing

Future developments:

- Even smaller pixels (28 nm process technology), lower detection threshold
- New hybridisation methods: Cu pillars, Indium, Anisotropic Conductive Film, …
- Module/stave building studies

CLICdp-Conf-2017-010

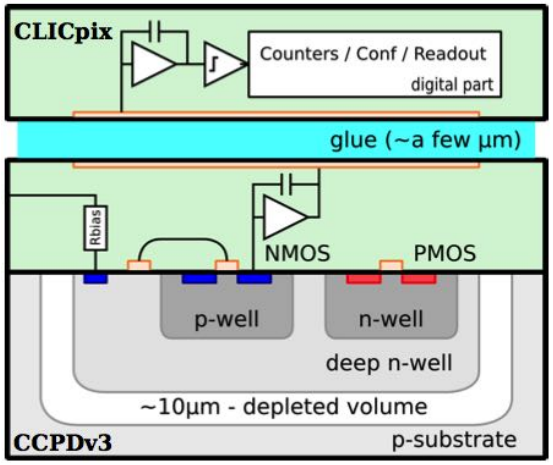
Capacitively coupled HV-CMOS sensors

- Active High-Voltage (HV) CMOS sensors, large fill factor: electronics inside charge-collection well, depletion through HV
- Capacitive coupling to r/o ASICs
  → thin glue layer replaces costly small-pitch bump bonds
- Considered for vertex detector

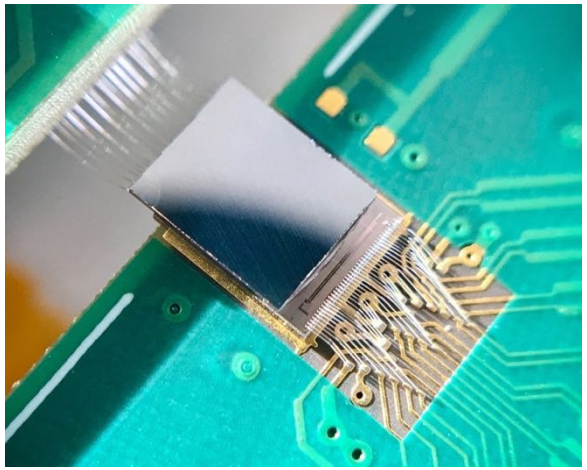
Results:

- Two generations of active sensors (CCPDv3, C3PD) in AMS 180 nm HV-CMOS process, 10-1000 Ohm cm substrates, 25x25 μm^2 pitch
- Glue assemblies with CLICpix/CLICpix2: ~90-100% efficiency, few ns timing, σ_{SP}~6 µm
- Finite-element simulation of capacitive coupling

Capacitively Coupled Pixel Detector

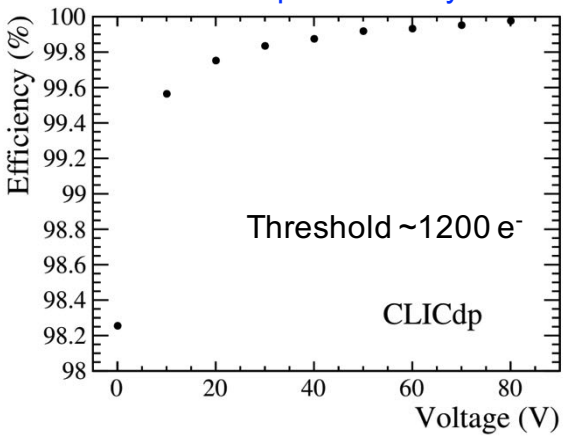


C3PD/CLICpix2 glue assembly

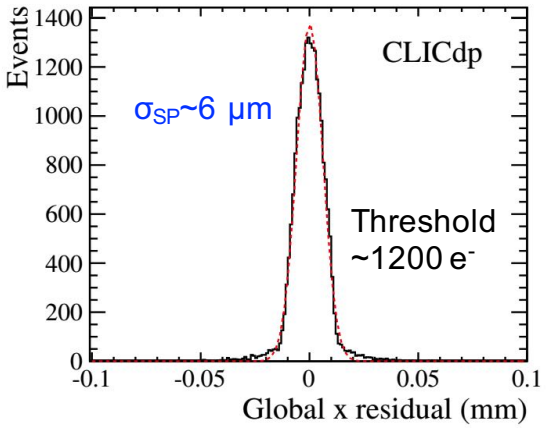


NIM A 823 (2016) 1-8;
JINST 12 P09012 (2017)

CCPDv3/CLICpix efficiency



CCPDv3/CLICpix residuals



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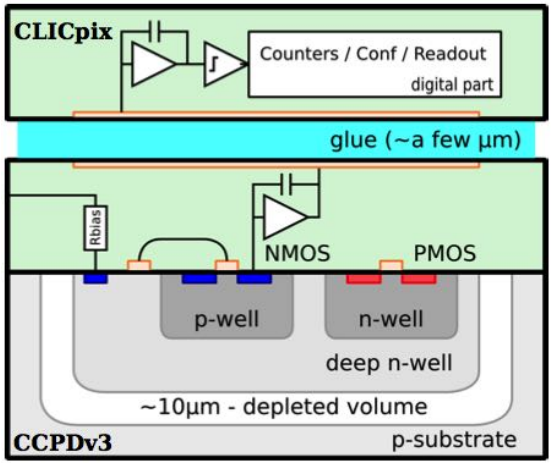
Ongoing work:

- Evaluation of sensors with high-resistivity substrates
- Optimization of gluing process (uniformity, reproducibility)
- Simulation of the entire transfer chain

Future developments:

- Module concept? (difficult!)
- A/C coupling at the fab (wafer) level + TSV
- A/C coupled passive CMOS sensors?

Capacitively Coupled Pixel Detector



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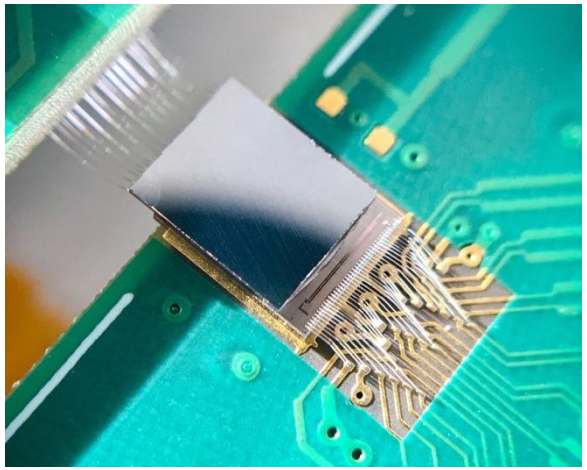

NIM A 823 (2016) 1-8;
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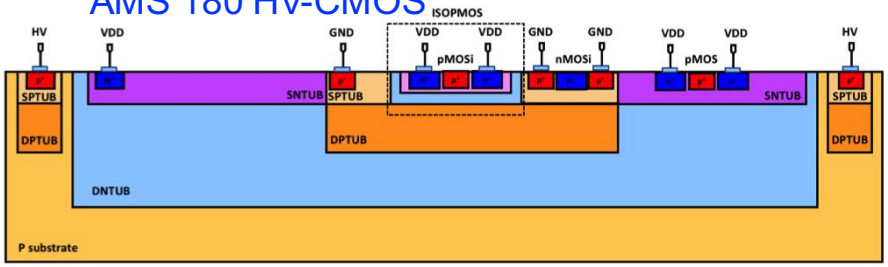
Monolithic HV-CMOS sensors

- Active HV-CMOS sensors with fully integrated readout
- Considered for tracker

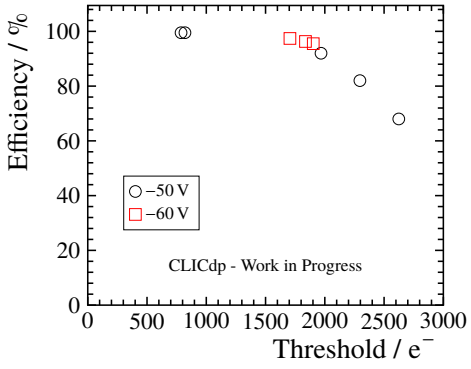
AMS 180 HV-CMOS



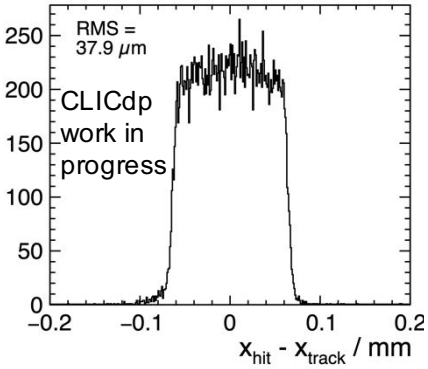
Results:

- ATLASPIX prototypes in AMS 180 nm HV-CMOS process: 40 x 120 µm^2 pitch, data-driven column-drain readout
- 99.5% efficiency, σ_t~16-20 ns, σ_{SP}~13 µm (almost no charge sharing; timing limited by r/o system)
- Similar developments with LFoundry HV-CMOS process

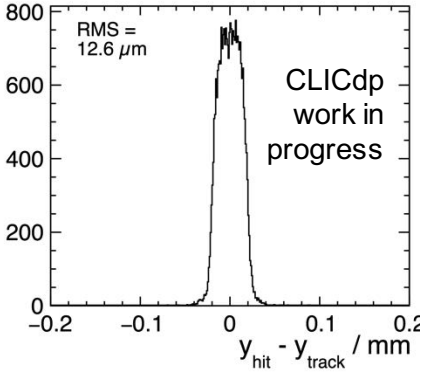
Efficiency



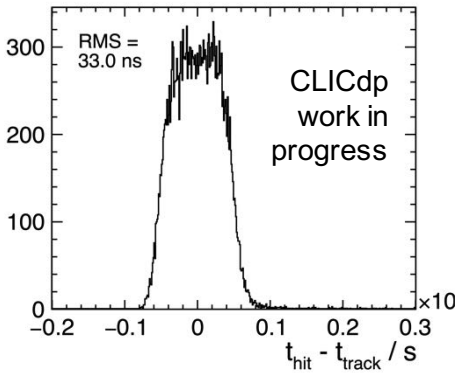
Residual in column direction



Residual in row direction



Timing residual



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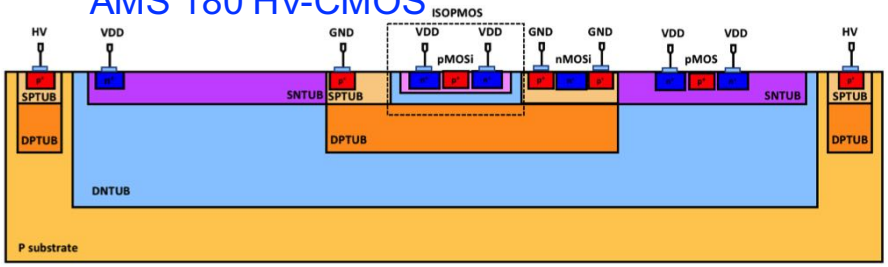

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- Similar developments with LFoundry HV-CMOS process

Ongoing work:

- Beam tests of ATLASPIX with improved readout system (timing, lower threshold, power consumption tests)

Future developments:

- Adapt pixel layout to CLIC requirements (~30 µm pixel width)
- Improve digital design: power pulsing
- Reduce periphery area?

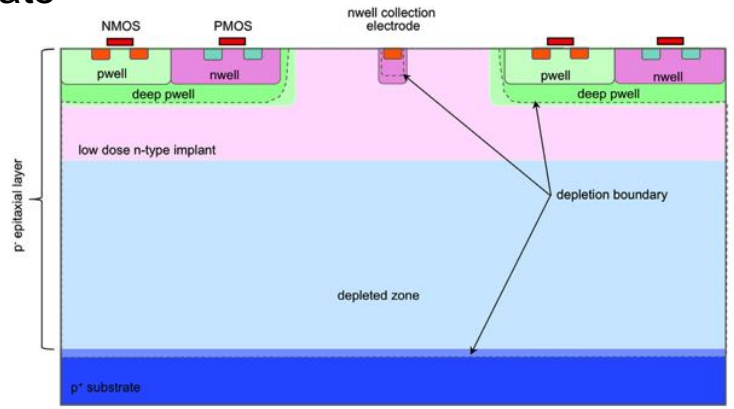
Integrated HR-CMOS sensors

- Integrated CMOS sensors on High-Resistivity (HR) substrate
- Small fill factor: electronics outside charge-collection well
- Considered for tracker

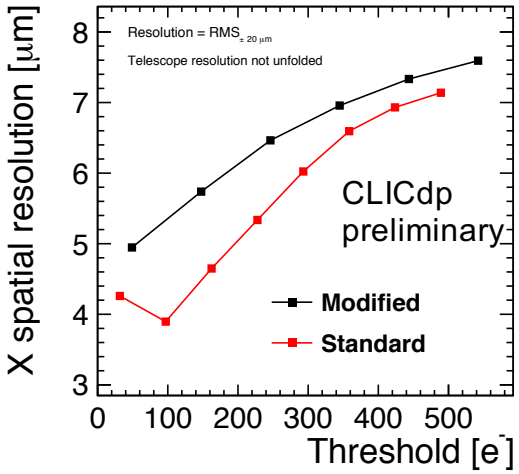
Results:

- Tests with INVESTIGATOR analog prototype chip in TowerJazz 180 nm HR-CMOS process (ALICE development), 20x20 - 50x50 μm^2 pitch
- For 28x28 μm^2 pitch, external readout: 99.3% efficiency, σ_t<5 ns, σ_{SP}~4 μm

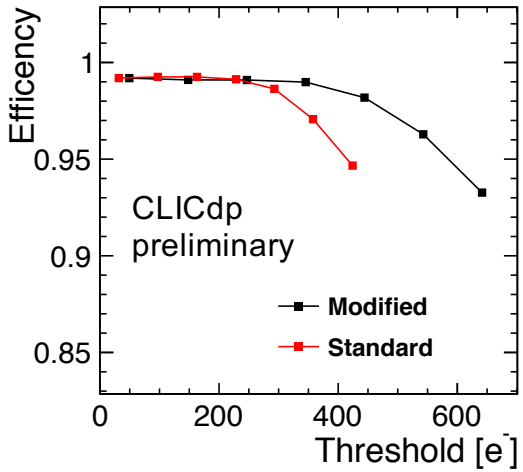
HR-CMOS process



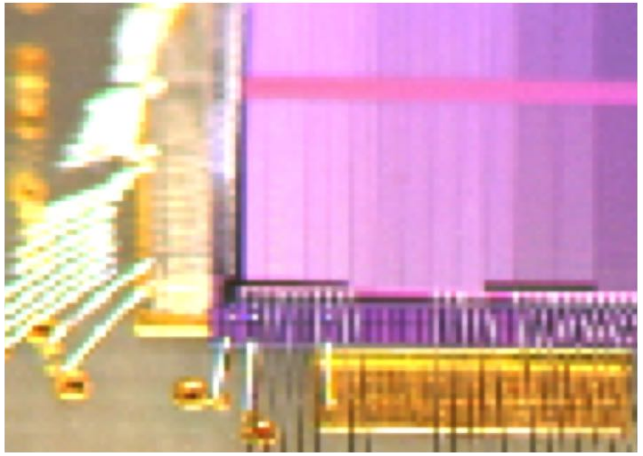
X resolution vs. threshold:



Efficiency vs. threshold:



INVESTIGATOR HR-CMOS test chip

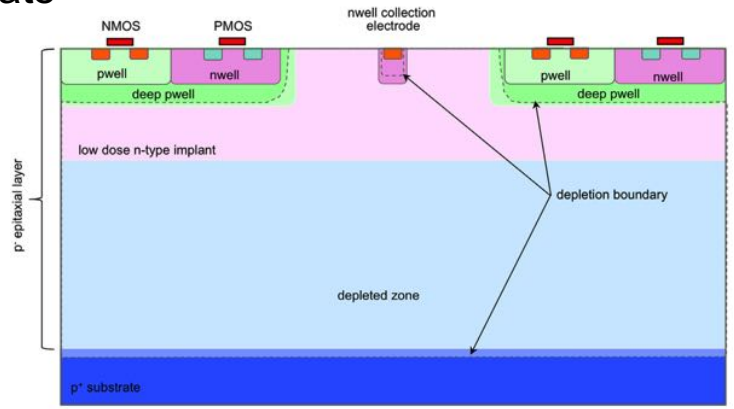


CLICdp-Note-2017-004

Integrated HR-CMOS sensors

- Integrated CMOS sensors on High-Resistivity (HR) substrate
- Small fill factor: electronics outside charge-collection well
- Considered for tracker

HR-CMOS process



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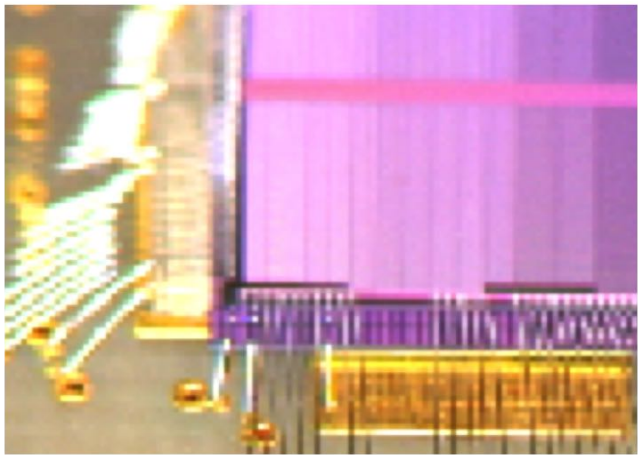
Ongoing work:

- Design of fully integrated CLICTD chip: 30 x 300 μm^2 pitch, segmented electrodes, in-pixel time + charge measurement

INVESTIGATOR HR-CMOS test chip



Future plans:

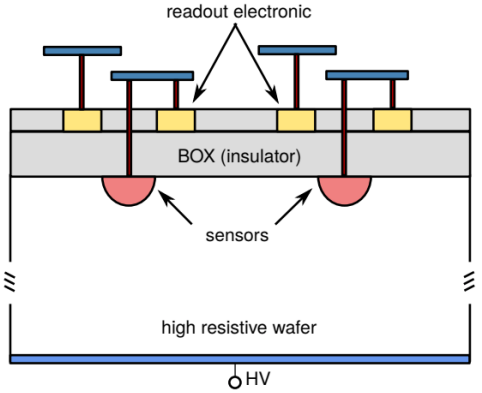
- Thinning to 100 µm
- Larger prototypes
- Further process optimization / smaller feature size?
  → could also become an option for the vertex detector

CLICdp-Note-2017-004

Monolithic SOI sensors

- Silicon-On-Insulator (SOI): Sensor and electronics integrated on single wafer with high-resistivity substrate, separated by insulation oxide layer + buried p-wells,
- Considered for vertex and tracker

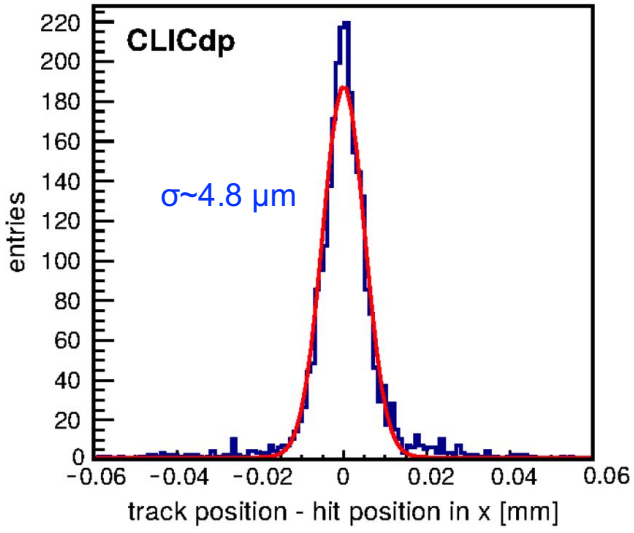
SOI pixel detector



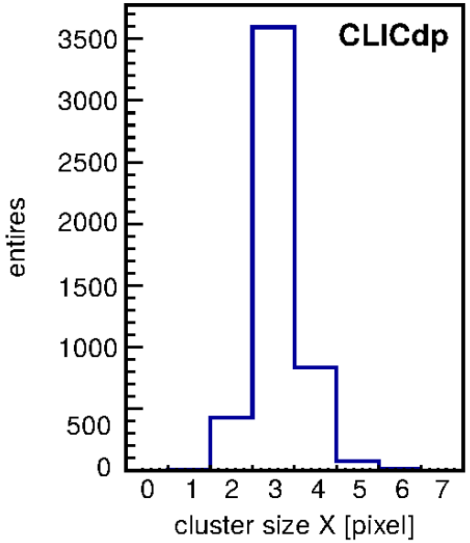
Results:

- Cracow SOI test chip in 200 nm LAPIS SOI process, with various geometries and technology parameters: >=30x30 μm^2 pitch, single SOI and double SOI, different r/o schemes
- Test results for 500 µm thickness, 30x30 μm^2 pitch, rolling-shutter r/o: >99% efficiency, σ_{SP}~4.5 µm

Residual in column direction



Cluster size in column direction



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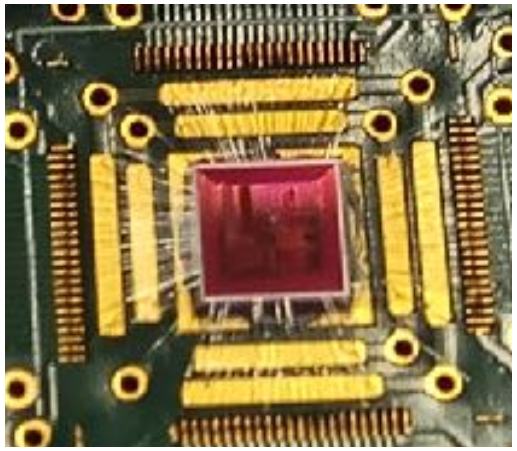
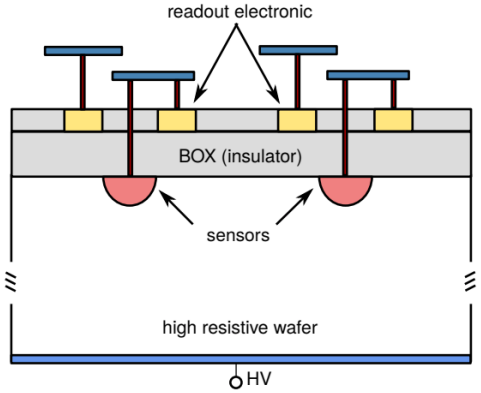


CLICdp-Pub-2018-001

Monolithic SOI sensors

- Silicon-On-Insulator (SOI): Sensor and electronics integrated on single wafer with high-resistivity substrate, separated by insulation oxide layer + buried p-wells,
- Considered for vertex and tracker

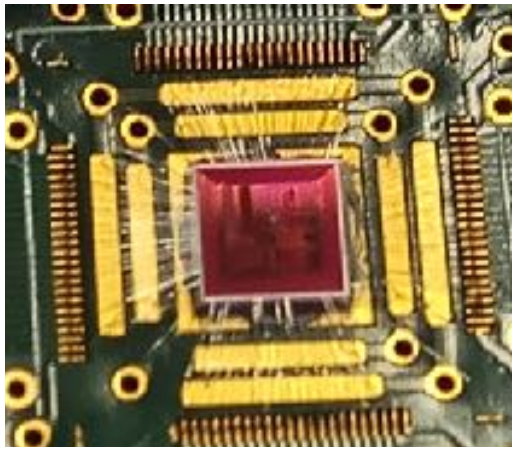
SOI pixel detector



Results:

- Cracow SOI test chip in 200 nm LAPIS SOI process, with various geometries and technology parameters: >=30x30 μm^2 pitch, single SOI and double SOI, different r/o schemes
- Test results for 500 µm thickness, 30x30 μm^2 pitch, rolling-shutter r/o: >99% efficiency, σ_{SP}~4.5 µm

Cracow SOI test chip



Ongoing work:

- Production of CLIPS vertex test chip, targeted to LC vertex requirements: 20x20 μm^2 pitch, snapshot r/o of analog time and charge measurement, $\geqq$100 µm thickness
- Analysis of first-generation prototype test-beam data
- Development of readout system for CLIPS

Future plans:

- Larger chips, improved readout

CLICdp-Pub-2018-001

Sensor and readout simulation

- Simulations are crucial for understanding performance of prototypes and developing new sensors and readout ASICs
- Complex simulation chain: ionization process, charge transfer, capacitive coupling, r/o ASIC response, beam-telescope setup
- Various tools available: Geant4, TCAD process and device simulation, COMSOL multi-physics, parametric models, SPICE circuit simulation

Results:

- 2D TCAD simulations of planar and HV/HR-CMOS sensors
- COMSOL results for capacitive coupling
- Parametric simulations and circuit simulations for r/o ASIC optimization
- Geant-4 simulations combined with parametric models
  → Allpix^2 simulation framework, validated for planar sensors

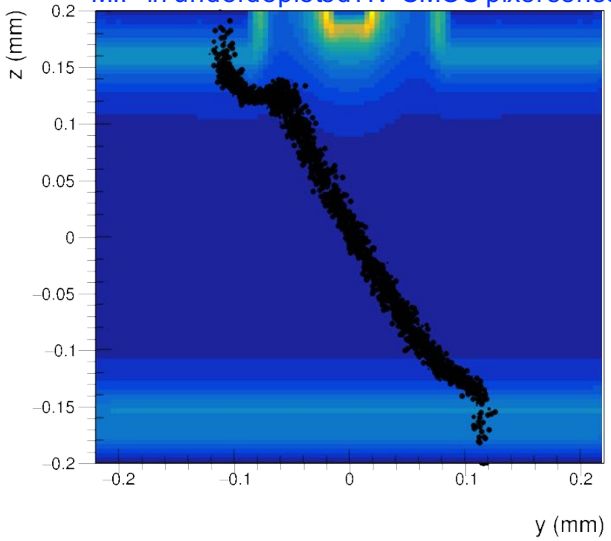
Ongoing work:

- Validation of Allpix^2 simulations for SOI, HV/HR-CMOS
- 3D TCAD simulations for HV/HR-CMOS sensors

Future plans:

- Include Timing in Allpix^2 simulations
- Allpix^2 simulations of new prototypes

MIP in underdepleted HV-CMOS pixel sensor



CLICdp-Note-2017-006

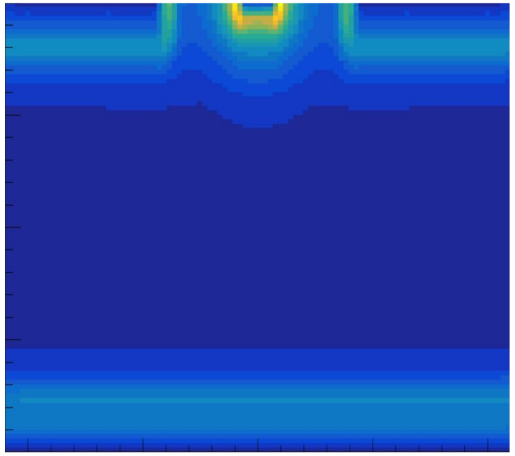
Sensor and readout simulation

- Simulations are crucial for understanding performance of prototypes and developing new sensors and readout ASICs
- Complex simulation chain: ionization process, charge transfer, capacitive coupling, r/o ASIC response, beam-telescope setup
- Various tools available: Geant4, TCAD process and device simulation, COMSOL multi-physics, parametric models, SPICE circuit simulation

Results:

- 2D TCAD simulations of planar and HV/HR-CMOS sensors
- COMSOL results for capacitive coupling
- Parametric simulations and circuit simulations for r/o ASIC optimization
- Geant-4 simulations combined with parametric models
  → Allpix^2 simulation framework, validated for planar sensors

MIP in underdepleted HV-CMOS pixel sensor



Ongoing work:

- Validation of Allpix^2 simulations for SOI, HV/HR-CMOS
- 3D TCAD simulations for HV/HR-CMOS sensors

Future plans:

- Include Timing in Allpix^2 simulations
- Allpix^2 simulations of new prototypes

CLICdp-Note-2017-006

DAQ

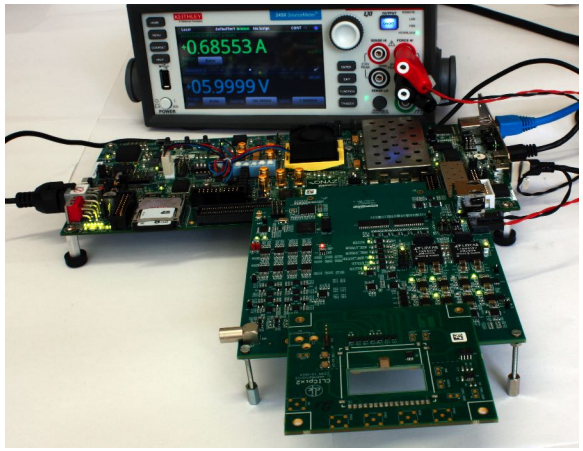
- Lab and beam tests require flexible scalable DAQ hardware and software

Results:
- High-rate beam telescope with Timepix3 detector planes (~1 MHz track rate, ≲2 µm resolution, ~1 ns time resolution)
- CaRIBOu universal readout system developed with ATLAS:
  - System-on-Chip (SoC) architecture
  - Peary DAQ software in Linux system inside FPGA core
  - Integration of CLICpix2, C3PD, ATLASPIX

CLICdp Timepix3 telescope in SPS H6 beam line

Ongoing work:
- New Carboard hardware release with enhanced features
- CLICTD and CLIPS integration
- Preparing for beam tests outside CERN during LS II in 2019/20

CaRIBOu with CLICpix2 r/o ASIC



Future plans:
- Integrate FCAL readout electronics
- Scale to larger systems:
  → Timepix4 beam telescope with CaRIBOu?
  → Prototype of functional ladder?

CLICdp-Conf-2017-012

Powering

- Powering concept has major impact on material budget and heat load
- Small duty cycle of CLIC machine (<10^{-5}) allows for power pulsing, reducing average power consumption

Results:

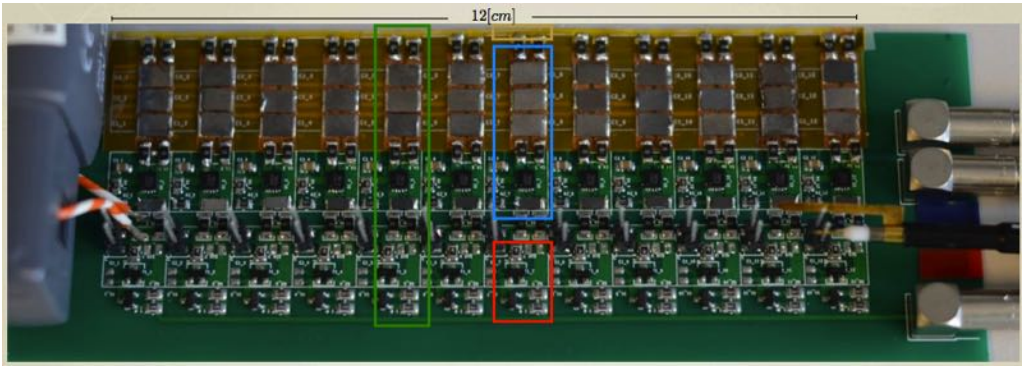
- Prototypes for low-mass power pulsing and power delivery concept for vertex detector
- Local energy storage and voltage regulation
- Small continuous current through low-mass Al cables, stable voltages for r/o ASICs
- ~0.1%X0 material in detector area, expected to decrease to 0.04%X0 in future
- Through-Silicon-Via (TSV) interconnect process (developed for Timepix3 ASICs)

Future plans:

- Adapt concept to requirements of new chips for vertex and tracker?
- Prototype ladder with real ASICs?
- Prototypes of low-mass flex cables?
- Investigate serial powering?

→ More details on power pulsing in talk on DAQ / readout by Eva Sicking in this session

Power-pulsing prototype



CLICdp-Note-2015-004

Cooling

- Vertex detector and tracker require cooling systems with sufficient cooling power and minimal impact on physics performance (material budget, vibrations, constraints for detector layout)

Results:

- Simulations and prototype measurements for vertex air cooling concept with spiral-shaped disc layers
  → ~50 mW/cm^2 feasible
- Water cooling concept for tracker (copied from ALICE ITS upgrade, no dedicated CLIC studies)
  → ~150 mW/cm^2 feasible

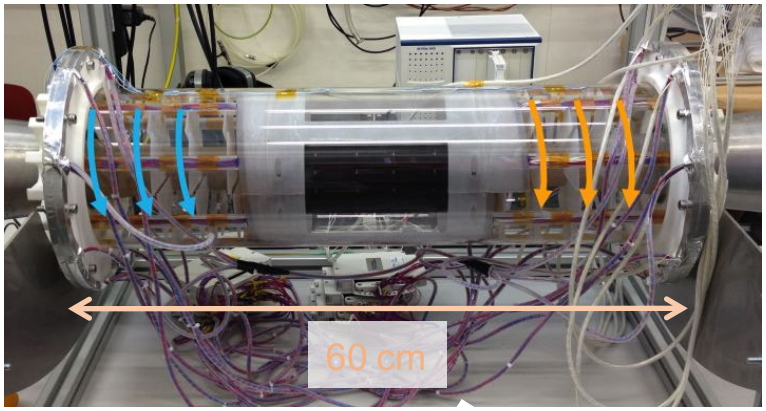
Ongoing work:

- Micro-channel cooling studies (for DEPFET)

Future plans:

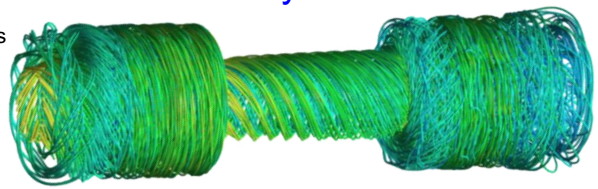
- Optimization study for vertex/tracker operation temperature?
- Develop liquid (micro-channel, CO2?) cooling concept as backup solution for vertex?
- Refine tracker cooling concept?

1:1 scale air cooling thermal test setup



Mass Flow: 20.1 g/s
Average velocity:
@ inlet: 11.0 m/s
@ z=0: 5.2 m/s
@ outlet: 6.3 m/s

Finite-element simulation of air velocity



CLICdp-Note-2016-002

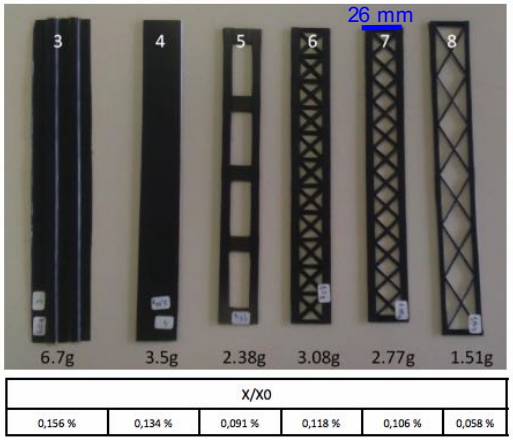
Mechanical integration

Material budget allows for only ~0.1%X0 from cables+supports in vertex region, <1%X0 in tracker
→ Development of low-mass supports with sufficient rigidity required
→ Low-mass services, optimized routing concepts

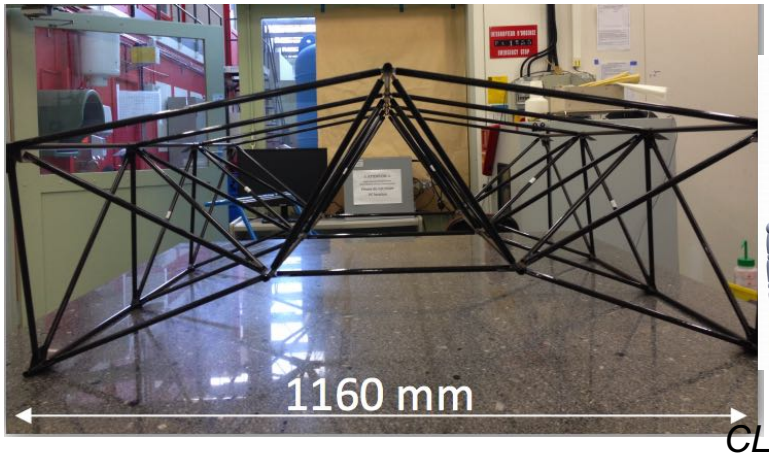
Results:
- Low-mass CFRP stave prototypes for vertex detector, FE simulations
- Concept for supports, beam pipe and cabling in vertex region, FE simulations
- Low-mass tracker support-structure concept, validated in FE simulations
- Prototype for outer tracker support segment

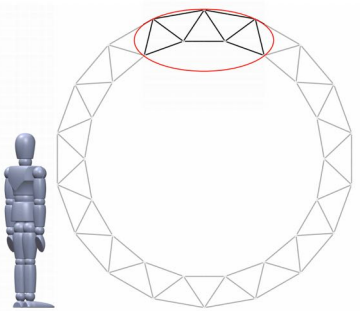
Future plans:
- Investigate new technologies: truss-like carbon structures (→ ALICE ITS upgrade)
- Build more refined prototypes (including cables, …)?
- Concept for services routing through outer detector elements?
  N.B.: details depend strongly on r/o technology choices

CFRP support prototypes



Prototype of outer barrel tracker support structure





CLICdp-Note-2015-002

Conclusions

- Stringent requirements for CLIC vertex and tracking detectors have inspired broad and integrated technology R&D program
- Various sensor + readout technologies under study
- Resolution target for vertex layers remains challenging
- Monolithic pixel detectors under development for large-area tracker
- Detector integration studies demonstrate feasibility of proposed detector concepts

Thanks to everyone who provided material for this talk!

Additional Material

Detector R&D document

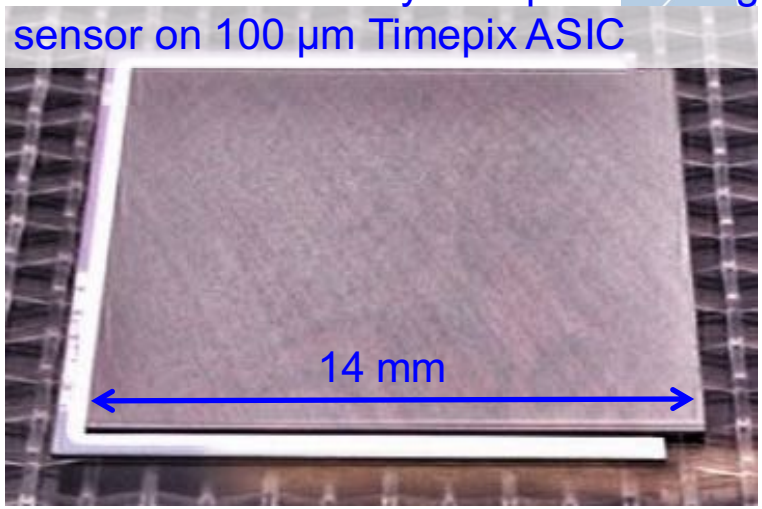
- Document in preparation: Detector Technologies for CLIC
  → Input to European Strategy Update process in 2019
- Description of R&D status for vertex/tracker, calorimetry, readout electronics, tools
- Defined scope, team of editors
- Targeting CERN yellow report, 80-90 pages, ~50% vertex/tracker
- Aim for first draft by summer 2018

Thin-sensors with Timepix(3) r/o

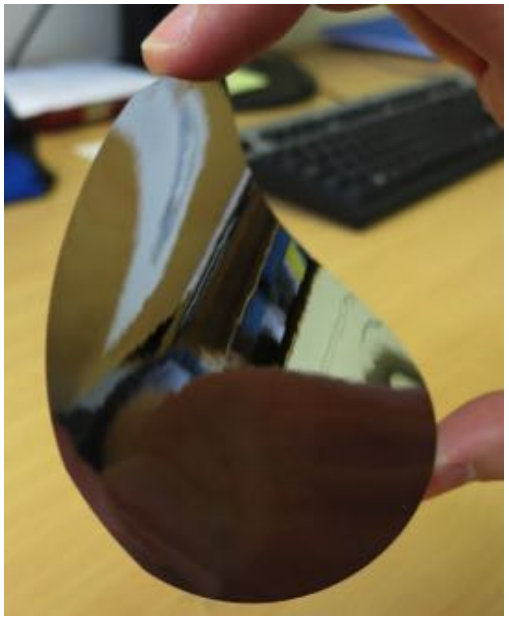
Planar sensor assemblies with 55 µm pitch

- Goal: test feasibility of ultra-thin sensors with minimized inactive regions
- Producers: Micron and Advacam/VTT
- Readout: Timepix / Timepix3
- 50-500 µm sensor,100-700 µm ASIC thickness
- slim-edge and active-edge layouts
- Test-beam campaigns at DESY and CERN PS/SPS
- ultimate goal: 50 µm sensors on 50 µm ASICs

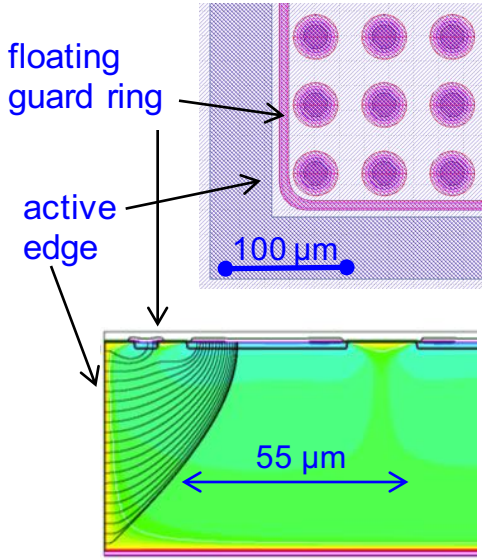
Micron/IZM assembly: 100 µm slim-edge sensor on 100 µm Timepix ASIC



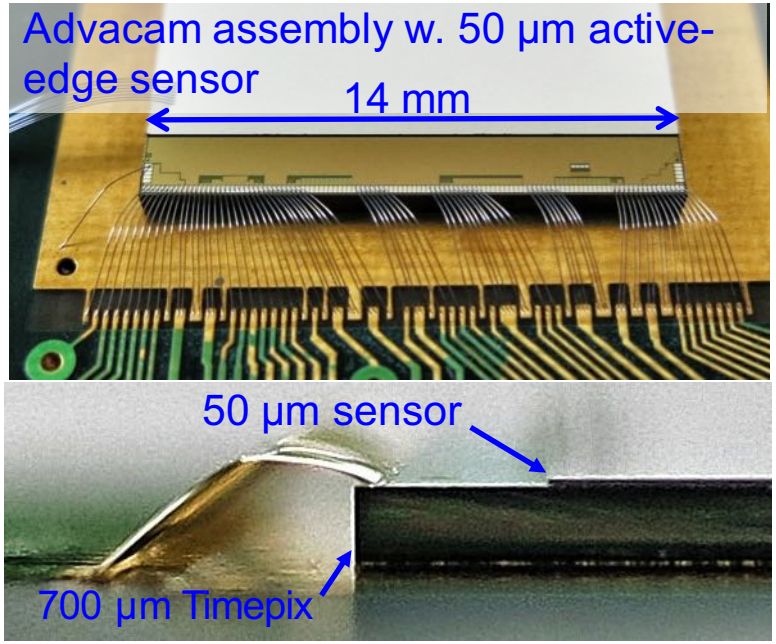
50 µm silicon wafer



Advacam active-edge sensor

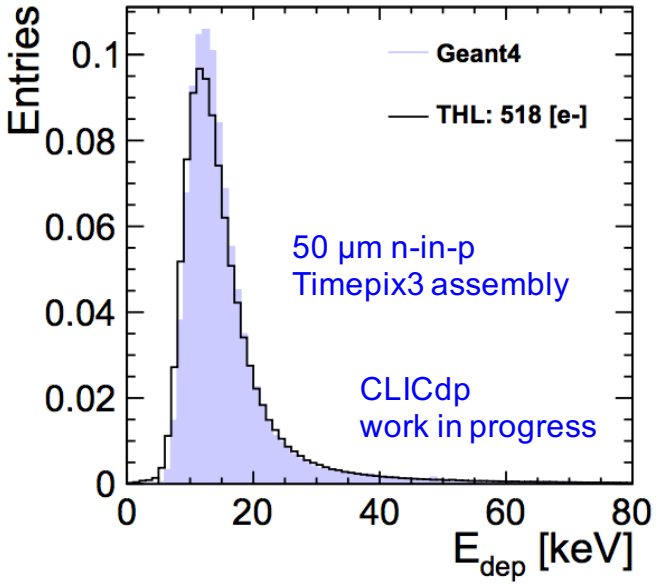


Advacam assembly w. 50 µm active-edge sensor



Efficiency of thin-sensor assemblies

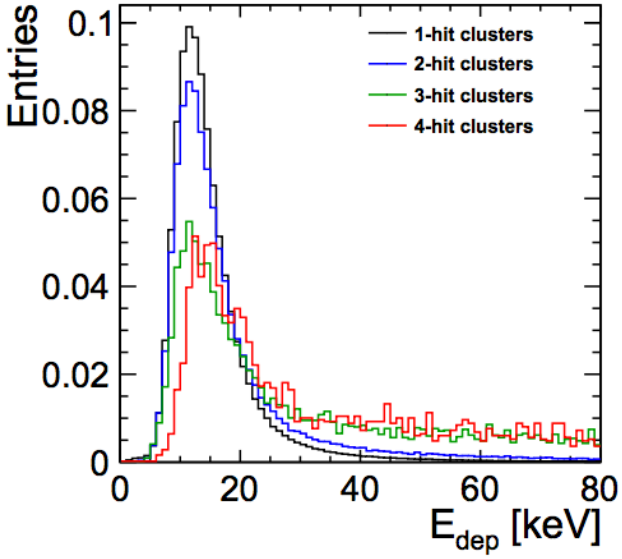
Energy deposition (all clusters)



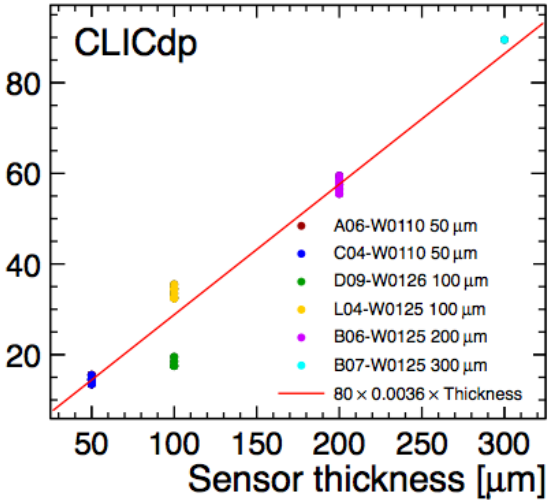
- Test-beam measurements of Timepix/Timepix3 assemblies with different sensor thicknesses:
  - Sufficient energy deposition for MIPs, even for 50 µm sensors
  - Good agreement with Geant4 simulations
  - High detection efficiency (>99%) under normal operating conditions

CLICdp-Note-2016-001

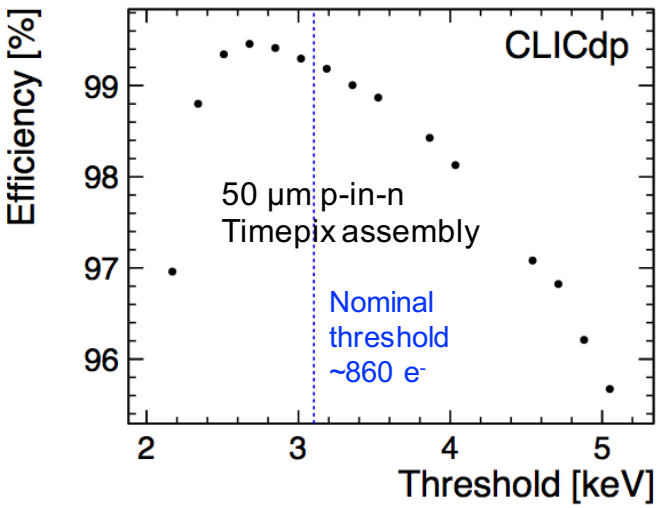
Energy deposition (per cluster size)



Most probable energy deposition

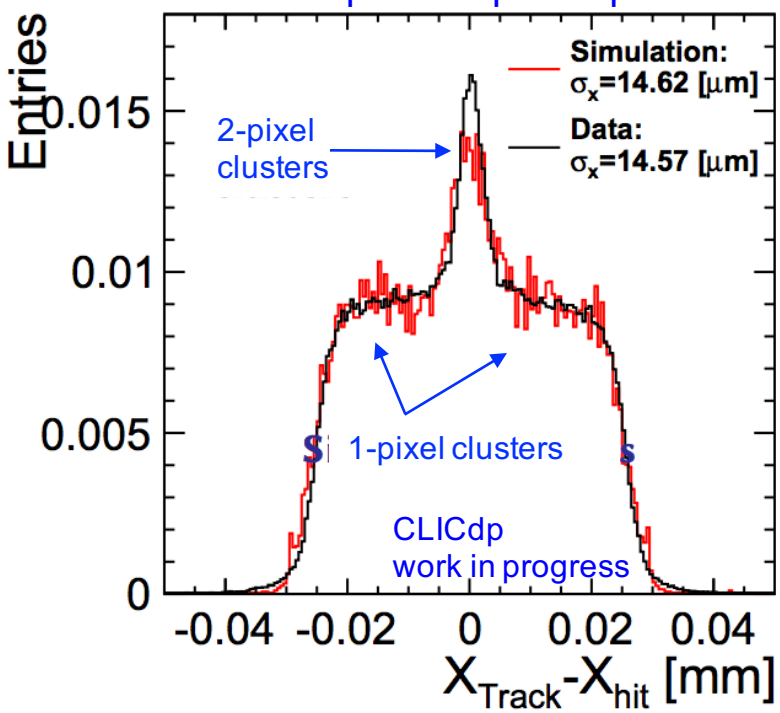


Detection efficiency

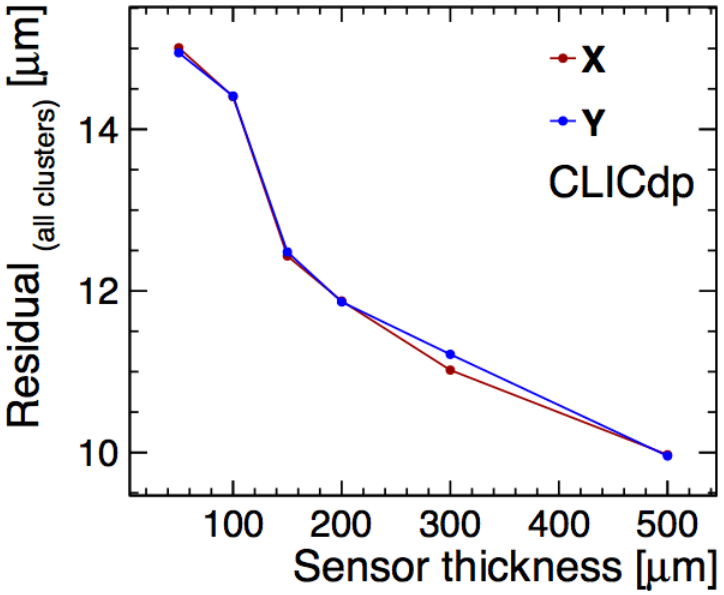


Resolution of thin-sensor assemblies

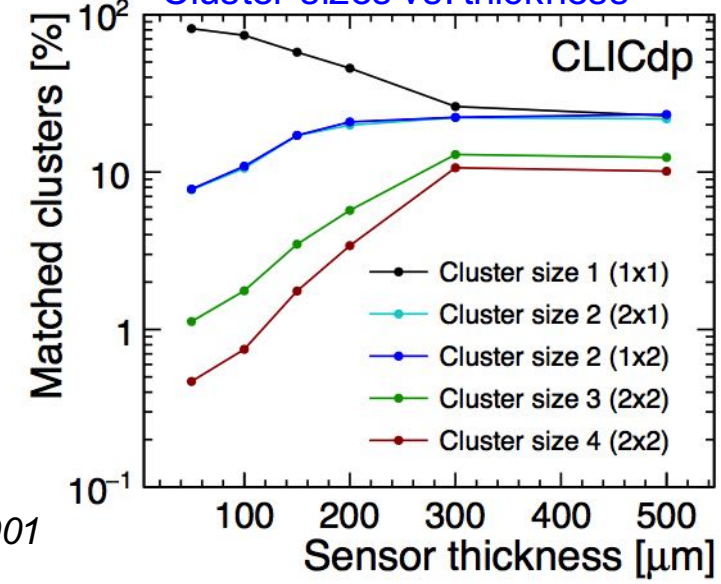
Track residuals 50 µm n-in-p Timepix3 assembly



Track residuals vs. thickness



Cluster sizes vs. thickness



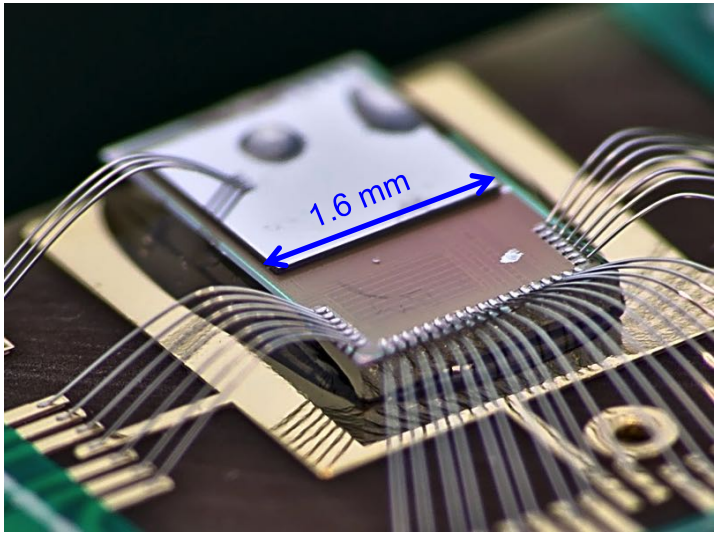
- Achievable resolution limited by fraction of 2-hit clusters
  → Not enough charge sharing in ultra-thin sensors
- Smaller pixel pitch required (see following slides)

CLICdp-Note-2016-001

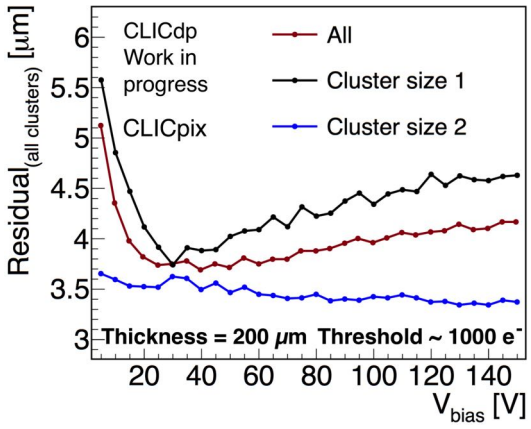
CLICpix planar-sensor assemblies

- 65 nm demonstrator CLICpix r/o ASIC:
  - 64 x 64 pixel matrix
  - **25 µm** pixel pitch
  - simultaneous **4-bit time (TOA) and energy (TOT)** measurement per pixel
- Single-chip indium bump-bonding with 25 µm pitch at SLAC (C. Kenney, A. Tomada)
- Functional assemblies produced with 50-200 µm thick planar sensors (Micron, Advacam active edge)
- <4 µm single-point resolution for 200 µm thickness
- For 50 µm thickness not enough charge sharing, limits resolution to >~7 µm (~1300 e- threshold)

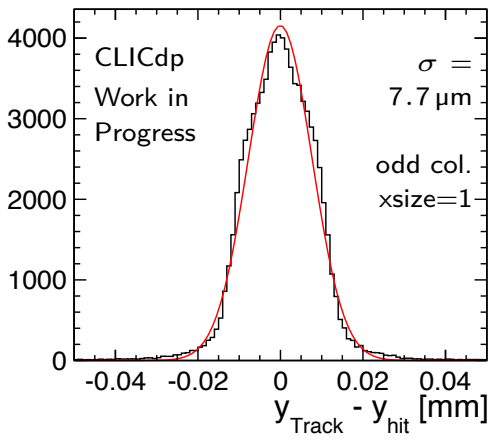
CLICpix with 50 µm planar sensor



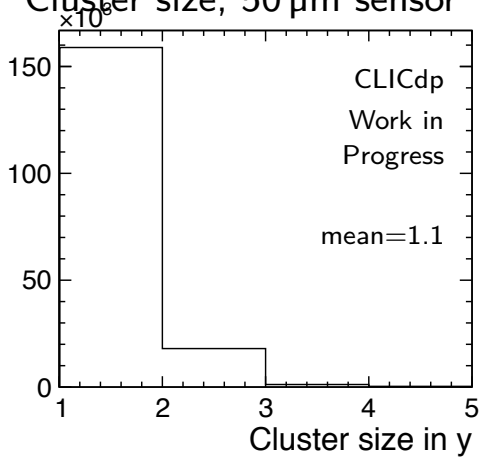
Residual, 200 µm sensor



Residual, 50 µm sensor



Cluster size, 50 µm sensor

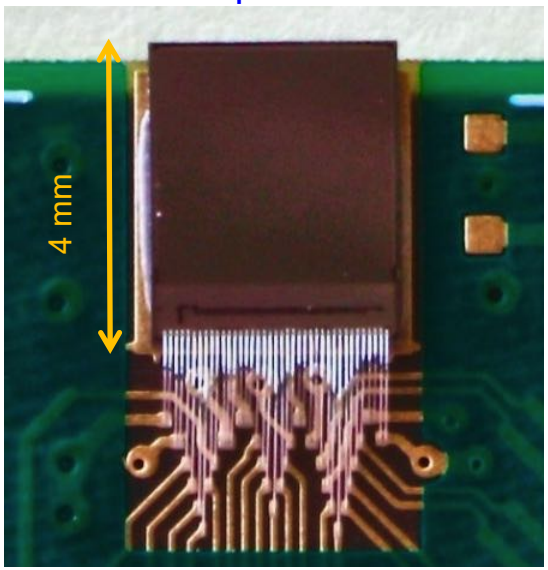


CLICpix2 r/o ASIC

- New CLICpix2 in same 65 nm process as CLICpix:
  - Increased matrix size to 128 × 128 pixels
  - Longer counters for charge (5-bit) and timing (8-bit) measurements
  - Improved noise isolation and removal of cross-talk issue observed in first CLICpix
  - More sophisticated I/O with parallel column readout and 8/10 bit encoding
  - Integrated test pulse DACs and band gap

- Test results with chips from Multi-Project-Wafer-Run
- Same chip on RD53 wafer, received in Dec 2017 (change from 5+1 to 7+1 metal layers)
  → access to full wafers for bump-bonding process development

CLICpix2



CLICpix2 analog F/E specifications

Parameter	Value
Power dissipation	≤ 12 µW
Area	≤ 12.5x25 µm²
Input charge, Q_{in}	nominal 4 ke-, max. 40 ke-
Minimum threshold, $Q_{th,min}$	≤ 600 e-
Equivalent input-referred noise, $Q_{n,in}$	≤ 70 e-
ToT dynamic range	≥ 40 ke-
ToA accuracy	≤ 10 ns
Total ionizing dose (for 10 yr)	1 Mrad
Input charge types	e-, h+
Testability	in-pixel test pulse (i.e. Q_{test}) injection

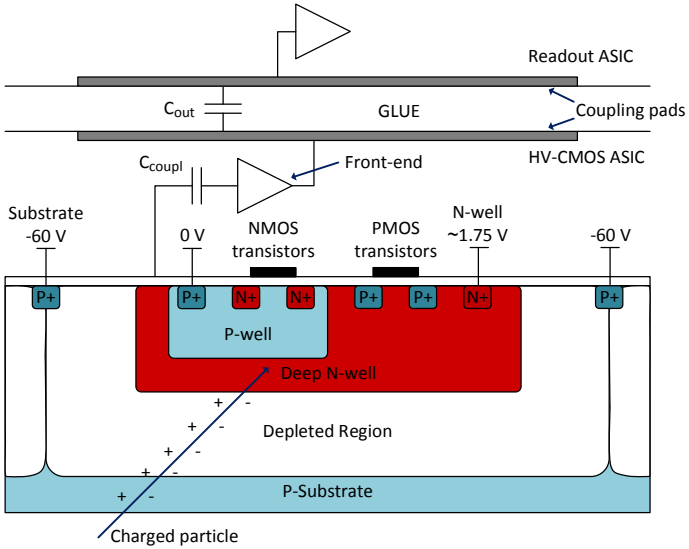
C3PD HV-CMOS sensors

- C3PD: active HV-CMOS sensor for capacitive coupling
- Commercial 180 nm High-Voltage CMOS process: transistors in deep n-well, acting as collecting electrode
- Footprint matching CLICpix2: 128 x 128 pixels, 25x25 μm^2
- Charge Sensitive Amplifier (CSA) + unity gain buffer

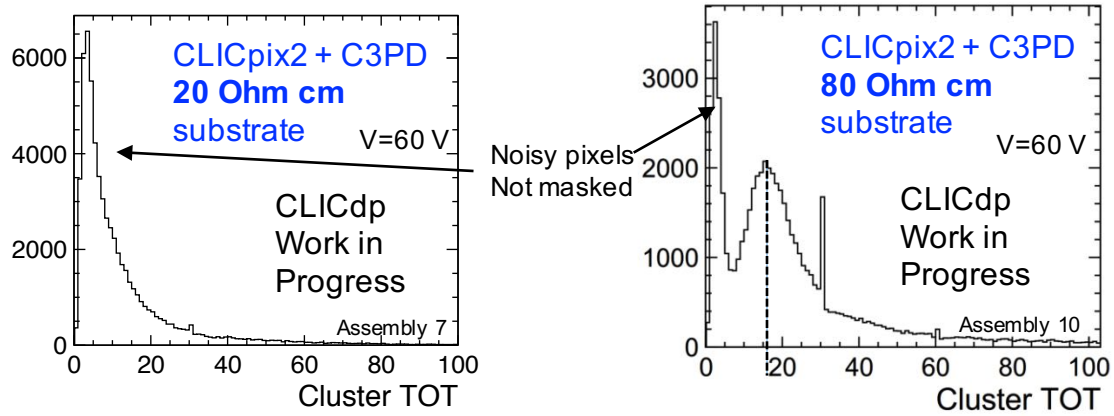
- Production wafers of various resistivities: 20, 80, 200, 1000 Ohm cm
- Test-beam results for standard bulk resistivity: ~20 Ohm cm, ~15 µm depletion at 60 V

- First lab tests for assemblies with 80 Ohm cm confirm larger drift signal, increased active depth ~25 µm

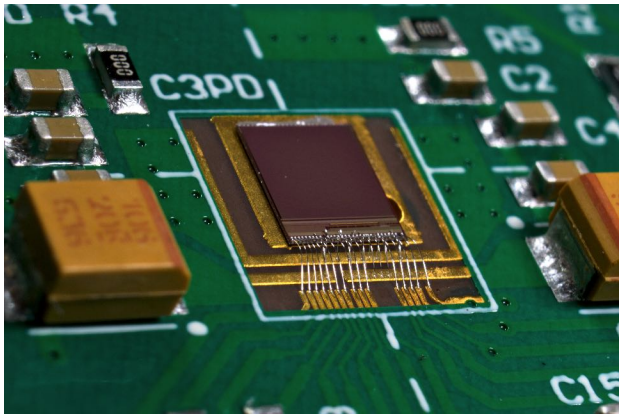
Schematic cross section of C3PD



Sr-90 source exposure



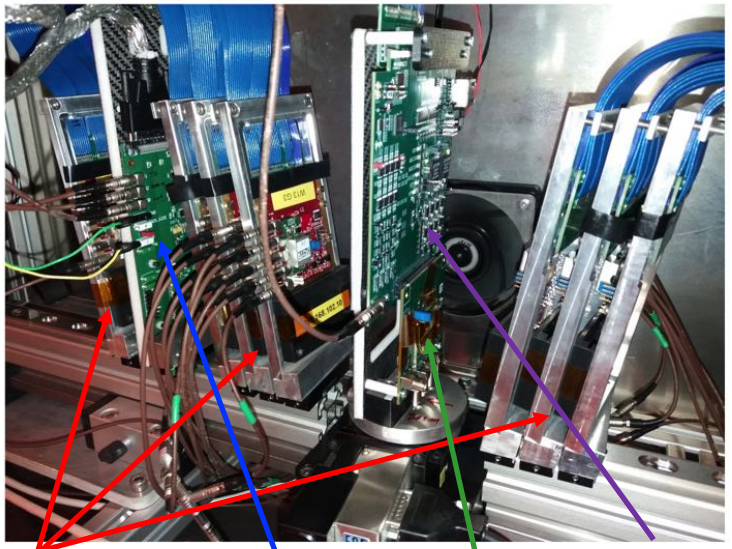
C3PD chip thinned to 50 µm



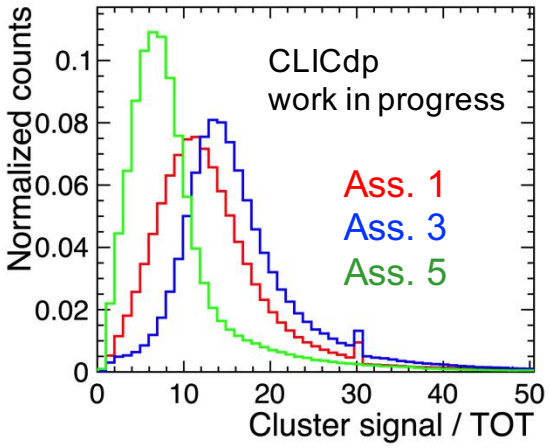
C3PD+CLICpix2 in test beam

- Test-beam measurements in CLICdp Timepix3 telescope for 5 assemblies with 20 Ohm cm substrate:
  - C3PD bias scans
  - CLICpix2 threshold scans
  - Angles between 0° (perpendicular) and 30°
- Analysis in progress
- Preliminary results show difference in cluster signals and sizes (varying glue-assembly quality)
- Similar residuals of 8.5-9 µm (threshold <~1000 e^-), as expected from low cluster multiplicities
- Expect improved performance for high-res. substrates

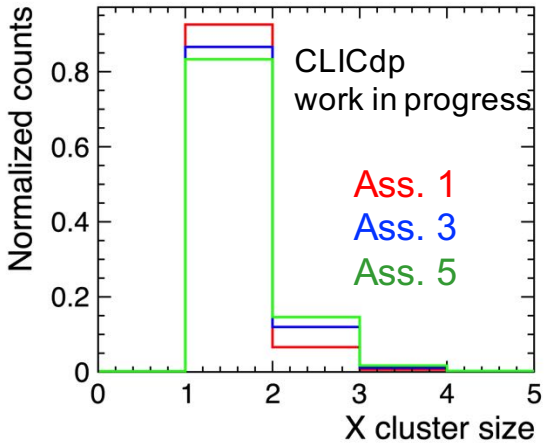
C3PD+CLICpix2 assembly in Timepix3 telescope



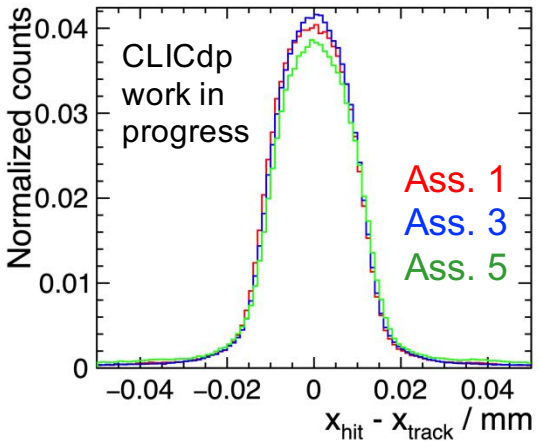
Cluster signal



Cluster size



Position resolution

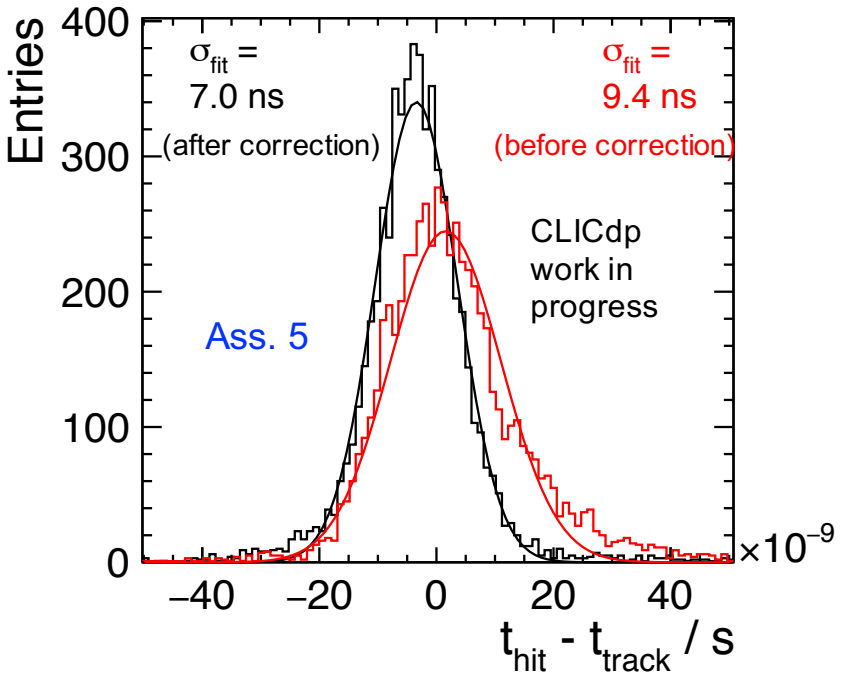


C3PD+CLICpix2 time resolution

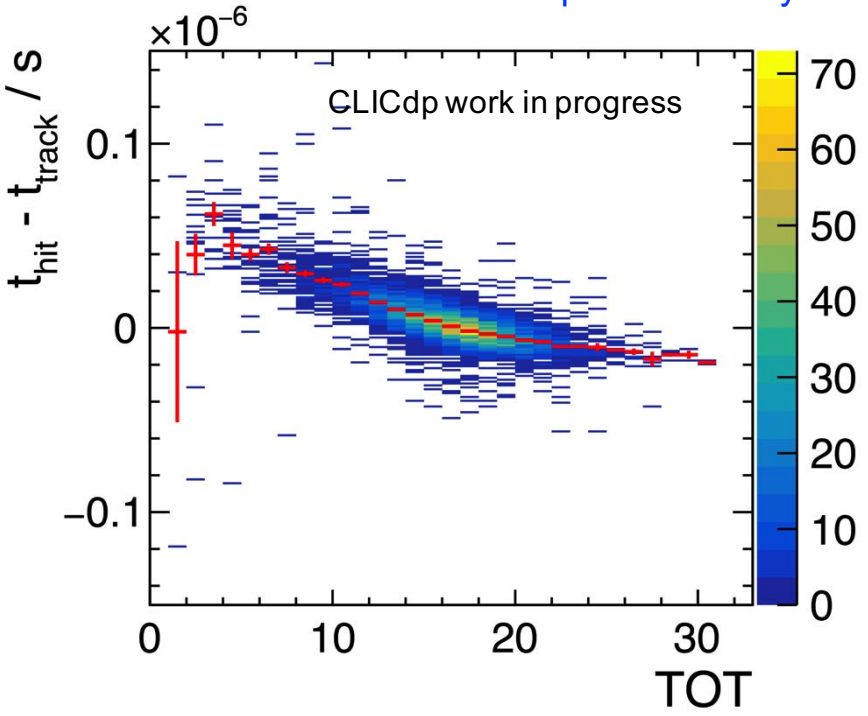
- Track time resolution of CLICdp Timepix3 telescope <~1 ns
  → precise characterization of DUT timing capabilities
- CLICpix2: 100 MHz ToA clock → 10 ns time binning
- Gauss fit of time residuals shows width of ~9 ns
- Tail towards later times, as expected from time walk

→ Time residual reduced to ~7 ns after time-walk correction

Hit time residuals in C3PD+CLICpix2 assembly

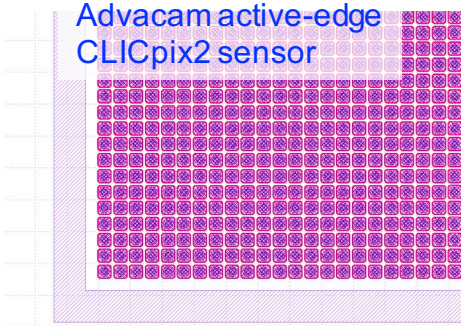


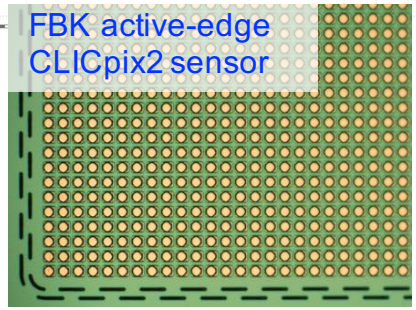
Time Walk in C3PD+CLICpix2 assembly



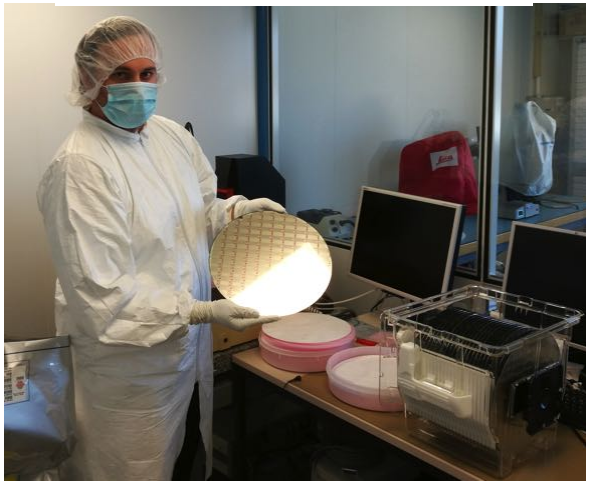
Planar sensors on CLICpix2

- Test results with planar sensors (25x25 μm^2 pitch) needed for full assessment of CLICpix2 performance
- Planar active-edge CLICpix2 sensors with UBM available:
  - Advacam MPW production with ATLAS (50-150 μm thick)
  - FBK AIDA-2020 production (130 μm thick)
- Single-chip bump-bonding on carrier wafers in progress at IZM + thinning of ASICs
- Future plan: develop wafer-level bump deposition process for CLICpix2 wafer from RD53 submission

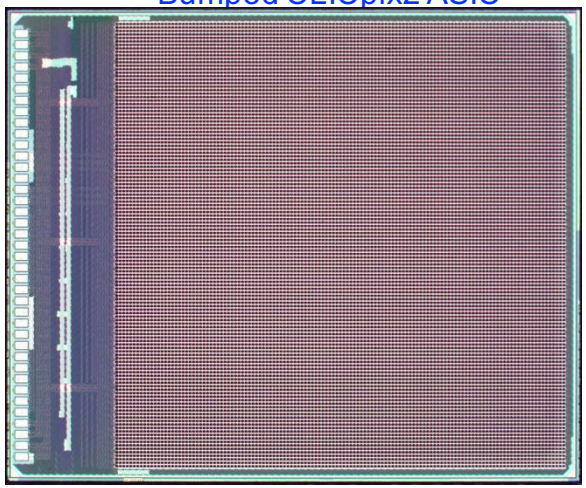


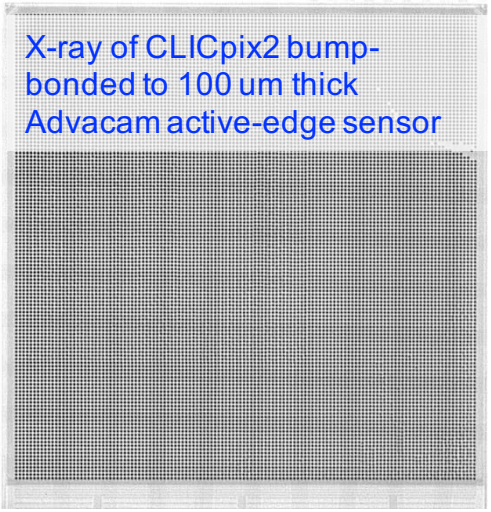


RD53 12" wafer with CLICpix2



Bumped CLICpix2 ASIC



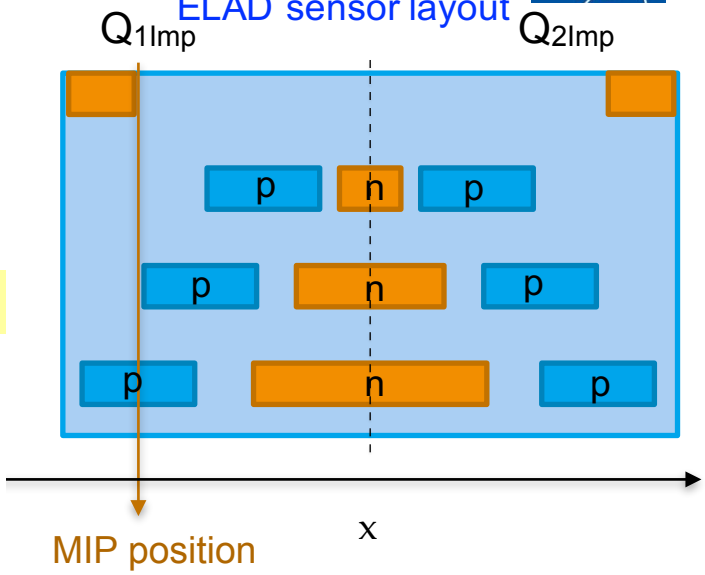


ELAD sensors

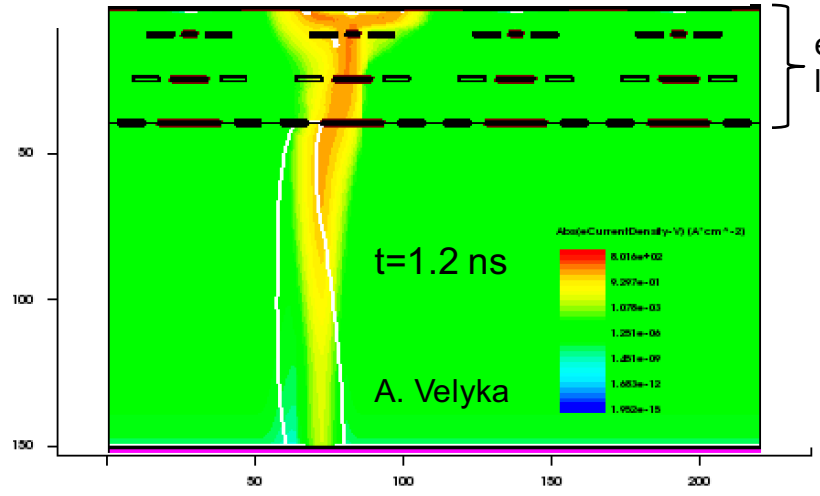
- Position resolution in very thin sensors so far limited to ~pixel pitch / √12 (almost no charge sharing)
- New sensor concept for enhanced charge sharing
  Enhanced **LA**teral **D**rift sensors (ELAD), H. Jansen (DESY/PIER)
- Deep implantations to alter the electric field
  → lateral spread of charges during drift, cluster size ~2
  → improved resolution for same pitch
- Challenges:
  - Complex production process, adds cost
  - Have to avoid low-field regions (recombination)
- Ongoing TCAD simulations:
  - Implantation process
  - Sensor performance for MIPs
- First production in 2018: generic test structures, strips and test sensors with Timepix footprint (55 µm pitch)

Patent DE102015116270A1

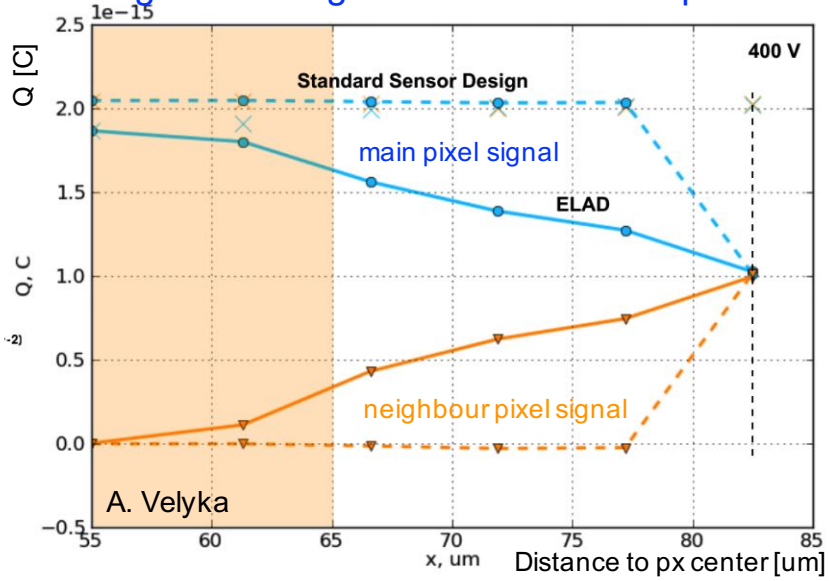
ELAD sensor layout



TCAD simulation of current from MIP



Integrated charge as function of MIP position

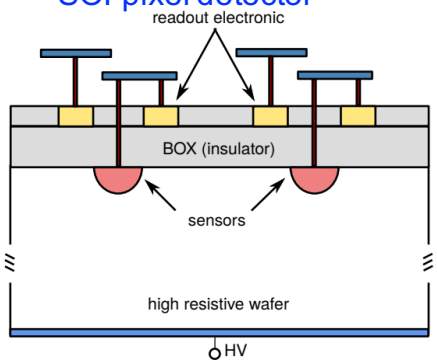


Monolithic SOI sensors

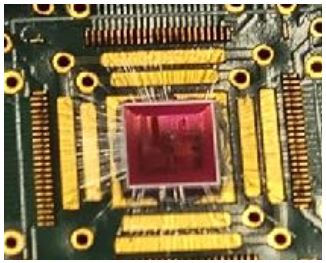
- Sensor and electronics integrated on single wafer with high-resistivity substrate, separated by insulation oxide layer + buried p-wells,
- Considered for vertex and tracker

- Cracow SOI test chip in 200 nm LAPIS SOI process, with various geometries and technology parameters: >=30x30 μm^2 pitch, single SOI and double SOI, different r/o schemes
- Test results for 500 μm thickness, 30x30 μm^2 pitch, rolling-shutter r/o: >99% efficiency, σ_{SP}<~2 μm

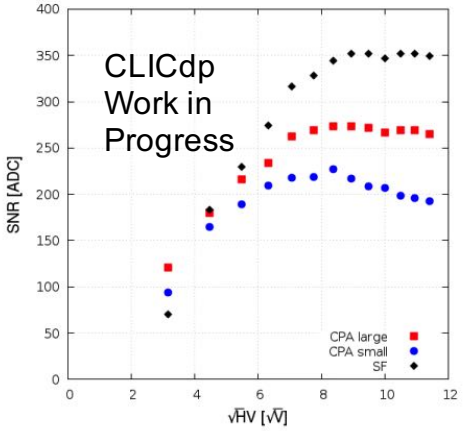
SOI pixel detector



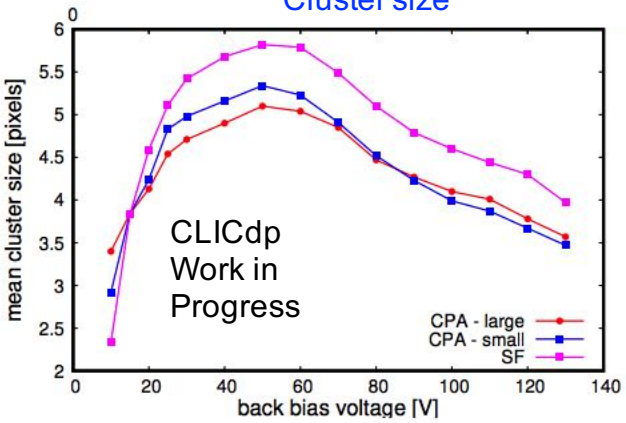
Cracow SOI test chip



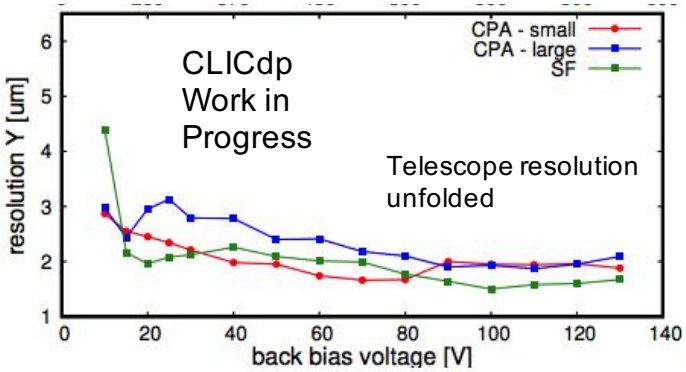
Signal-to-Noise



Cluster size



Resolution in y-direction

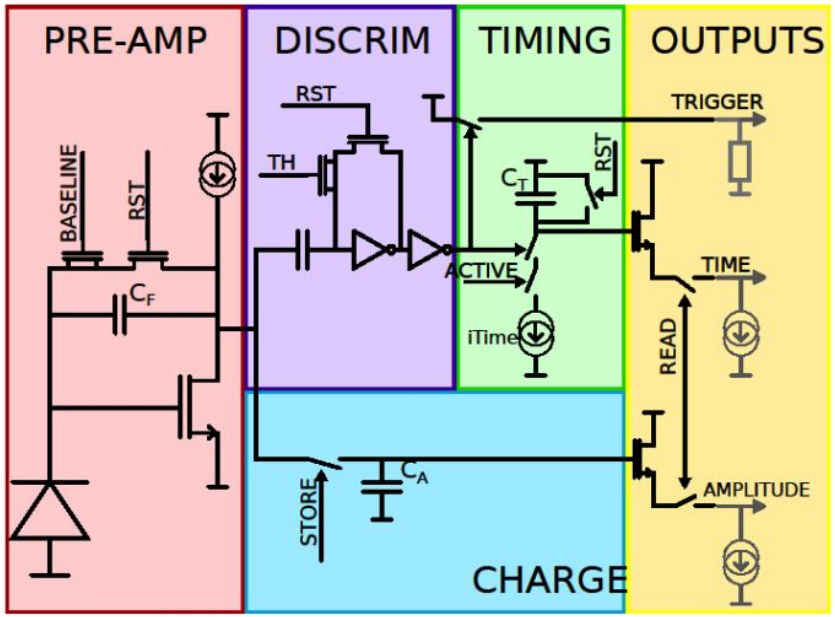


CLIPS SOI sensor

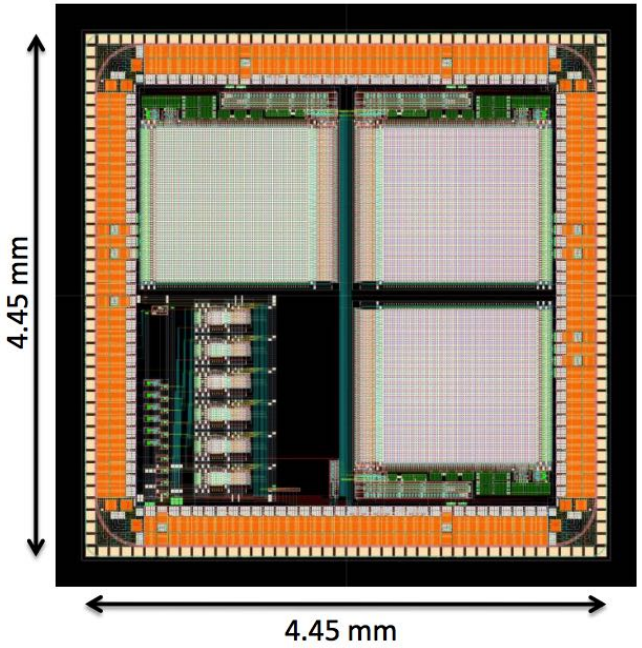
- CLIPS: New AGH SOI chip design targeted to Linear Collider VTX detectors:
  - 64x64 matrix with 20x20 µm^2 pixels
  - Targets spatial resolution <3 µm, time resolution <10 ns
  - Analog charge and time information in storage capacitors in each pixel
    → no need for fast clock distribution into matrix
  - Snapshot analog readout between bunch trains with external ADC
  - On chip trigger to reduce the data rate
  - Chip submitted November 2017
    → 300-500 µm thick samples expected in April 2018
    → 75-100 µm thinned wafers ~June 2018

CLIPS
CLIc Pixel Soi

CLIPS pixel design



CLIPS layout

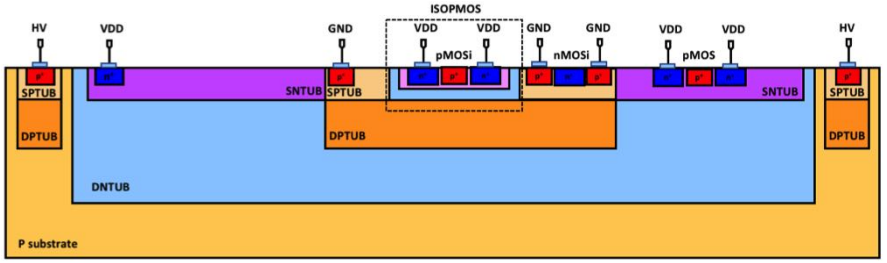


Monolithic HV-CMOS: ATLASPIX

180 nm HV-CMOS process:

- Fully integrated chip designed for ATLAS ITk upgrade
- Process modification: isolated PMOS
- 25 x 400 pixels, 130 µm x 40 µm pixel size
- 20-1000 Ω cm substrates
- Charge amplifier, discriminator in pixel
- ToT and ToA in periphery (point-to-point connection)

ATLASPIX process cross section

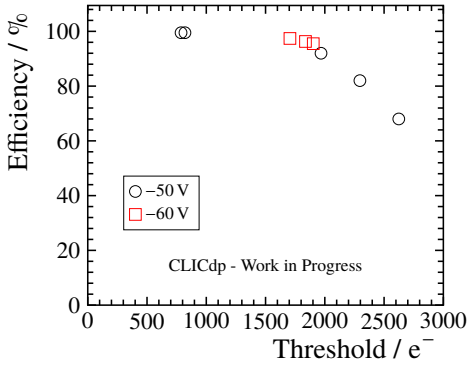


I. Peric et al.

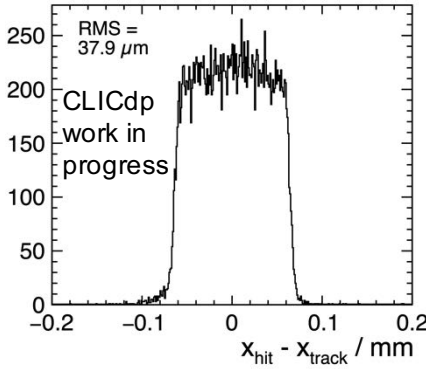
Tests for 80 Ω cm ATLASPIX_Simple in view of CLIC tracker requirements:

- Laboratory calibration and beam tests in CLICdp Timepix3 telescope at CERN SPS
  - Efficiency 99.6%
  - Limited charge sharing → box-shaped residuals, σ~pitch/√12
  - Time resolution ~30 ns, dominated by 10 MHz r/o clock, to be improved with new Caribou r/o system

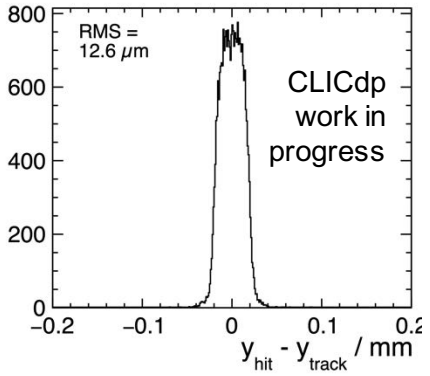
Efficiency



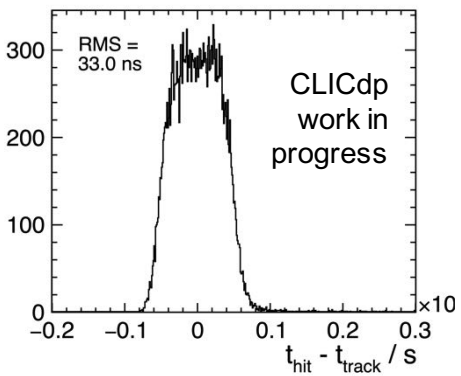
Residual in column direction



Residual in row direction



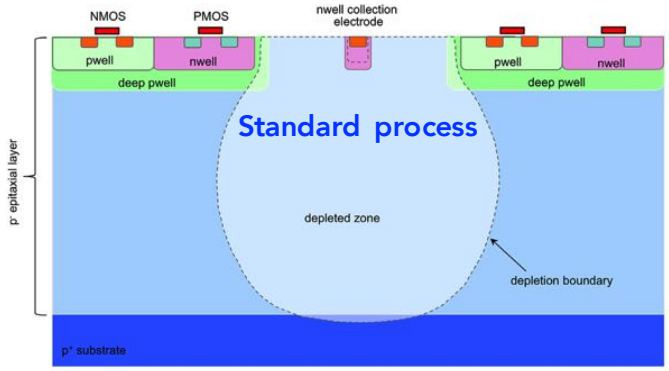
Timing residual



Monolithic HR-CMOS: INVESTIGATOR

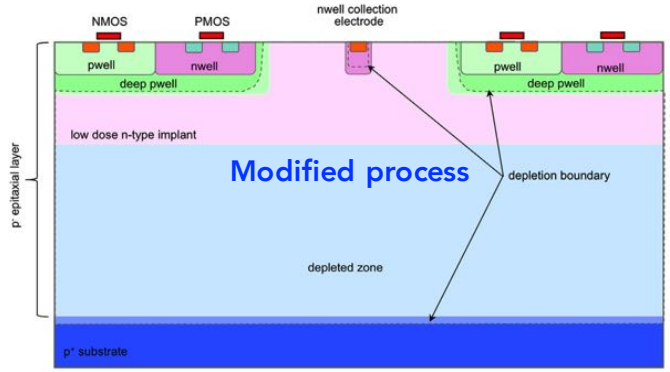
180 nm HR-CMOS process:

- High-Resistivity epitaxial layer (15-40 µm, 1-8 kΩ cm)
- CMOS circuitry shielded by deep P-well
- Small collection diode → small capacitance:
  - Maximise signal/noise
  - Low analogue power consumption and fast timing
- Frontside biasing:
  - Bias voltage limited by CMOS transistors to -6 V



Modified process:

- Additional low-dose N-implant to achieve full lateral depletion:
  - Improved radiation tolerance
  - Faster charge collection
  - Backside biasing possible (not limited to -6 V)

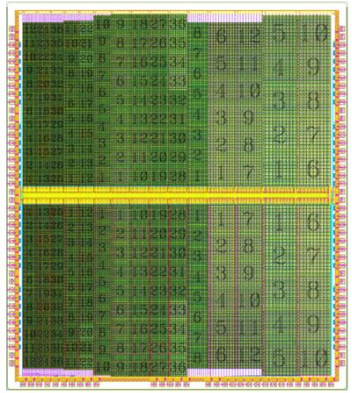


W. Snoeys et. al: http://dx.doi.org/10.1016/j.nima.2017.07.046)

INVESTIGATOR test chip developed for ALICE (W. Snoeys et al.):

- 134 mini-matrices with 8 x 8 pixels (variation of pixel size, collection electrode size, …)
- Source follower in each pixel, analog signals routed to periphery
- Readout with external 65 MHz sampling ADC per pixel
- Beam tests in CLICdp Timepix3 telescope, using chips with 25 µm epi thickness and 28 µm pitch, both processes

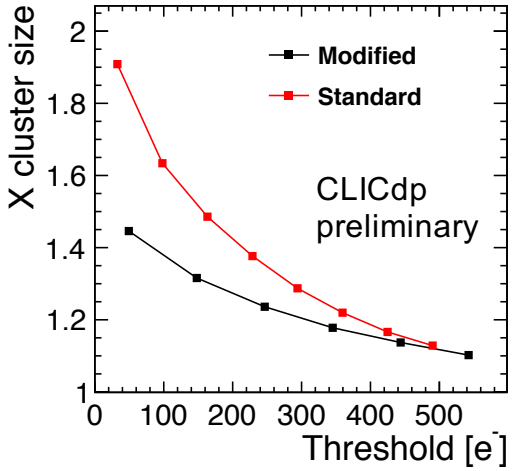
Investigator chip layout



INVESTIGATOR resolution and efficiency

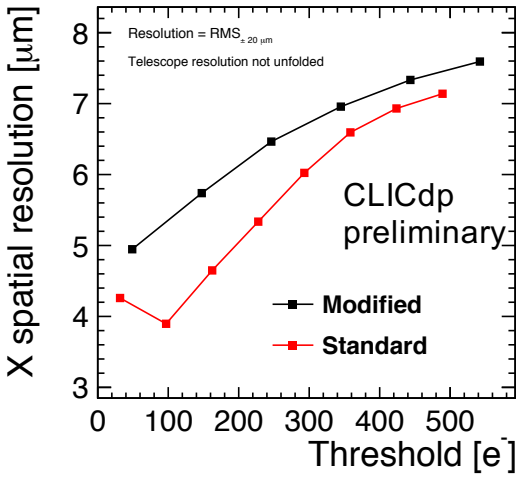
Impact of charge sharing on spatial resolution and efficiency for standard & modified process (pitch of 28 µm, bias voltage of -6 V):

X cluster size vs. threshold:



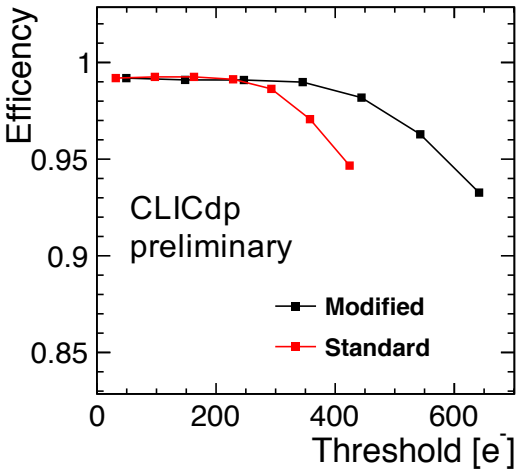
- More charge sharing for standard process
- Expected from non depleted regions (diffusion)

X resolution vs. threshold:



- Better spatial resolution for standard process down to ~ 3.5 µm

Efficiency vs. threshold:



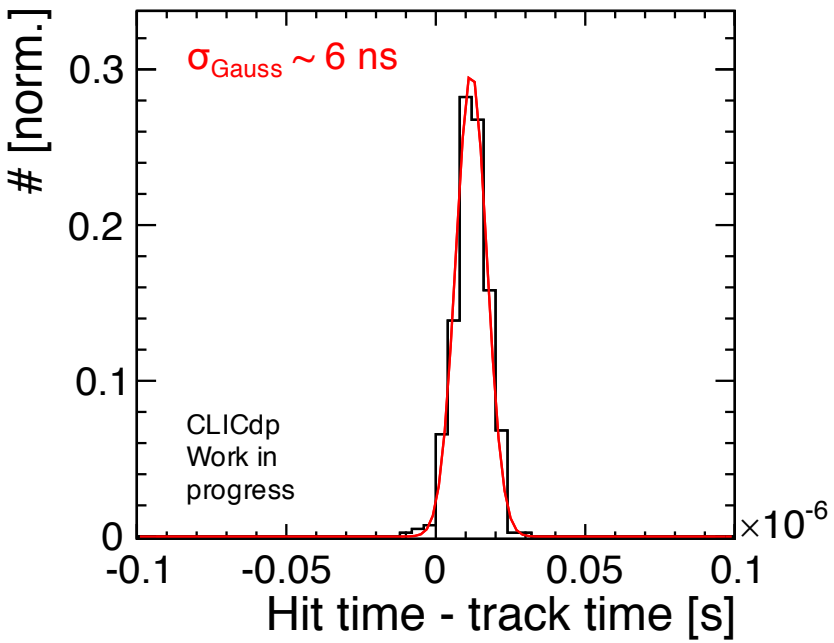
- Earlier drop of efficiency (at lower thresholds) for standard process

→ Efficiency & spatial resolution for both process variants within requirements for CLIC tracker.

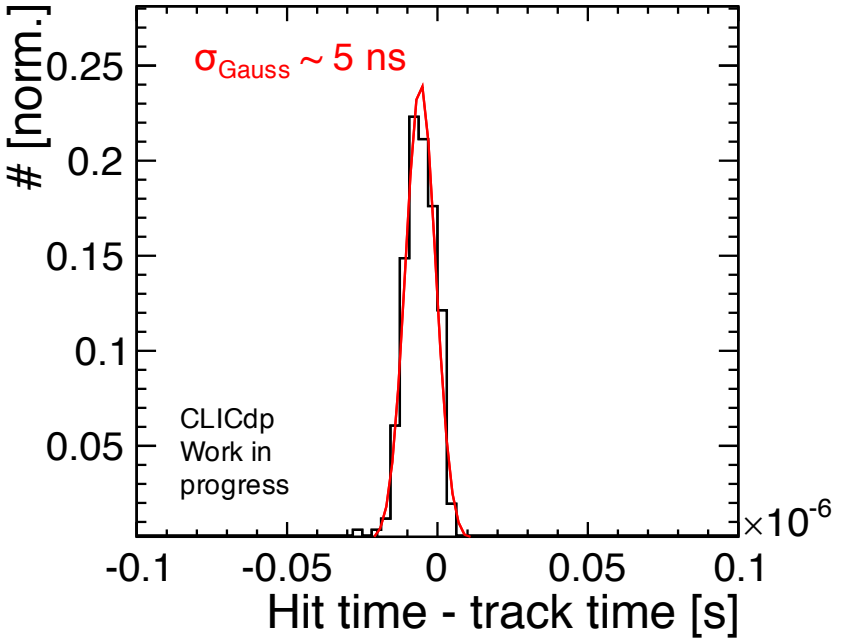
INVESTIGATOR timing

Timing resolution for standard & modified process (pitch of 28 µm, bias voltage of - 6 V):

Standard process:



Modified process:



Comparable timing resolution for both processes
(Readout sampling frequency of 65 MHz limits achievable precision)

CLICTD monolithic HR-CMOS tracker chip

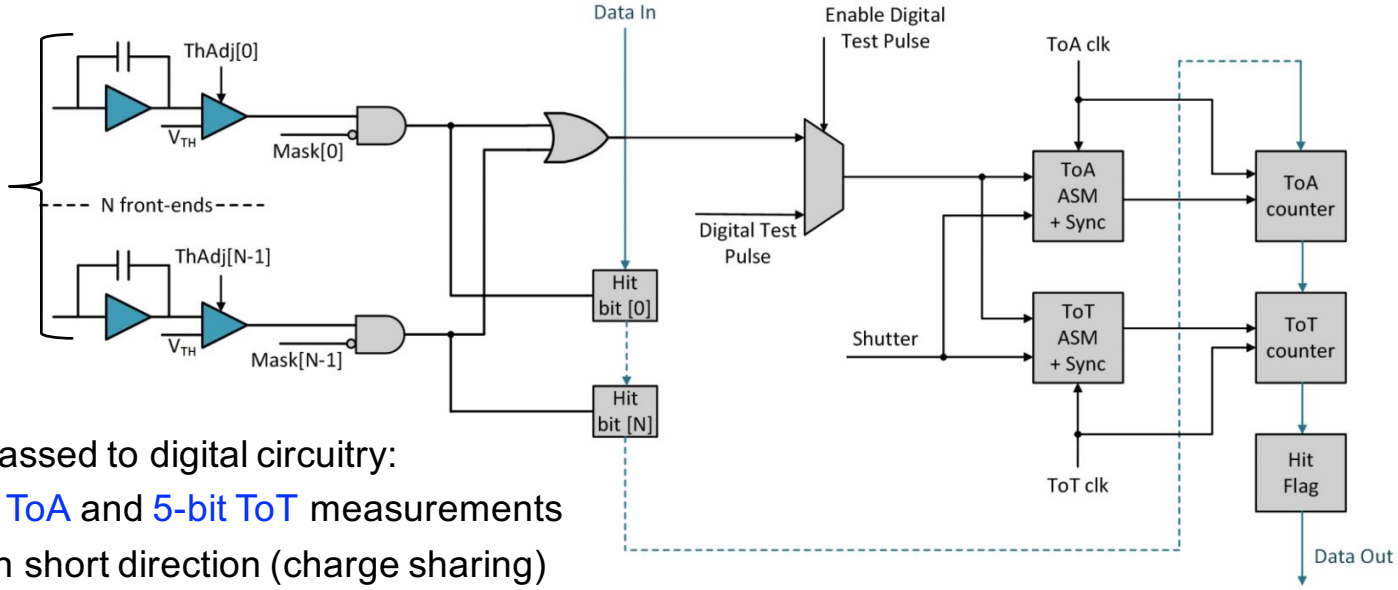
Good performance of studied 180 nm HR-CMOS technology with respect to requirements of CLIC tracker

→ Technology used for ongoing design of a fully integrated chip for the CLIC tracker

CLIC Tracker Detector (CLICTD) – monolithic HR-CMOS sensor with 30 µm x 300 µm pixels

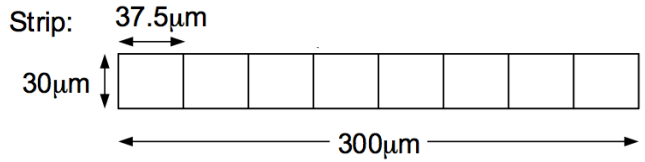
Segmented macro-pixel structures to maintain advantages of small collection diode (prompt and fully efficient charge collection) while reducing digital logic:

Discriminator output of 8 collection diodes combined in logical OR



Output of logical OR passed to digital circuitry:

- Simultaneous 8-bit ToA and 5-bit ToT measurements
- Expect σ_{SP}~7 µm in short direction (charge sharing)
- Hit bit pattern → maintain good resolution also in long direction
- 100 MHz clock to achieve 10 ns time binning

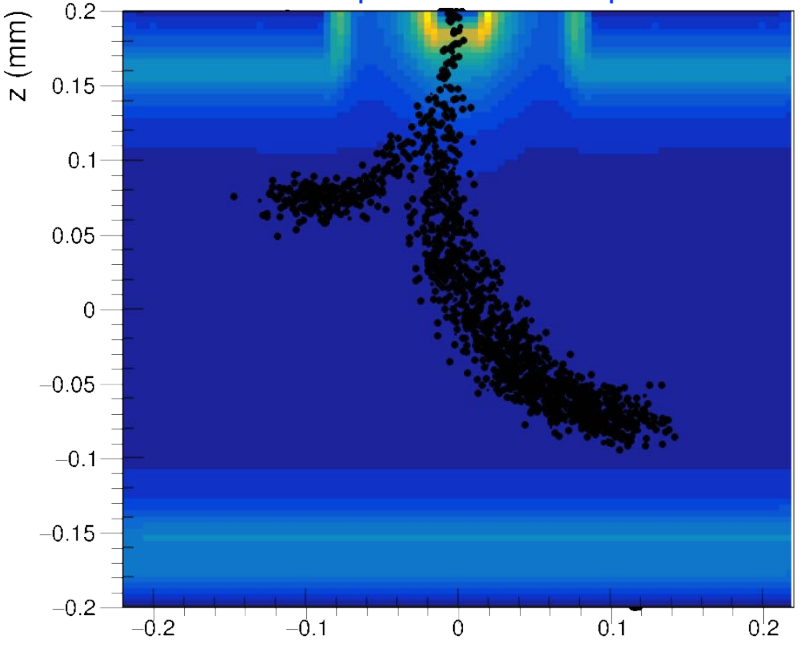


Chip design in progress, target submission date: ~May 2018

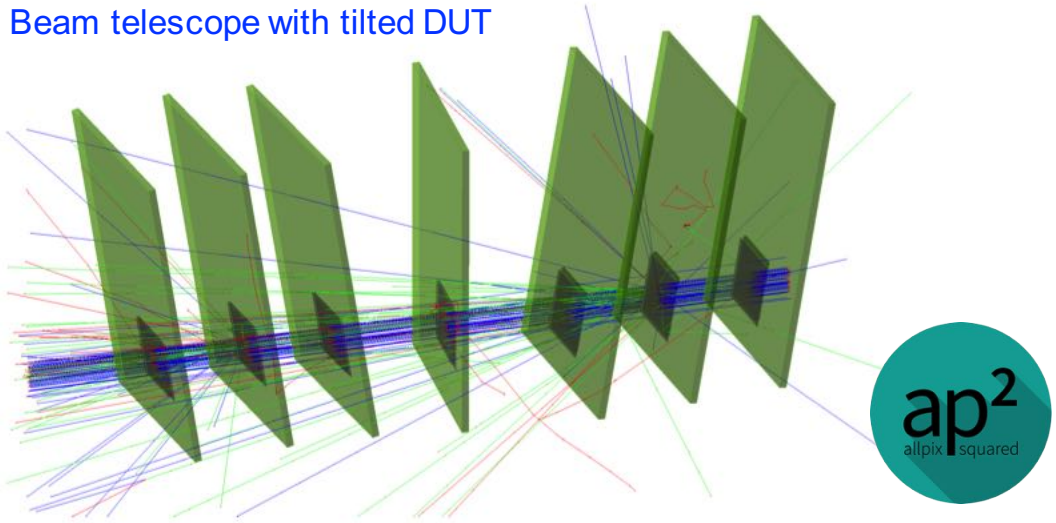
Allpix² simulation framework

- Modular simulation framework for silicon tracking detectors
- Simulates full chain from incident radiation to digitized hits
- Modern and well-documented C++ code
- Full Geant4 simulation of charge deposition
- Fast charge propagation using drift-diffusion model, can import electric fields in the TCAD DF-ISE format
- Simulation of HV-CMOS sensors with capacitive coupling
- Easy to add new modules for new digitizers, other output formats, etc.
- For Introduction, User manual and code reference visit: https://cern.ch/allpix-squared

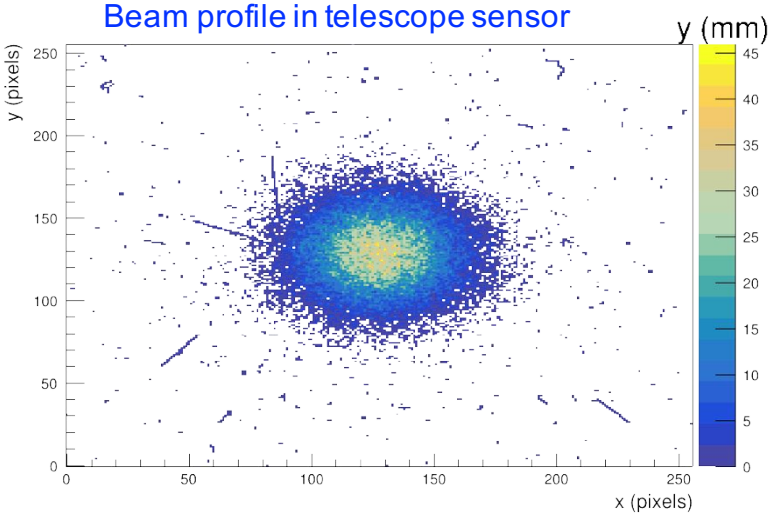
MIP in underdepleted HV-CMOS pixel sensor



Beam telescope with tilted DUT



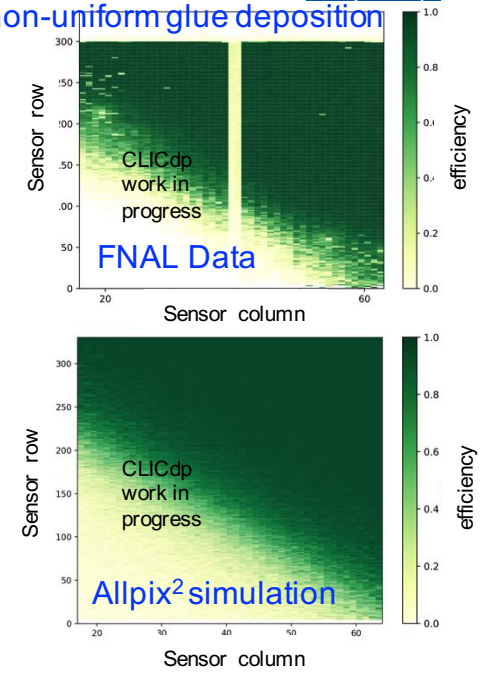
Beam profile in telescope sensor



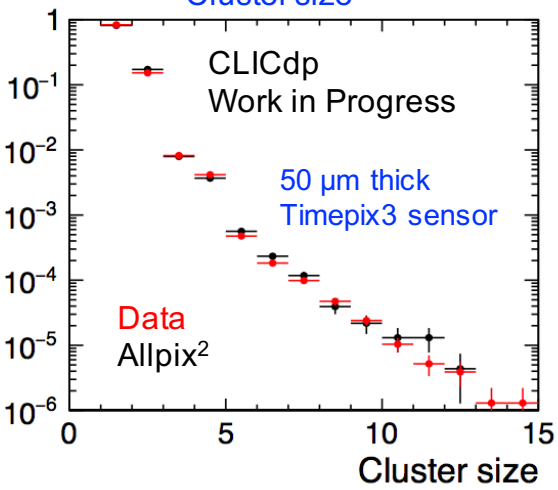
Allpix² validation

- Validation ongoing using test-beam data:
  - Timepix3 planar sensor assemblies:
    Charge distribution, cluster size and spatial residuals
    in good agreement with test beam data
- New sensor types and features are being added by users:
  - SOI pixel detectors
  - capacitively coupled HV-CMOS sensors
  - ELAD sensors
  - …

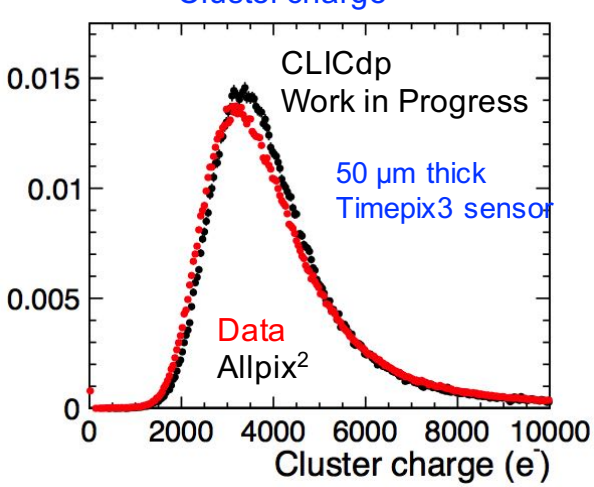
FEI4/H35DEMO: capacitive coupling with non-uniform glue deposition



Cluster size



Cluster charge



Spatial residuals