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Book of Abstracts

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Precision Timing Detectors I / 1

Recent Results with Ultra-Fast Silicon Detectors

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Comprehensive overview of results of measurements with Silicon Detectors with gain. (UFSD).

Time resolution, signal-to-noise, bias voltage as a function of irradiation levels with neutrons and protons will be shown for sensors with thickness from 35um to 60um, some with substitution of Boron by Gallium and infusion of Carbon.

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Very thin LGAD for tracking particles at fluences above 5E15 n/cm2

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In this contribution, we explore the possibility of using very thin LGAD (~ 20 microns thick) as tracking detector at very high fluences. Current silicon detectors generate signals at most of 1-2 fC: we believe that very thin LGAD can provide signals of this magnitude via the interplay of gain in the gain layer and gain in the bulk.

Up to fluences of 1-2E15 n/cm2, thin LGAD still have a gain of ~ 10 while at higher fluences the increased bias voltage will trigger the onset of multiplication on the bulk.

Key to this idea is the possibility of a reliable, high-density LGAD design able to hold large bias voltages (~500V)

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Application of p-i-n photodiodes to charged particle fluence measurements beyond 10^15 1-MeV-neutron-equivalent/cm^2

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Methods are developed for the application of forward biased p—i—n photodiodes to measurements of charged particle fluence beyond 10^15 1-MeV-neutron-equivalent/cm^2. An order of magnitude extension of the regime where forward voltage can be used to infer fluence is achieved for OSRAM BPW34F devices.

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DAQ development for the characterization of the RD50 HV-CMOS devices

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This contribution will describe the developments foreseen for the characterization of the RD50 MPW1 HV-CMOS monolithic pixel sensors implemented in the LFoundry 150 nm technology in the framework of the RD50 collaboration. A custom board to accommodate the RD50 MPW1 device under test is being designed. This board will be fully compatible with the CaR (Control and Readout) interface board used in the CaRIBOu (Control and Readout Inner tracking Board) data acquisition system (DAQ). The CaRIBOu DAQ is widely used for the characterization of new pixel detectors and ASICs (CLICpix2, C3PD, FEI4 or H35Demo). The CaR board is an open hardware FMC mezzanine which can be used as a general purpose multi-chip interface board. As a first approach, some firmware and software will be developed to adapt the CaRIBOu DAQ to read out the RD50 MPW1 devices. Subsequently, the experience gained will allow us to develop our own modular and versatile DAQ system to be used with different radiation sensors or ASICs, such as the RD50 ENGRUN1 HV-CMOS monolithic pixel sensor currently being developed, as well as for other applications (accelerator instrumentation, medical physics, etc.).

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Measurements of NitroStrip detectors irradiated with 23MeV protons

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Nitrogen enrich material showed an improvement of some defects after irradiation. NitroStrip is an RD50 project that aims to compare nitrogen enriched silicon wafers with FZ, DOFZ and MCz material. This presentation will show CCE measurements and electrical characterization of NitroStrip samples irradiated at different fluences with 23MeV protons.

Design of high-speed front-ends for HV-MAPS within the CERN-RD50 collaboration

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The High Voltage-Monolithic Active Pixels Sensors (HV-MAPS) detector technology is a promising candidate for particle physics experiments. While standard hybrid sensors require bump-bonding or gluing to assemble the sensor and the readout electronics together, fully monolithic HV-MAPS allow integrating these parts onto one single chip, which makes them more cost-efficient especially for tracking applications that require large area silicon sensors. The high bias voltage that can be applied to the sensors forms a wide depletion region that improves the signal-to-noise ratio and a strong electrical field that drifts charges to the collecting node. Moreover, the radiation tolerance of HV-MAPS is also improved, which has been demonstrated to be up to a few $10^{15} n_{eq}/cm^2$.

As the HV-CMOS technology has many advantages, the RD50 collaboration is making efforts to study it in view of future particle physics experiments such as the High Luminosity-LHC (HL-LHC) and beyond. A large area demonstrator (RD50-ENGRUN1) with several matrices dedicated to improving the time resolution and speed of the sensor using different solutions at the readout circuit level amongst other matrices is being designed.

One of the pixel matrices will include four differently flavoured pixel types. These pixels are distinguished by two types of Charge Sensitive Amplifier (CSA) that use either a PMOS or an NMOS as the input transistor and two mechanisms of reset that are continuous or switched. The first two types use continuous current sources as their reset circuits resulting in the CSA's fall time being proportional to the number of input charges. The rise time of these two pixel types is less than 10 ns. Adjusting the reset current to a high value, it is possible to process a particle hit that generates 10K electrons in the sensing diode within 100 ns. The latter two use the discriminators'outputs to control the reset circuits that reset the CSAs with a switched large current while keeping the power consumption low. Such high current can discharge the feedback capacitors almost immediately and limits the fall time below 10 ns no matter how many input charges a particle generates. The total processing time is thus less than 25 ns. The continuously reset pixels will provide both rising and trailing edge time stamps to obtain Time over Threshold (ToT) information. In contrast, the switched reset pixels will only give the time stamp of the rising edge.

The timing information mentioned above is all obtained from simulations that use schematic models. All pixel flavours will integrate both analog and digital readout electronics into the 50 $\mu m \times 50~\mu m$ sensing area and be read out using a column-drain readout strategy. More details about the RD50-ENGRUN1 and the high-speed pixel matrix will be presented at the talk.

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Overview of sensor measurements session at LHC inter-experiment workshop

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Overview of the sensor measurements session at the CERN workshop 23-24 April 2018 on Radiation Effects at the LHC experiments and Impact on Operation and Performance

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Overview of sensor simulation session at LHC inter-experiment workshop

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Overview of the sensor simulation session at the workshop 23-24 April on Radiation Effects at the LHC experiments and Impact on Operation and Performance

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Overview of radiation simulation session at LHC inter-experiment workshop

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Overview of the radiation simulation session at the workshop 23-24 April on Radiation Effects at the LHC experiments and Impact on Operation and Performance. For more details see:

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Effect of thinning and backplane processing on charge collection of irradiated CMOS pixel detector structures

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Two sets of passive CMOS detectors were studied: thinned with processed and metalized backplane and not thinned without backplane processing with substrate biased through the implant on top of the device. Detectors were irradiated with neutrons in reactor in Ljubljana. Collected charge was measured with electrons from Sr-90 source using an external amplifier. Depletion depth and charge collection was measured also with Edge-TCT and compared with Sr-90 measurements. Results obtained with two sets of devices were compared. Measurements showed that thinning and backplane processing improves charge collection after irradiation.

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A new model for the TCAD simulation of the silicon damage by high fluence proton irradiation

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For the high-luminosity phase of the Large Hadron Collider (HL-LHC), at the expected position of the innermost pixel detector layer of the CMS and ATLAS experiments, the estimated equivalent neutron fluence after 3000 fb $^{-1}$ is $2\cdot 10^{16}~\rm n_{eq}/cm^2$, and the IEL (Ionizing Energy Loss) dose in the SiO $_2$ is 12 MGy. The optimisation of the pixel sensors and the understanding of their performance as a function of fluence and dose makes a radiation damage model for TCAD simulations, which describes the available experimental data, highly desirable. The currently available bulk-damage models are not able to describe simultaneously the measurements of dark current (I-V),capacitance-voltage (C-V) and charge collection efficiency (CCE) of pad diodes for fluence $\geq 1\cdot 10^{15}~\rm n_{eq}/cm^2$.

Therefore, for the development and validation of a new accurate bulk damage model we use I-V, C-V and CCE measurements on pad diodes available within the CMS-HPK campaign and data from samples irradiated recently with 24 GeV/c protons. For the determination of the radiation-induced damage parameters we utilise the "optimiser" of Synopsys TCAD, which allows the minimisation of the difference between the measured and simulated I-V, C-V and CCE. The outcome of this optimisation, the Hamburg Penta Trap Model (HPTM), provides a consistent and accurate description of the measurements of diodes irradiated with protons in the fluence range from

 $3{\cdot}10^{14}~\text{n}_{eq}/\text{cm}^2$ to $1.3{\cdot}10^{16}~\text{n}_{eq}/\text{cm}^2.$

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CNM activities on LGADs for ATLAS/CMS Timing Layers

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We will present the last technological developments at CNM on LGAD detectors for ATLAS HGTD and CMS ETL. In this sense, we will summarize the actual status of the new AIDA2020 fabrication run to integrate thin LGADs in 4-inches, 35 and 50 microns thick, silicon on silicon wafers, showing a description of the integrated structures in the mask set and a summary of the fabrication process. In addition, we will present a basic description of the new run to integrate, on 4-inches, 50 microns thick silicon on silicon wafers, LGADs with Gallium doped multiplication layer and its first electrical characterization results.

Besides, we will present the main results of the current status of the first 6-inches LGAD run electrical characterization, showing the first results of the gain values measured with a Tri-alfa source. Also, a basic description of the new run to integrate on 6-inches SOI wafers, thin LGADs for timing applications, and the mask description for a new 6-inches thin LGAD fabrication process for ATLAS/CMS, will be presented. This run will be fabricated using 35 and 50 microns thick, silicon on silicon wafers.

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First measurements with silicon detectors irradiated above 3e17 n/cm2

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Silicon detectors were recently irradiated with reactor neutrons up to fluence of 3e17 n/cm2. The irradiated samples include detectors previously irradiated with 1.6E17 n/cm2 so these were exposed to total of 4.6E17 n/cm2. Measurements have just started and first results will be presented in this contribution.

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TCAD Process and device simulation of OVERMOS, a CMOS 180nm MAPS detector

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OVERMOS is a MAPS detector test structure fabricated using high resistivity substrate in 180nm CMOS process provided by TowerJazz.It consists of several arrays of 40 x 40 um2 and 40 x 400 um2 pixels which also feature in-pixel CA and full analogue read out.

A number of these device have been irradiated with neutrons and are currently being tested to investigate radiation damage effects.

Extensive 3D device simulations, including CMOS fabrication process simulations, have been performed using Synopsis TCAD. Modelling of device electrical behaviour, including breakdown process, which acount for radiation bulk damage effects and Si/SiO2 traps defects have been performed, using different implementation of radiation damage models. Results of simulations and comparisons with test results will be presented and discussed.

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A novel HV silicon JFET for ATLAS and other silicon R&D activities at BNL

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We present a High-Voltage vertical JFET, conceived as a candidate for the High-Voltage Multiplexing switch in the ATLAS upgrade of the silicon microstrip Inner Tracker (ITk). Both n-type and p-type HV-JFETs have been successfully fabricated in the silicon processing facility of Brookhaven National Lab. Probe station measurements of un-irradiated devices show low leakage currents and high breakdown voltages (up to 600V) in the OFF state, and high currents in the ON state. We also present other on-going silicon R&D activities, such as LGAD testing and fabrication, and our efforts towards the commissioning of BLIP (Brookhaven Linear Isotope Producer) as an in-house neutron and proton irradiation facility.

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Status of HV-CMOS developments within the RD50 collaboration

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Following from work in the wider community, specific High Voltage-CMOS (HV-CMOS) developments within the RD50 collaboration have started with a small test prototype (RD50-MPW1) in the 150 nm HV-CMOS technology from LFoundry S.r.l. The prototype, manufactured using mid (500 Ω ·cm) and high (1.9 k Ω ·cm) resistivity substrates, integrates two fully monolithic matrices of pixels and test structures aimed at Transient Current Technique (TCT) measurements. A dedicated DAQ based on Caribou, a modular readout system for pixel sensor R&D, is also being developed within the collaboration and an extensive measurement campaign will start soon. The knowledge gained with RD50-MPW1 will be used to design a large area demonstrator (RD50-ENGRUN1) in the same technology. The large area demonstrator will be produced using different resistivity substrates (low,

mid, high and very high range) and processed directly at the foundry to allow thinning to $100~\mu m$ or less and sensor backside biasing. It will integrate five fully monolithic large matrices of pixels and test structures aimed mostly at improving the speed and time resolution of the detector. TCAD simulations to study the performance of the sensors prior to their fabrication are running in parallel to the design. To evaluate the radiation tolerance of this sensor technology, the manufactured devices will be irradiated at a wide range of fluences and their performance compared with that of high resistivity float zone passive sensors.

This contribution describes the status of the HV-CMOS project within the RD50 collaboration. The design details of the test prototype RD50-MPW1 and the large area demonstrator RD50-ENGRUN1 will be presented at the workshop, together with TCAD simulated results and the very first measurements of RD50-MPW1.

Defect and Material Characterization / 18

Forward and reverse current of highly irradiated silicon pad diodes

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The current of initially p- and n-type bulk silicon pad diodes has been studied for low and high forward and reverse bias voltages at -30 °C. The diodes were irradiated to neutron equivalent fluences $\Phi_{eq} > 10^{15} \ {\rm cm}^{-2}$ with GeV protons.

At low bias voltages, the current is ohmic. The neutral bulk of highly irradiated diodes has approximately zero net fixed space charge and the free carrier concentrations are approximately equal to intrinsic silicon, which is known as carrier removal. Consequently, the resistivity of the neutral bulk is very high. Since the generation lifetime is very short, the resistivity of the space-charge region SCR has been found to be similar to the bulk resistivity for low bias voltages. Accordingly, the current at low bias voltages is determined by the bulk rather than the SCR.

It has been observed that the voltage-independent bulk resistivity $\rho = \left(en_i\left(\mu_0^e + \mu_0^h\right)\right)^{-1}$ measured at low bias voltages increases with the fluence. This is interpreted as a decrease of the carrier mobilities $\mu_0^{e,h}$ due to the scattering of carriers by ionized defects. The dependence of $\mu_0^{e,h}\left(\Phi_{eq}\right)$ on the fluence has been estimated from the measurements of the bulk resistivity assuming ionized impurity scattering.

At higher reverse bias voltages the current changes abruptly from the ohmic behavior $\rho\left(U\right)=const$ to a dependence $\rho\left(U\right)\propto U^S$ with S<1. The transition occurs once the generation current of the SCR cannot sustain the linear ohmic current of the bulk anymore. The SCR partially depletes of free carriers and dominates the current for higher voltages. The transition between bulk-dominated behavior and SCR-dominated behavior occurs at a characteristic threshold $\frac{U_{th}}{d^2}\left(\Phi_{eq}\right)\propto\Phi_{eq}$, with the thickness of the diode d and the threshold voltage U_{th} . An empirical model has been developed to describe the current of pad diodes as function of the fluence and the applied voltage for small to medium reverse bias voltages. The measurements are described within a few percent by the model.

For forward bias the diode current is ohmic with the field-dependent carrier mobilities until the current suddenly increases exponentially at high bias voltages. The forward current at all bias voltages can be reasonably described within about $10\,\%$ assuming space-charge-limited currents for a semiconductor containing traps uniformly distributed in the band gap.

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Comparative investigation of irradiated small-pitch 3D strip detectors

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The HL-LHC is expected to reach luminosities of up to 3000 fb–1; the upgrade of innermost tracking detectors of the ATLAS experiment foresees a decrease in pixel size in order to enhance the positional resolution. In this talk, the collected charge characterisation of different pixel size geometry will be presented. Following irradiation, sensors with $50\mu m \times 50\mu m$ pixel size show higher charge collection efficiency than $100~\mu m \times 25~\mu m$ (1E), due to the smaller distance between the electrodes. The latter implies a shorter drift distance and a lower trapping probability of the generated electron-hole pairs.

Device Simulation / 20

ILGAD TCAD Simulations

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Where we present TCAD simulations results on the brand new ILGAD device, in two flavours, 300 um and 50 um thickness. Radiation effects in signal formation an particularly in the risign time are considered.

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High-Density Low Gain Avalanche Detectors (HD-LGAD)

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The FBK, Universities and INFN of Turin and Trento groups are proposing an R&D project to RD50 collaboration, aimed at developing a new detector structure named high-density Low Gain Avalanche Detectors (HD-LGAD). The novel structure consists in a thin LGAD sensor with segmented multiplication junction, featuring small pixels and a reduced inter-pixel border region.

Standard LGADs made on thin (30-50 μm) substrates recently demonstrated a superb timing resolution down to ~30 ps. On the other hand, the pixel size of such detectors is typically limited to 0.5-1 mm, due to the presence of an inter-pixel region (~60-70 μm wide), which hosts the pixel guard ring and the junction termination edge. In such a region, the gain is completely suppressed and, consequently, the pixel fill factor (FF) is strongly reduced.

The final goal of the proposed project is to produce pixel arrays and micro-strips sensors with pixels and strips dimension down to $100~\mu m$, keeping at the same time the FF higher than 80%. We are investigating different strategies to reduce the inter-pixel border region: i) re-design the pixel guardring by using shallow trench isolation (STI); ii) improve the microfabrication process to reduce the feature size of all the structures at the pixel border (trenches, contacts, field plates). In this presentation, we will describe the project goals and motivations and we will present the first simulation results on the new designed structures.

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Charge Collection Efficiency of proton-irradiated small-cell 3D strip sensors up to 1.7E16 neq/cm2 equivalence fluence

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A study of Silicon strip 3D sensors of sizes 50 um x 50 um and 25 um x 100 um, fabricated at CNM using double-sided technology is shown. Sensors are wire-bonded to ALIBAVA read-out system. Results about charge collection of non irradiated sensors are presented, and also irradiated up to fluences of 1.7E16. The response of the sensors in both a test beam of 120 GeV protons and pions, and radioactive source 90Sr measurements is analyzed.

Defect and Material Characterization / 24

FORMATION AND ELIMINATION OF RADIATION DEFECTS RE-SPONSIBLE FOR CHARGE CARRIER REMOVAL IN BORON DOPED SILICON

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When irradiated with fast particles, the radiation damage associated with the removal of charge carriers in n-type silicon (n-Si) is mainly due to the formation of vacancy-type defects (divacancy, A and E centers). In p-Si, an important role in the removal of charge carriers is related with interstitial defects. The appearance of silicon interstitial atoms induced by irradiation initiates a series of branching reactions. As a result of these branching reactions, interstitial impurity atoms appear in the crystal and their subsequent migration and trapping results in formation of defect complexes which are stable at room temperatures.

The aim of this work is to analyze factors which influence on the behavior of interstitial-type defects in irradiated silicon doped with boron. The analysis is based on our experimental data obtained after irradiation with electrons (E=5.5 MeV) or alpha-particles (E=5.15 meV).

It has been shown that the distribution of primary self-interstitials between impurity traps depends not only on impurity concentrations but also on the dose rate and type of bombarding particles.

The irradiation induced boron-oxygen complex in Si diodes can be annealed at room temperature by applying forward current injection. This injection helps to restore the initial concentration of substitutional boron. However, the hole concentration is restored only partially due to the additional formation of interstitial carbon-interstitial oxygen complexes.

At temperatures of about 370 K a new compensating defect is formed after annealing of the interstitial oxygen-silicon di-interstitial complex. It appears in DLTS spectra as ME1 center or double peak BH1/BH2. The comparison of its formation in diodes made from epitaxial and Czochralski-grown silicon lead to the conclusion that the ME1 center is related to a boron containing complex.

The possibilities to mitigate radiation damage of diode structures made of boron-doped silicon are also discussed.

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Front-side biasing of n-in-p silicon strip detectors

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Front-side biasing is an alternative method to bias a silicon sensor. Instead of directly applying high voltage to the back-side, one can exploit the conductive properties of the edge region to bias a detector exclusively via top-side connections. This option can be beneficial for the detector design and might help to facilitate the assembly process of modules. The effective bias voltage is affected by the resistance of the edge region and the sensor current. The measurements of n-in-p sensors performed to qualify this concept have shown that the voltage drop emerging from this resistance is negligible before irradiation. After irradiation, however, the resistivity of the edge region increases with fluence and saturates in the region of 10^7 at a fluence of $1 \times 10^{15} n_{eq} cm^{-2}$. The measurements are complemented by TCAD simulations and interpretations of the observed effects.

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Performance of thin LGADs after long term annealing

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Thin LGAD detectors from CNM were irradiated with neutrons to 6e14 and 3e15 cm-2 and annealed in steps up to 10000 min at 60C. After each annealing step charge collection and leakage currents were measured to determine gain, break-down performance and evolution of leakage currents. It was found that apart from leakage current which decreases with annealing in accordance with expectations the annealing has little effect on sensor performance.

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Charge multiplication in irradiated sensors after long annealing times

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In previous studies we presented results on long term annealing studies in irradiated p-type sensors until charge multiplication occurred.

Recently we carried out a deeper investigation on the charge multiplication phenomena of the annealed sensor, in particular its instability. We will show how it depends on bias voltage cycling and (less) on temperature. One sensor irradiated with neutrons to a fluence of $2e15\frac{n_eq}{cm^2}$ and annealed at 70° C showed dramatic changes in the signal behavior in time. A deeper investigation suggests the onset of plasma effect in the conduction mechanisms when in heavy charge multiplication.

Defect and Material Characterization / 28

Characterization of acceptor removal in silicon pad diodes irradiated by protons and neutrons

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Acceptor removal has been studied on p-type silicon sensors irradiated with protons and neutrons up to 7E15 n_{eq}/cm^2 . Two sets of diodes were used: thin epitaxial diodes with different resistivities (10, 50, 250 and 1000 Ohm cm) and high resistivity float zone diodes with different thicknesses (100, 150, 200 and 285 um).

CV and IV measurements were performed to extract the effective doping concentration of these devices. TCT collected charge versus voltage was used to evaluate the sensor's bulk space charge. Defect spectroscopy was conducted using TSC technique in order to study the correlation between the BiOi defect concentration and acceptor removal.

All collected data is used to revise the fitting of the Neff to extract acceptor removal rate parameters, while comparing proton vs neutron irradiation.

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Charge collection and annealing studies on 800 MeV proton irradiated AMS H18 HV-CMOS sensors.

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With the upcoming HL-LHC upgrade, there is ongoing investigations on the viability of HV-CMOS sensors for the upgrade of the ATLAS pixel detector. The HV-CMOS technology is showing great promise, however, a drawback in the standard process is the use of low resistivity silicon (10 - 20 Ω cm) wafers, as this commonly only provides a rather small depletion region before breakdown voltage is reached. This is usually circumvented by using high resistivity (~1k Ω cm) silicon. On the other hand, after NIEL irradiation above 1e15 neq/cm2 fluences low and medium resistivity sensors show somewhat higher charge collection compared to high resistivity silicon. This makes the low and medium resistivity HV-CMOS highly interesting if close to 100% efficiency can be guaranteed below this fluence.

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In this study 10 Ω cm AMS H18 test chips have been irradiated with 800 MeV protons at LANSCE up to 1.3e16 neq/cm2 to closer mimic the average energy of the simulated proton background radiation in HL-LHC ATLAS. Edge-TCT was used to investigate the change in charge collection, and an annealing study was carried out to confirm the signal behaviour over time.

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CMOS Detectors Overview

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A parametrization of initial acceptor removal

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In this brief talk I will present the available data on Initial acceptor removal and propose a simple parameterization to explain the basic feature of the data.

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Proposal for RD50 common project Mobility of carriers in irradiated Silicon

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Welcome

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Effects of protons and neutrons irradiation to the gain layer and bulk of 50-micron thick FBK LGAD sensors doped with Boron, Boron Low diffusion, Gallium, Carbonated Boron and Carbonated Gallium

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RD50 –recent news

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A Brief History of the RD50 Collaboration

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Highlights of Silicon microscopic defects spectroscopy

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Highlights of Eckhart career