DAQ development for the characterization of the RD50 HV-CMOS devices

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Outline

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- DAQ architecture.
- CaRIBOu system for the RD50-MPW1 prototype.
- CaR board.
- Chip board for the RD50-MPW1.
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Motivations

- High Voltage-CMOS (HV-CMOS) developments within the RD50 collaboration.
  - Small test prototype (RD50-MPW1) manufactured in the 150 nm HV-CMOS technology from LFoundry.
  - A large area demonstrator (RD50-ENGRUN1) will be designed in the same technology.
- Measurement and characterization of these devices requires a specific Data Acquisition System (DAQ).
- From our previous experience in radiation sensors and developing DAQ for radiation sensors like ALIBAVA, we learned:
  - A considerable effort is required to develop a custom DAQ for a specific purpose.
  - Once the DAQ has been developed is very difficult to use it for other purposes.
  - Commercial modular DAQ systems are expensive and sometimes not so flexible as required.
- We started to think about a DAQ system which could:
  - Be used for different purposes (radiation detectors, medical physics, accelerators, etc.) without redesigning all the hardware again and again.
  - Be scaled up easily and have new functionalities using the same basic hardware.
  - Be as open as possible (in terms of hardware, firmware and software) to facilitate future developments.
- We found a preliminary DAQ architecture which could fulfill these goals.
- We also found a DAQ system already developed (CaRIBOu) following this architecture which we can use as a first step for the RD50-MPW1 chip characterization.

DAQ requirements

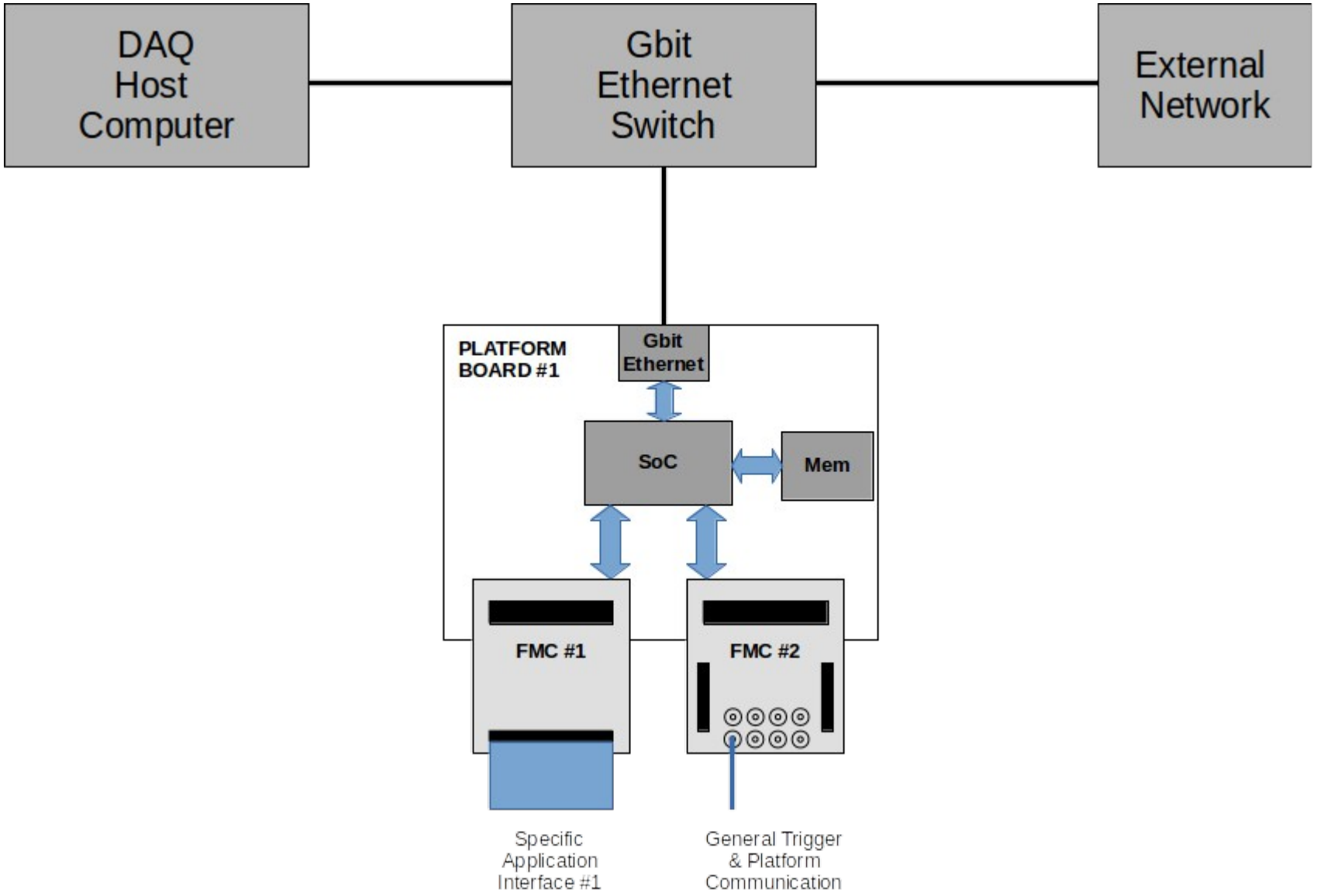
- To read out and to control different HVCMOS structures.
- To be able to process external trigger input signals (e.g. signal derived from a radioactive source).
- To be able to generate trigger output signal (e.g. for driving a laser system).
- It must work both in standalone mode (e.g. a basic laboratory test bench) and in a test beam environment (e.g. several read out planes are required with synchronization).
- Easy to operate with user friendly DAQ software.
- In order to have flexibility for current and future applications, it must be easily scalable, configurable and modular.

DAQ architecture: first approach

- Programmable logic is needed for this application: FPGA.
- Combining FPGA resources with processor(s) to have more flexibility: System-on-chip (SoC).
- Modularity and standardization: FMC connectors to connect function specific FMC modules to a common platform board.
- Data storage capability: on-board volatile and non-volatile memory required.
- Fast system control and bulk data transfer to host computer: Gigabit Ethernet communication.
- Use a development board to shorten development time.

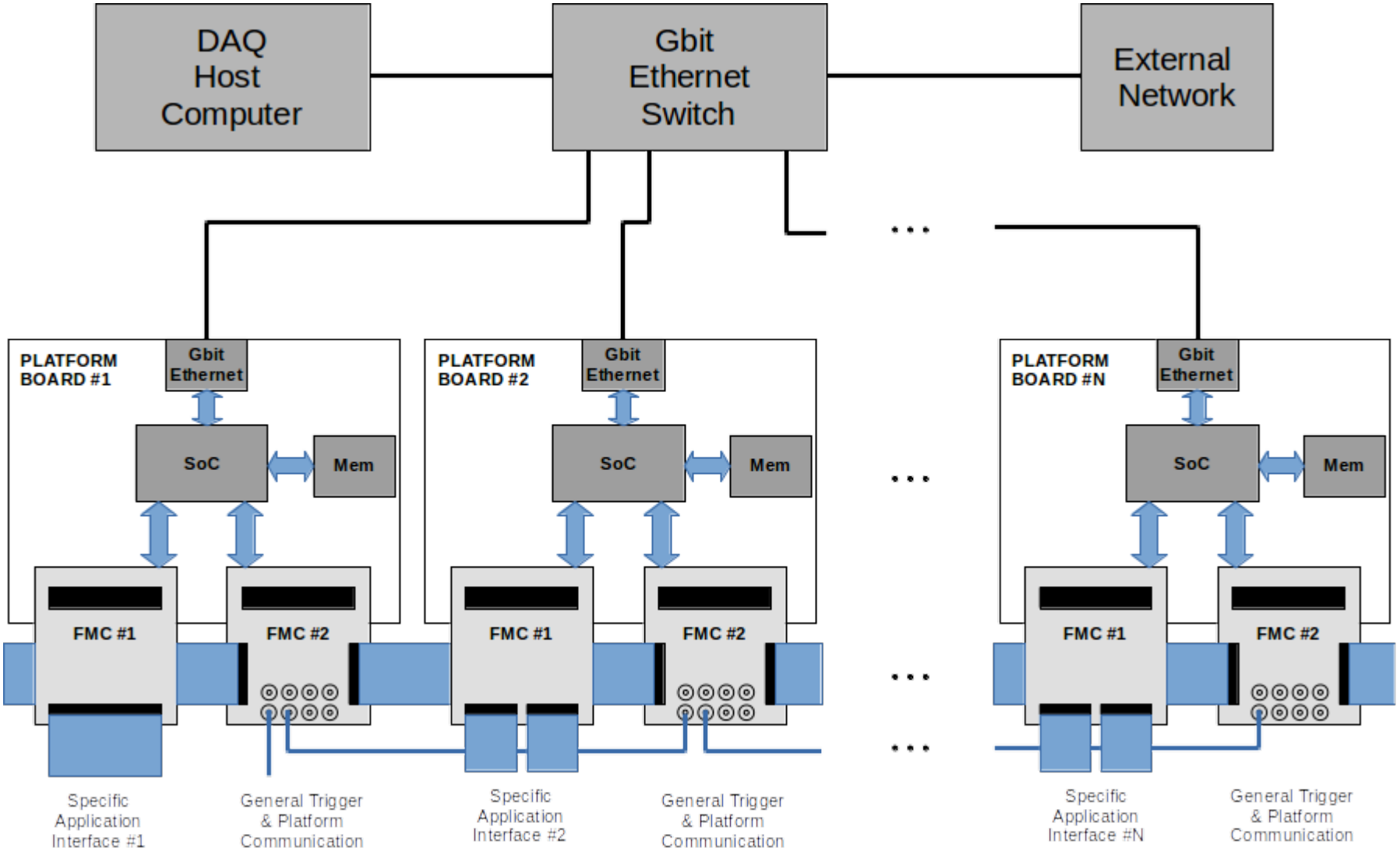
DAQ architecture: standalone DAQ

- FMC board 1 is a custom board for a specific application (e.g. read-out/control HVCMOS structure(s)).
- FMC board 2 is a custom board used for trigger input/output processing.



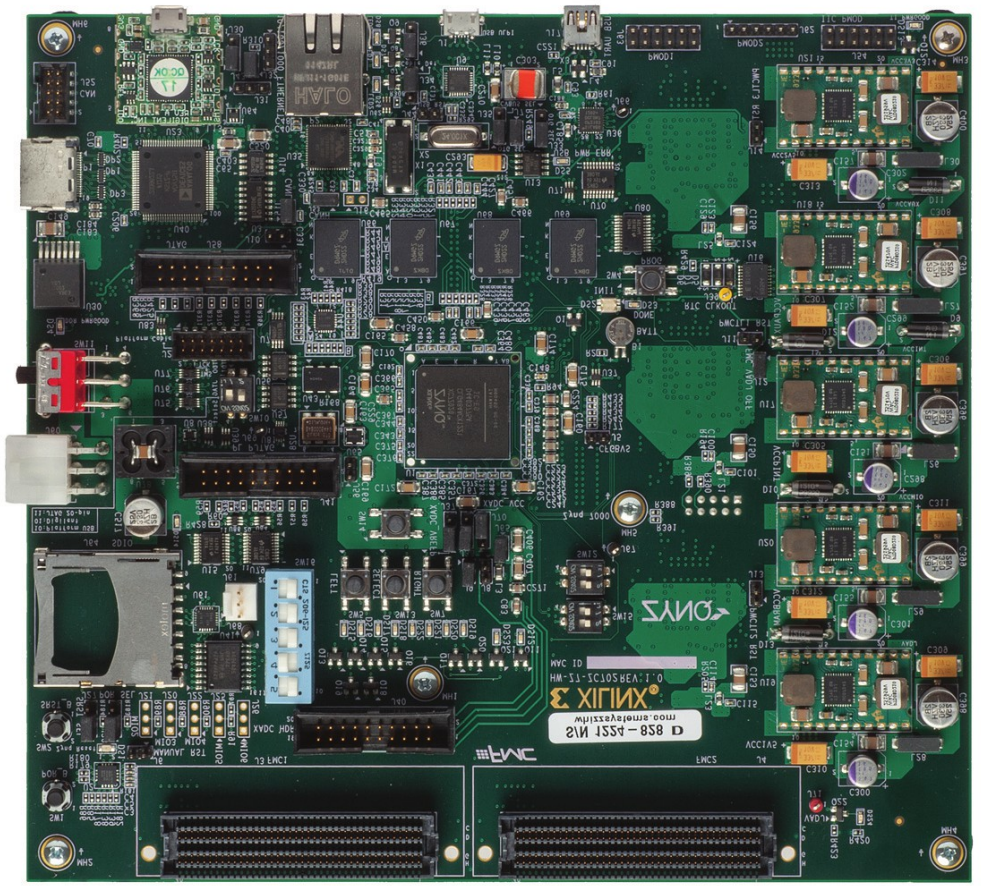
DAQ architecture: DAQ with several platform boards synchronized

- FMC board 1 is a custom board for a specific application (e.g. read-out/control HVCMOS structure(s)).
- FMC board 2 is a custom board used for trigger input/output processing and platform communication & synchronization (I2C and LVDS signals).



DAQ architecture: platform board candidate

- ZC702 development board from Xilinx.
- SoC is Zynq-7000 XC7Z2020 with a dual-core ARM Cortex-A9 and a mid-range Artix 7 FPGA (85k programmable logic cells).
- Two FMC connectors (160-pin low pin count) with up two 68 single-ended (34 differential) signals, 2 differential clocks, I2C signals and power/gnd signals (12V, 3.3V and 2.5V).
- Tri-mode Ethernet PHY (10/100/1000 Mbps).
- 1 GB DDR3 SDRAM memory.
- 128 Mb SPI flash memory.
- SD card interface (8GB card included).
- 12 V/5 A power input.
- Other features (USB, HDMI, XADC, etc).
- All the board documentation (schematics, PCB design files, etc.) available from Xilinx.
- Board distributed by Xilinx. Easily available at Farnell (896€).



ZC702 development board

DAQ architecture: tasks to develop

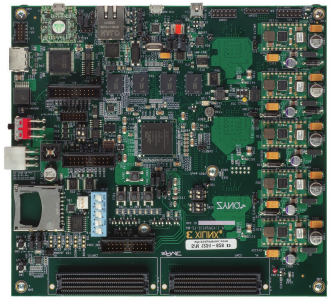
- Hardware:
  - One or several custom FMC cards for HVCMOS read out and control.
  - Custom FMC card for trigger processing and platform communication.
  - Optionally, a custom platform board with the trigger processing and platform communication implemented on board to have both FMC connectors free.
- SoC firmware:
  - Specific firmware blocks implemented in the SoC FPGA for interfacing the FMC cards designed.
- SoC software:
  - SoC dual-core ARM A9 processor can run a light Linux distribution (PetaLinux) where custom pieces of software (C/C++ programs as well as python or bash scripts) can be run to interface the firmware blocks or peripherals (Ethernet MAC, memory interfaces, I2C, SPI, GPIO, etc.).
  - Alternatively, a standalone C/C++ piece of code can be run by the processor.
- Host Computer software:
  - Low level tasks (communication with different platforms, data processing, etc.) with python scripts or C/C++ programs.
  - Graphical user interface for monitoring the data and controlling the DAQ.
  - Post processing scripts for the data acquired (Python or ROOT).

CaRIBOU system for the RD50-MPW1

- Our colleagues from HEPHY proposed to use a system already developed to start with the characterization of the RD50-MPW1 chip.
- CaRIBOu (Control and Readout Inner tracking Board) is a multi-chip modular DAQ system used for the characterization of pixel detectors.
- Developed by CERN, U. Geneva and BNL (https://gitlab.cern.ch/Caribou).
- Multi-chip modular DAQ system: support for different pixel devices (CLICpix2, C3PD, FEI4 and H35Demo).
- Application specfic chip board to be designed for the RD50-MPW1 chip with minimum functionality.
- CaR (Control and Readout) interface board close to the chip to provide commonly required resources (voltage regulators, ADCs, bias sources, clock generator, etc.).
- Zynq SoC platform board (ZC706 or ZC702) can be placed in a safe distance (~ 50 cm) from the chipboard using FMC cable assembly.
- Zynq firmware and DAQ software developed for supported pixel devices: need to adapt both for the RD50-MPW1 chip board.
- Good opportunity to gain experience to develop our own DAQ system.

ZC706 board

or



ZC702 board

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FMC cable (optional)

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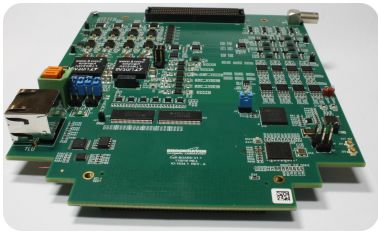

CaR board

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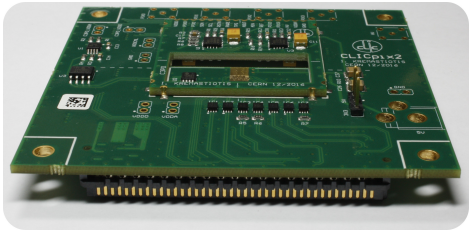
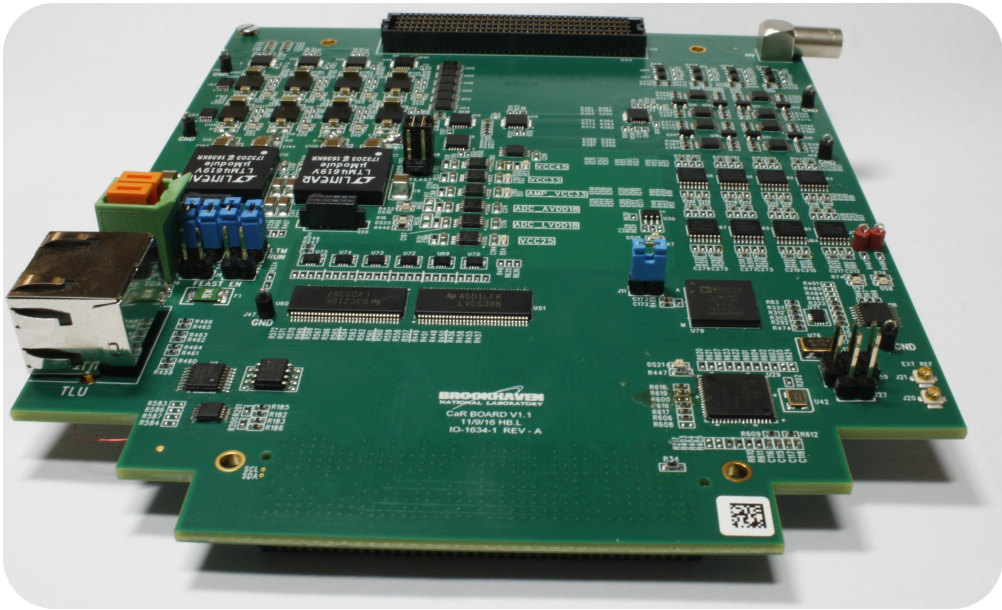


Application specific chip board

CaR interface board

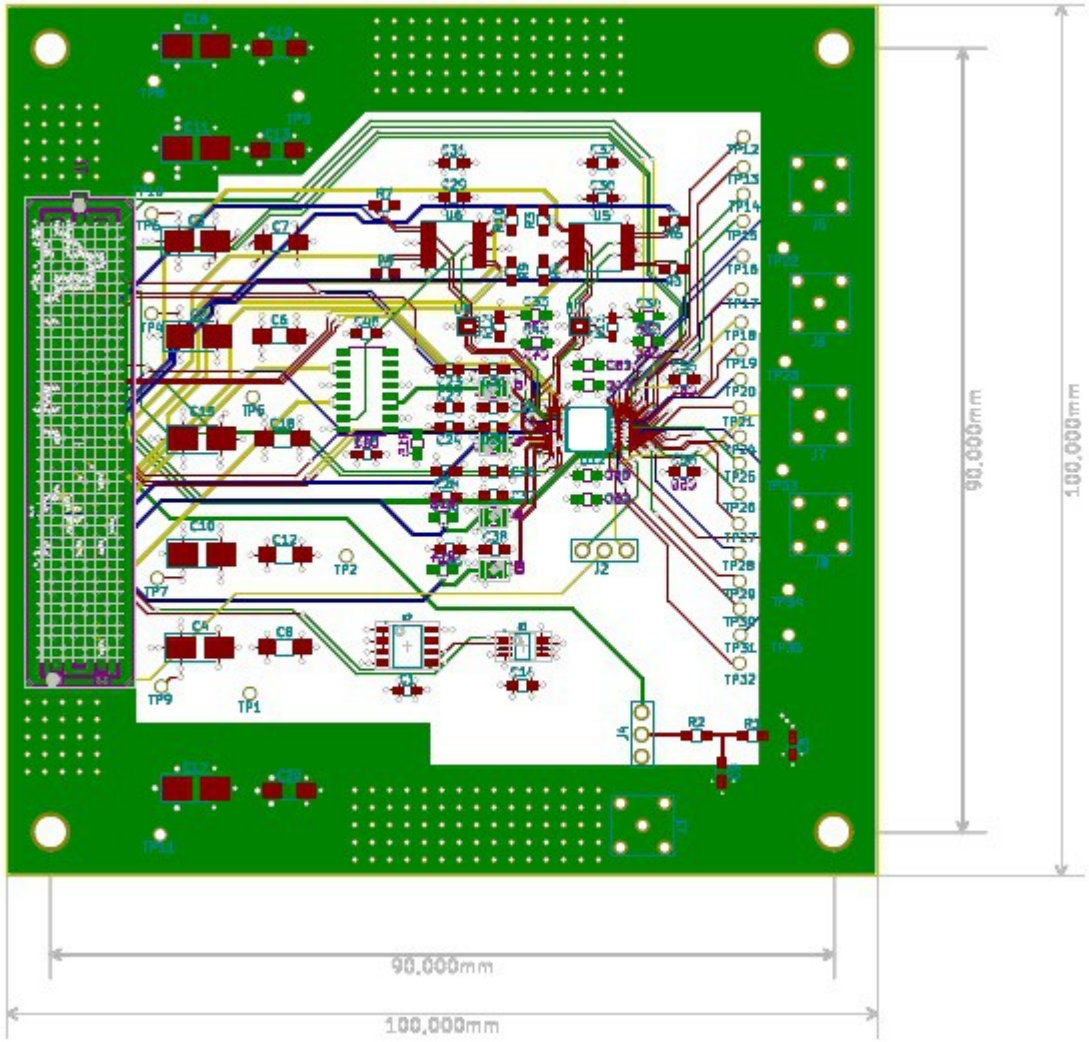
- FMC mezzanine board to interface multiple chip boards.
  - 8 power supplies (0.8 - 3.6 V/3 A).
  - 32 adjustable voltage outputs (0 - 4 V).
  - 8 current outputs (0 – 1 mA).
  - 8 voltage inputs (0 - 4 V).
  - 8 full-duplex SERDES links.
  - ADC (16 channels, 65 MSPS and 14-bit).
  - 4 injection pulser.
  - HV input.
  - I2C bus.
  - TLU RJ45 input
  - General CMOS signals (10 outputs and 14 inputs).
  - 17 LVDS pairs.
  - Output jitter attenuator and clock multiplier.
- Support of many voltage levels and communication standards with local measurement and monitoring capabilities.
- Very interesting board to be used as a generic FMC mezzanine in any DAQ.



CaR interface board

•Chip board for the RD50-MPW1

- A specific board which accomodates one RD50-MPW1 chip.
  - Both pixel matrices of the chip interfaced.
  - Specific board for the chip test structures.
- Compatible with the CaR board of the CaRIBOu DAQ.
- PCB characteristics:
  - 100 mm x 100 mm size.
  - 8 layers (top-sig1-gnd1-pwr1-pwr2-gnd2-sig2-bottom).
  - FR4 as dielectric.
  - 100 um min track width and separation.
  - Through-hole vias. 150 um min drill diameter.
  - Electroless nickel inmersion gold (Ni/Au) surface finish.
- LVDS-CML and CML-LVDS converters on board.
- I2C thermometer, unique ID and 2k EEPROM.
- PCB layout being finished.
- Production and assembly planned during June.



RD50-MPW1 chip board (ground and power planes not showed)

Future plans

- Finish the RD50-MPW1 chip board layout.
- Production and assembly of the RD50-MPW1 chip board.
- Procurement of CaR boards.
- DAQ development for the RD50-MPW1 chip:
  - Zynq firmware and DAQ software modification and upgrade of CaRIBOu DAQ (with ZC706 board).
  - Zynq firmware and basic DAQ software development for reading out the CaR board with a ZC702 platform board.
- RD50-MPW1 chip characterization using the DAQs.
- DAQ development for the RD50-ENGRUN1 chip based on feedback from RD50-MPW1 DAQ.
  - Specific chip board for RD50-ENGRUN1.
  - CaR board interface if positive feedback from RD50-MPW1.
  - Probably, firmware and software upgrade of CaRIBOu DAQ for RD50-ENGRUN1 if CaR used.
  - Development of a specific DAQ following the proposed architecture and compatible with CaR board for RD50-ENGRUN1.

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